



POLITÉCNICA



NI Big Physics Summit

# DEVELOPMENT OF ADVANCED DATA AND IMAGE ACQUISITION SYSTEMS USING RIO TECHNOLOGY AND EPICS: INTEGRATION IN ITER

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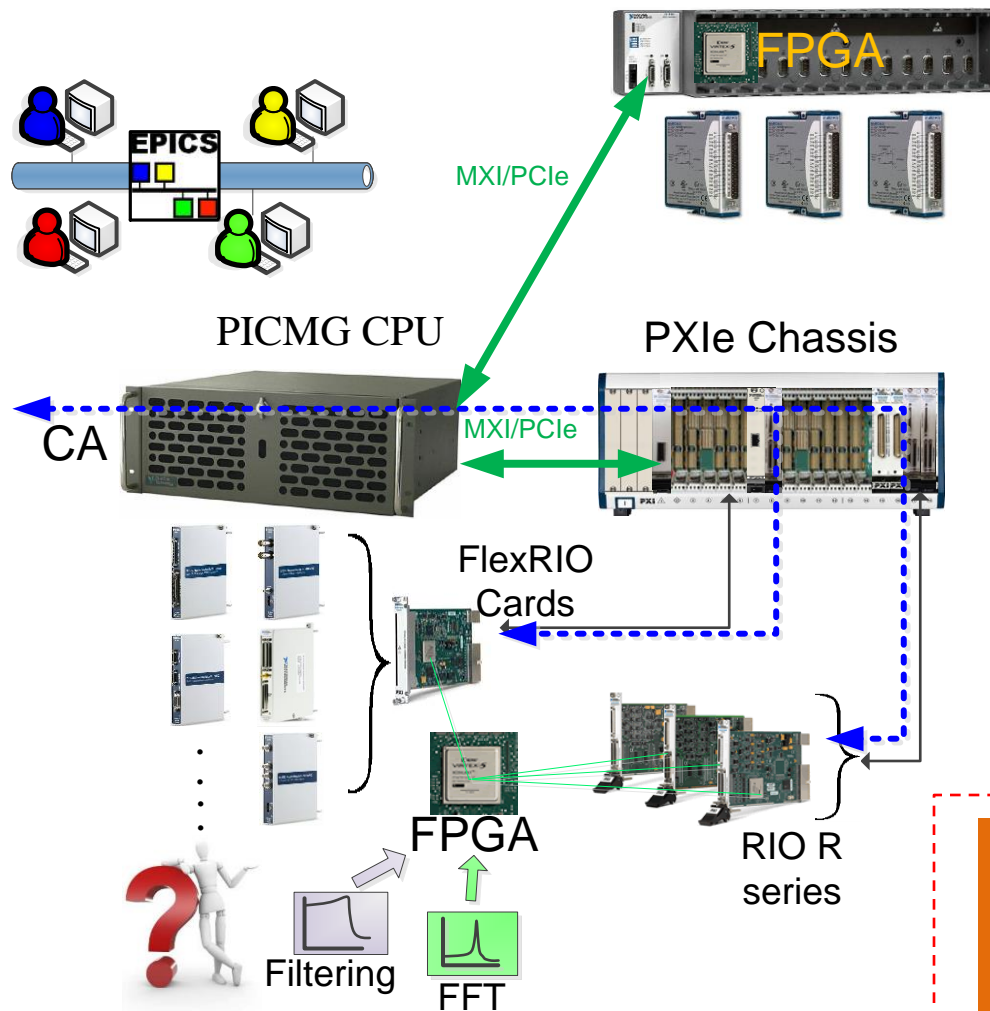
GRUPO DE INVESTIGACIÓN EN  
INSTRUMENTACIÓN Y  
ACÚSTICA APLICADA



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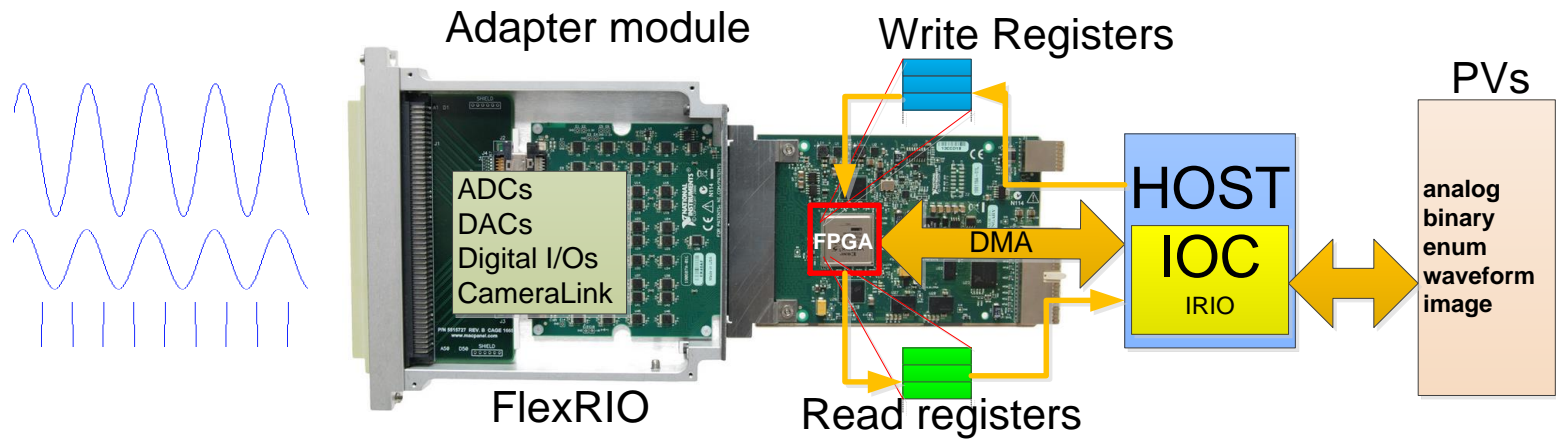
# Motivation



- FPGAs provide reconfigurable hardware with deterministic data preprocessing capabilities
- EPICS is a very common solution for SCADA in large scientific experiments
- The combination of both technologies simplifies the development of complex data acquisition and processing systems.

**I-RIO is a set of software tools simplifying the integration of RIO devices in EPICS**

# RIO/FlexRIO Devices



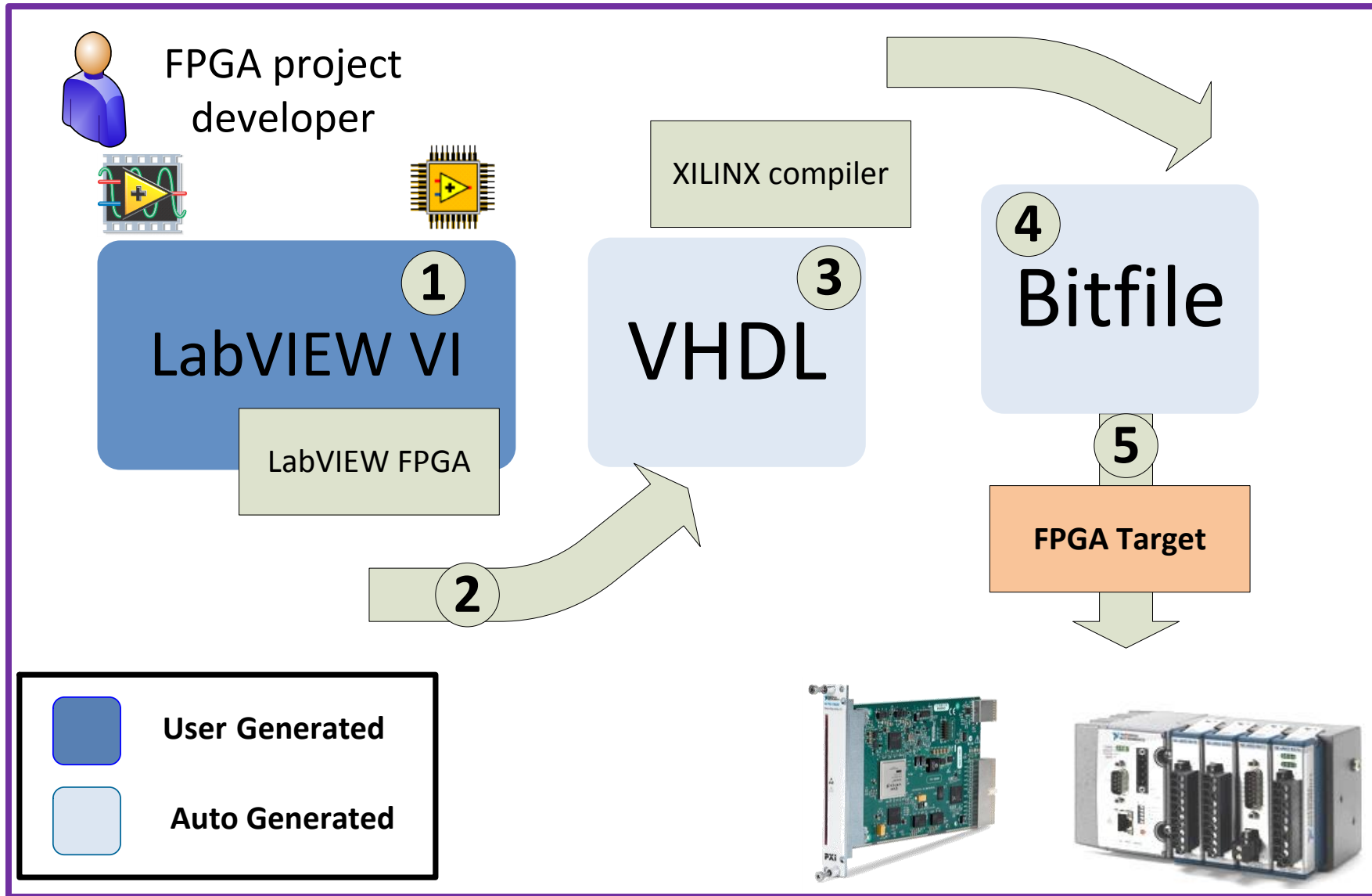
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The user defines the functionality programming the FPGA

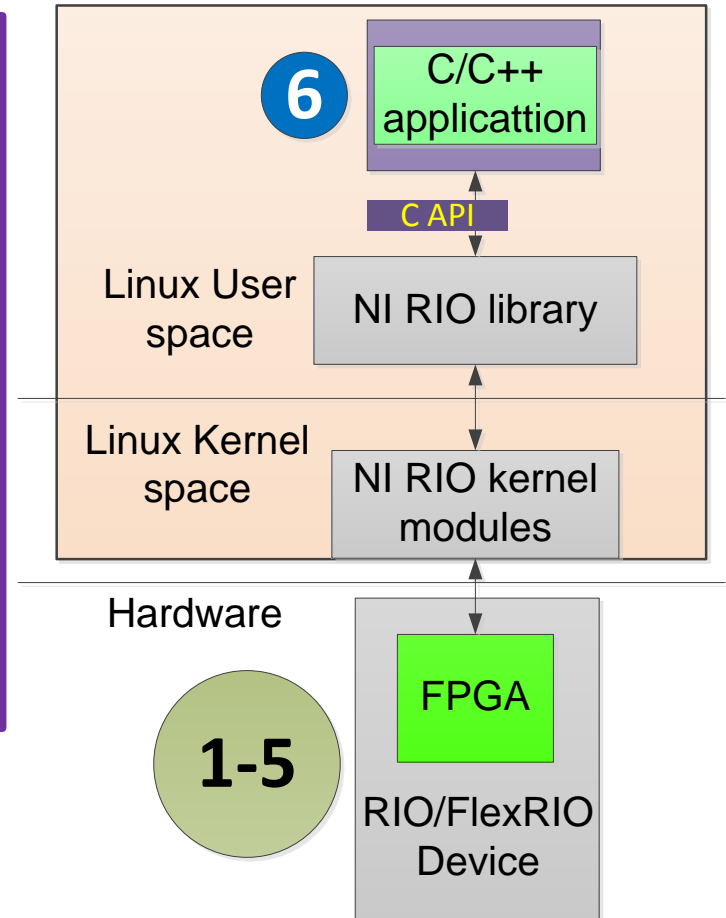
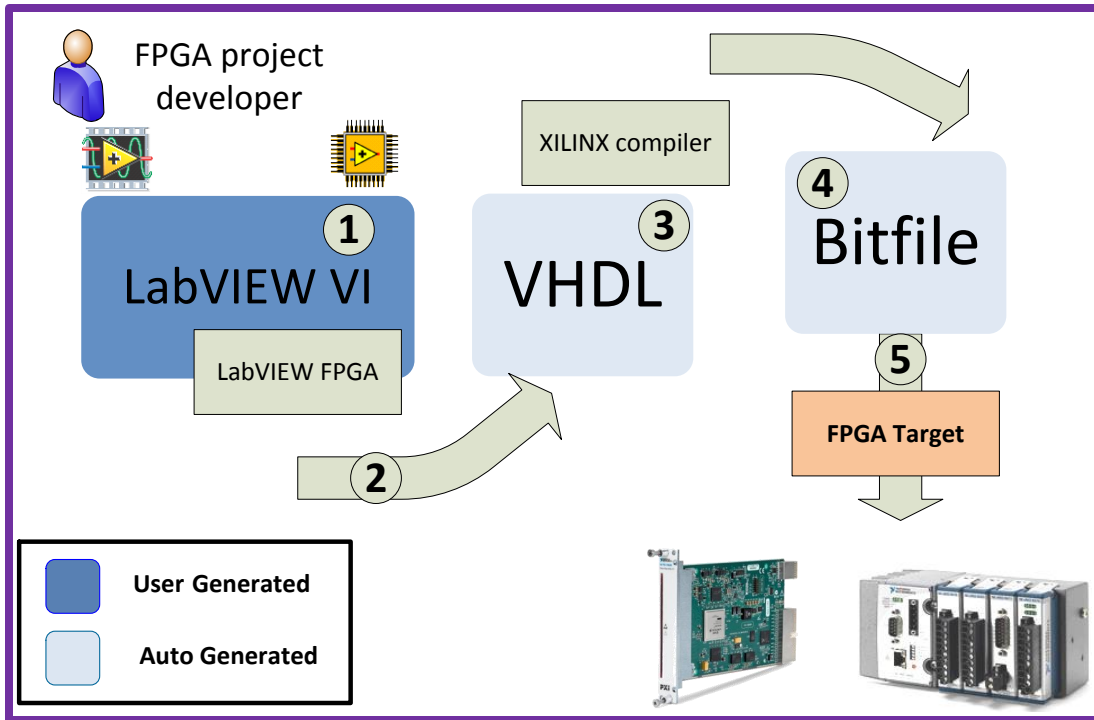
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EPICS connects a user defined device with PVs for configuration and supervision

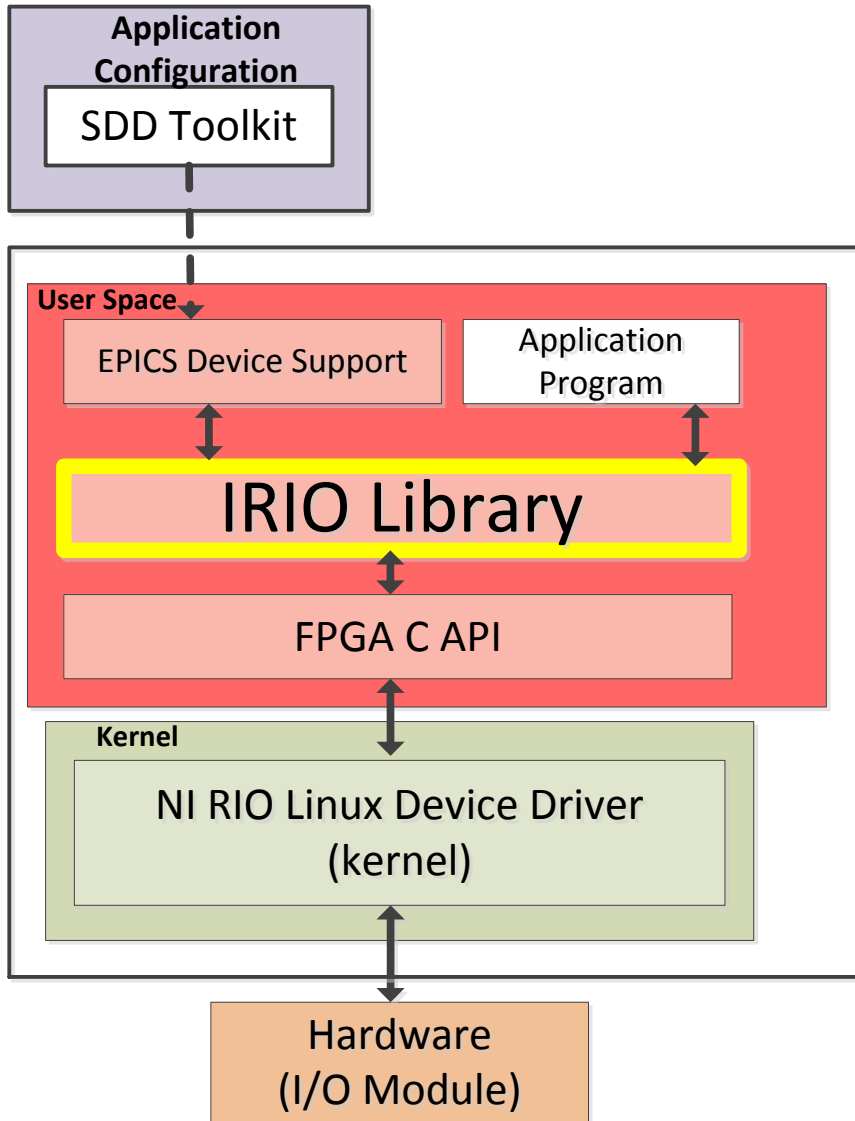
# Development cycle: LabVIEW for FPGA



# Using RIO devices in Linux

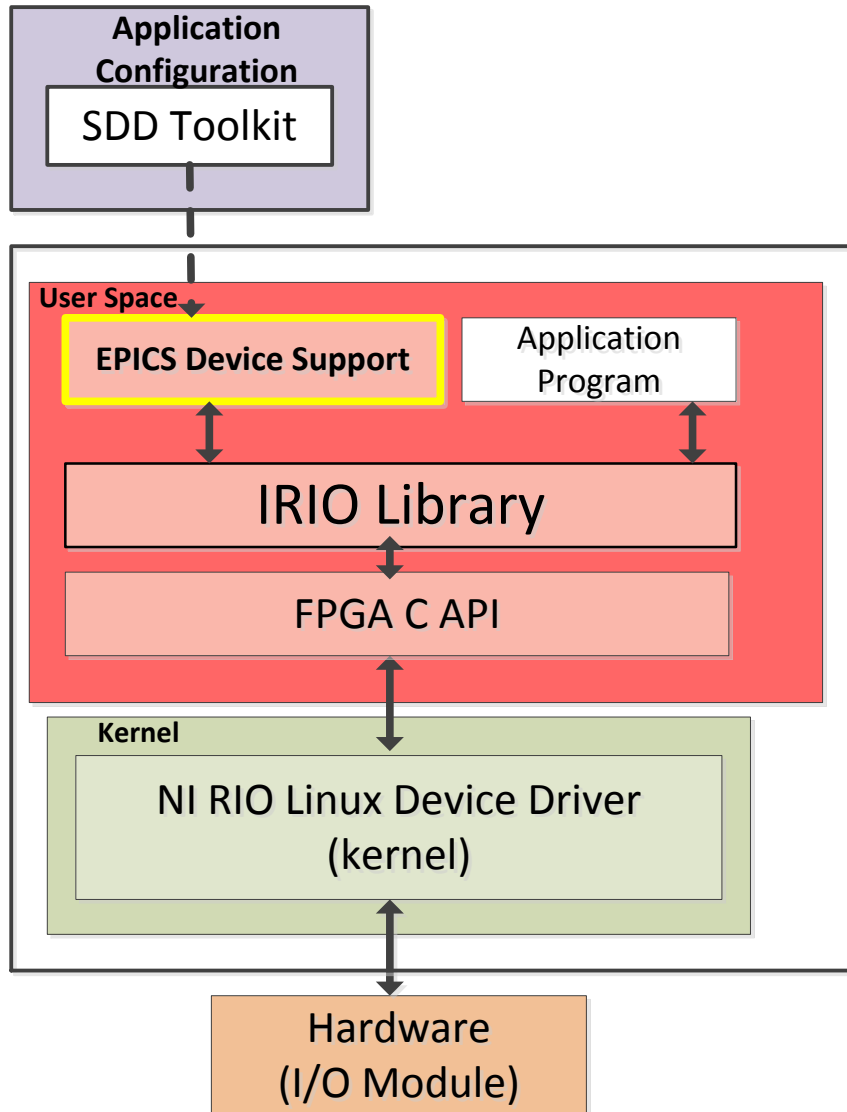


# IRIO Project: IRIO Library



- Identification of the resources implemented in the FPGA
  - The Design Rules document describes the rules for the FPGA implementation.
- Provides an API simplifying the interface with the FPGA.
  - Access to FPGA registers.
  - Analog input
  - Digital I/O
  - DMA acquisition
  - Image acquisition using cameraink
    - Serial line for camera configuration
  - Signal Generation (DDS)

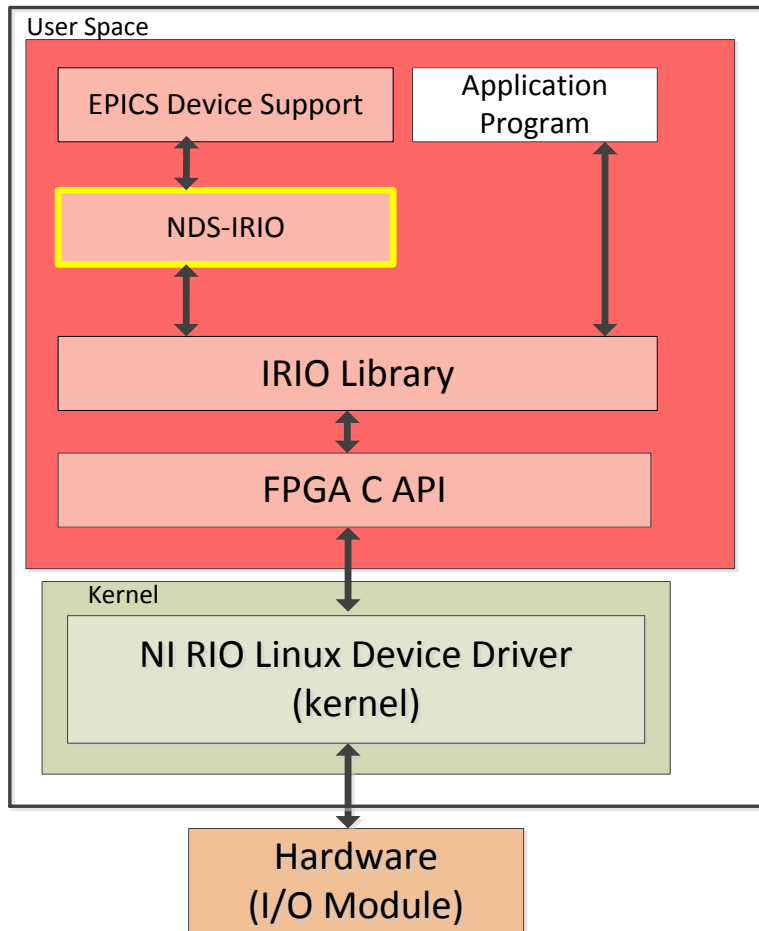
# IRIO Project: EPICS driver using asynDriver



- ✓ EPICS device driver using **asynDriver** implementation for RIO devices (FlexRIO and cRIO) using IRIO library
  - ✓ Automatically connects the PVs with FPGA resources using IRIO library.
- ✓ **If the user changes the FPGA design no compilation is needed**

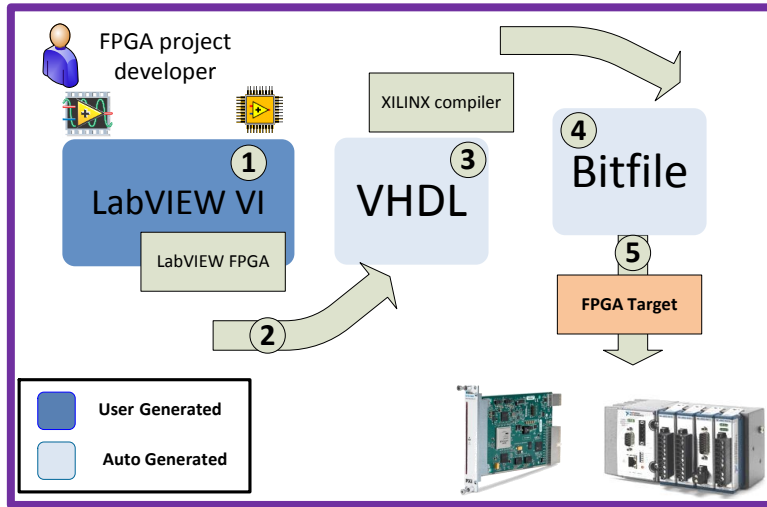


# IRIO Project: C++ classes for Nominal Device Support

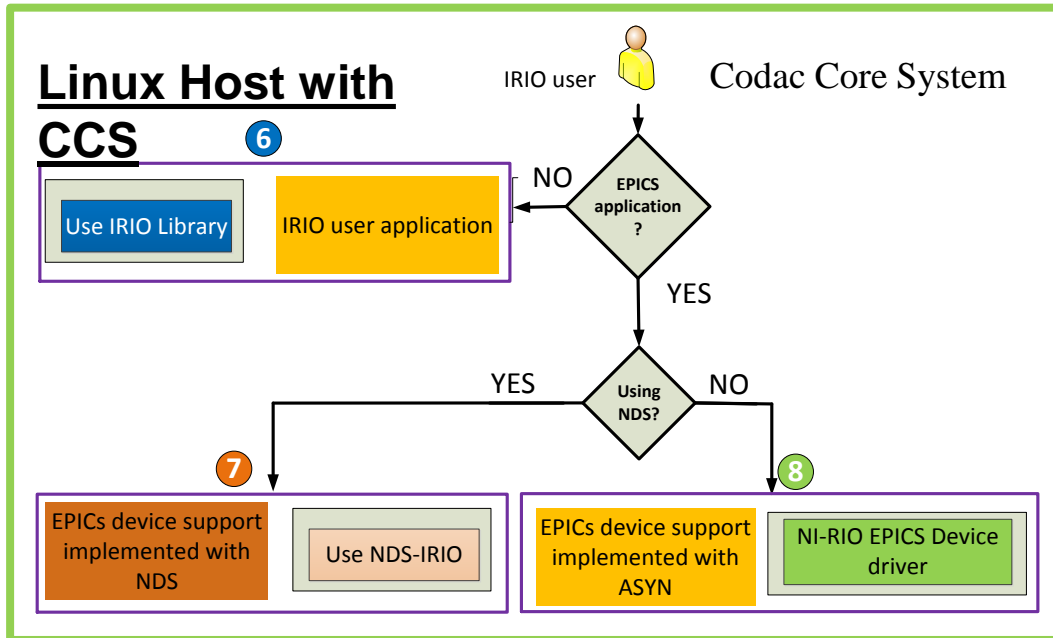
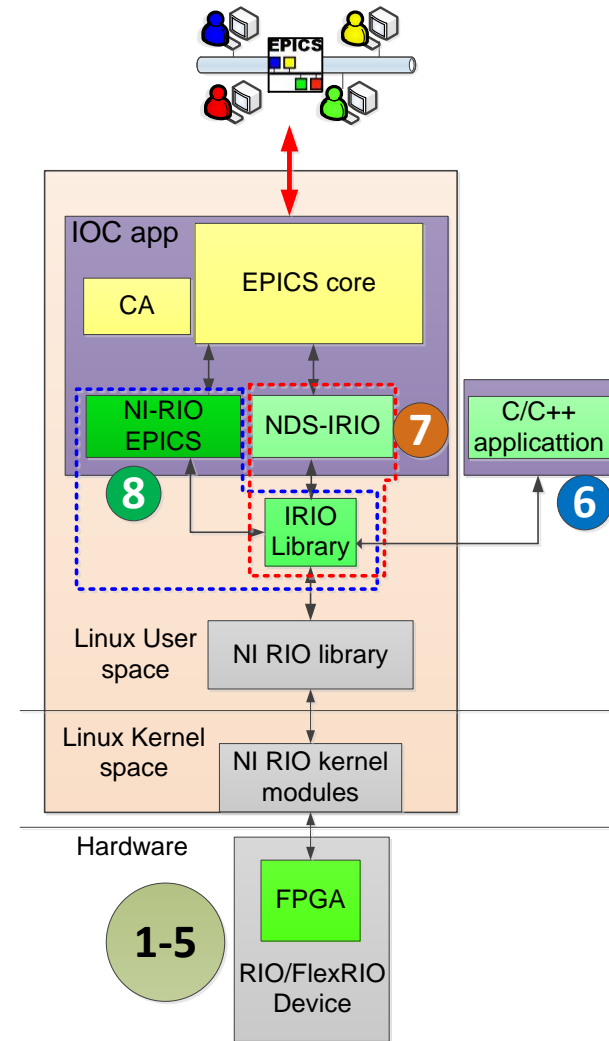


- Nominal Device Support (cosylab) approach defines a set of classes and PVs to be used for EPICS driver implementation.
- NDS-irio is the set of NDS extended classes to use FlexRIO devices
- Simplify the implementation of EPICS device support for FlexRIO using NDS

# Design Methodology



## Windows Host



# ITER PXIe Fast controller: Image acquisition (cameralink).

PICMG  
Fast Controller  
(fc18-3)



PCIe 1.1  
x4 1GB/s



NI PXIe Chassis 1065



NI PXIe 7962R + NI  
CameraLink adapter

EoSens\_3CL  
\_MC3010



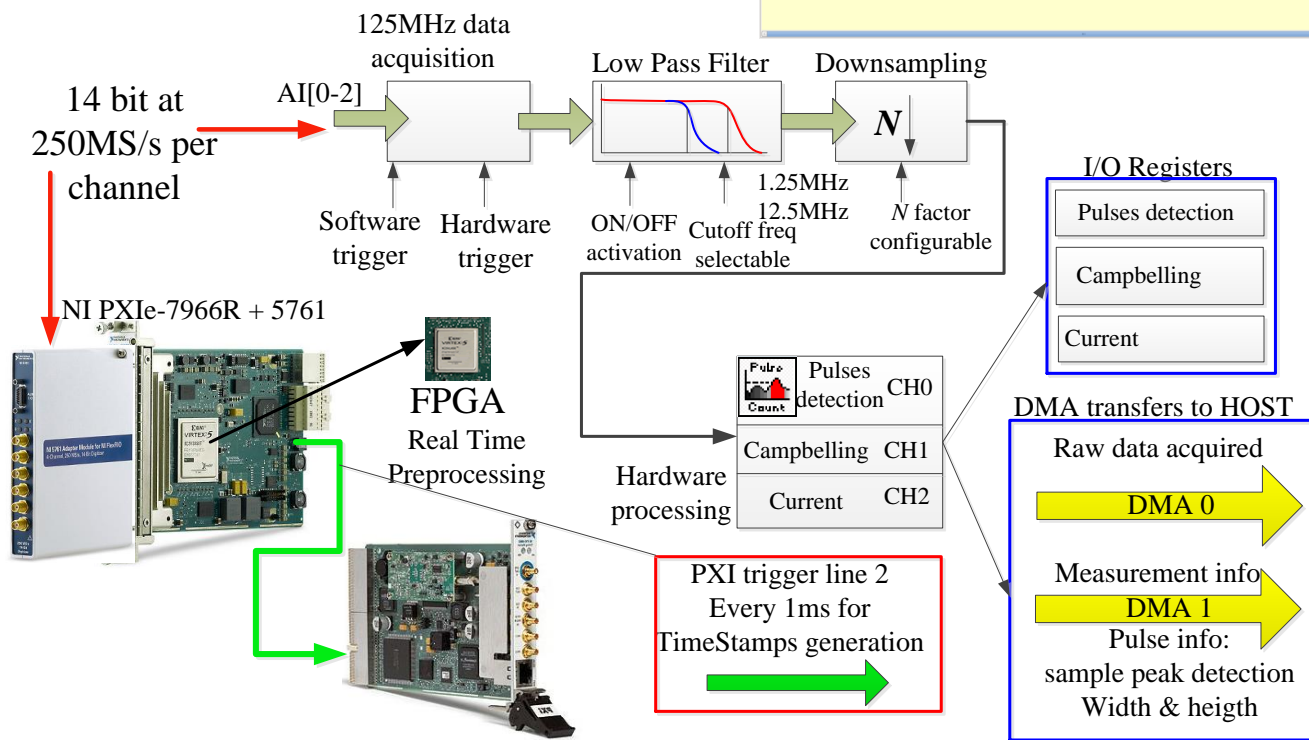
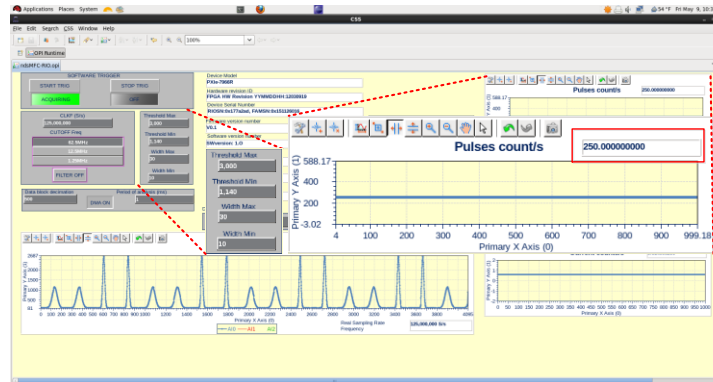
The screenshot displays a software interface for image acquisition. At the top left is a live camera feed showing a grayscale image of a document with a coordinate system (X and Y axes). To the right of the feed is a control panel with the following sections:

- ACTUAL SETTINGS:** A table showing Origin X (0 pix), Origin Y (0 pix), Width (640 pix), Height (480 pix), Resolution (307200 bps), spp (8 spp), FPS (20 fps), and FPN (ON).
- Black level <50..200>:** A field containing the value 128.
- Readback:** A blue callout bubble pointing to the FPS and FPN settings.
- Image:** A blue callout bubble pointing to the live camera feed.
- Setup:** A blue callout bubble pointing to the ACTUAL SETTINGS section.
- Device PVs:** A blue callout bubble pointing to the DEVICE CONTROL section.
- Channel PVs:** A blue callout bubble pointing to the CHANNEL GROUP CTRL section.
- Channel PVs (continued):** A blue callout bubble pointing to the IMAGE CH CTRL section.
- Channel PVs (continued):** A blue callout bubble pointing to the ROI settings section.
- Channel PVs (continued):** A blue callout bubble pointing to the FPS and Black level <50..200> section.

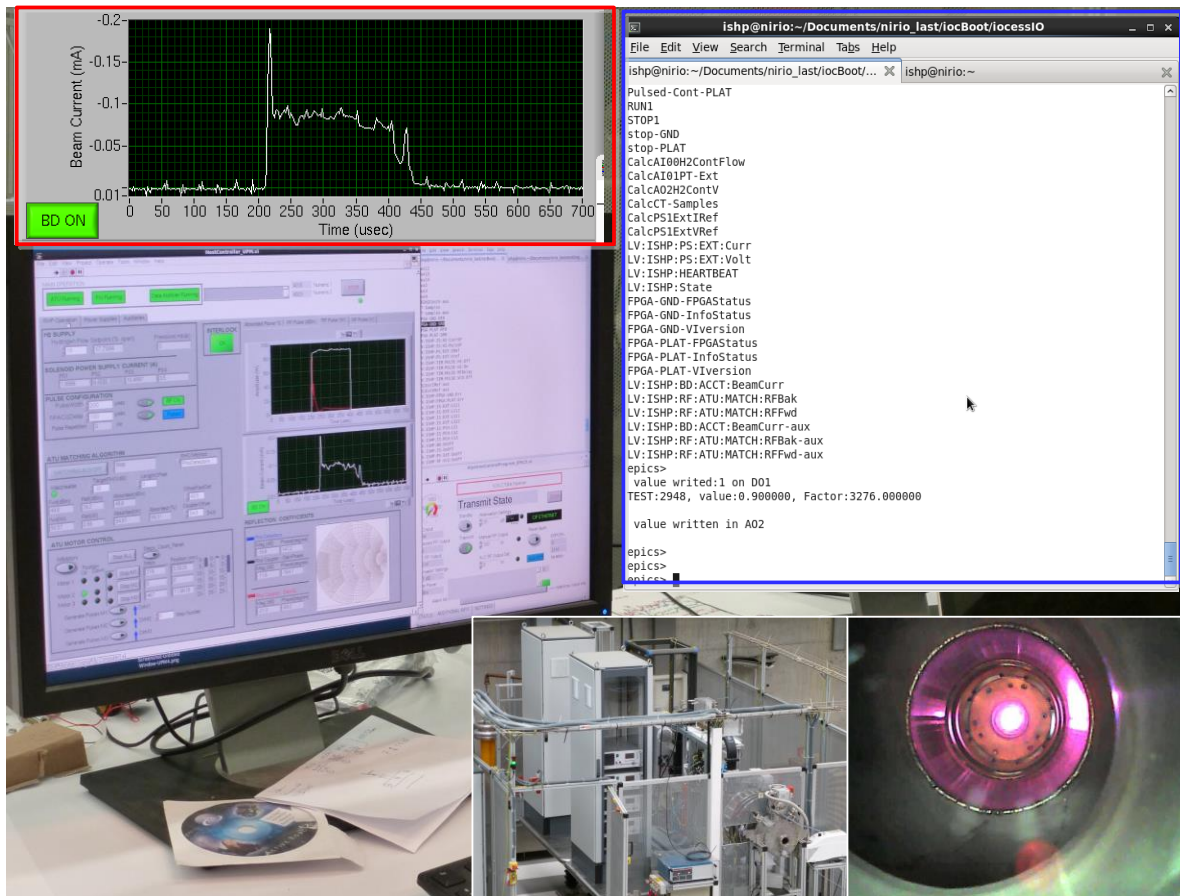
Other visible controls include 'TxUart message' (set to %k8f), 'RxUart message' (set to \*\*\*\*), 'IMAQ START/STOP' (ON), 'DEVICE CONTROL' (ON), 'CHANNEL GROUP CTRL' (START, PROCESSING), 'IMAGE CH CTRL' (START, PROCESSING), 'ROI settings' (Origin X: 0 pix, Origin Y: 0 pix, Width: 640 pix, Height: 480 pix, LOAD Conf), and 'FPS' (20 fps).

# ITER Fission chamber diagnostic use case application based on FlexRIO

- Integrates deterministic diagnostic into the FPGA (4 ADC sampling at 125MS/s). Data processing to detect/count pulses, RMS, and campbelling.

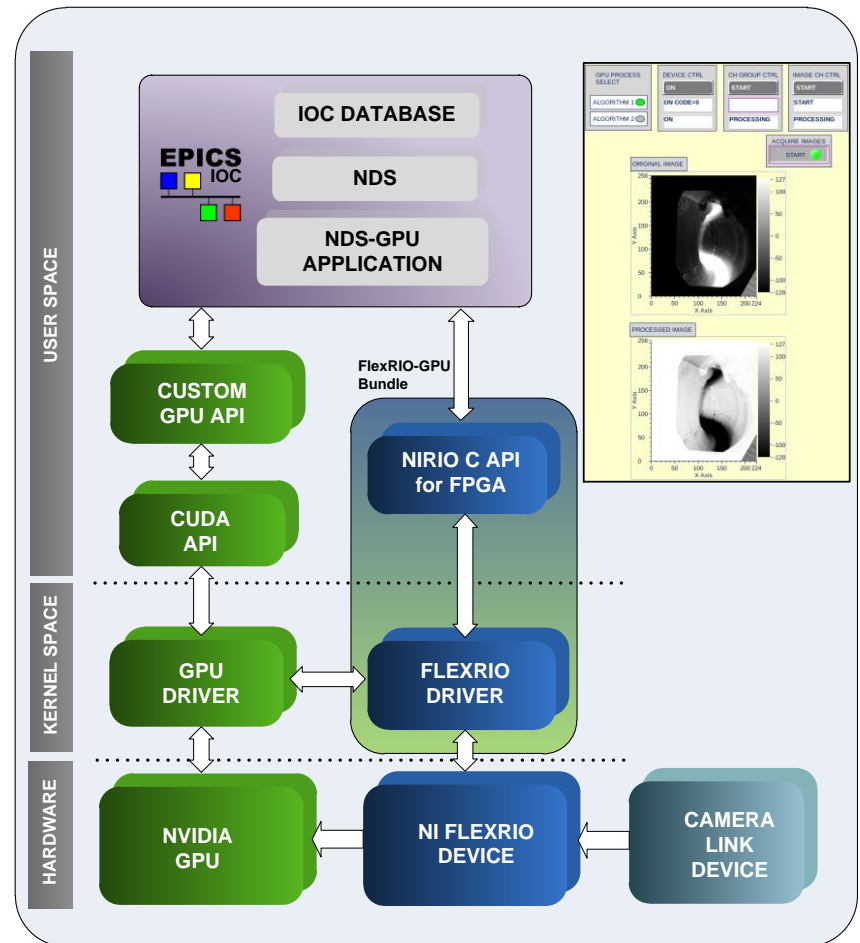
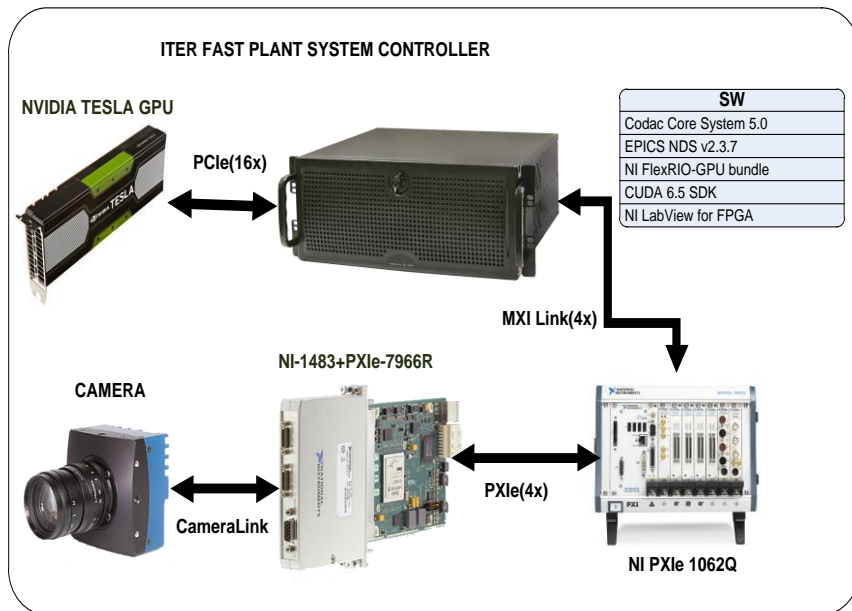


- Control and monitorization of the Ion Source Hydrogen Positive (ISHP): PXI-7852R



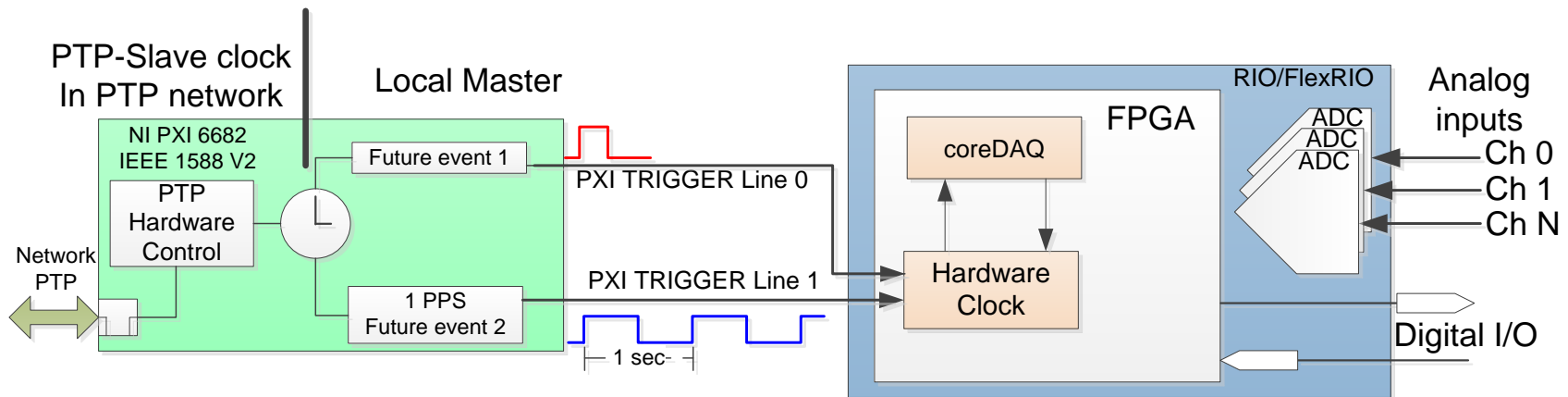


- NI-RIO Linux Device Driver modified to implement direct DMA from FPGA to GPU



## Other Applications

- Integration of Hardware clock into the RIO/FlexRIO devices synchronized with IEEE1588-V2 (tenth of nanoseconds accuracy)
  - Allows real-time timestamping in the DAQ for all acquired data (or blocks) without CPU intervention. Very useful for timestamped data streaming.
  - It requires a PXI device compliant with PTP-V2.



# Conclusions

- We have defined a design methodology for implementing advanced data and image acquisition applications with RIO/FlexRIO devices, integrated with EPICS using IRIO software.
- We have developed different LabVIEW/FPGA patterns and libraries for RIO devices.
- It is not necessary to rewrite or even recompile the EPICS device support for every RIO/FlexRIO configuration.
- IRIO tools integrated in ITER CODAC Core System V5.2 (February 2016)
- IRIO tools are GPLv2.
- Current users of IRIO:
  - ITER Diagnostics use cases: KSTAR project (FlexRIO), Russian DA (cRIO).
  - University of Basque Country/ESS Bilbao





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Thank you very much for your attention!!  
questions?