# DEVELOPMENT OF ADVANCED DATA AND IMAGE ACQUISITION SYSTEMS USING RIO TECHNOLOGY AND EPICS: INTEGRATION IN ITER

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# Outline

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  - ESS-Bilbao/University of Basque Country
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- Future works
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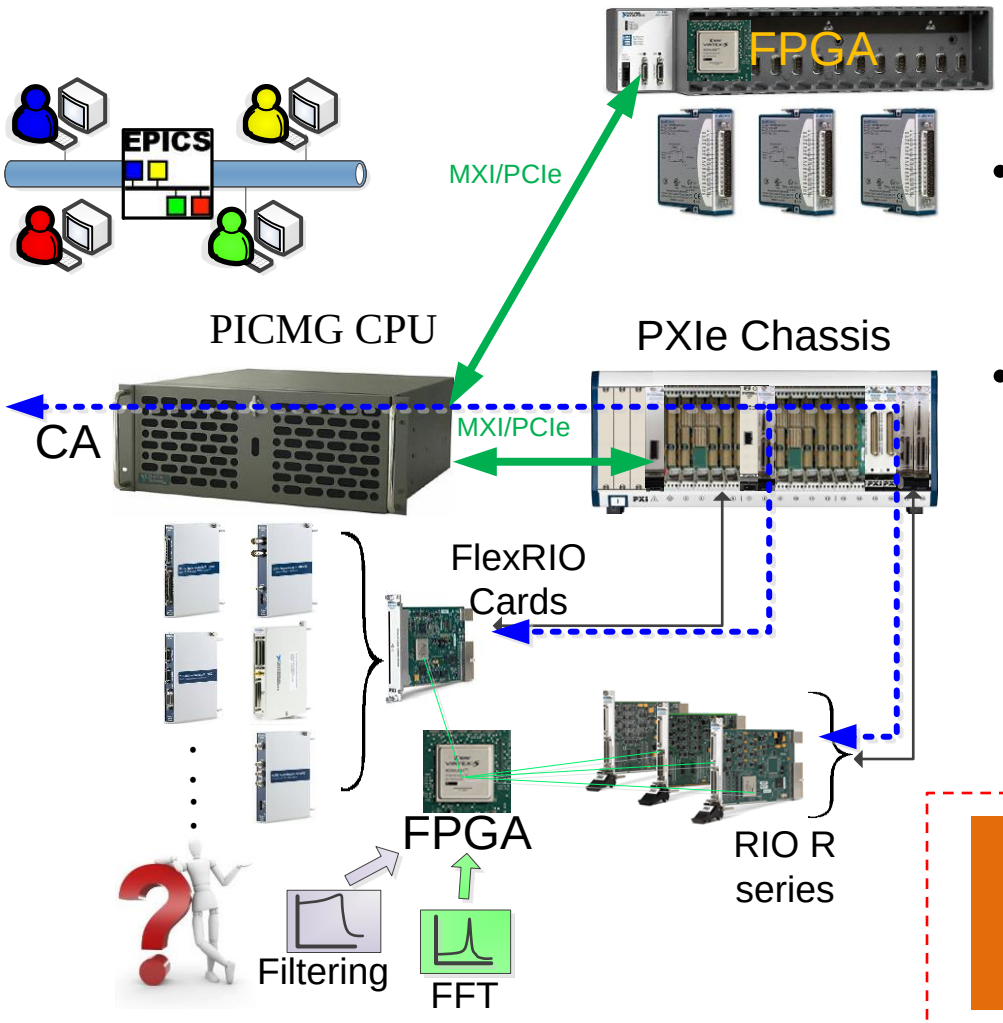
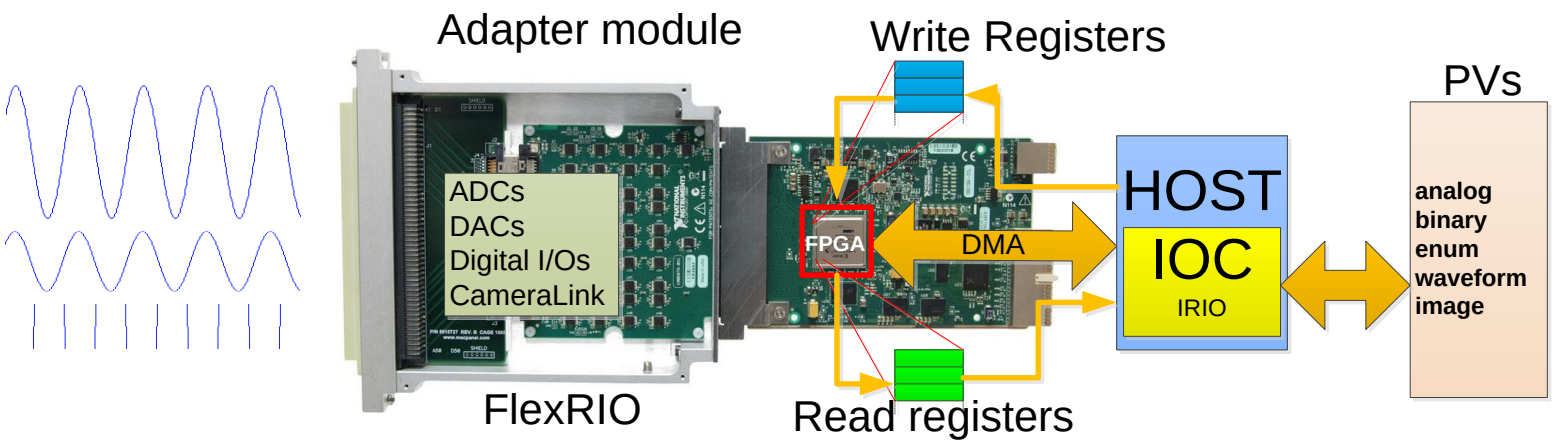
# Motivation




- FPGAs provide reconfigurable hardware with deterministic data preprocessing capabilities
- EPICS is a very common solution for SCADA in large scientific experiments
- The combination of both technologies simplifies the development of complex data acquisition and processing systems.

**I-RIO is a set of software tools simplifying the integration of RIO devices in EPICS**

# RIO/FlexRIO Devices



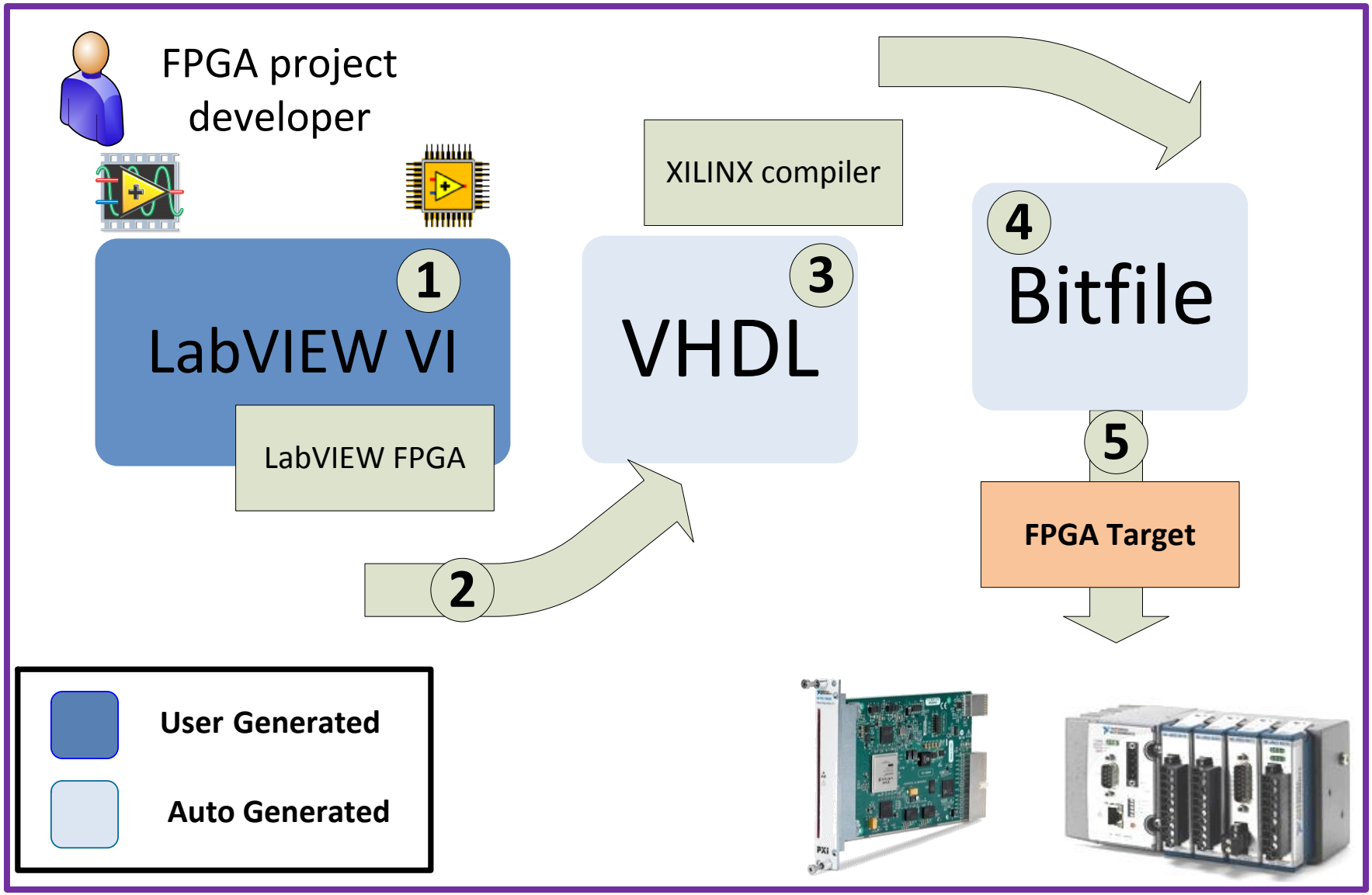

1

**The user defines the functionality programming the FPGA**

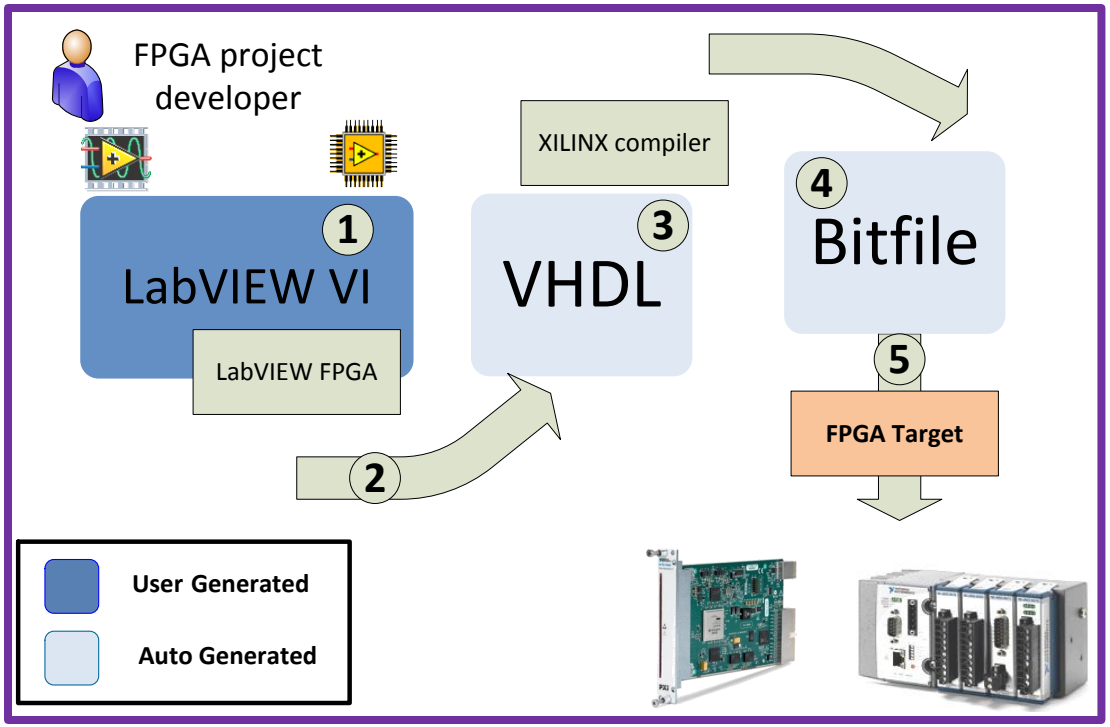
2

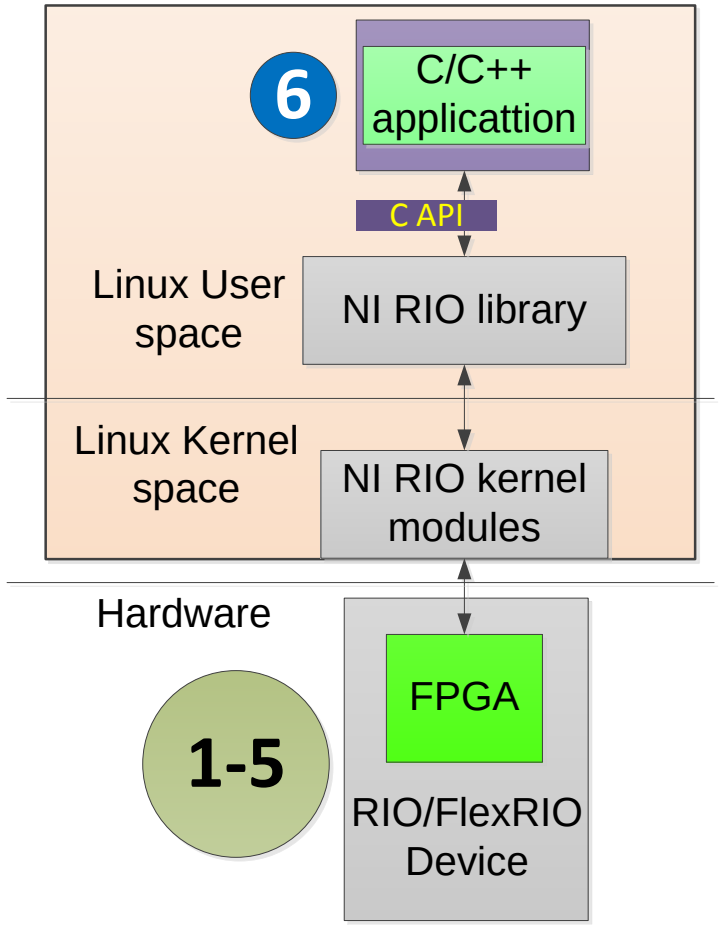
**EPICS connects a user defined device with PVs for configuration and supervision**

# Development cycle: LabVIEW for FPGA

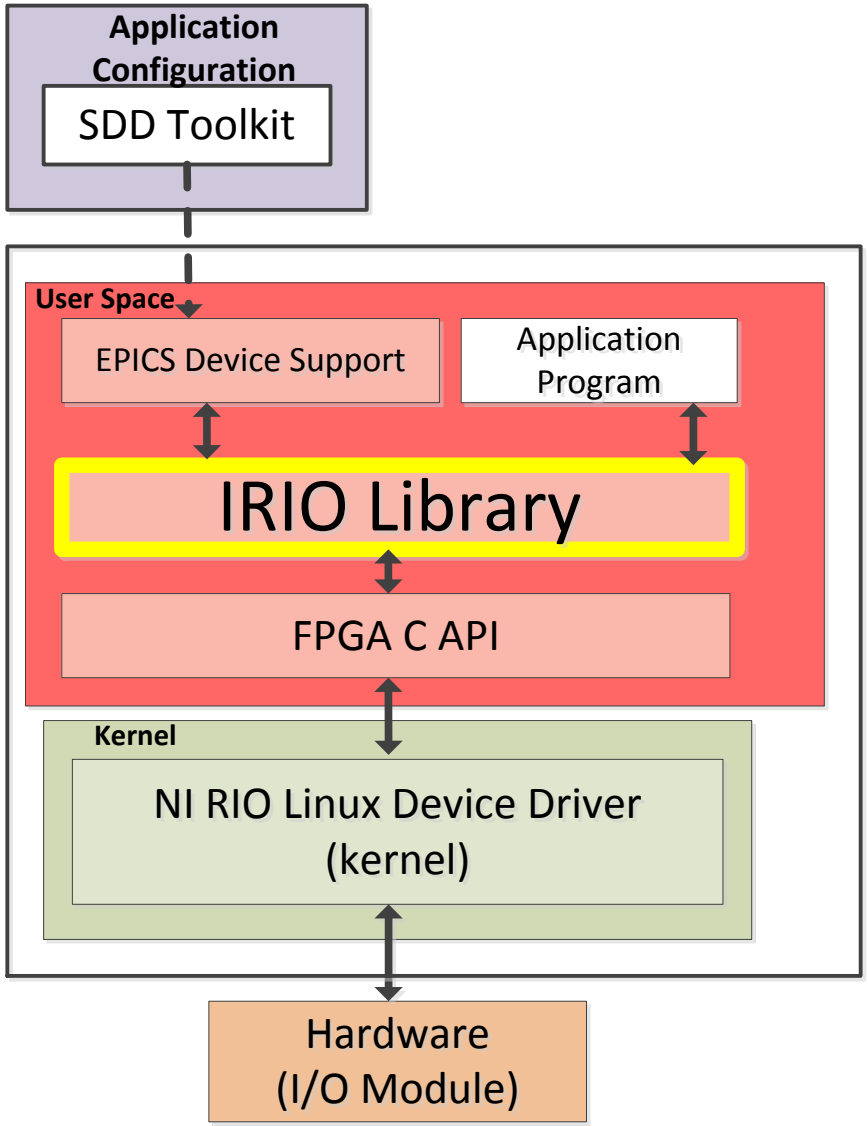


# Using RIO devices in Linux



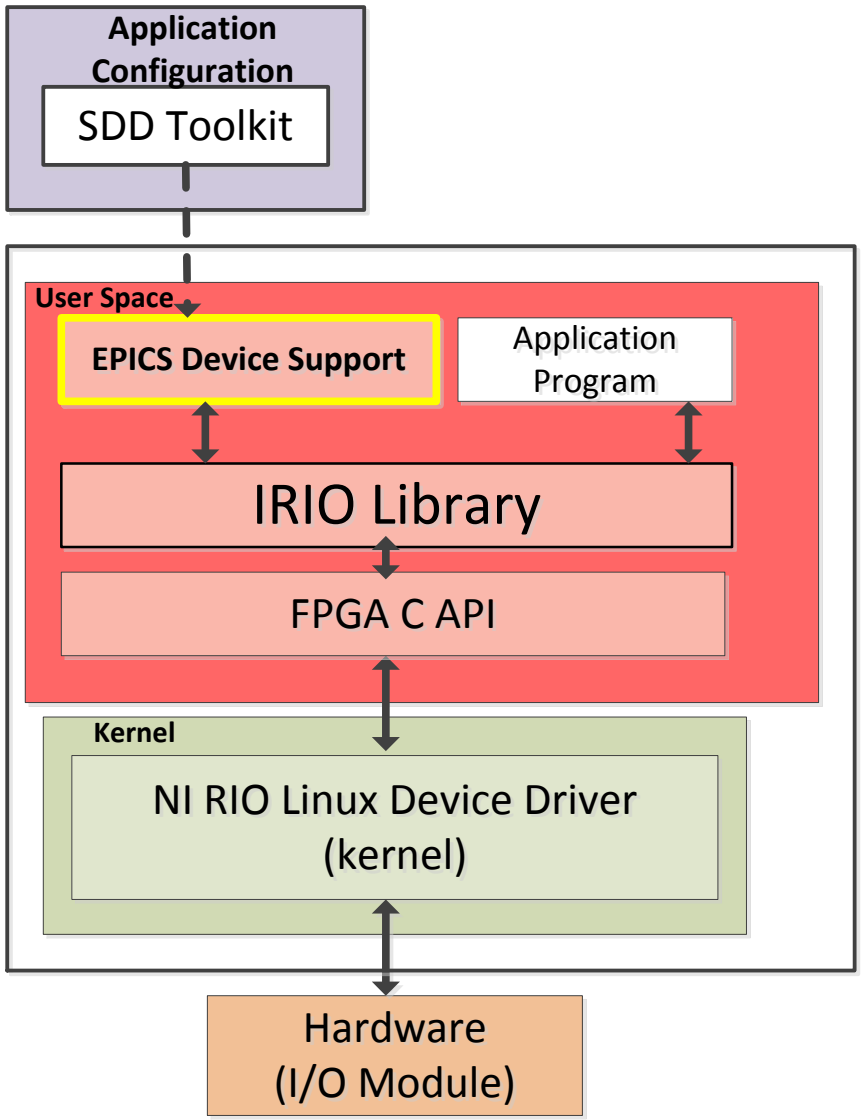



# IRIO Project: IRIO Library



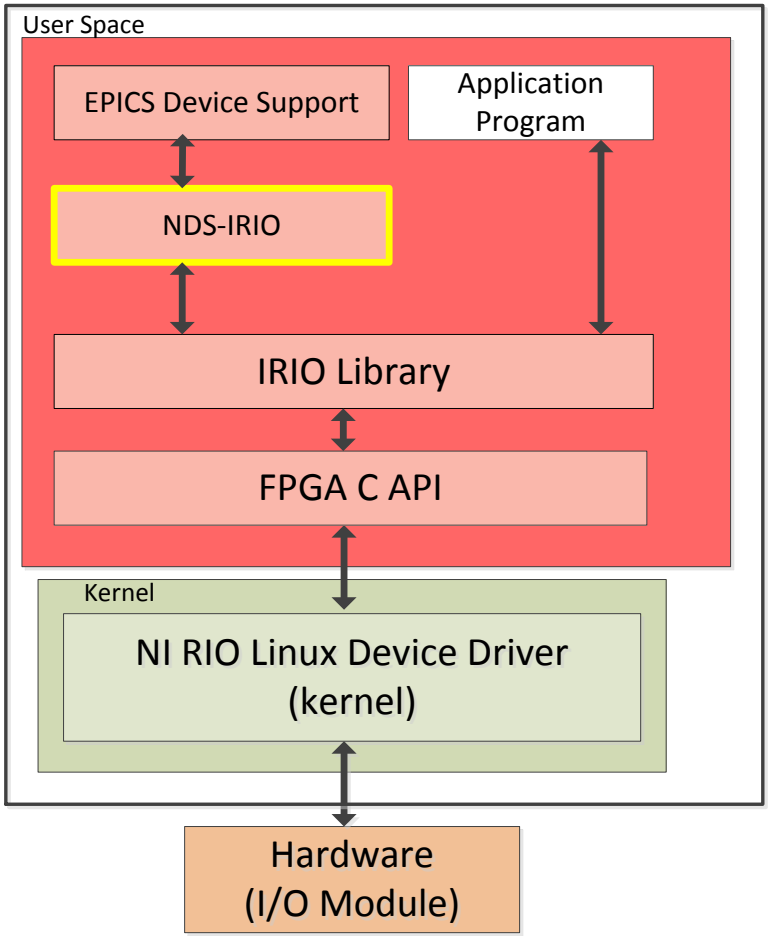

- Identification of the resources implemented in the FPGA
  - The Design Rules document describes the rules for the FPGA implementation.
- Provides an API simplifying the interface with the FPGA.
  - Access to FPGA registers.
  - Analog input
  - Digital I/O
  - DMA acquisition
  - Image acquisition using cameralink
    - Serial line for camera configuration
  - Signal Generation (DDS)

# IRIO Project: EPICS driver using asynDriver



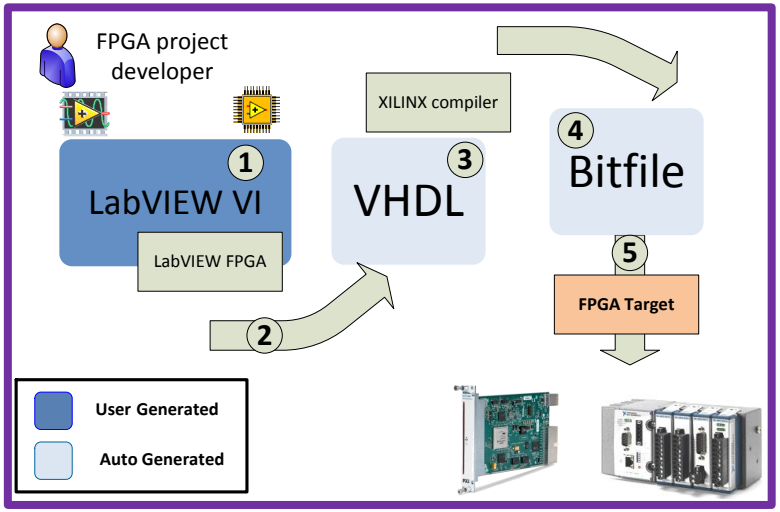

- ✓ EPICS device driver using asynDriver implementation for RIO devices (FlexRIO and cRIO) using IRIO library
  - ✓ Automatically connects the PVs with FPGA resources using IRIO library.
- ✓ If the user changes the FPGA design no compilation is needed

# IRIO Project: C++ classes for Nominal Device Support

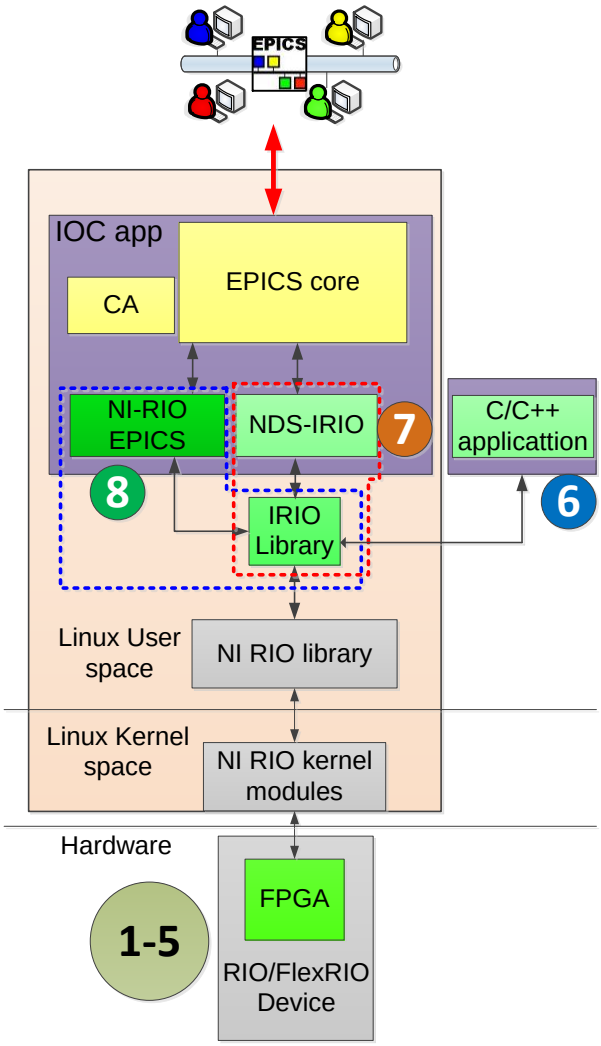



- Nominal Device Support (cosylab) approach defines a set of classes and PVs to be used for EPICS driver implementation.
- NDS-irio is the set of NDS extended classes to use FlexRIO devices
- Simplify the implementation of EPICS device support for FlexRIO using NDS

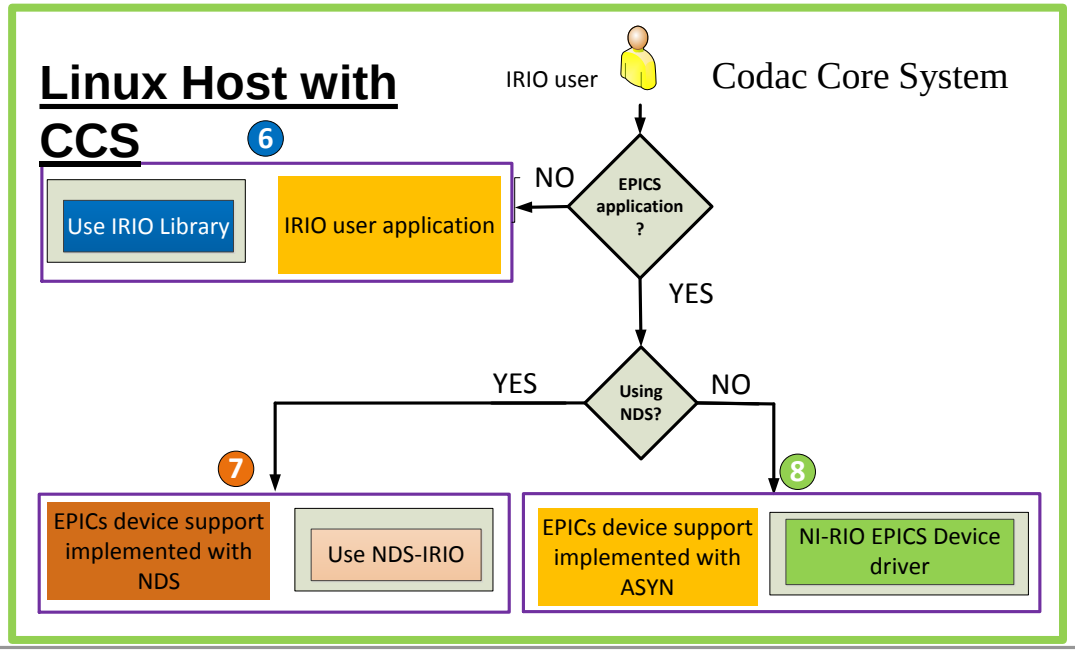
# Design Methodology



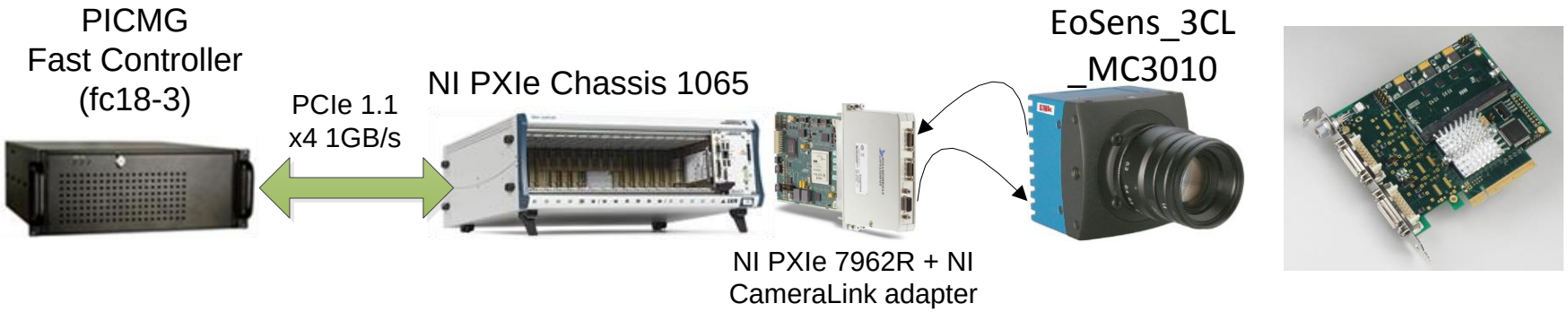

## Windows Host

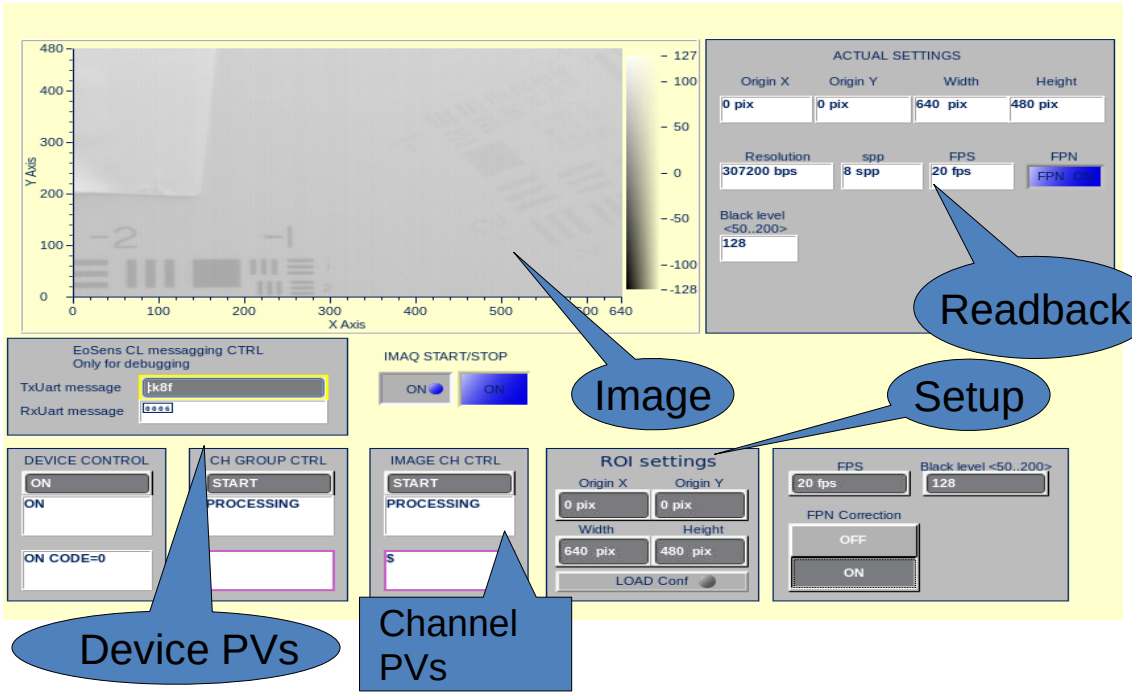



## Linux Host with CCS



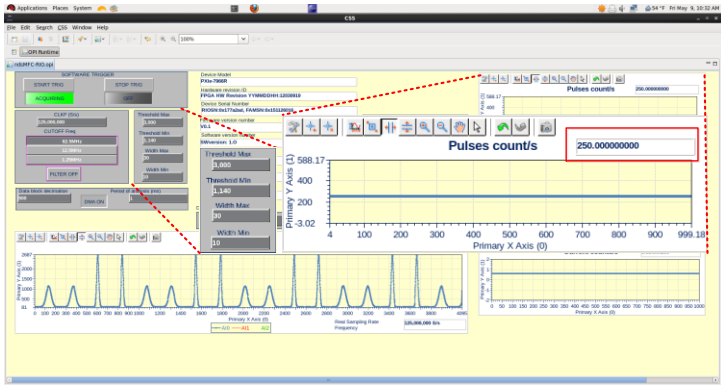
# ITER PXIe Fast controller: Image acquisition (cameralink).

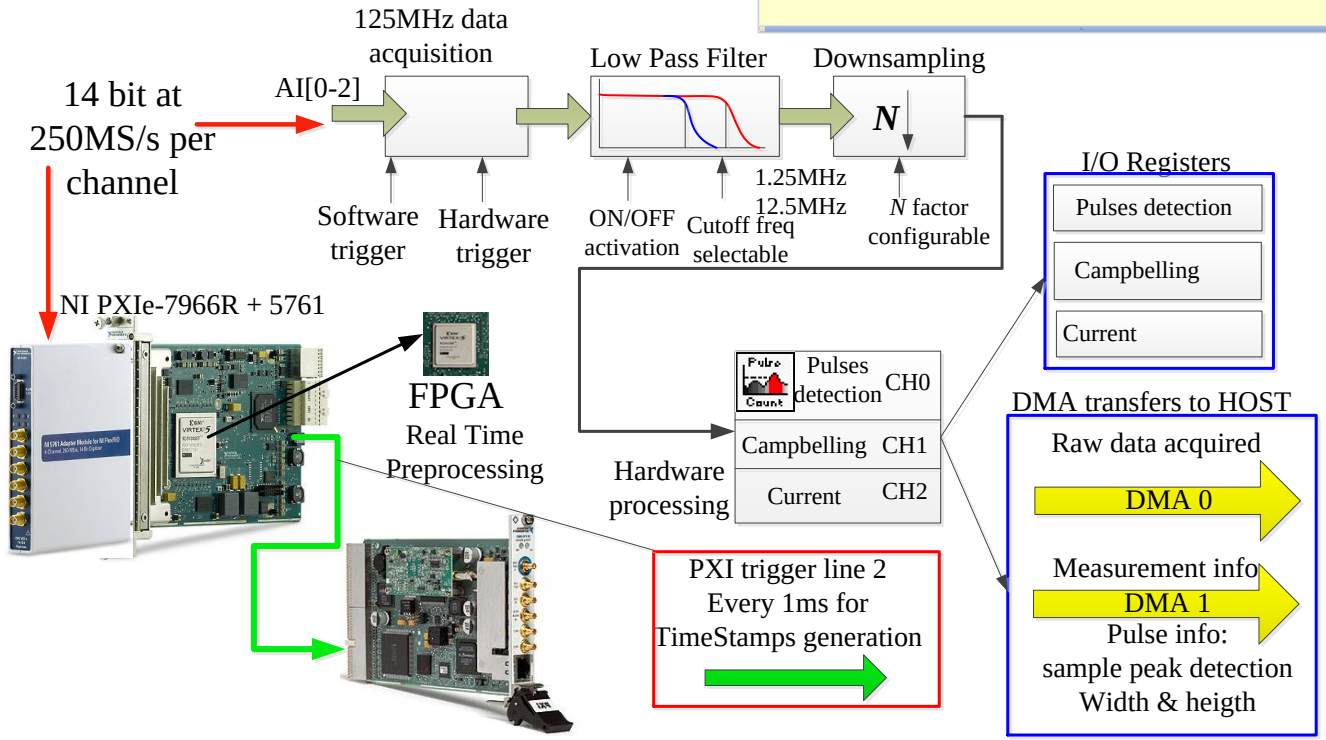


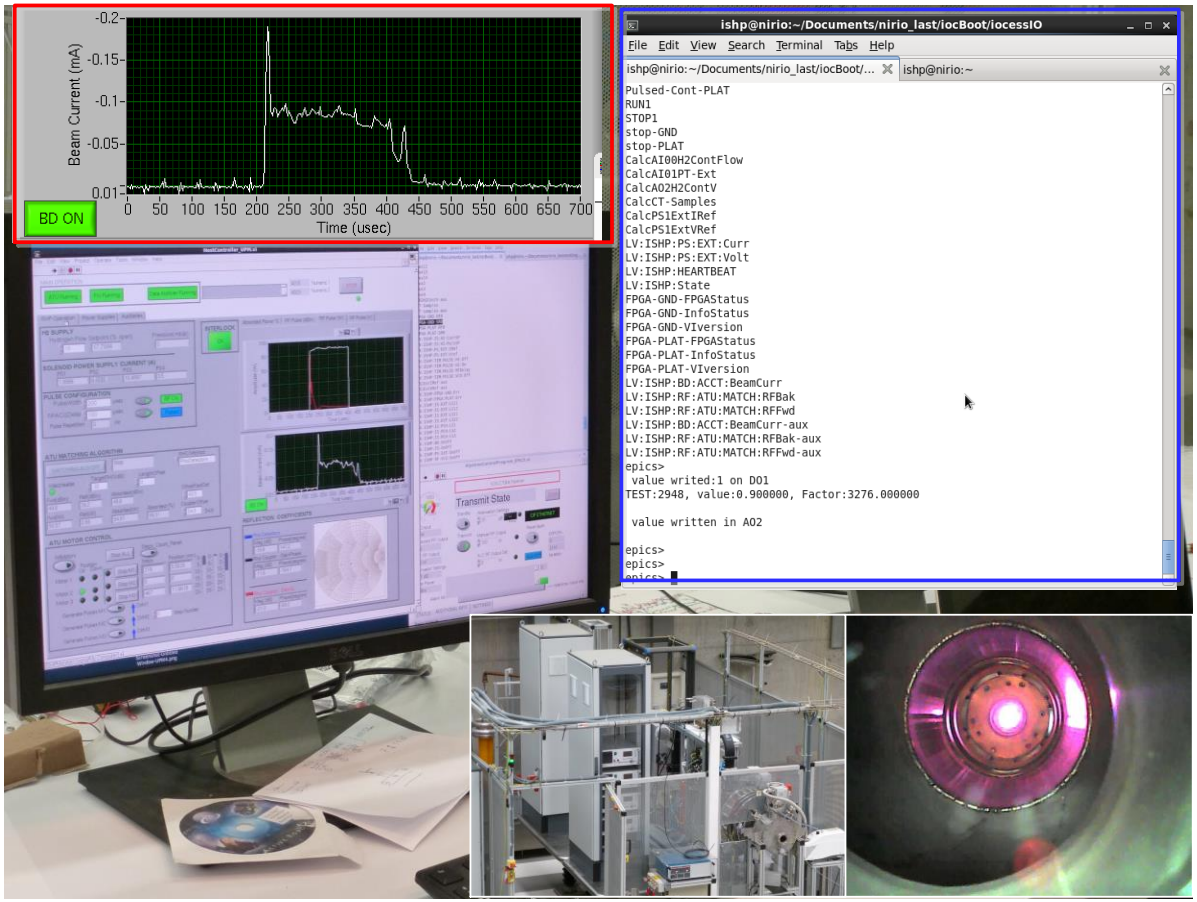
# ITER Fission chamber diagnostic use case application based on FlexRIO

- Integrates deterministic diagnostic into the FPGA (4 ADC sampling at 125MS/s). Data processing to detect/count pulses, RMS, and campbelling.



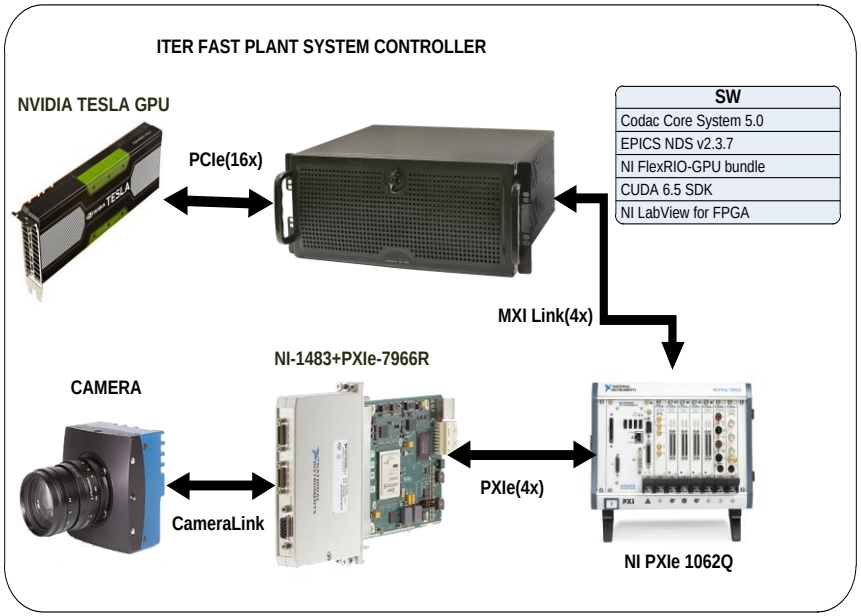



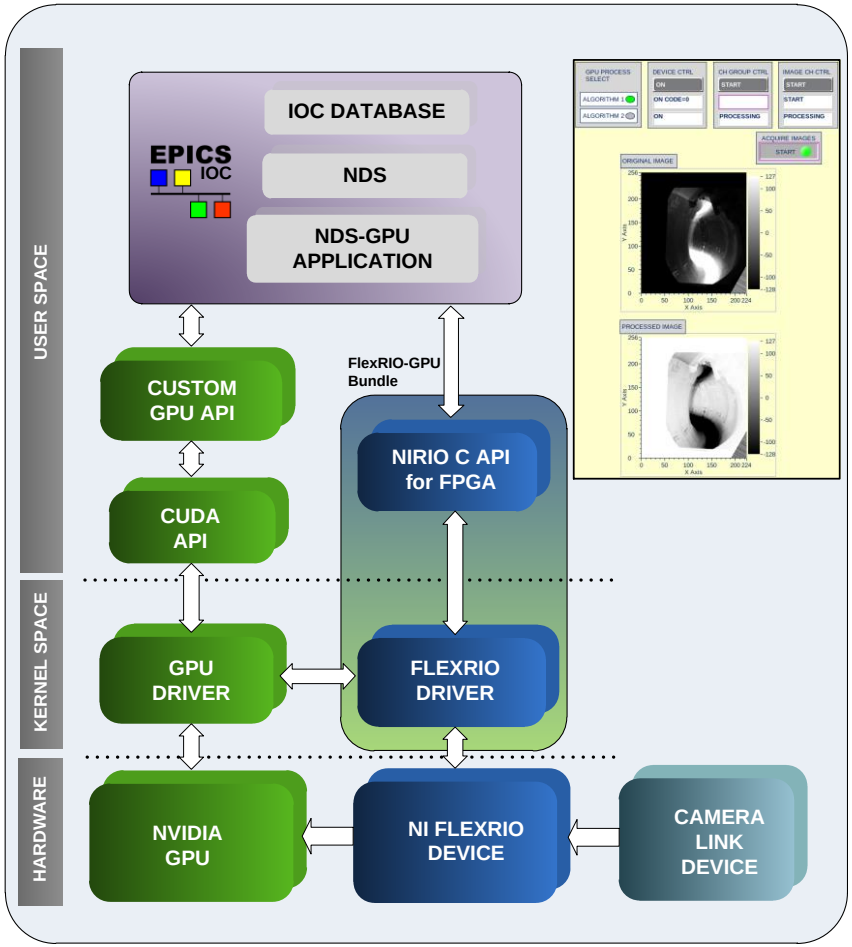
- Control and monitorization of the Ion Source Hydrogen Positive (ISHP): PXI-7852R



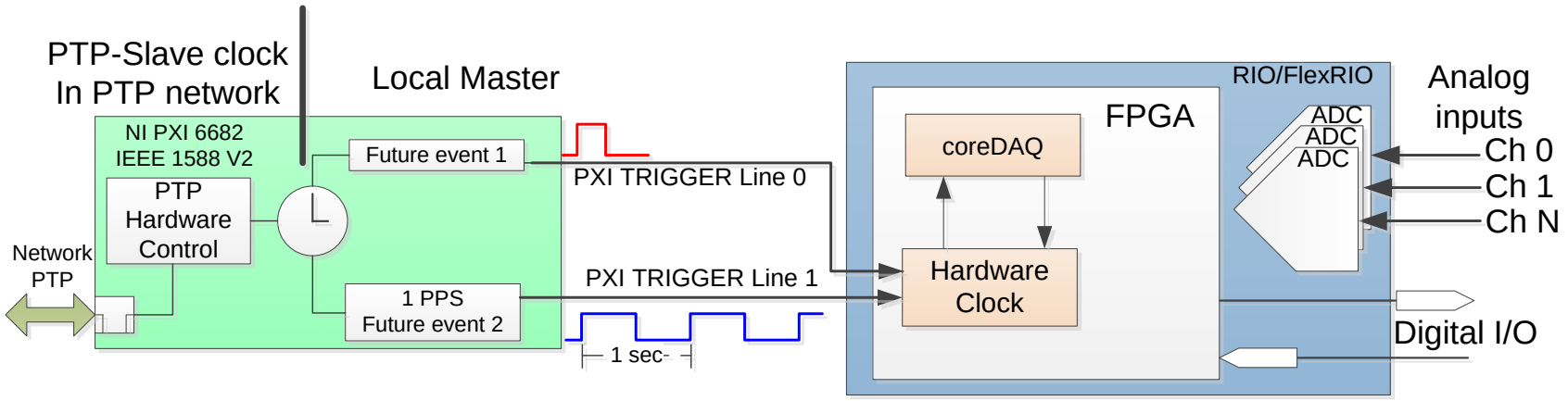
# FPGA+GPU processing

- NI-RIO Linux Device Driver modified to implement direct DMA from FPGA to GPU



- Integration of Hardware clock into the RIO/FlexRIO devices synchronized with IEEE1588-V2 (tenth of nanoseconds accuracy)
  - Allows real-time timestamping in the DAQ for all acquired data (or blocks) without CPU intervention. Very useful for timestamped data streaming.
  - It requires a PXI device compliant with PTP-V2.



# Conclusions

- We have defined a design methodology for implementing advanced data and image acquisition applications with RIO/FlexRIO devices, integrated with EPICS using IRIO software.
- We have developed different LabVIEW/FPGA patterns and libraries for RIO devices.
- It is not necessary to rewrite or even recompile the EPICS device support for every RIO/FlexRIO configuration.
- IRIO tools integrated in ITER CODAC Core System V5.2 (February 2016)
- IRIO tools are GPLV2.
- Current users of IRIO:
  - ITER Diagnostics use cases: KSTAR project (FlexRIO), Russian DA (cRIO).
  - University of Basque Country/ESS Bilbao

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Thank you very much for your attention!!

questions?