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Ciemat · Centro de Investigaciones Energéticas, Medioambientales y Tecnológicas

Implementation of Distributed Image Acquisition and Processing System based on FlexRIO, CameraLink and areaDetector

S. Esquembri[a], M.Ruiz[a], E.Barrera[a], D.Sanz[a], A.Bustos[a], R. Castro[b], J.Vega[b]

[a]Instrumentation and Applied Acoustic Research Group, Technical University of Madrid (UPM), Madrid, Spain. Email: s.esquembri@upm.es
[b]Data acquisition Group EURATOM/CIEMAT Association for Fusion, Madrid, Spain

ABSTRACT

Image processing systems are commonly used in nuclear fusion experiments. This experiments usually require of multiple cameras of different characteristics, complicating its integration and the complexity of the acquisition system. This works presents the implementation of a distributed image acquisition and processing system for CameraLink cameras. The framegrabber is implemented FlexRIO devices, reconfigurable hardware devices with real-time preprocessing capabilities based on Field Programmable Gate Arrays (FPGAs). The frame grabber is integrated into Experimental Physics and Industrial Control System (EPICS) using the areaDetector EPICS software module, which offers a common interface shared among tens of cameras to configure the image acquisition and process these images in a distributed control system. The use of areaDetector also allows the image processing to be parallelized and concatenated using: multiple computers; areaDetector plugins; and the areaDetector standard type for data, NDArrays. The architecture developed is fully compatible with ITER Fast Controllers and the entire system has been validated using a camera hardware simulator that stream videos from fusion experiment databases.

HARDWARE ARCHITECTURE
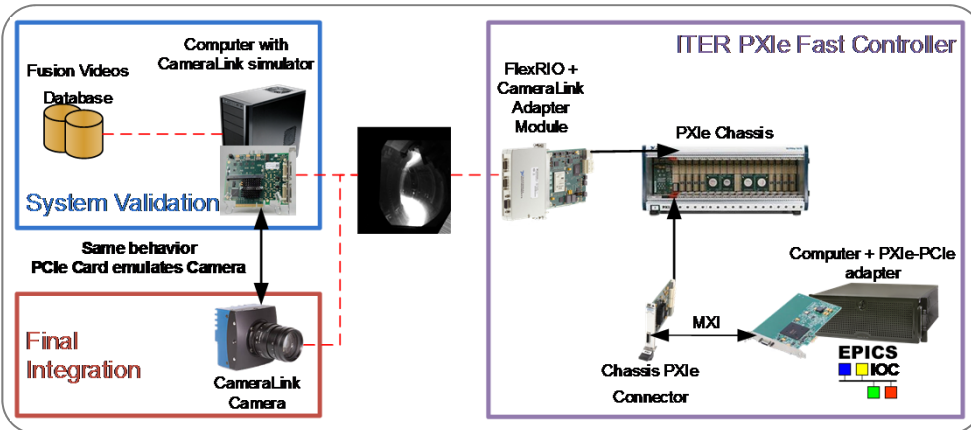
- Fully compatible with ITER Fast Plant System Controllers
- Framegrabber implemented with reconfigurable hardware:
  - Hardware timestamping
  - Preprocessing capabilities
- Using CameraLink standard:
  - High throughput (up to 850MB/S)
  - Wide range of cameras available
  - Camera simulator for validation and testing

SOFTWARE ARCHITECTURE
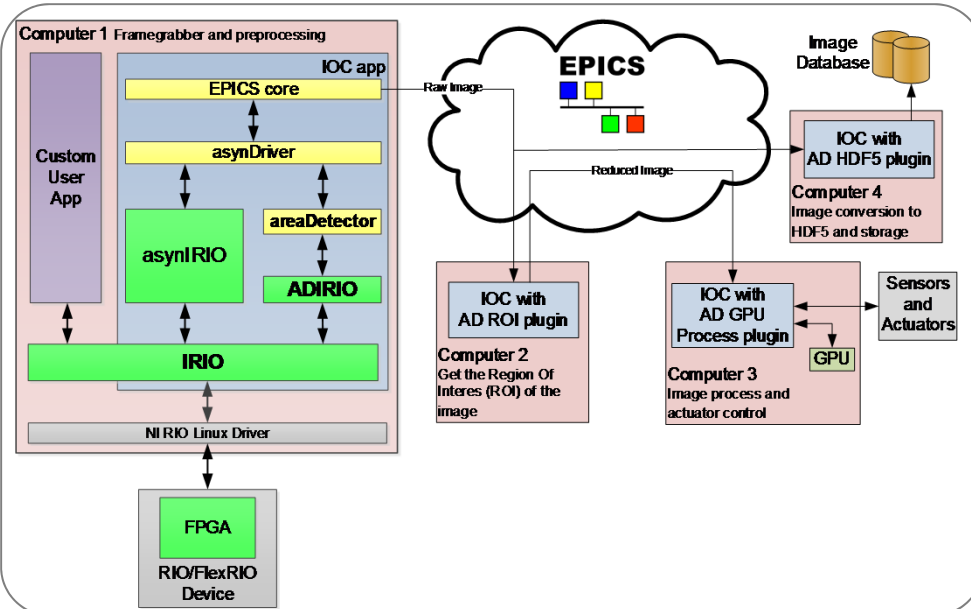
- Using IRIO methodology (Design rules + C Library)
  - Hardware implemented resources available using high level API oriented to DAQ/IMAQ systems
  - Several EPICS interfaces available
    - asynDriver
    - NDS
    - **areaDetector**
- Using areaDetector:
  - High flexibility/configurability
  - Easy to pipeline/parallelize image processing
  - Standardized PVs for easy integration and unified control
  - Multiple image process plugins already available

METHODOLOGY

1. Include the user custom image preprocessing in the LabVIEW FPGA template.
2. Compile the template using LabVIEW tools
3. Configure processing chain using existing or custom plugins even during the acquisition.

ACKNOLEDGEMENTS

CONCLUSIONS

- Fully compatible with ITER FPSC architecture
- Compatible with wide range of cameras (CameraLink standard)
- Easy integration and acquisition control (EPICS + areaDetector)
- Acquiring images at simulator top speed (680MB/s)
- Processing chain easy to configure