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High Performance Image Acquisition and Processing Architecture for Fast Plant System Controllers based on FPGA and GPU

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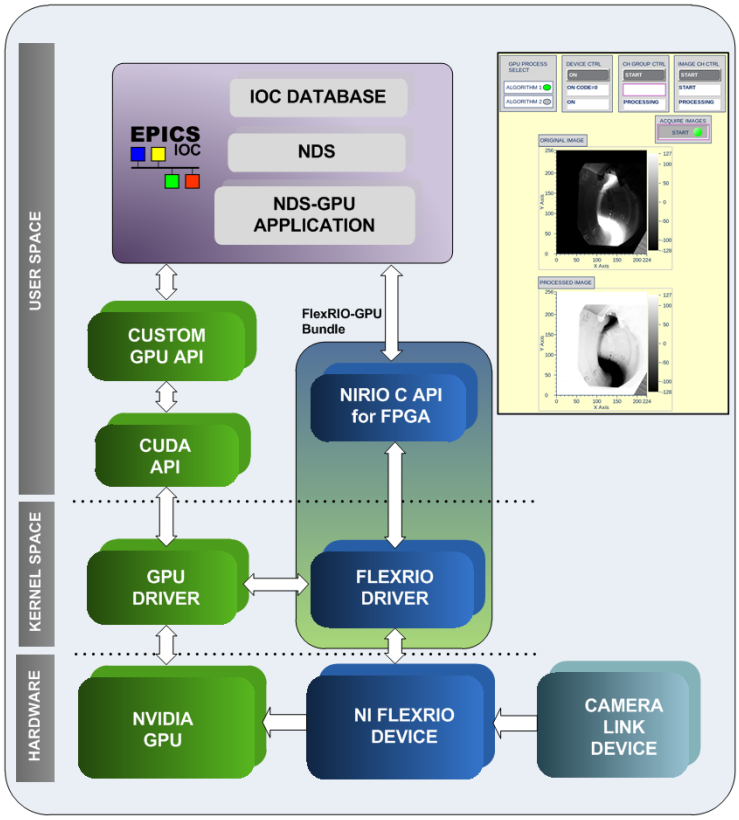
ABSTRACT

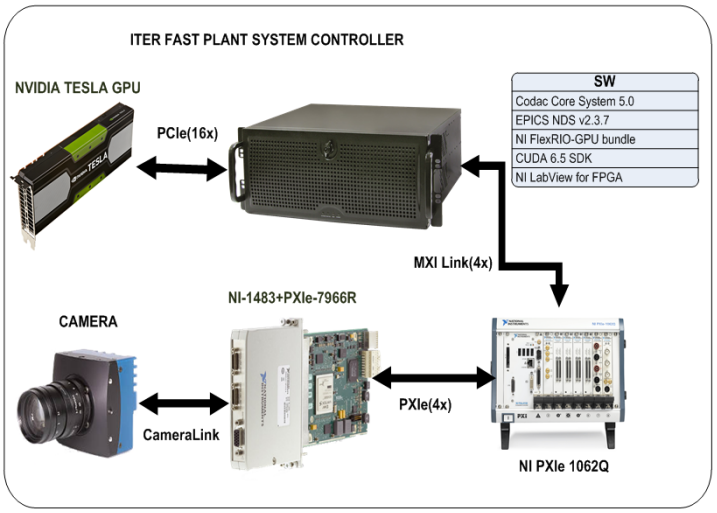
The two dominant technologies that are being used in real time image processing are FPGA and GPU due to their algorithm parallelization capabilities. But not much work has been done to standardize how these technologies can be integrated in data acquisition systems where control and supervisory requirements are in place, such as ITER. This work tests an image acquisition and processing system for Cameralink devices based in a FPGA DAQ device (National Instruments FlexRIO technology) and a NVIDIA Tesla GPU series card. This integration, compliant with ITER fast controller solutions, simplifies the implementation of advanced data (images) acquisition systems. The most important advantage of this solution is that data acquired from the set NI1483-NIPXIe7966R is moved directly to GPU avoiding the use of CPU memory buffers using NVIDIA GpuDIRECT RDMA technology. Thus it is possible to increase the performance of the system because CPU intervention is minimized due to data transfer is done using PCI Express and DMA. The system has been developed using CODAC Core System standards (EPICS and Nominal device Support) in order to guarantee an easy integration in ITER's solutions.

GOALS	SOLUTIONS
➢ Propose a standard methodology to include GPUs in ITER Fast Plant Controllers	✓ EPICS integration through Nominal Device Support
➢ Maximize DAQ-GPU-HOST throughput	✓ FLEXRIO-GPU bundle supporting RDMA for direct data transfers
➢ Provide seamless integration (high level access w/o GPU)	✓ High level abstraction layer that minimizes technical knowledge requirements

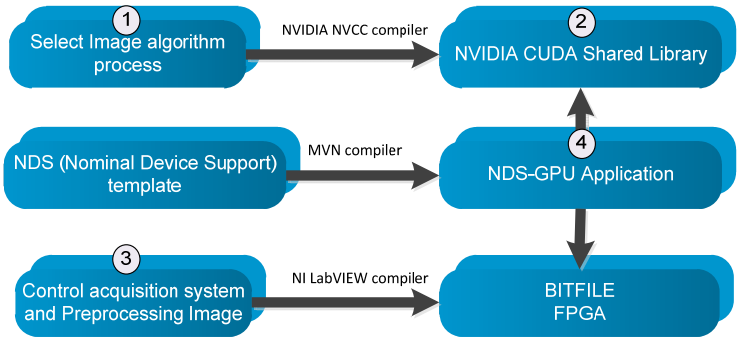
SYSTEM ARCHITECTURE



TEST SYSTEM



METHODOLOGY



1. Select a parallelized algorithm image processing for GPU.
2. Build a shared library that contains the kernel GPU process functions and managed GPU resources.
3. Implement LabVIEW Code for FPGA to control CameraLink interface.
4. Using NDS (Nominal Device Support) template, build a user application that:
   a) Acquire images from Cameralink device to GPU using GPUdirect RDMA technology.
   b) Process images in GPU.
   c) Publish and show images results using EPICS PVs in a CSS OPI panel.

CONCLUSIONS

- A model and a methodology to include GPUs in FPSCs using FlexRIO has been proposed and tested using a generic use case for continuous image acquisition and processing
- Data transfers between DAQ-GPU-HOST are maximized by using RMDA technology avoiding unnecessary memory copies
- GPU processing algorithms can be easily updated through the CUDA Shared Library provided.
- Full integration in EPICs is provided through Nominal Device Support

ACKNOWLEDGEMENTS

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