Contribution ID: **112** Type: **not specified**

PixFEL: high resolution, fast, multi-tier detectors for diffraction imaging at next generation X-ray FELs

The use of large accelerator-driven X-ray sources, such as those available at the synchrotron light and X-ray free-electron lasers (FEL) facilities, continues to grow and expand to many scientific disciplines worldwide. These research centers are now driving the state of the art of X-ray science, therefore shaping the requirements for many types of X-ray detectors. X-ray FELs in particular can offer unprecedented capabilities in penetrating the microscopic structure of organic and inorganic systems, new materials and matter under extreme conditions and in recording and understanding the time evolution of fast biochemical phenomena at the nanoscale.
The aim of the PixFEL collaboration is to provide the X-ray FEL users community with a new, hybrid pixel detector for X-ray diffraction imaging applications compliant with the very challenging specifications set by fourth generation FELs in terms of input dynamic range, processing speed, amplitude measurement resolution and radiation hardness. The detector will have a multi-tier structure. The sensitive layer will consist of a slim edge silicon pixel detector to minimize the dead area at the sensor edge. The front-end chip will result from the vertical integration of two layers, one devoted to the analog front-end and the ADC, the second one to dedicated memories used to accumulate data in applications with high X-ray pulse rates. The analog processor is based on a time variant solution, including a charge preamplifier with a dynamic compression feature based on the non linear characteristic of a MOSFET capacitor. The converter relies on a 10 bit resolution, time interleaved, SAR architecture with split capacitor DAC. The power dissipation per channel, including dynamic power consumption in the SAR ADC, is about 230 uW. A 65 nm CMOS technology will be used to accommodate all the needed functions in a pixel pitch of 100 um. More scaled technologies may be employed in the memory layer to increase the storage capacity of the chip. Maximum flexibility will be pursued in the front-end design, to broaden the detectable photon energy range as much as possible and make the detector suitable for different beam structures and rates. Interconnection of the sensor to the front-end electronics will be accomplished through vertical integration techniques to minimize parasitic capacitances and optimize the system noise performance. The target of the project is the fabrication of an elementary tile based on a 64x64 cell array to compose a 20 cm x 20 cm, 4 Mpixel camera with less than 2% dead area, more than 5 MHz sampling rate and more than 1 ksample per cell storage capacity.

Summary

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