Contribution ID: **120** Type: **not specified**

Highly granular MAPS detectors with fully integrated data processing for particle detection and imaging

The next generation of CMOS MAPS detectors for particle physics applications are driven by the need for optimal resolution, which requires high pixel granularity and minimal material. At the same time, the need for high-speed readout imply sophisticated in-pixel and on-sensor data processing, which is very difficult to achieve with current technologies. Hybrid solutions are prohibitive in terms of material and cost. A natural way forward is to move in the third dimension and to stack several CMOS layers on top of each other. This will allow all the necessary in-pixel electronics to be distributed over several CMOS layers and to separate analog front-end and digital back-end of each pixel. However, the technological advantages do not stop there as individual layers can now be optimized for a particular functionality which then allows us to take advantage of the best materials and processing for: sensing, digital and mixed mode applications. The availability of deep-submicron (65 nm or smaller) layers will enable us to integrate advanced digital data-processing like e.g. machine-learning-based clustering, or to provide precise sub-ns timing for pixel hits, providing a key ingredient for a 4D-Tracking approach. By combining the hits over several sensitive layers we can form tracklets within a sensor unit, which can further reduce the occupancy due to fake hits or extremely low-momentum tracks. In the next few years there will be a paradigm shift in the way we construct tracking detectors which will allow us to exploit flexible and adaptive technologies to optimize performance.

Summary

MAPS, Stacking, deep sub-micron , CMOS, 3D Integration

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