"Heterogeneous computing for future triggering"

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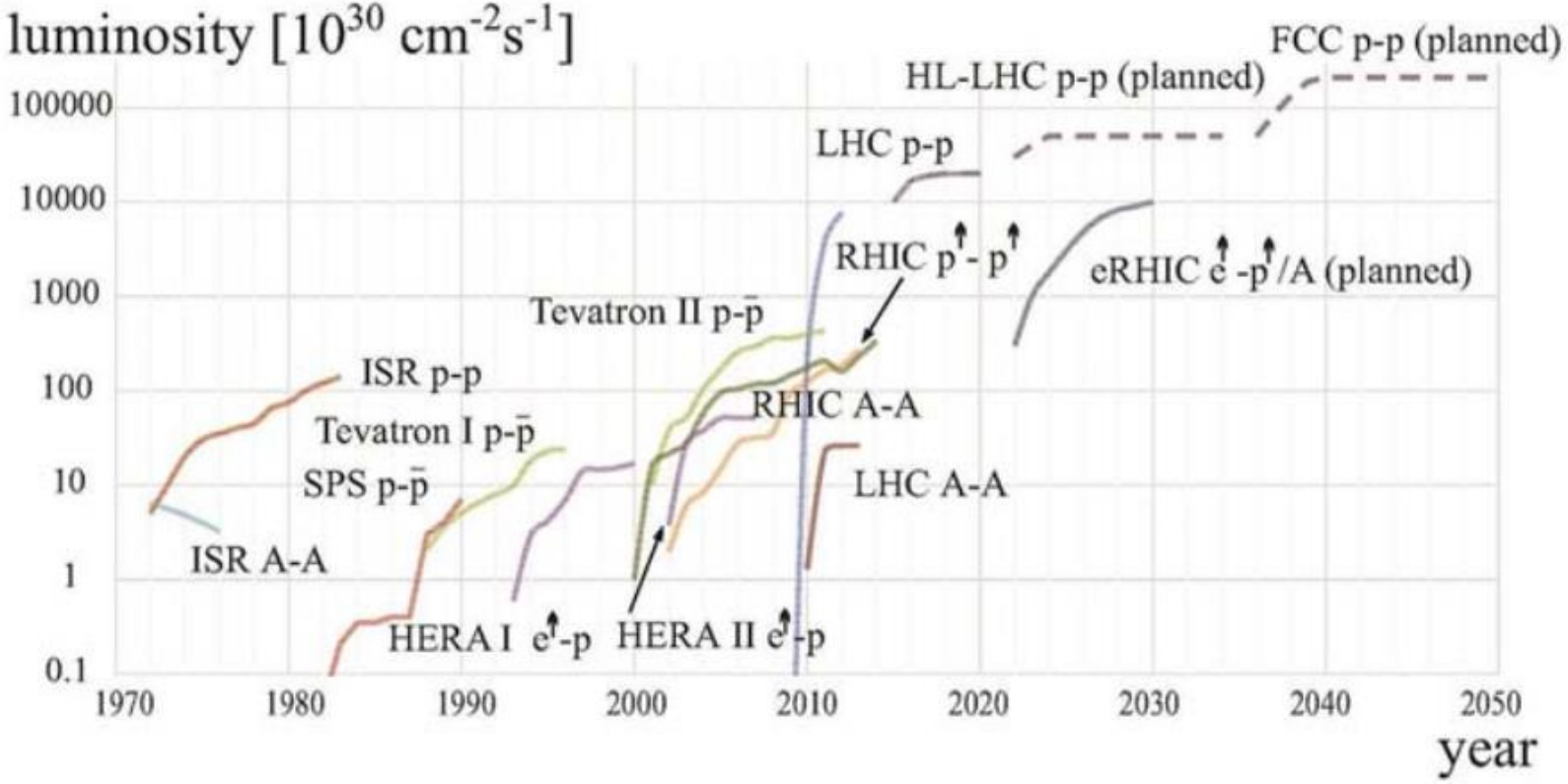
The problem



- FCC (Future Circular Collider) is only an example
  - Fixed target, Flavour factories, … the physics reach will be defined by trigger!
- The triggers in 2035 will be something different from today

Trigger in 2035

Standard trigger requirements

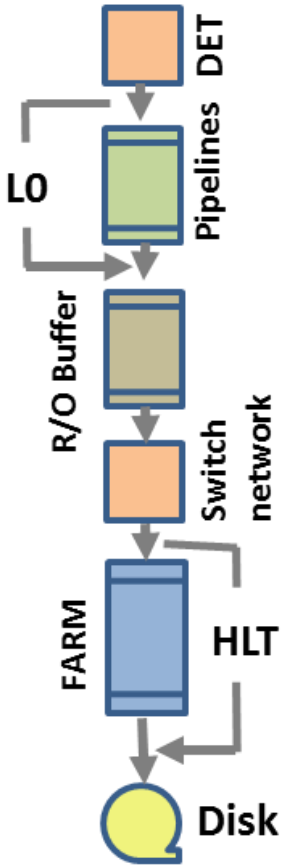
- High reduction factor
- High efficiency for interesting events
- Fast decision
- High resolution

- The higher background and Pile Up will limit the ability to trigger on interesting events
- The primitives will be more complicated with respect today: tracks, clusters, rings

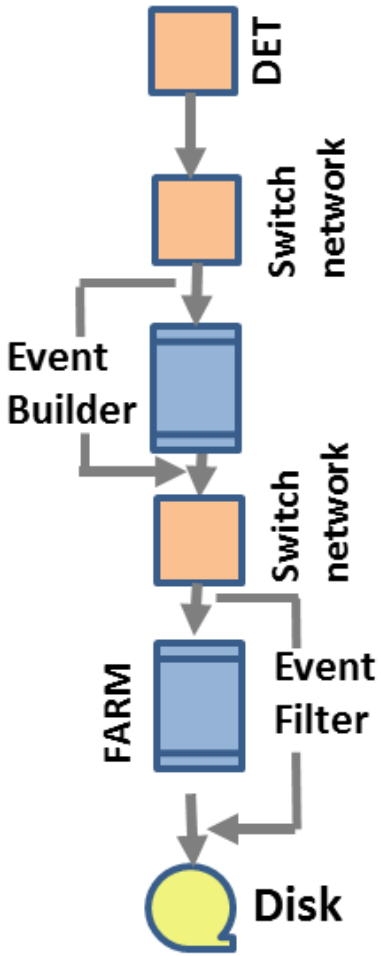
- Higher energy
  - Resolution for high pt leptons → high-precision primitives
  - High occupancy in forward region → better granularity
- Higher luminosity
  - track-calo correlation
  - Bunch crossing ID becomes challenging, pile up
- All of these effects go in the same direction
  - More resolution & more granularity → more data & more processing

Classic trigger in the future?

- Is it a traditional "pipelined" trigger possible?
  - Yes and no
  - Cost and dimension
  - Getting all data in one place
    - New links -> data flow
    - No "slow" detectors can participate to trigger (limited latency)
  - Pre-processing on-detector could help
    - FPGA: not suitable for complicated processing
    - Software: commodity hw
- <u>Main limitation</u>: high quality trigger primitives generation on detector (processing)



Triggerless?



- Is it possible to bring all data on PCs?
  - LHCb: probably yes (2020)
    - 40 MHz readout, 30 Tb/s data network, 4000 cores, 8800 links
  - CMS & ATLAS: probably no
    - 4000 Tb/s data, 4M links, x10 in performance for switch, x2000 computing
- Main limitation: data links

An alternative approach

Classic pipeline:

Focus on On-detector processing

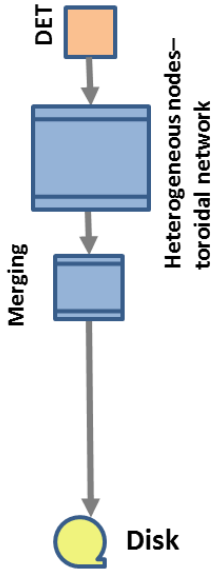
Triggerless:

Focus on Data Links

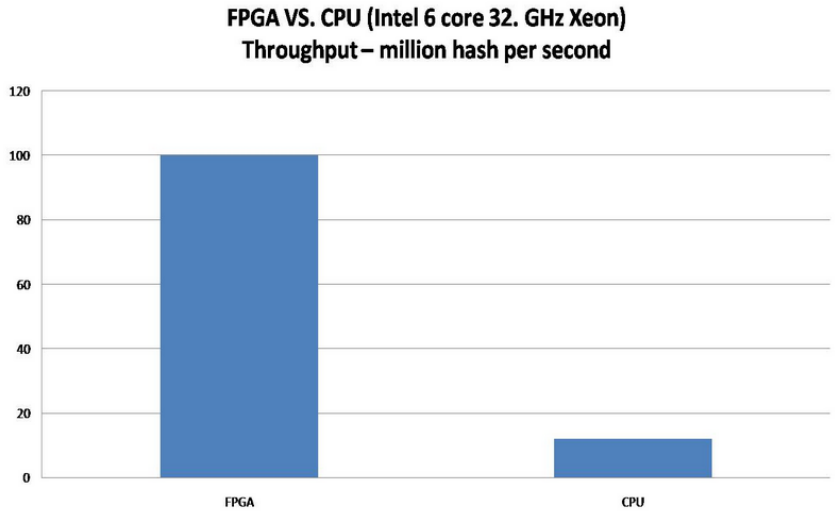
High Latency Trigger:

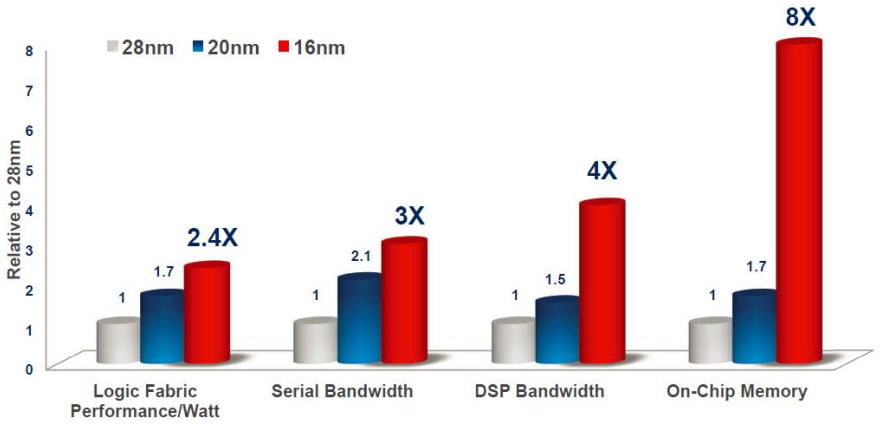
- Heterogeneous computing
- Toroidal network
- Time multiplexed trigger
- Trigger implemented in software

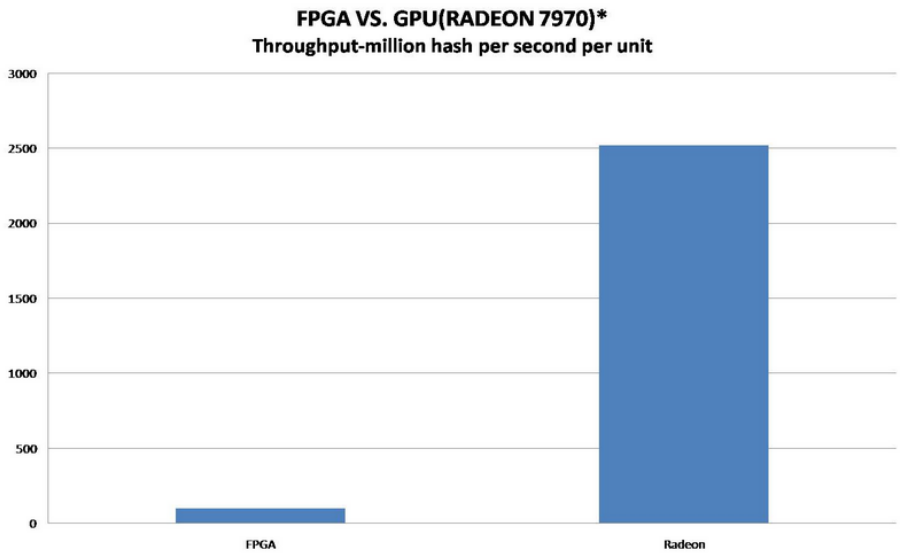
Focus on On-detector Buffers



Classic Pipeline: Processing

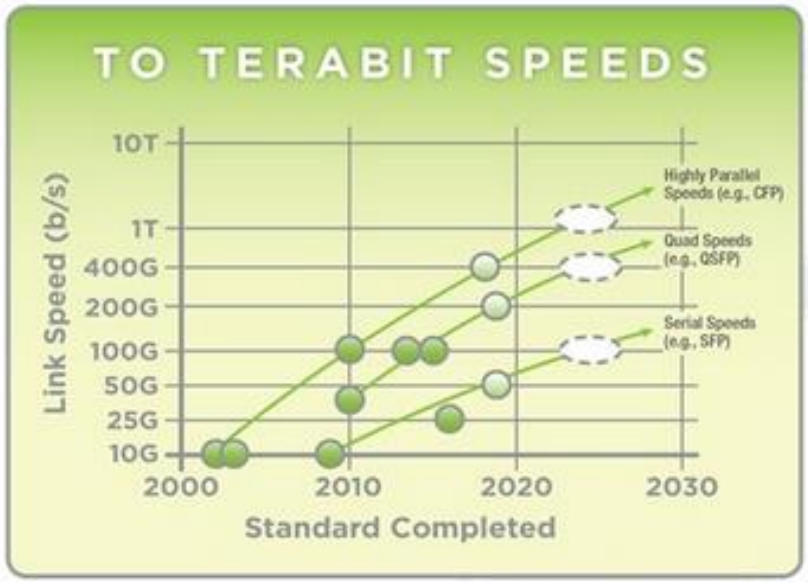


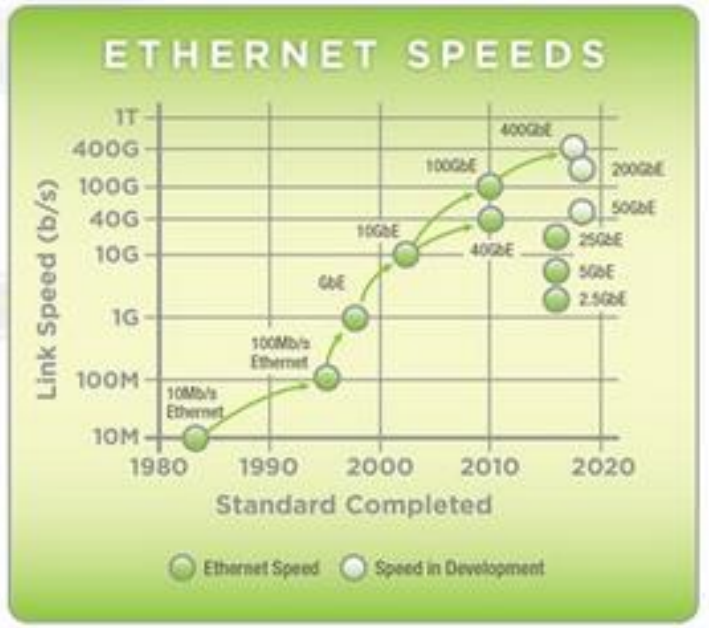




- The performances of FPGA as computing device depends on the problem
- The increasing in computing capability is not as fast as CPU

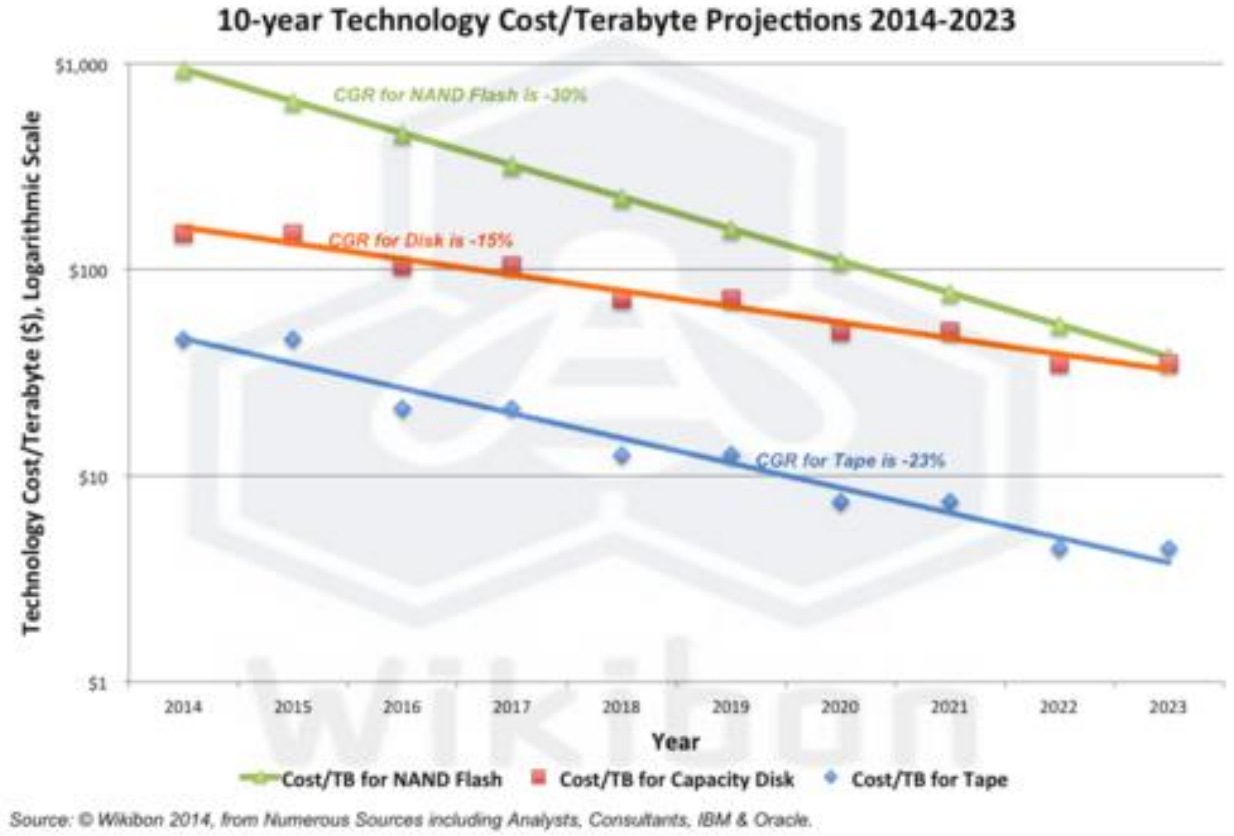
Triggerless: Data Links





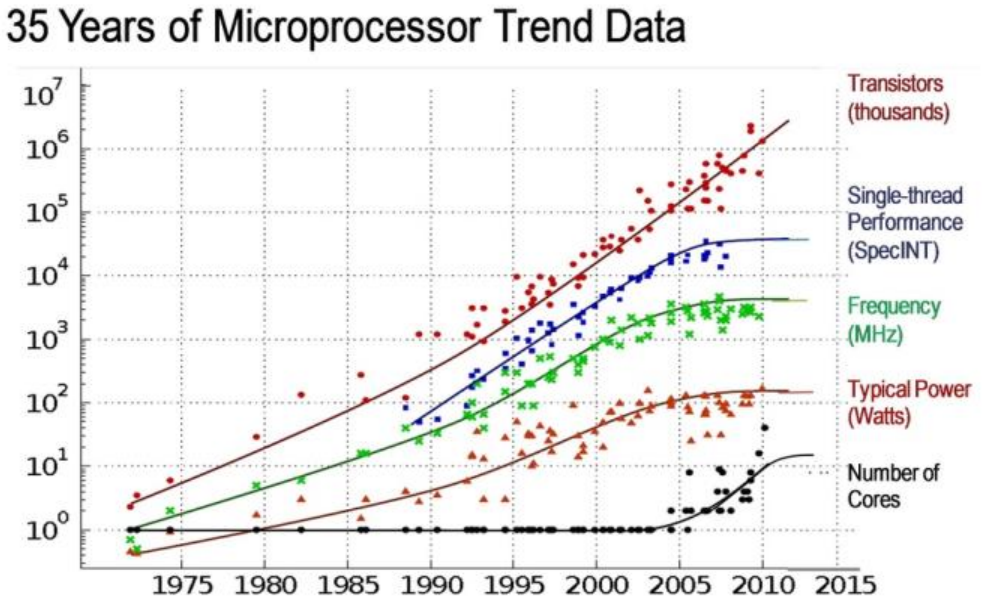
- The links bandwidth is steadily increasing
- But the power consumption is not compatible with HEP purposes (rad hard serializers):
  - lpGBT is 500mW per 5GB/s
  - 4M links → 2 MW only for links on detector
- Nowadays standard market is not interested in this application: room for co-innovation

High Latency: Memories



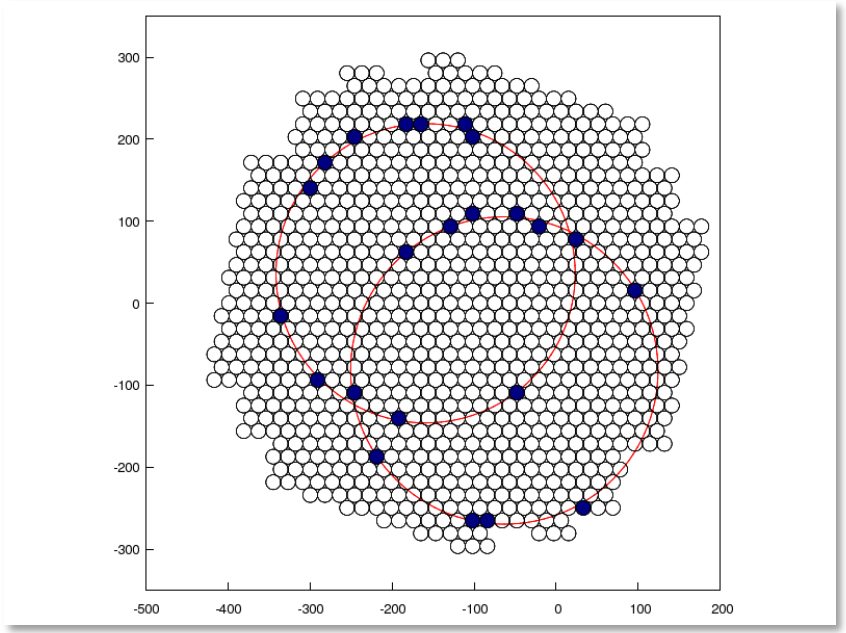
- The memories price decrease very fast with respect to the CPUs.
- Moore's law for memories predicts 10% increase per year

Heterogeneous computing

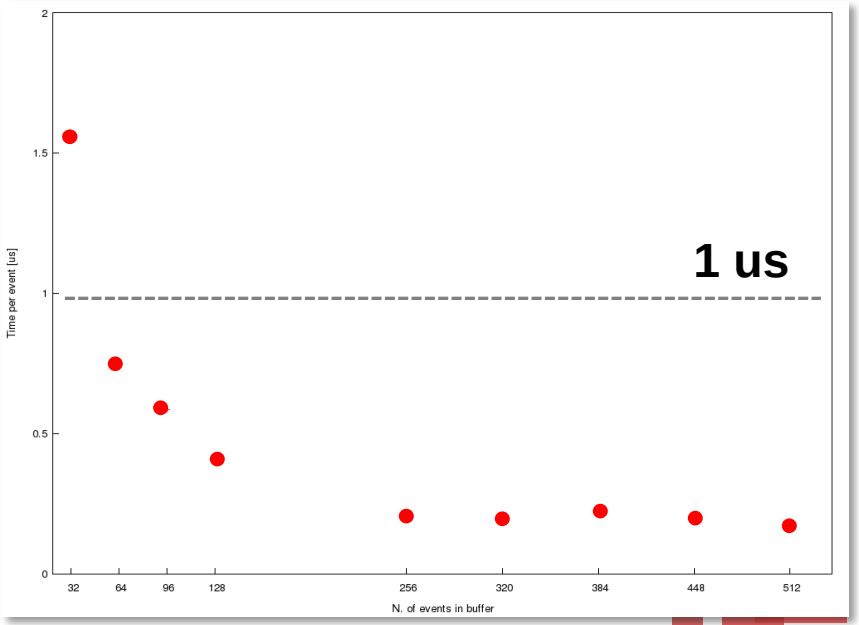


- Heterogeneous computing is a way to cheat the Moore law
- Computing on specialized processors (CPU, GPU, DSP, CAM, ARM, FPGA, ...)

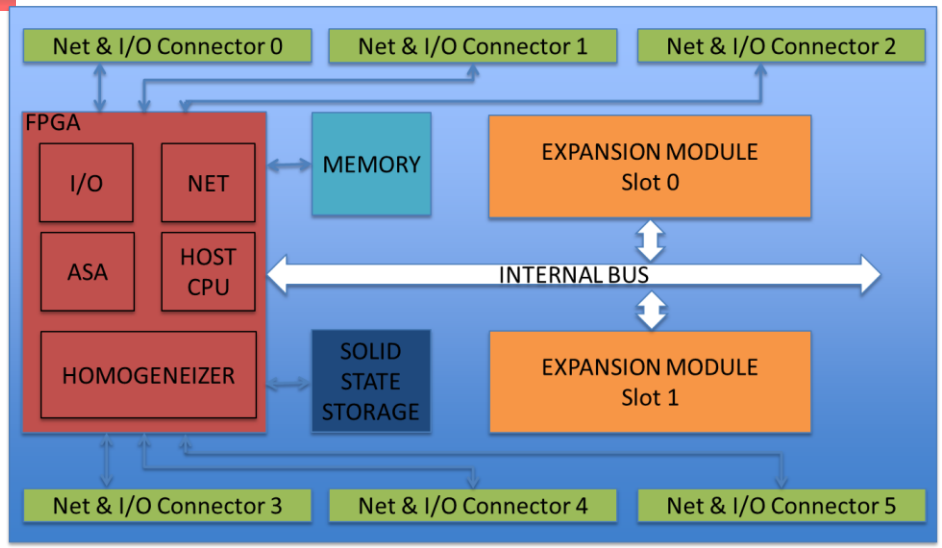
An example: GPU in NA62 for ring reconstruction

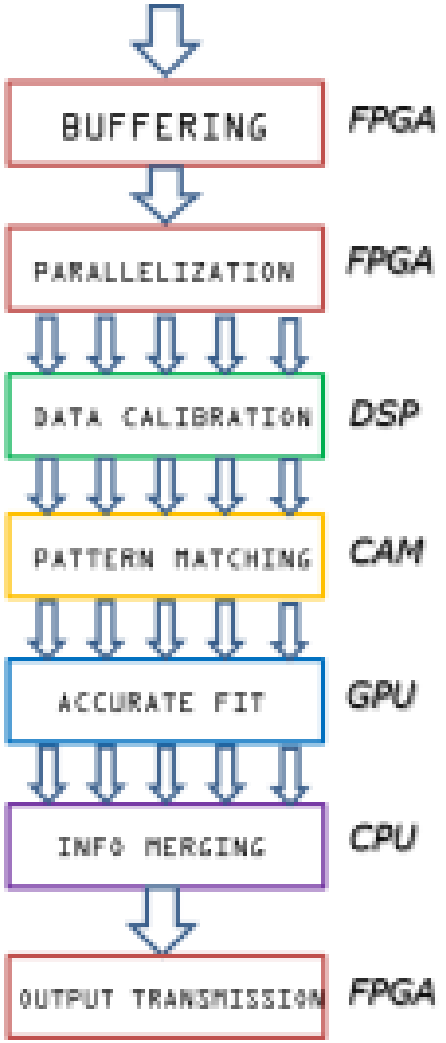


- Rings from RICH
- Custom R/O board built to bring data on GPU
- 500 ns per ring but with high latency (200 us)



Building a framework for realtime Heterogenous computing





- Splitting of algorithms among dedicated processors
- Toroidal network of nodes
- Internal switching
- Simple to program
- Possibility to house next generation processors

Conclusions

- Concerning real time processing, in the past HEP used to pose questions and found answer (**home made solutions**)
- Nowadays HEP can still propose very important challenges, but **we have to look in to the market** for solutions
- Co-innovation is the ideal framework to address the collaboration between research and industry on the edge of the technology
- Heterogeneous computing (creative use of computing units) could be a good opportunity for the European IT industry to address the challenges of future HPC and real time systems.