Development of 3D Associative Memory Chip

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LNF - INFN

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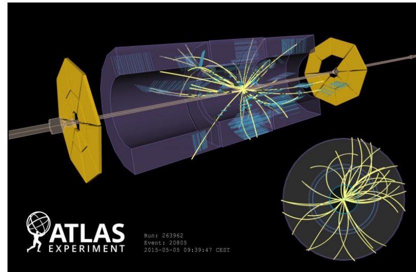
Introduction

Trends in High Energy Physics:

- Higher luminosity to produce rare events results in very high hit rate
- Increasing number of channels
- Larger detectors

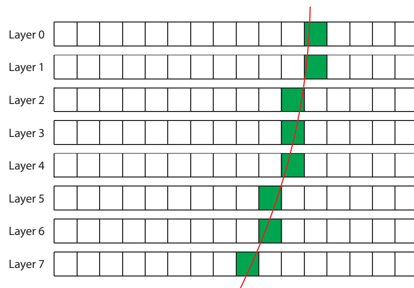
Tracking Trigger Challenge:

- Fast pattern recognition to identify useful traces.



Fast Tracking Trigger

Tracking triggers need an incoming hit to be compared to a set of known patterns:

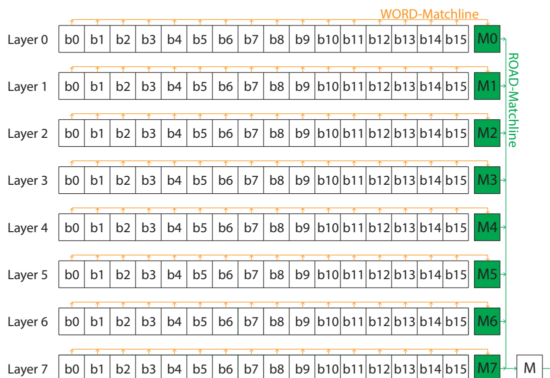


Associative memories:

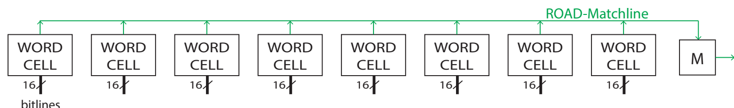
- comparison based on CAM cell
- pattern matching exploiting parallelism to the full (thousands of comparison in parallel)

Associative Memories

Working principle for one pattern comparison (Road):



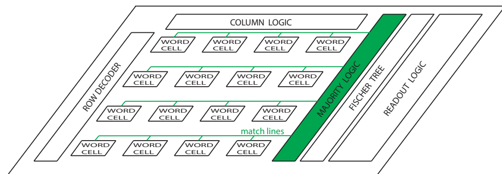
One road planar implementation:



State of the Art: Planar Associative Memories

Planar Associative Memories Limitations:

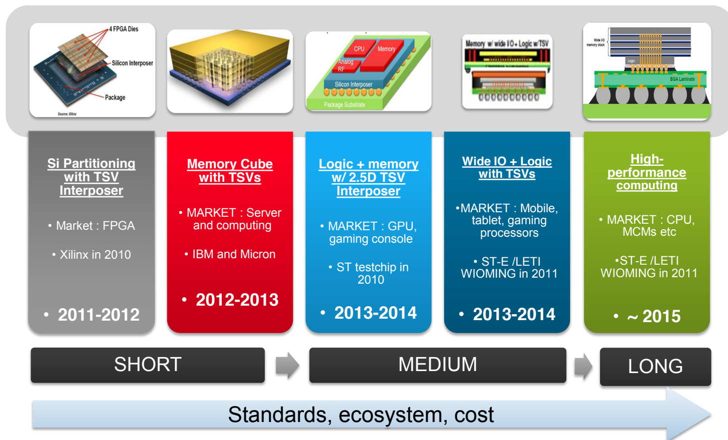
- Limited pattern density: limited number of comparisons per chip.
- Limited performance: long paths to propagate matches along a single road.
- Significant die area used for memory controller and readout logic.



Planar Associative Memory example:

- 4 layers per road
- 4 patterns

IC Trends towards 3D Integration

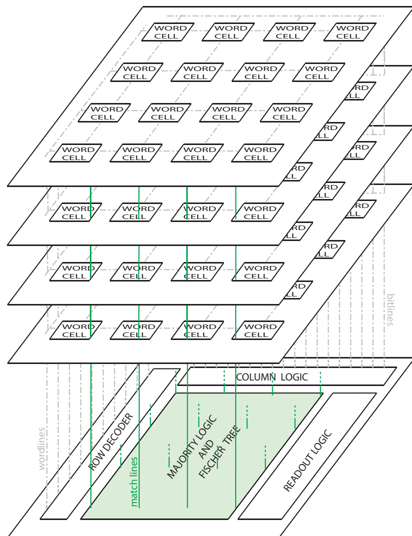


Source: Cadence

New 3D Associative Memory Concept

Proposed 3D stacking architecture:

- Maximize the pattern density:
  - Much higher integration
  - Array dies dedicated to store patterns
  - Separate optimization of memory arrays and control logic
- Increase performance and reduce power:
  - Reduced path length
- Reduced system dimension, power consumption and costs:
  - Less AM chips
  - Reduced PCB complexity



Potential Industrial Impact

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Impact in typical pattern matching applications:

- High energy physics
- Computer aided diagnosis
  - EEG
  - Mammography
- Bioinformatics
  - DNA sequence analysis
- Engineering
  - Image analysis
  - Data analysis
- Military
  - Automatic target recognition

Roadmap: Development of a Proof of Concept Device

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- 3 Dies Stacking (28*nm*):
  - Two cell array layers (custom cell)
  - One logic layer (standard cell)
- 2.5x increase in density:
  - 3D cell array density: +33%
  - Two stacked layers

Milestone	Timeline [months]	Costs [Euro]
Design & Test (2 fte manpower)	12	70*K*
28*nm* Cell Array Chip Development	4	27*K*
28*nm* Control Chip Development		27*K*
3D Stacking & Packaging	3	45*K*
Test HW	1	5*K*
Total	20	174*K*

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