# Level-1 Data Driver Card of the ATLAS New Small Wheel Upgrade Compatible with the Phase II 1 MHz Readout

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On behalf of the ATLAS muon collaboration

HEP, 12-14/05/2016, THESSALONIKI

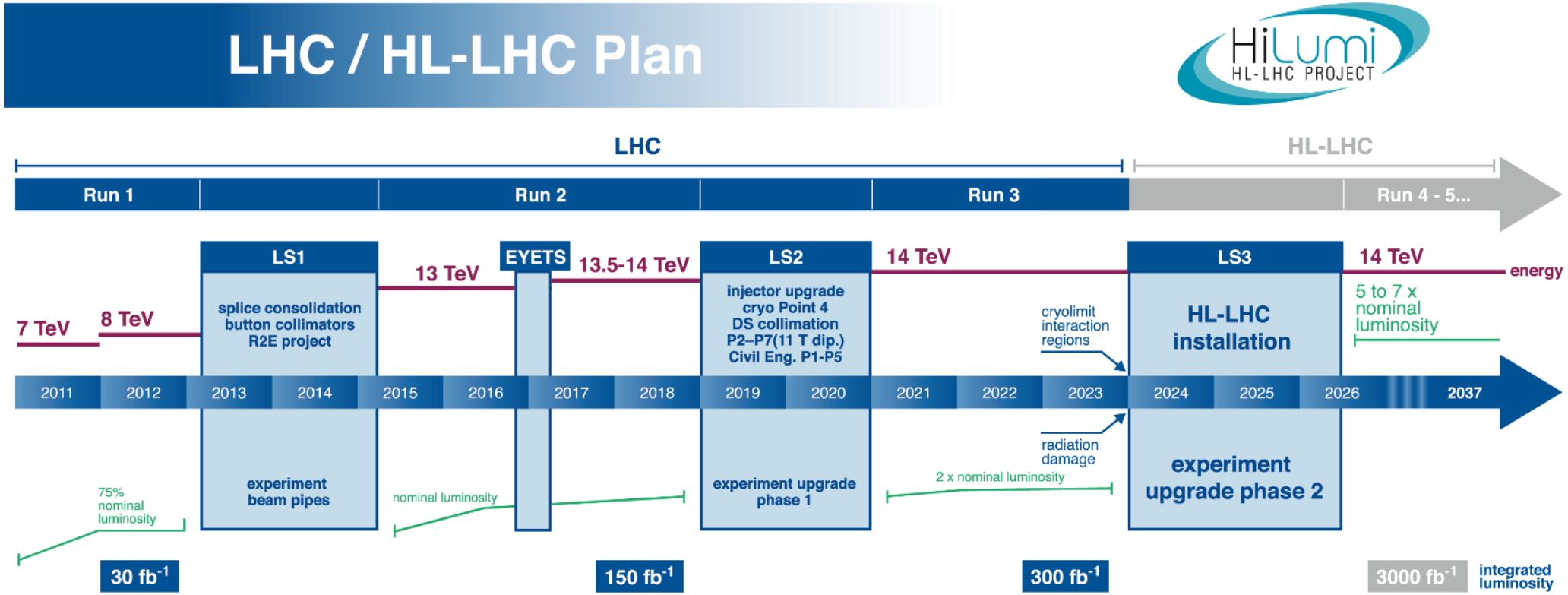


# Overview

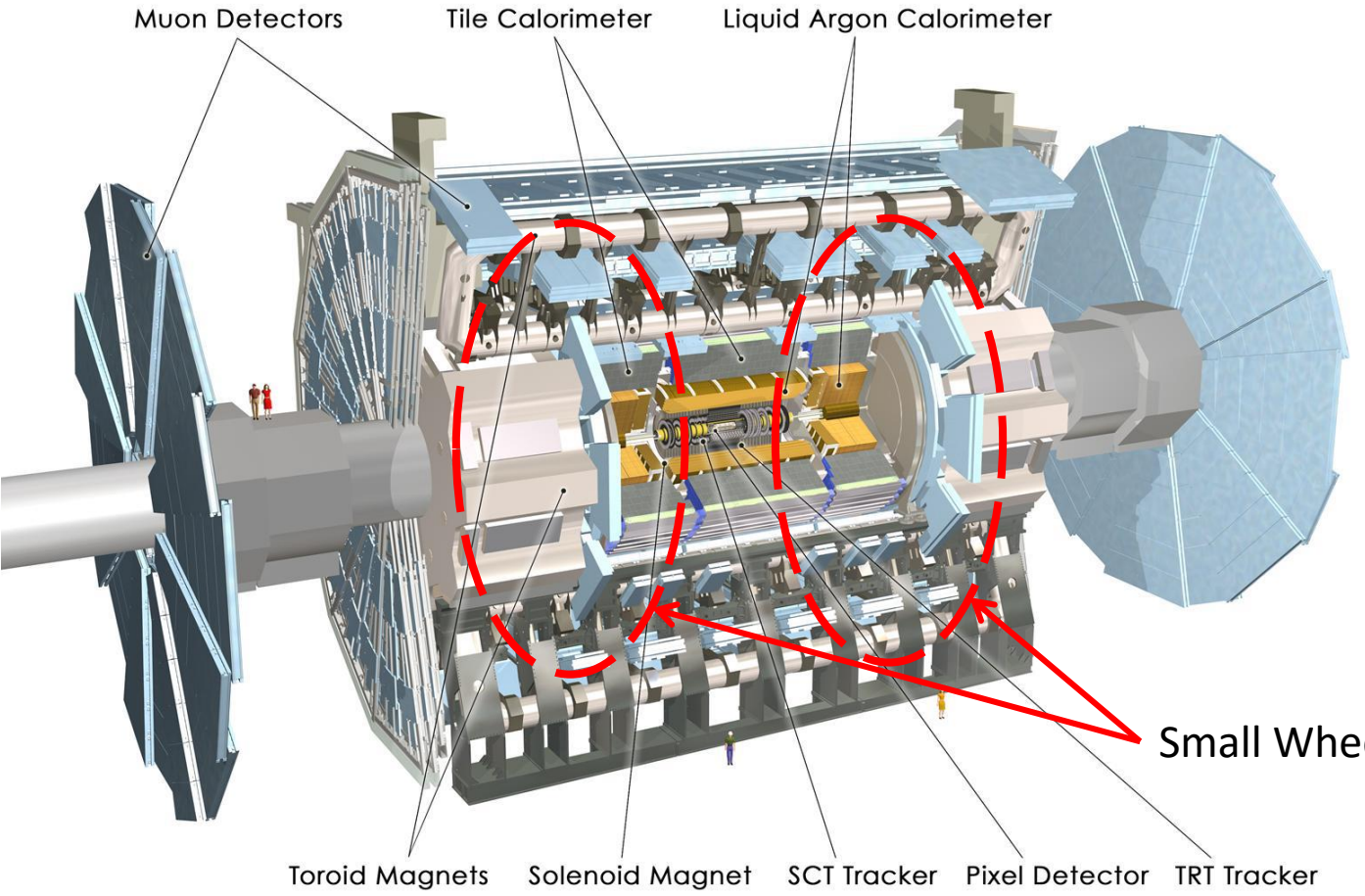
- LHC schedule
- ATLAS experiment & New Small Wheels
- NSW overall electronics
- The Level-1 Data Driver Card (L1DDC) for
  - Micromegas (MM)
  - Small Thin Gap Chambers (sTGC)
  - Trigger boards
- L1DDC prototype-1
- Summary

# LHC upgrade plans & impact on ATLAS

- Nominal luminosity: $\mathrm{L}=10^{34}\ \mathrm{cm}^{-2}\mathrm{s}^{-1}$
- Phase-1 requirements for the trigger rate:
  - Level-0 @ 1 MHz
  - Level-1 from 400 KHz → 1 MHz (Larger data rate)
- L1DDC must fulfil run 3 and 4 requirements

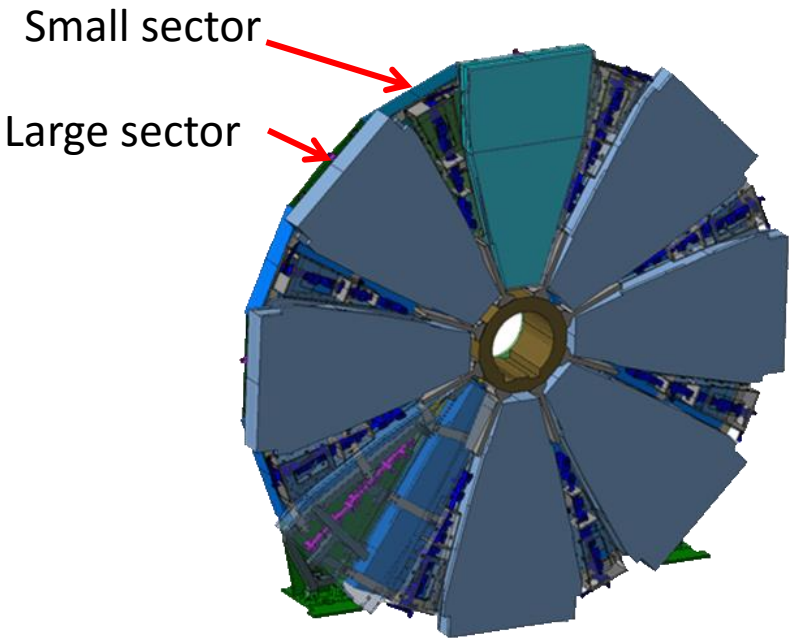


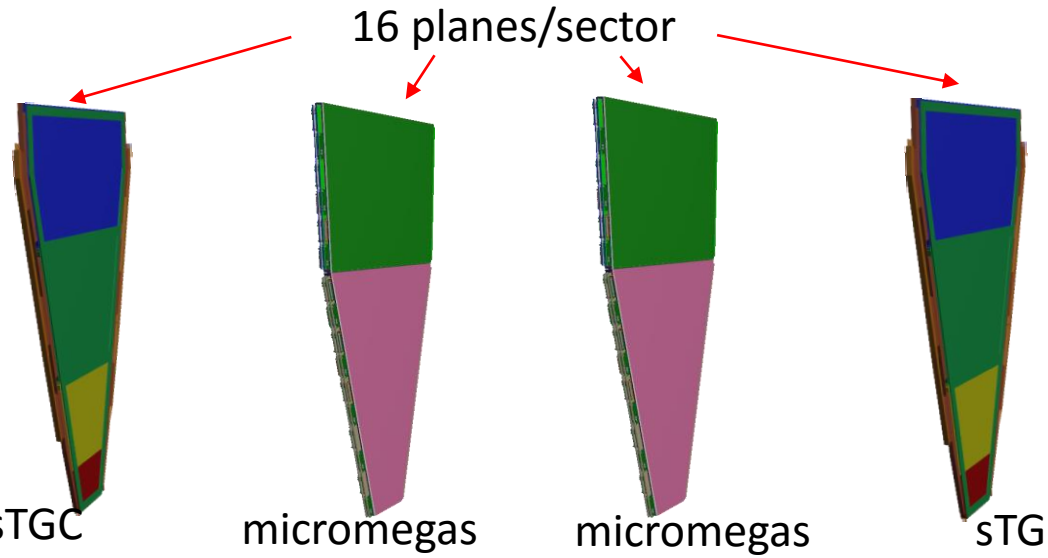
# The ATLAS experiment



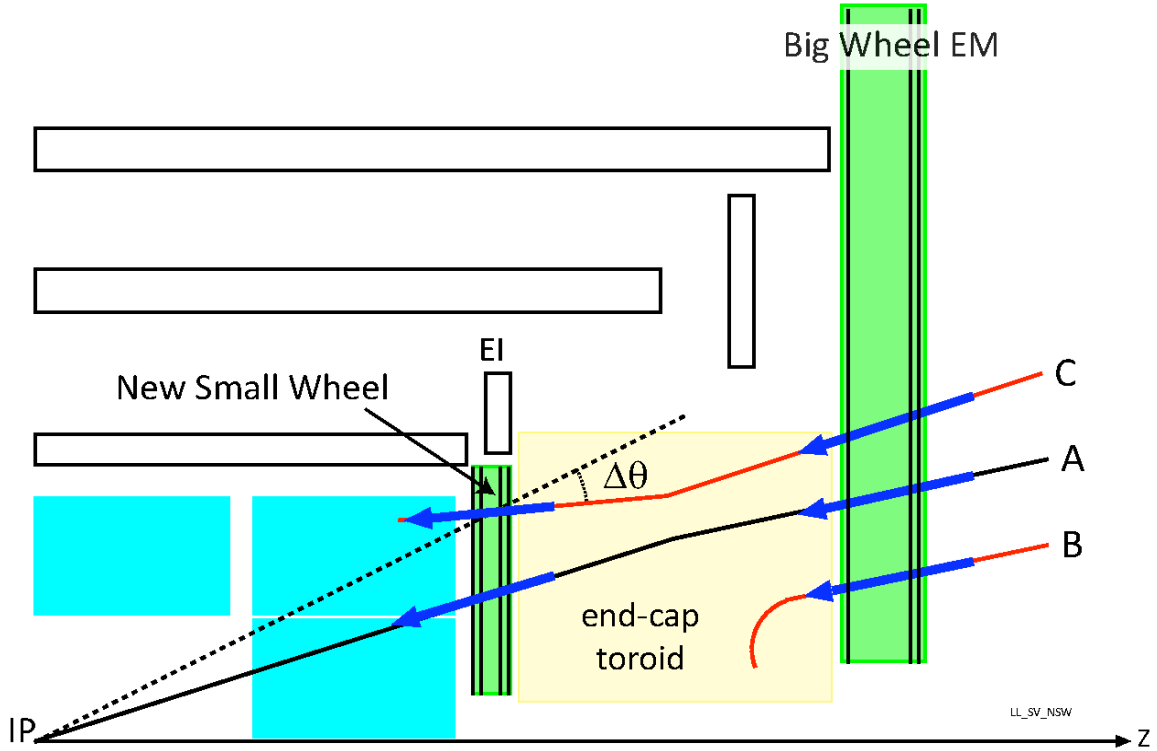

- ATLAS - General purpose detector
- Small wheels are part of the muon spectrometer and are located between the end-cap calorimeter and end-cap toroid
- 10 m in diameter
- Consist of:
  - Cathode Strip Chambers (CSC)
  - Thin Gap Chambers (TGC)
  - Monitor Drift Tube (MDT)
- Not efficient in high rates (maximum 20 KHz/cm$^2$)

# New Small Wheel



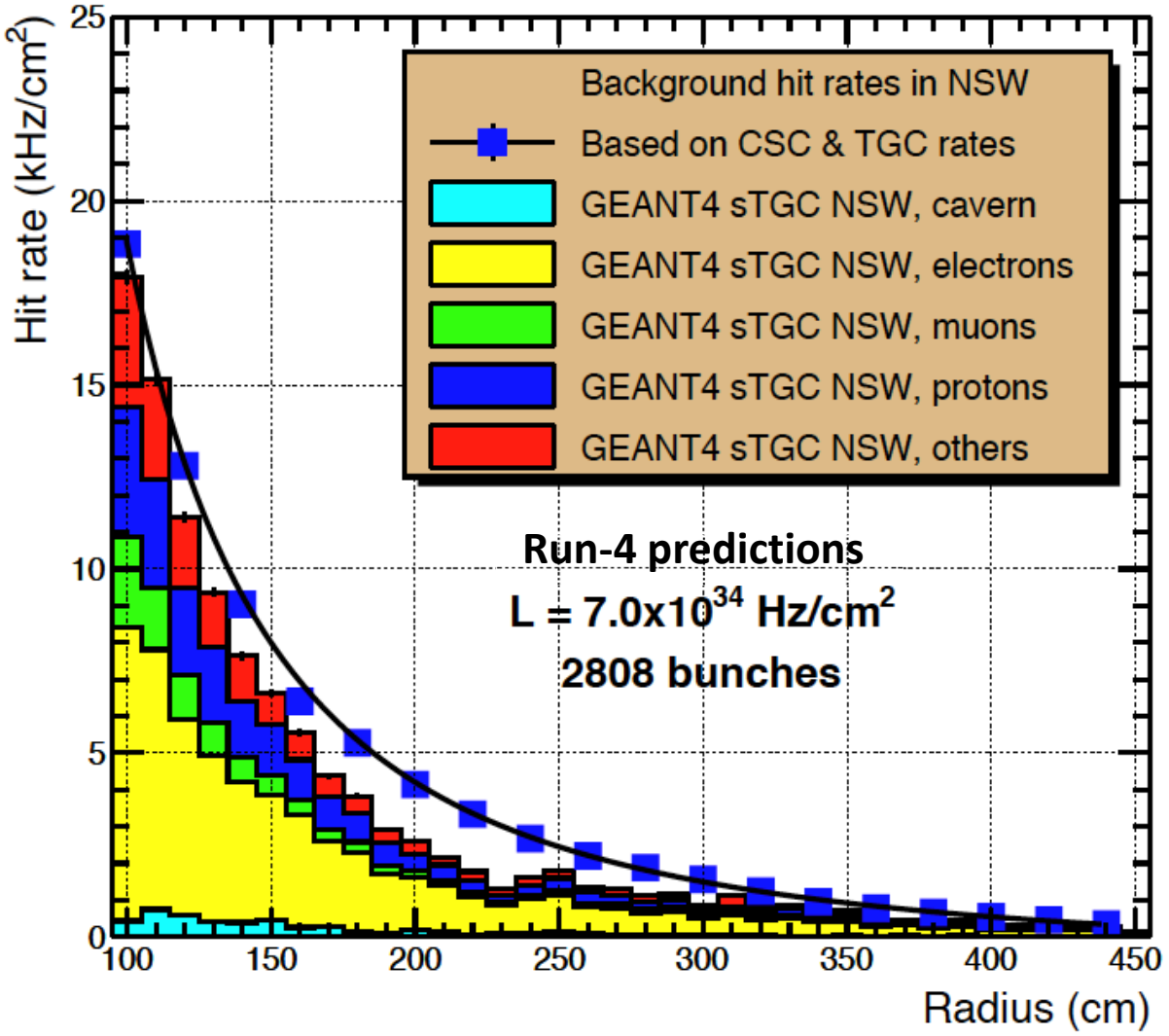




- NSW is a set of precision tracking and trigger detectors (MM and sTGC) able to work at high rates
- Sector = 16 planes (8 sTGC + 8 MM)
- 8 small + 8 large sectors per wheel
- Significant reduction of fake triggers

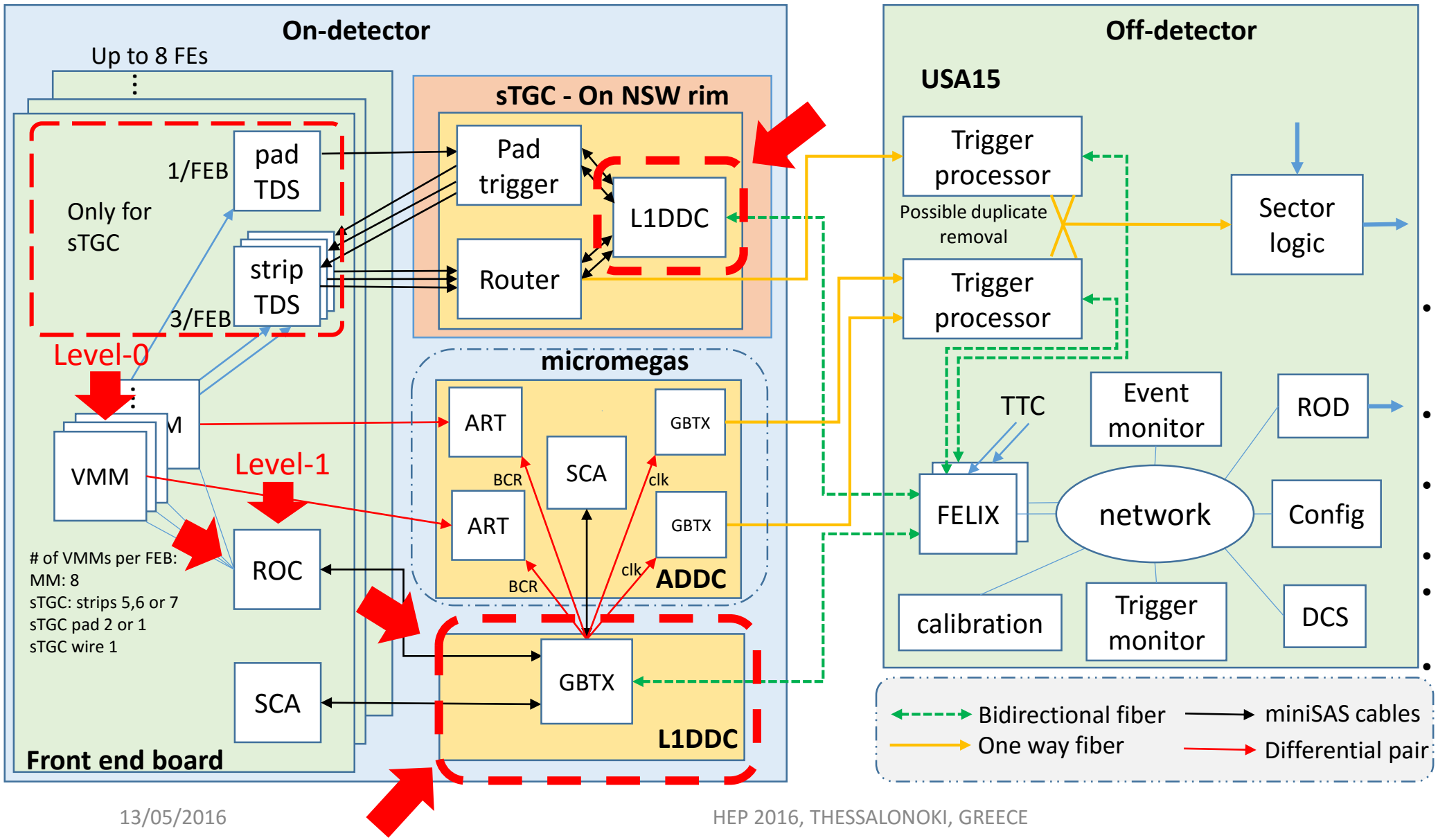


# NSW Run-4 updated expected rates

- Final rates for NSW predictions totally based on Run-2 Small Wheel measurements
- $\mathrm{L}=7*10^{34}\ \mathrm{cm}^{-2}\mathrm{s}^{-1}$
- Highest hit rates: ~19 kHz/cm$^2$
- Rate was increased compare to previous calculations
- Affects also the final data rate



# Overall readout and trigger scheme




- Radiation tolerant ASICs
  - Slow Control Adapter (SCA)
  - Read Out Controller (ROC)
  - Address Real Time (ART)
  - GigaBit Transceiver (GBTX)
  - Trigger Data Serializer (TDS)
  - VMM (amplifier, discriminator, shaper)
- Front-End LInk eXchange (FELIX) Interface network
- Timing Trigger & Control (TTC)
- Art Data Driver Card (ADDC)
- Read Out Device (ROD)
- Detector Control System (DCS)
- Front-ends (FE)

# GBTX ASIC architecture

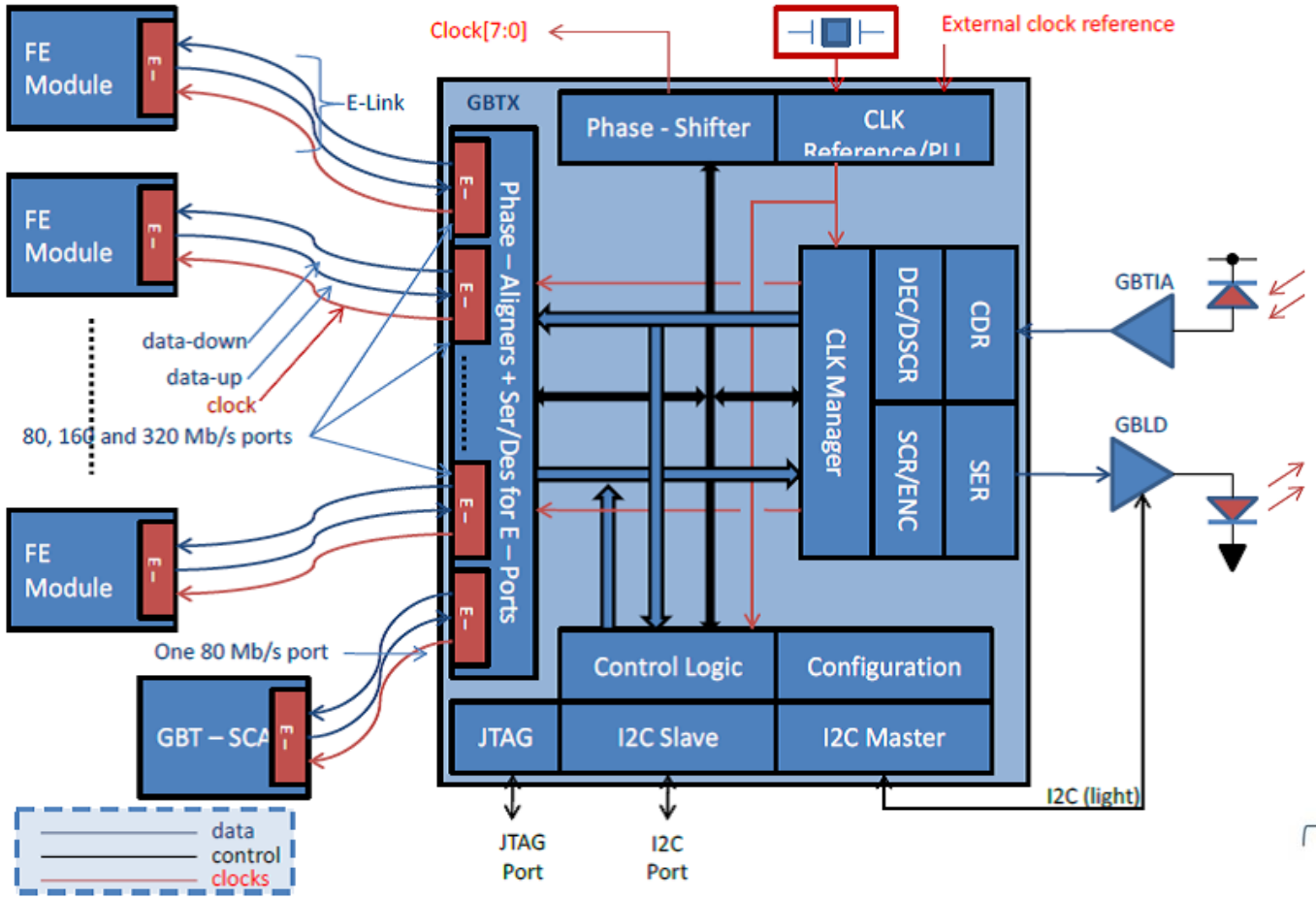
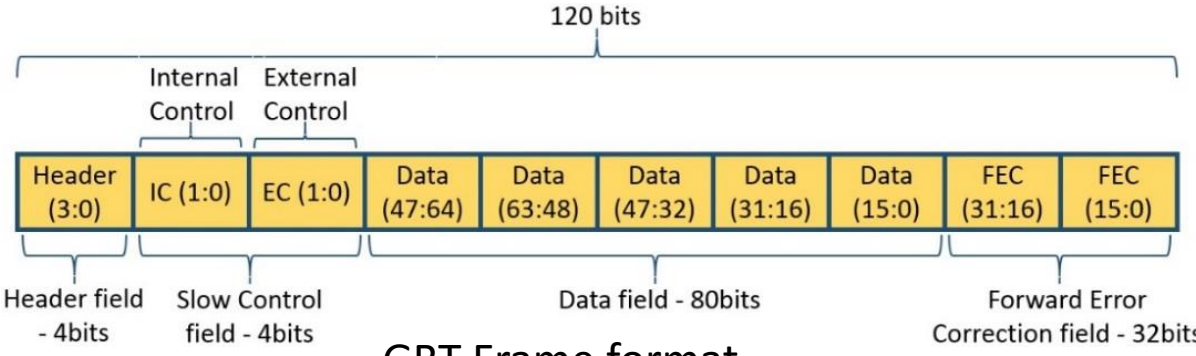


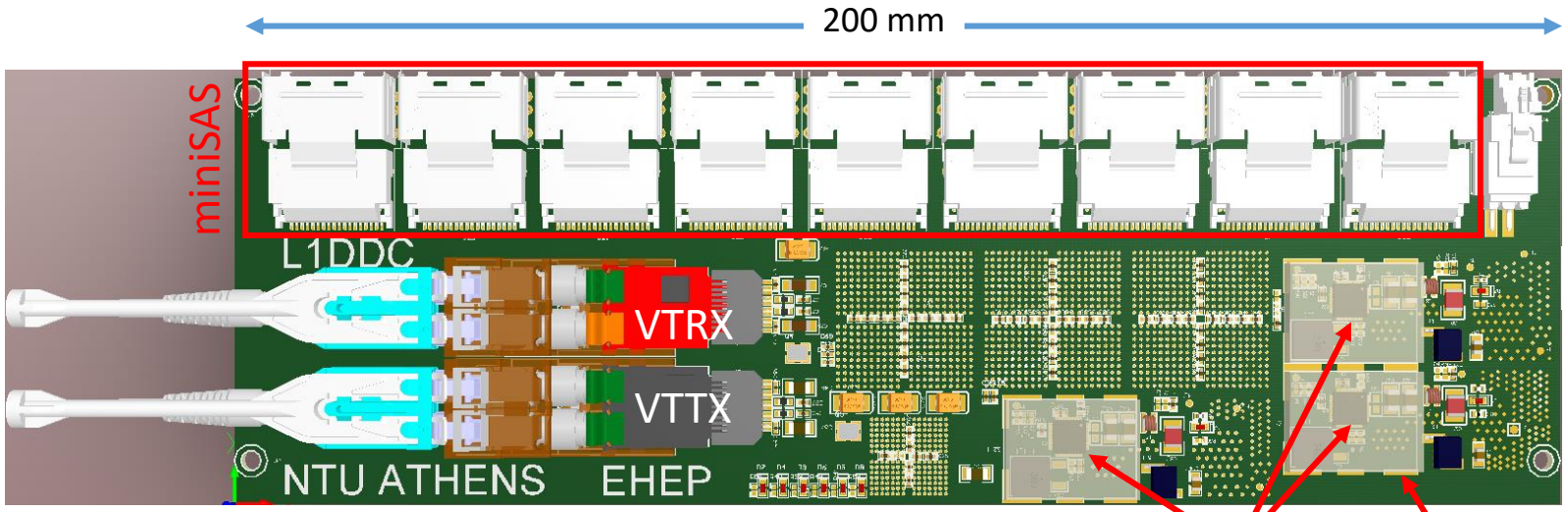

Figure taken from GBTX manual

- Radiation tolerant ASIC (Serializer/deserializer)
- 1 E-Link is 3 differential pairs
  - Clock (40, 80, 160 or 320 MHz)
  - data-up (monitoring data – Level-1 data)
  - data-down (configuration data)
- E-Links can be grouped in 5 independent banks that can support
  - 40 E-Links @ 80 Mbps
  - 20 E-Links @ 160 Mbps
  - 10 E-Links @ 320 Mbps
- Different E-Link configuration for each detector
  - MMs: 8 FEs/L1DDC
  - sTGC: 3 FEs/L1DDC
- Clock and data-down have the same phase
- Data-up are aligned to the GBTX clock
- Fiber side: 4.8 Gbps transmitting speed
- GBTX is configured by the Internal Control (IC) channel
- GBTX logic uses Triple Modular Redundancy (TMR)




GBT Frame format

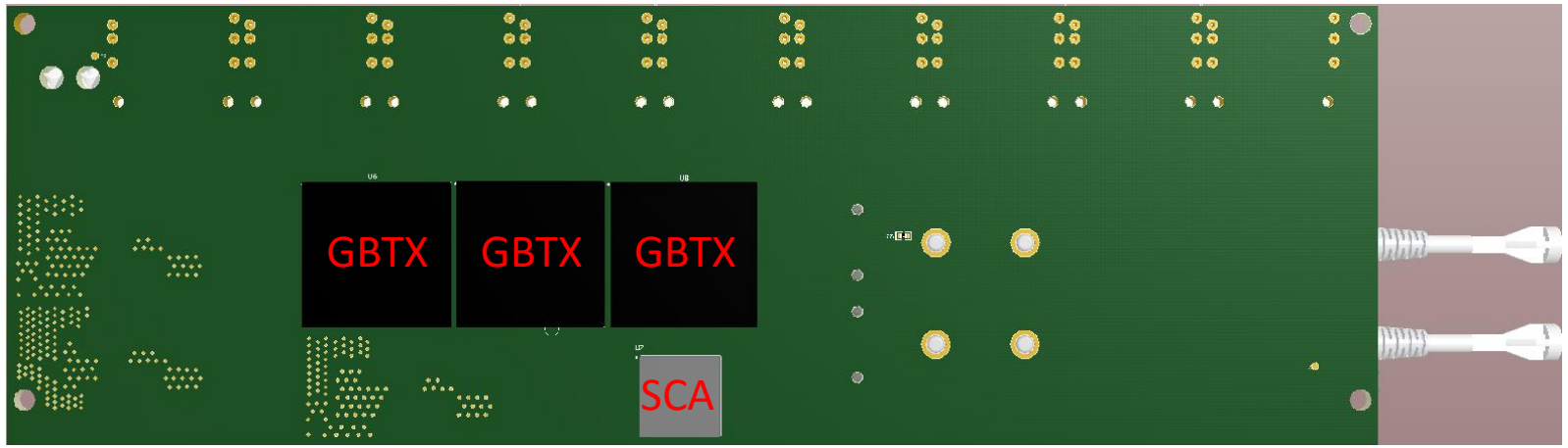
# L1DDC for MM detectors



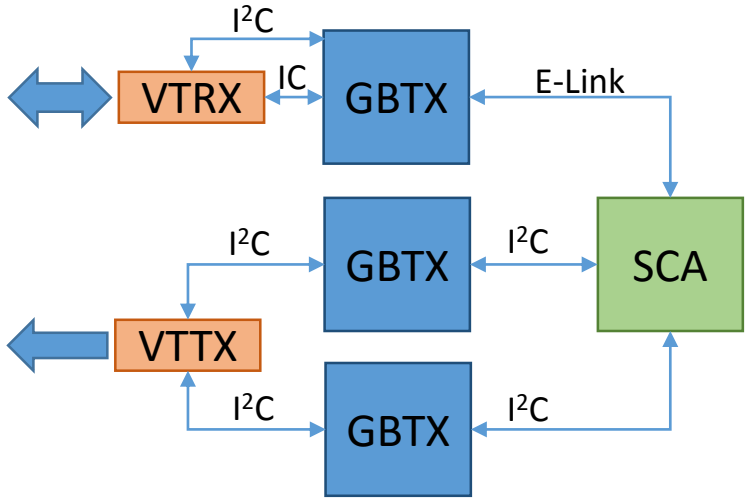

Top side

FEAST ASIC

Shield



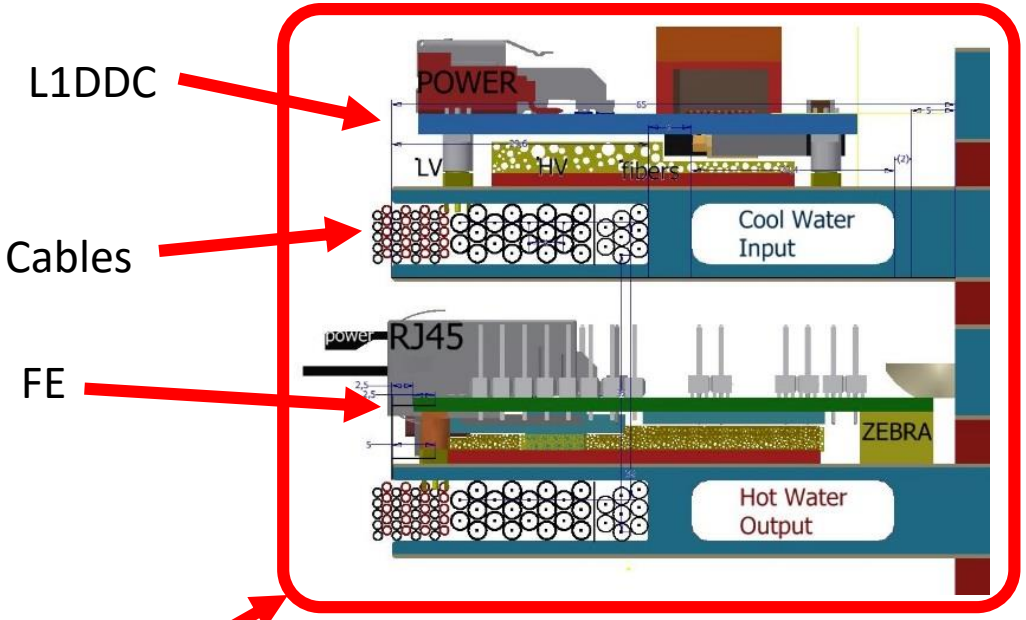

Bottom side

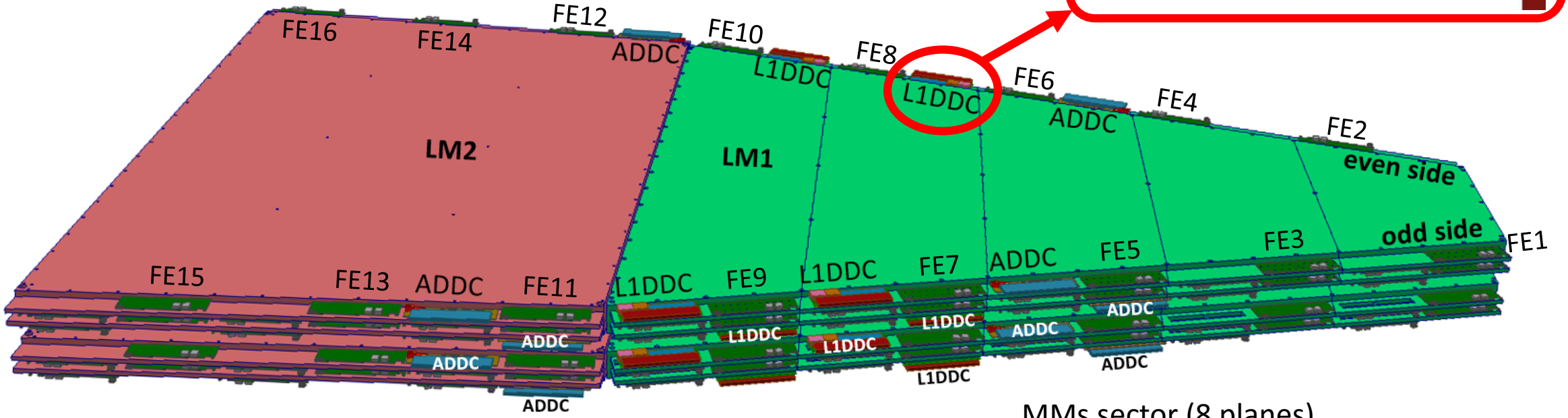



- Dimensions: 200 mm * 64 mm * 15.5 mm (l * w * h)
- Use only radiation and magnetic tolerant components
  - 3 GBTX ASICs
  - 1 GBT-SCA ASICs
  - 1 VTRX transceiver
  - 1 VTTX transmitter
- 9 miniSAS connectors
  - 8 for the FEs
  - 1 for the ADDC
- 3 FEAST DC-DC converters (1.5 V – 2.5 V)
- Bottom side of the board will be attached to the cooling channel
- Power consumption ~15 Watts
- Configuration of the 2 GBTX is performed by the SCA

# L1DDC placement on MM detectors

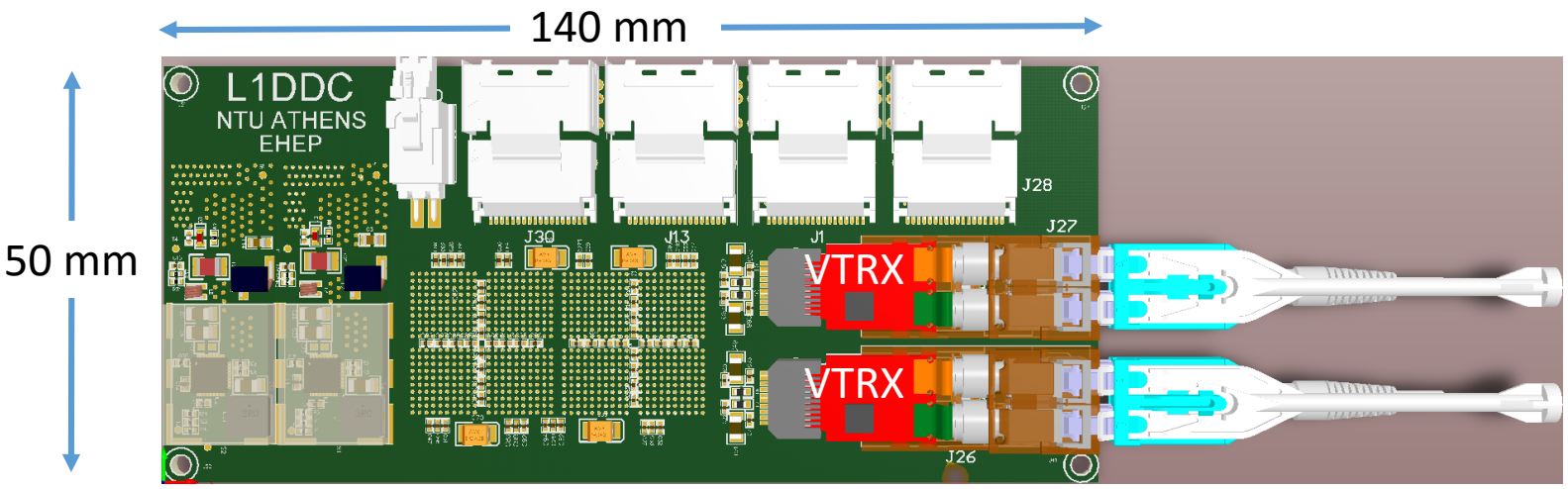
- L1DDC will be placed radially on both sides of MMs detectors and only on the 1st and 4th plane of each wedge (4 planes)
- 1 L1DDC will serve the 8 FE located on each side of a plane
- For the MM L1DDC will be placed on the center to minimize the cable length (fixed length @ 3 m)
- Non-conductive thermal foam will be used for better connectivity to the cooling channel
- 512 L1DDC will be fabricate for the MM



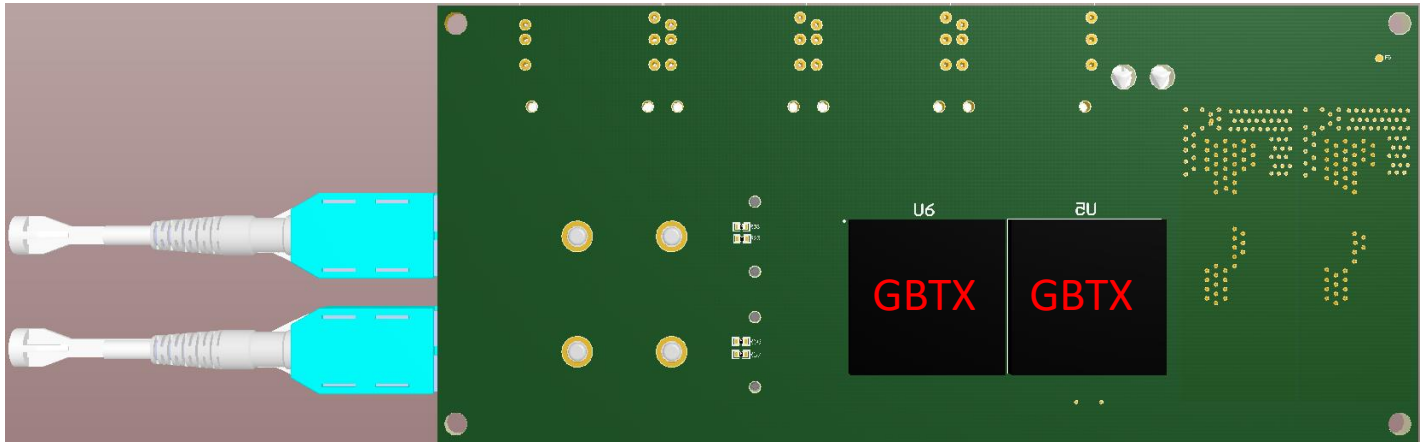




MMs sector (8 planes)

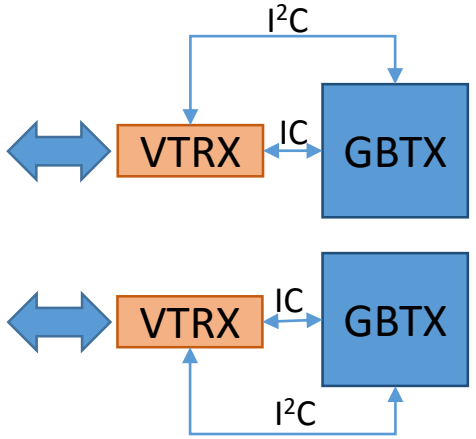
# L1DDC for sTGC detectors




Top side



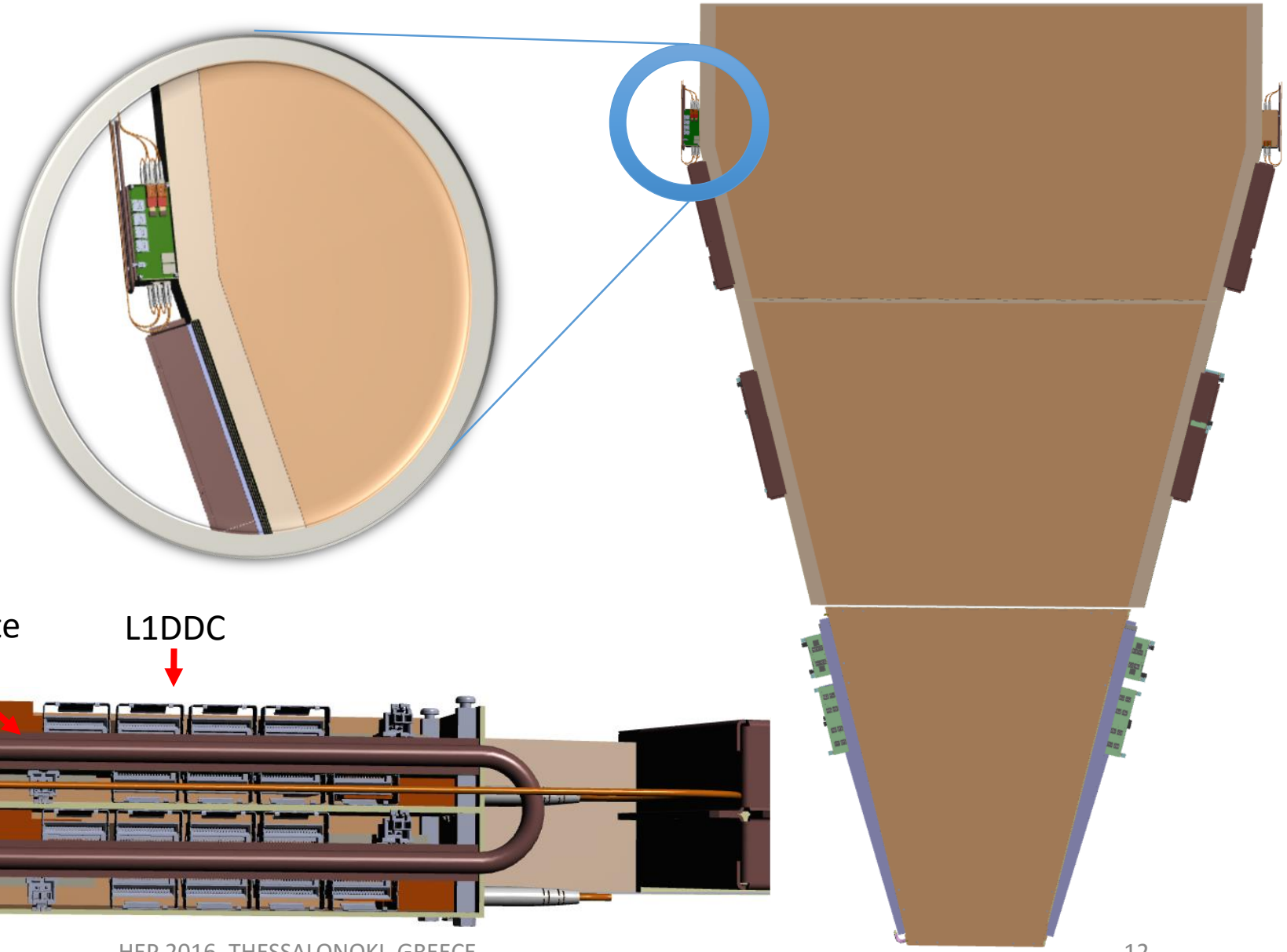

Bottom side




- Dimensions: 140 mm * 60 mm * 15.5 mm (l * w * h)
- 2 GBTX ASICS
- 2 VTRX transceivers
- 4 miniSAS connectors
  - 1 extra miniSAS is used for the inner strip FEs
- 2 FEAST DC-DC converters
- 2 voltage levels 1.5 V for GBTX and 2.5 V for VVTX and VTRX
- Bottom side of the board will be attached to the cooling channel
- Power consumption ~11 Watts
- Configuration of the 2 GBTX is performed by the IC channel
- 512 L1DDC will be fabricate for the sTGC

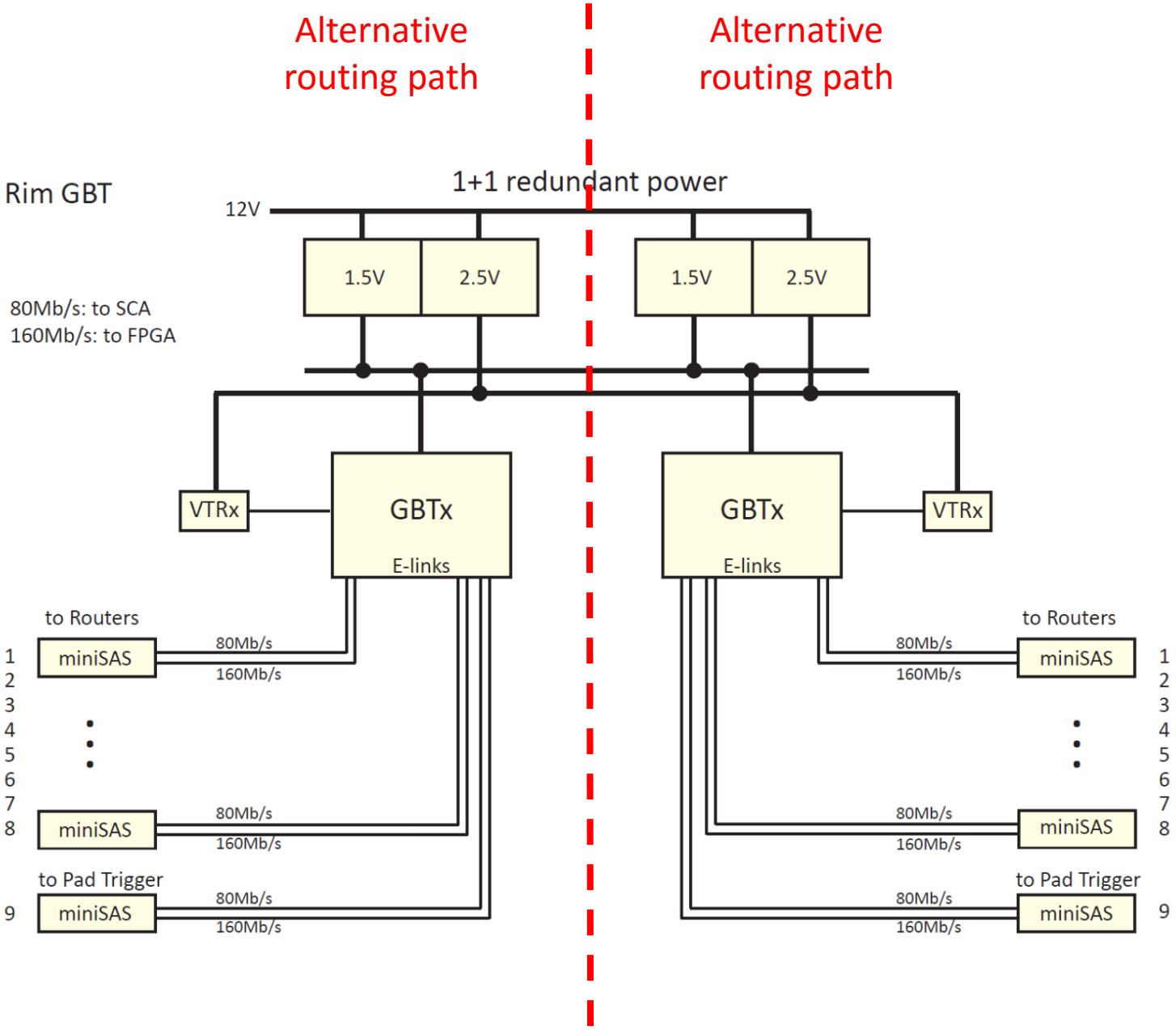
# L1DDC placement on sTGC detectors

- L1DDC will be placed on the upper part close to the rim for the sTGC detectors
- 1 L1DDC will serve 3 front ends of each plane
- Non-conductive thermal foam will be used for better connectivity to the cooling channel

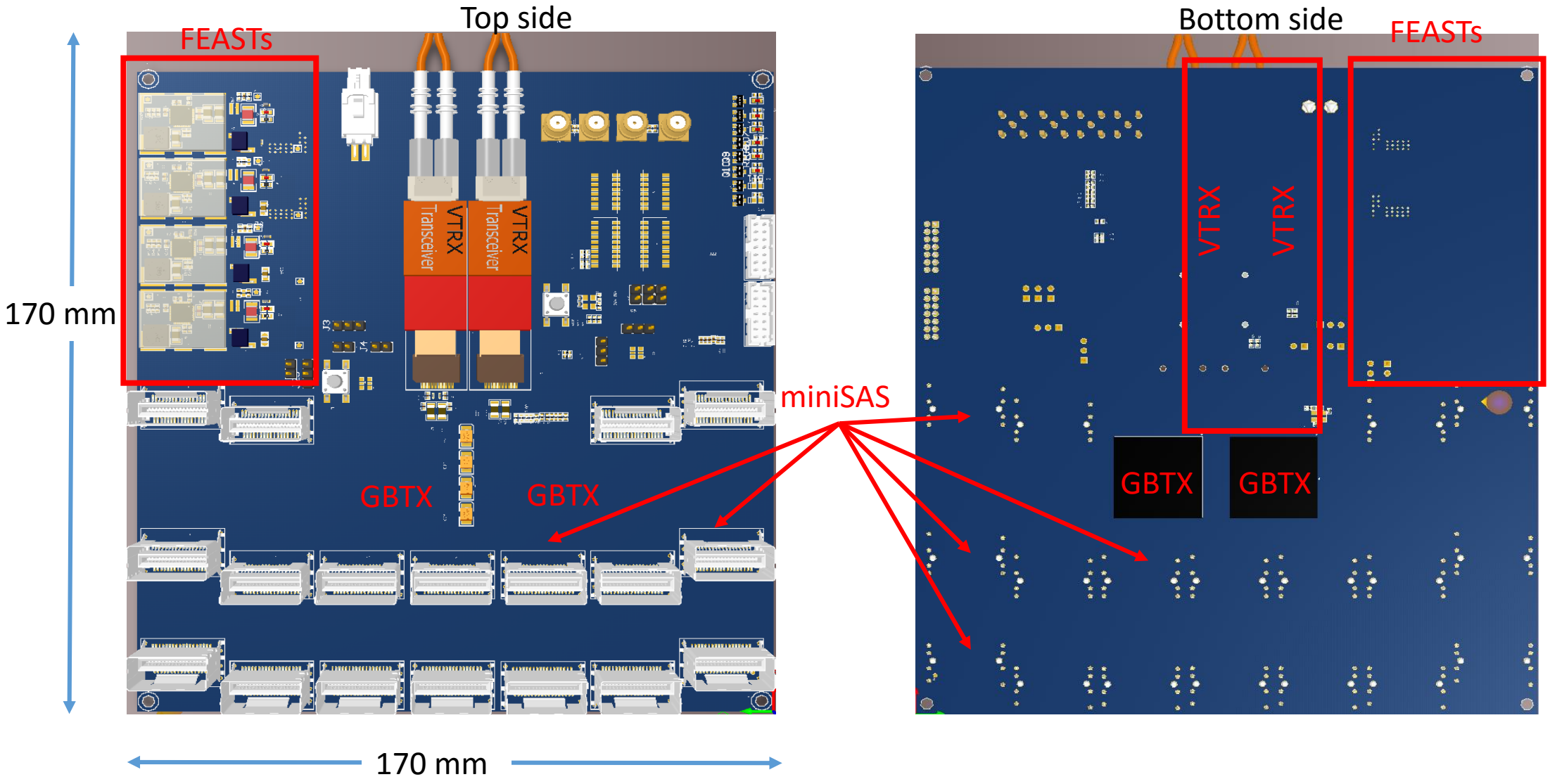


# RIM-L1DDC

- Transmits the TTC data to the trigger boards (Pad and Router)
- Receives monitoring and any additional data from the trigger boards
- Fully redundant board
  - 2 GBTX ASICs
  - 2 VTRX optical transceivers
  - 18 miniSAS vertical connectors
    - 8 + 8 for redundancy for Routers
    - 1 + 1 for redundancy for Pads
  - 2 voltage levels
    - 1.5 V for GBTX ASICs
    - 2.5 V for VTRX transceivers
  - 4 FEASTs (2 for redundancy)
- GBTX standards
  - SLVS for the Tx
  - LVDS and SLVS for Rx
- Power consumption ~11 Watts
- 32 L1DDC will be fabricate for the trigger boards

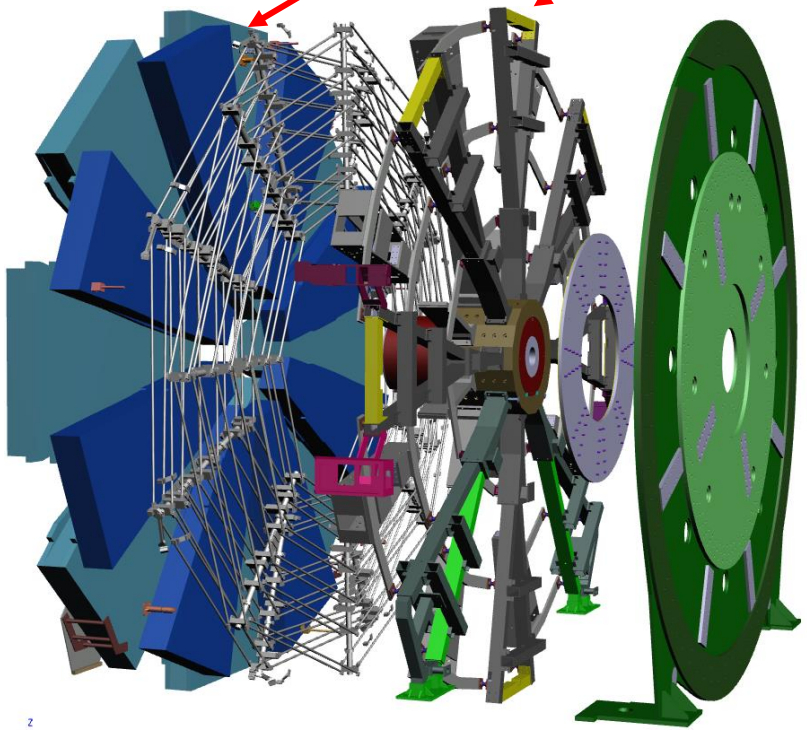


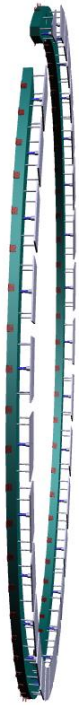
# RIM-L1DDC with vertical connectors

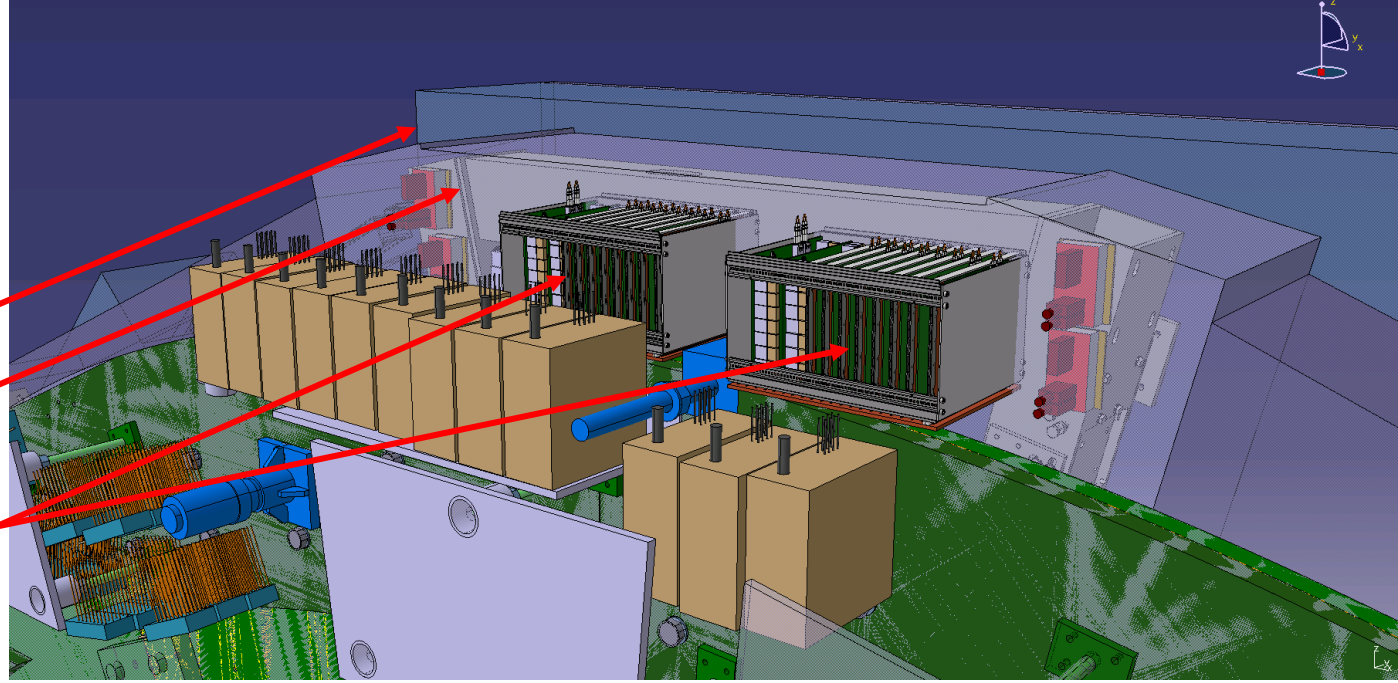


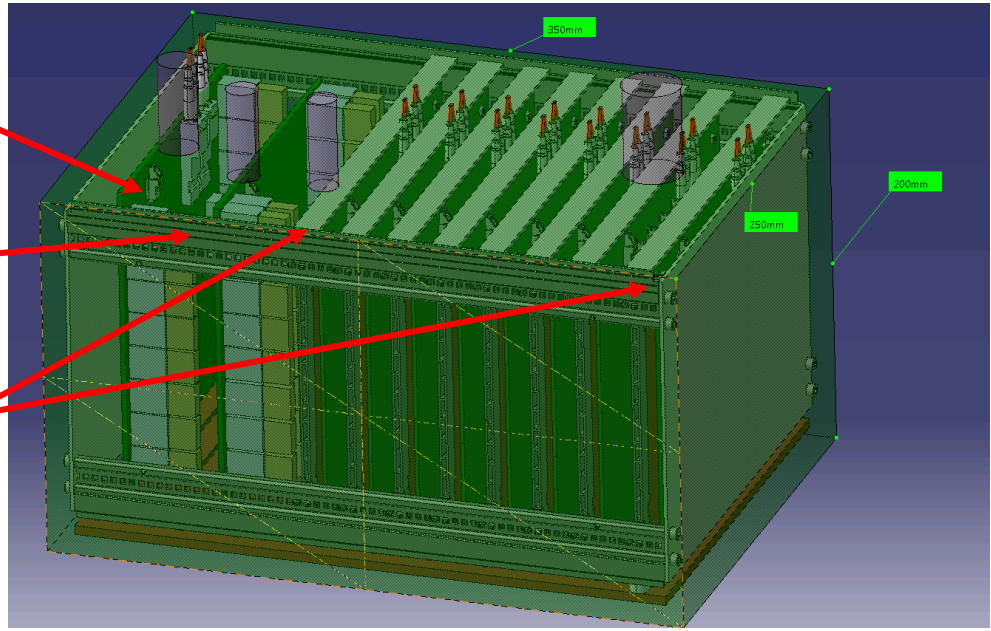
# Rim box position

- It will be placed on the rim
- 2 rim boxes (Small and Large Sectors)
- Commercial boxes will be used



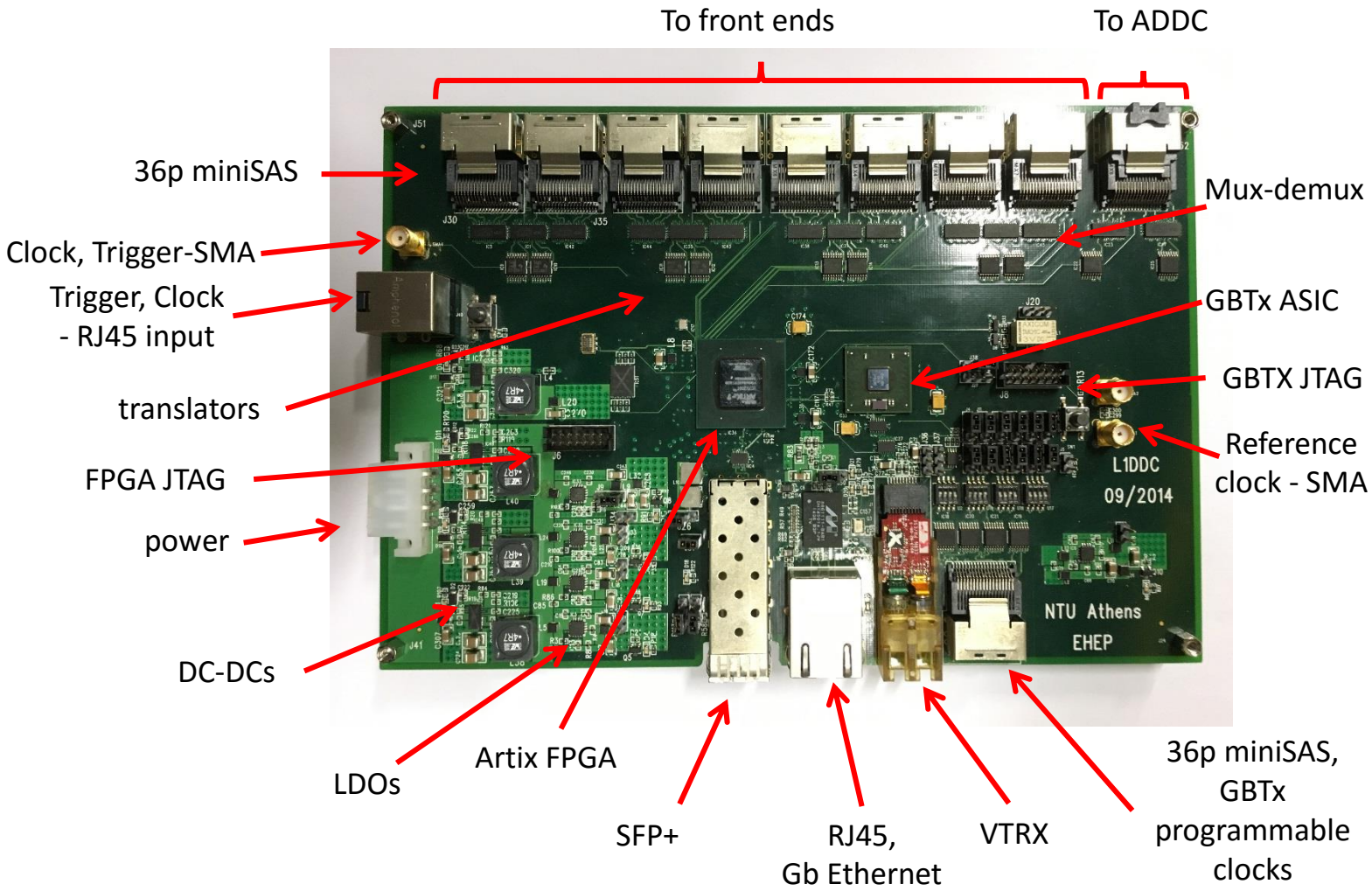




# L1DDC - Prototype 1

- Prototype 1
  - Already fabricated
  - Size 210 mm x 144 mm
  - Layers used : 14
  - Alternative paths in case of GBTX failure
  - Input voltage 3.6 V – 42 V
  - GBTx, GBTIA & GBLD (VTRX) ASICs
  - Xilinx FPGA Artix7 - xc7a200t-3FBG484
  - SFP+, Gigabit Ethernet, VTRX, miniSAS 36p, SMAs
  - Still in debugging process
  - Board is functional
  - Not radiation tolerant board



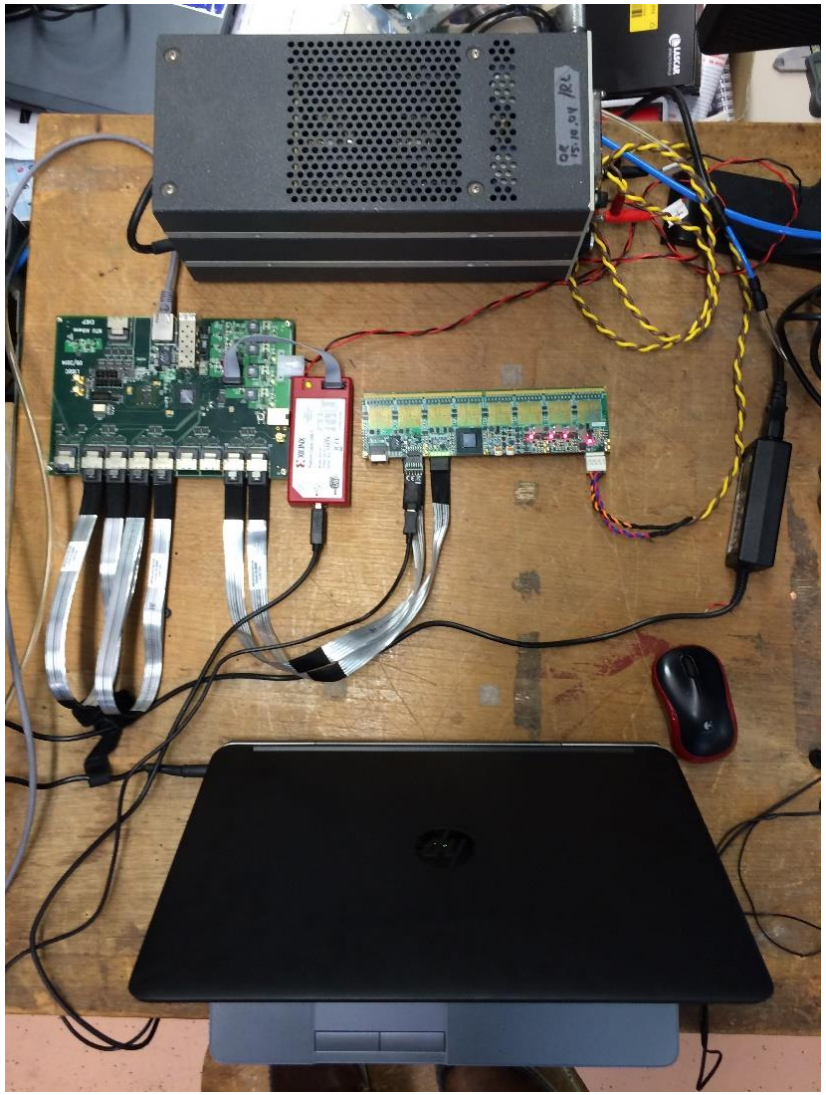

Top side of L1DDC prototype-1 board

# L1DDC tests

- E-links were tested with
  - Internal loopback test (both GBTX and FPGA)
  - The communication with the FE
- 0 errors received after transmission of more than 15.000 E-Link packets
- Data are send through Ethernet and UDP packets to a PC
- 0 errors received in UDP packets after 2 weeks of continuous operation
- FELIX software is not yet available – optical path is not tested yet
- A series of tests are also performed by Piraeus University of Applied Sciences

Send data back to L1DCC


UDP output at 1Gbps



Data are fed to the L1DDC by the FE

# Summary

- L1DDC is an intermediate aggregator board for the Level-1 data and distributes the TTC data to the front ends and trigger boards
- L1DDC will be able to cope with the high data rates of the HL-LHC
- It is a radiation and magnetic tolerant board, it has small size and SEU mechanisms to assure signal integrity
- Prototype boards have shown high reliability after continuous operation

# Thank you for your attendance!

# References

**ASICS**

- GBT project: https://espace.cern.ch/GBT-Project/default.aspx
- GBTX: https://espace.cern.ch/GBT-Project/GBTX/Manuals/gbtxManual.pdf
- GBT-SCA: https://espace.cern.ch/GBT-Project/GBT-SCA/Manuals/GBT-SCA_Manual_V8.0.pdf
- FEAST: http://project-dcdc.web.cern.ch/project-dcdc/public/Documents/FEAST%20datasheet.pdf
- GBLD: https://espace.cern.ch/GBT-Project/GBLD/Manuals/GBLDv4_Test_Report-October2015.pdf
- VMM: https://twiki.cern.ch/twiki/pub/Atlas/NSWelectronics/vmmSpecification.pdf
- ROC: https://twiki.cern.ch/twiki/pub/Atlas/NSWelectronics/VMM3_ROCspec.pdf

**Boards**

- L1DDC design review: https://twiki.cern.ch/twiki/pub/Atlas/NSWParameterBook/MM_Parameters.xlsx
- RIM-L1DDC: https://twiki.cern.ch/twiki/pub/Atlas/RimElectronics/RIM_GBT.docx

**Parameter books**

- sTGC: https://twiki.cern.ch/twiki/pub/Atlas/NSWParameterBook/sTGC.xlsm
- MMs: https://twiki.cern.ch/twiki/pub/Atlas/NSWParameterBook/MM_Parameters.xlsx

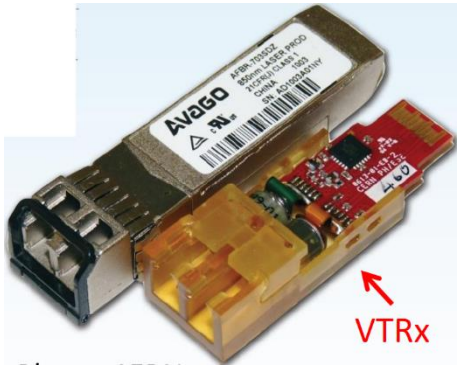
# Back up slides

# Radiation tolerant components

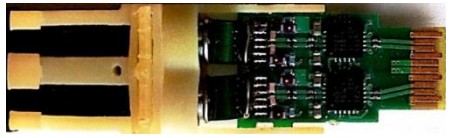
**GBTX ASIC**

- Is using the IBM/GlobalFoundries 130nm CMOS technology
- Power supply @ 1.5V
- Power consumption is 2.2W (full operation)
- E-Links use Scalable Low-Voltage Signalling (SLVS) for 400mV (SLVS-400)

GBTX ASIC




VTRX vs SFP



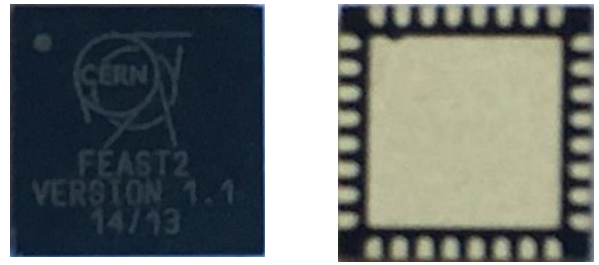
VTTX

**VTRX optical transceiver (consists of 2 ASICS)**

- The GigaBit TransImpendance Amplifier (GBTIA)
  - Bit rate of 5 Gbps (min)
  - Total jitter < 40 ps
  - Supply voltage: 2.5 V
  - Power consumption: 250 mW
- GigaBit Laser Diode (GBLD)
  - Bit rate of 5 Gbps (min)
  - Supply voltage: 2.5V
  - Power consumption: 325mW
- 45.3 mm * 14:5 mm * 10mm (w * l * h)

**FEAST ASIC**

- Input voltage range 5 to 12V
- Minimum output voltage 0.6 V
- Continuous 4A load capability
- Very low output noise (Low Drop Out regulators will not be used)
- Adjustable switching frequency 1-3 MHz
- Radiation and magnetic tolerant:



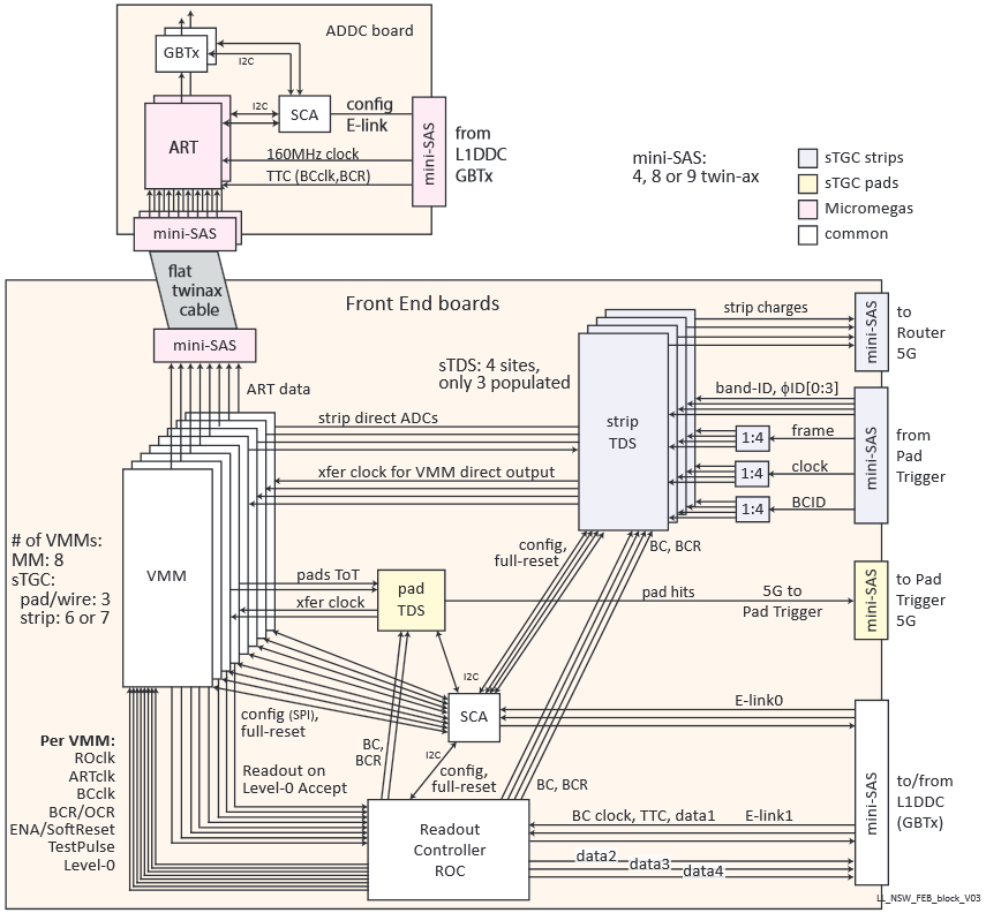

FEAST ASIC

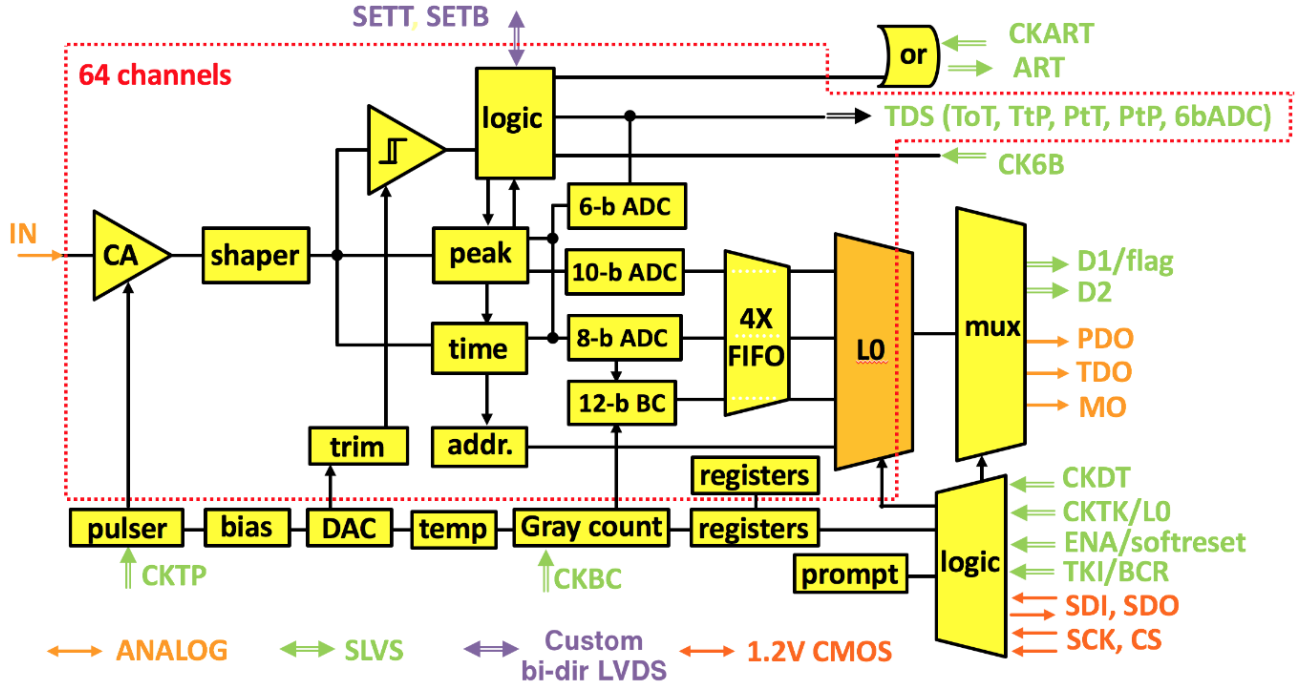
**GBT-SCA ASIC**

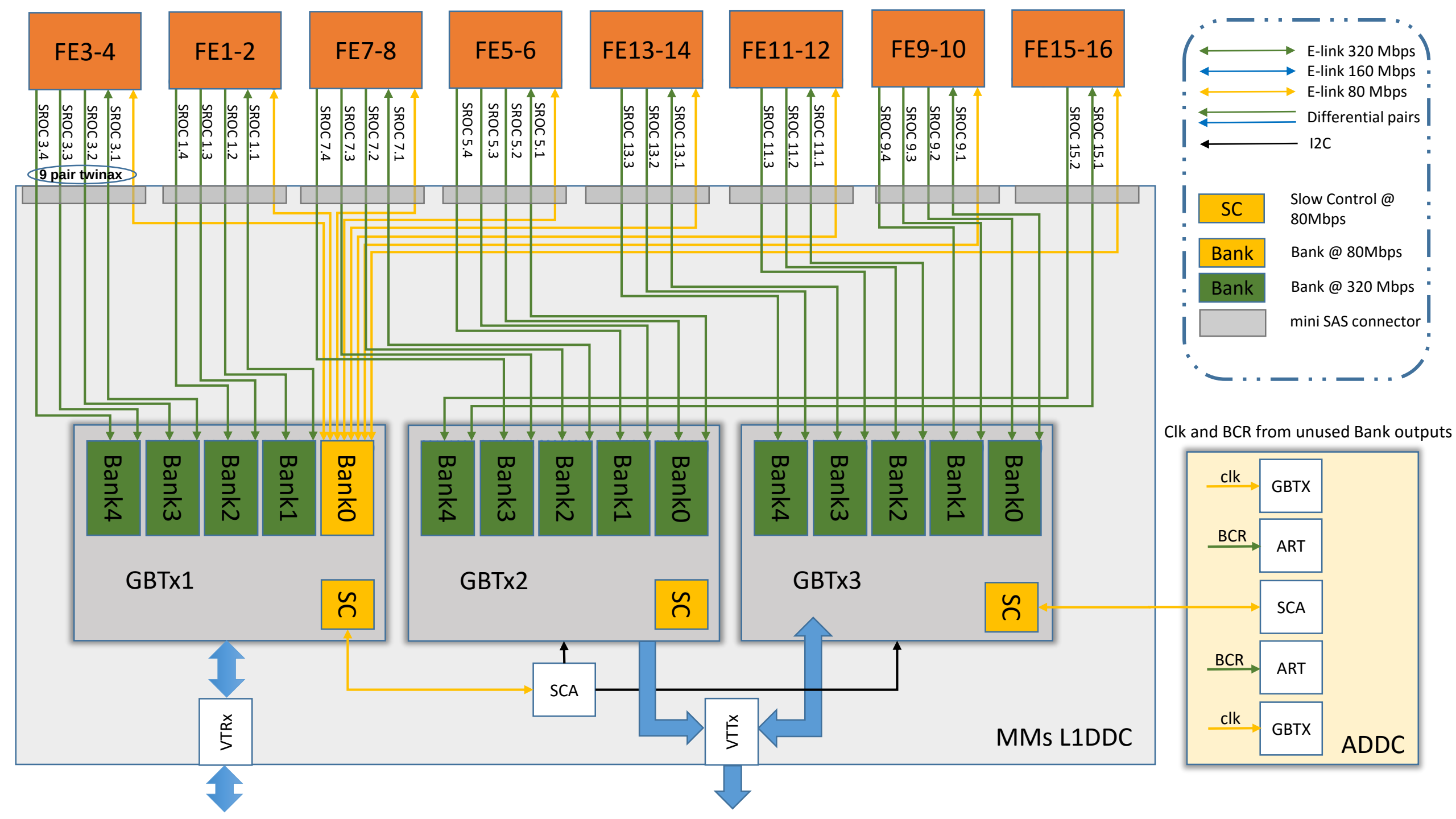
- Supply voltage: 1.5 V or 1.2 V
- Package Type: LFBGA
- 0.8 Pitch
- Pin count 196
- Ball size 0.5mm


GBT-SCA ASIC

# VMM architecture

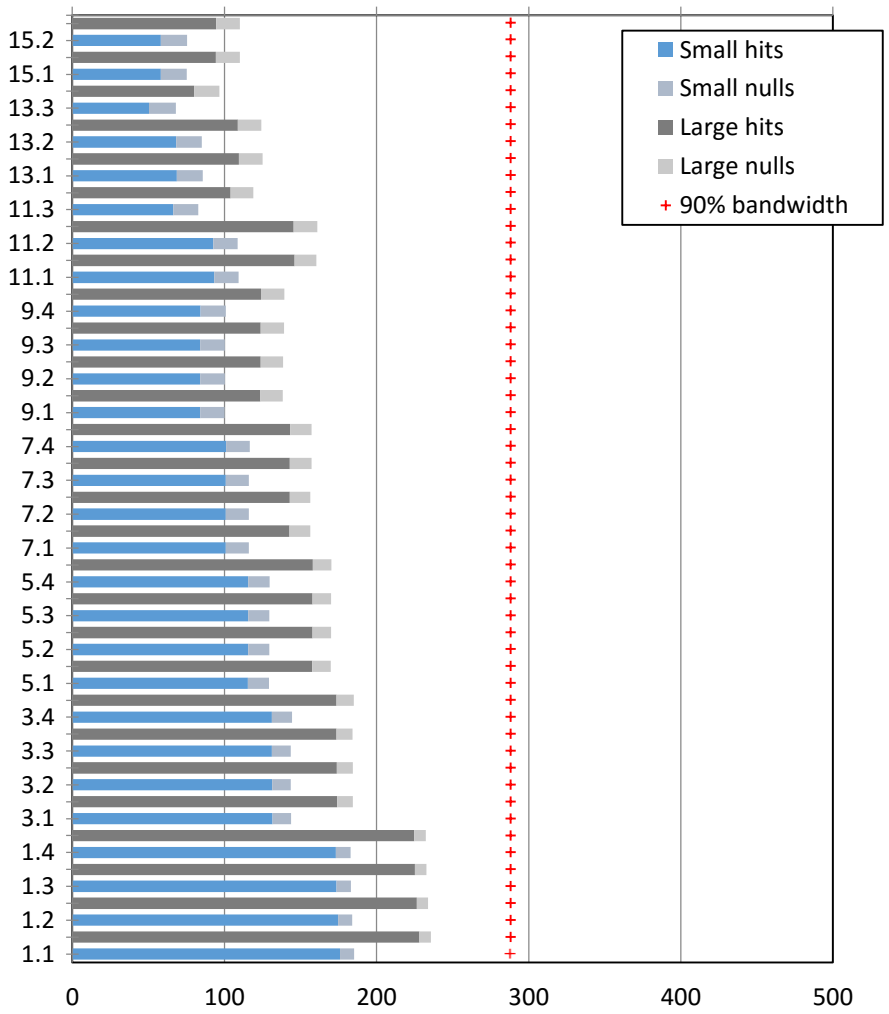


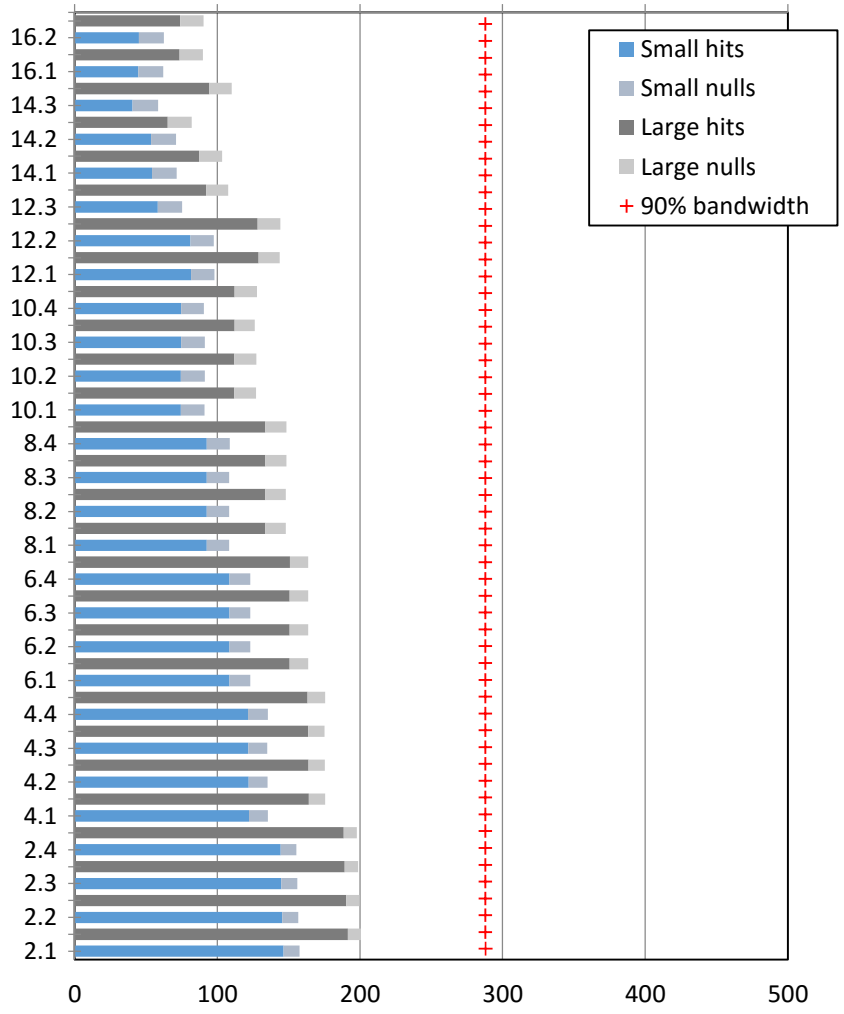




FE3-4
FE1-2
FE7-8
FE5-6
FE13-14
FE11-12
FE9-10
FE15-16
SROC 3.4
SROC 3.3
SROC 3.2
SROC 3.1
9 pair twinax
SROC 1.4
SROC 1.3
SROC 1.2
SROC 1.1
SROC 7.4
SROC 7.3
SROC 7.2
SROC 7.1
SROC 5.4
SROC 5.3
SROC 5.2
SROC 5.1
SROC 13.3
SROC 13.2
SROC 13.1
SROC 11.3
SROC 11.2
SROC 11.1
SROC 9.4
SROC 9.3
SROC 9.2
SROC 9.1
SROC 15.2
SROC 15.1
E-link 320 Mbps
E-link 160 Mbps
E-link 80 Mbps
Differential pairs
I2C
SC
Slow Control @ 80Mbps
Bank
Bank @ 80Mbps
Bank
Bank @ 320 Mbps
mini SAS connector
Bank4
Bank3
Bank2
Bank1
Bank0
GBTx1
GBTx2
GBTx3
SC
SCA
VTRx
VTTx
MMs L1DDC
Clk and BCR from unused Bank outputs
clk
GBTX
BCR
ART
SCA
BCR
ART
clk
GBTX
ADDC

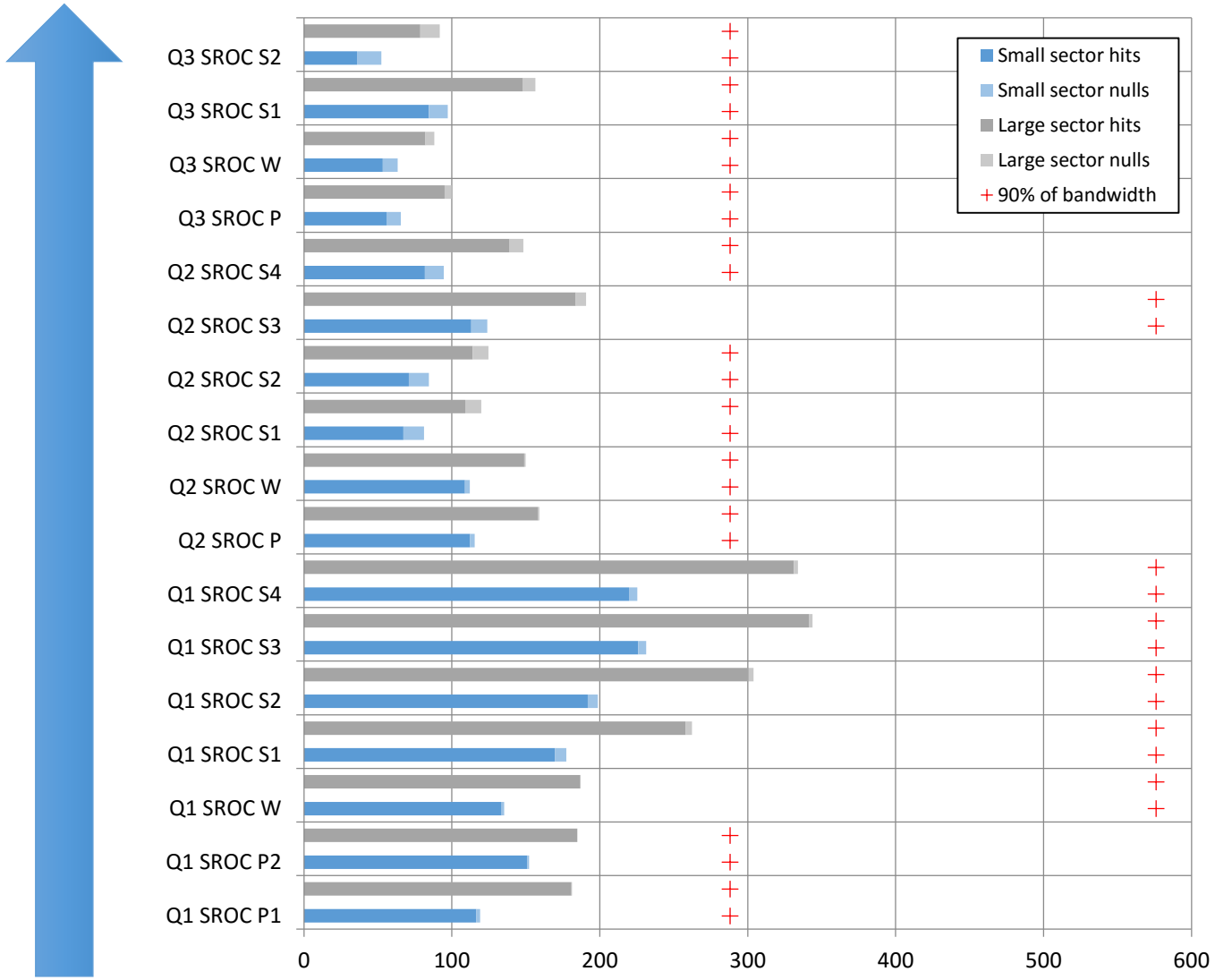
# E-Link rates for MMs detectors (3GBTX)

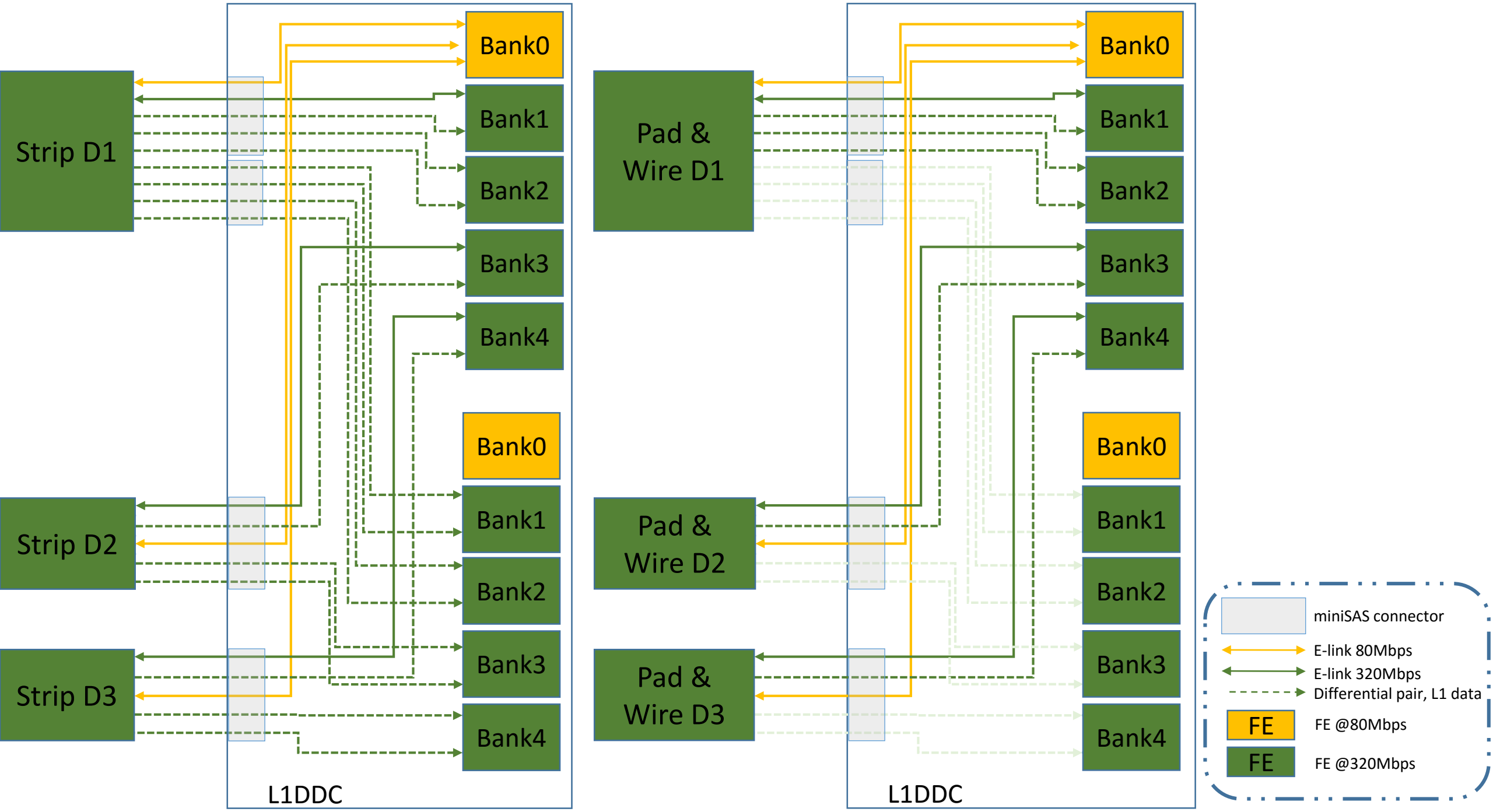
R



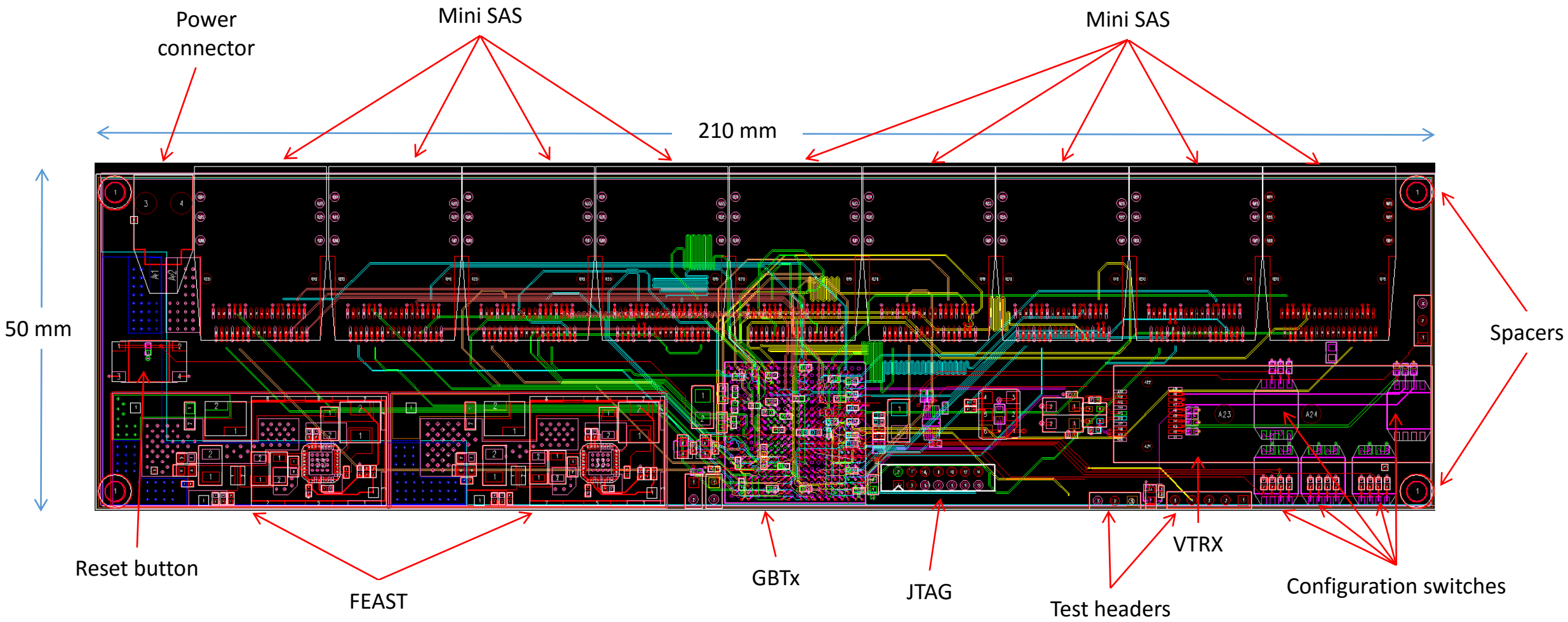



# E-Link rates for sTGC detectors

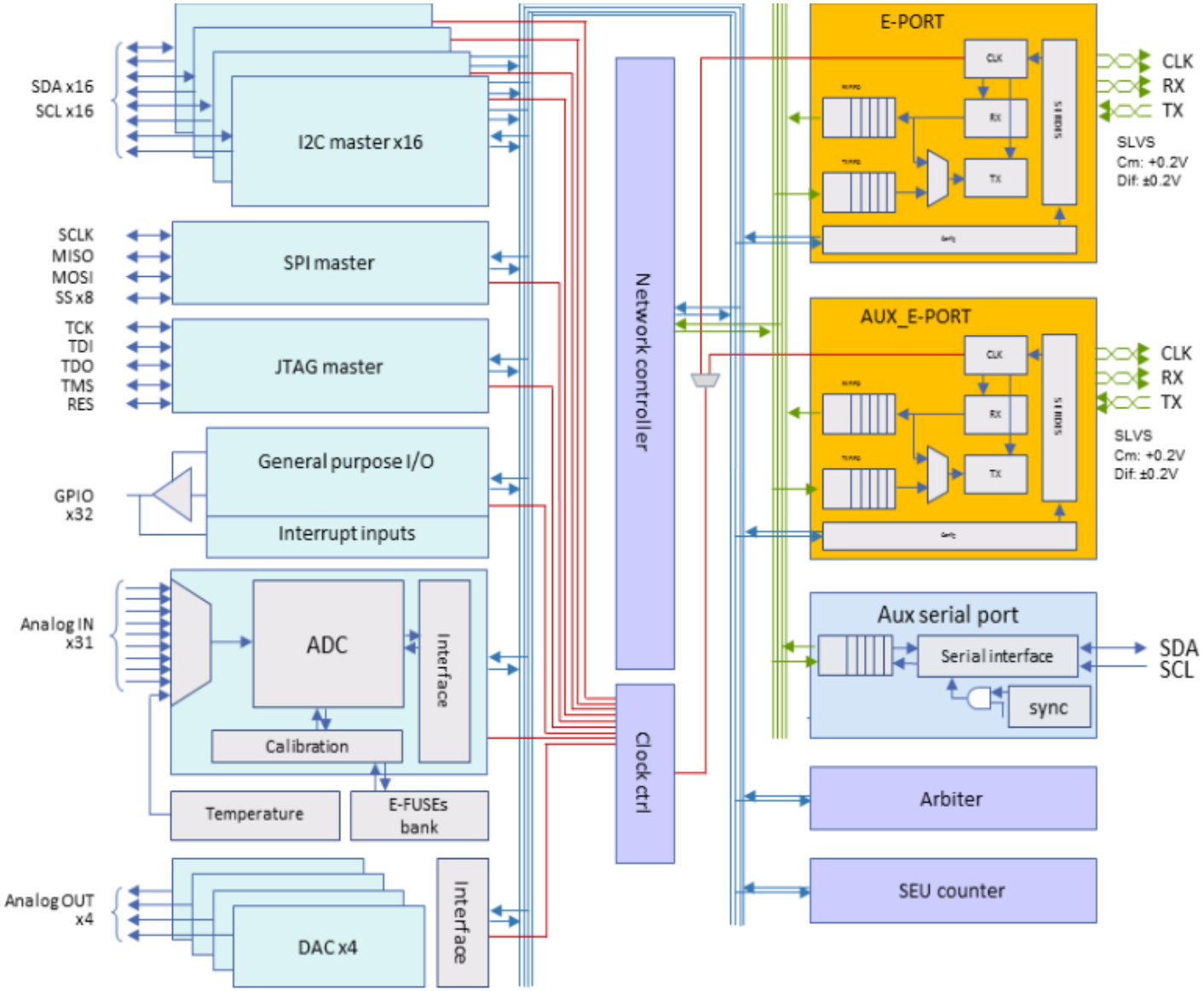



Strip D1
Strip D2
Strip D3
Bank0
Bank1
Bank2
Bank3
Bank4
L1DDC
Pad & Wire D1
Pad & Wire D2
Pad & Wire D3
Bank0
Bank1
Bank2
Bank3
Bank4
L1DDC
miniSAS connector
E-link 80Mbps
E-link 320Mbps
Differential pair, L1 data
FE
FE @80Mbps
FE
FE @320Mbps

# Current L1DDC prototype 2 layout (400 KHz Level-1)



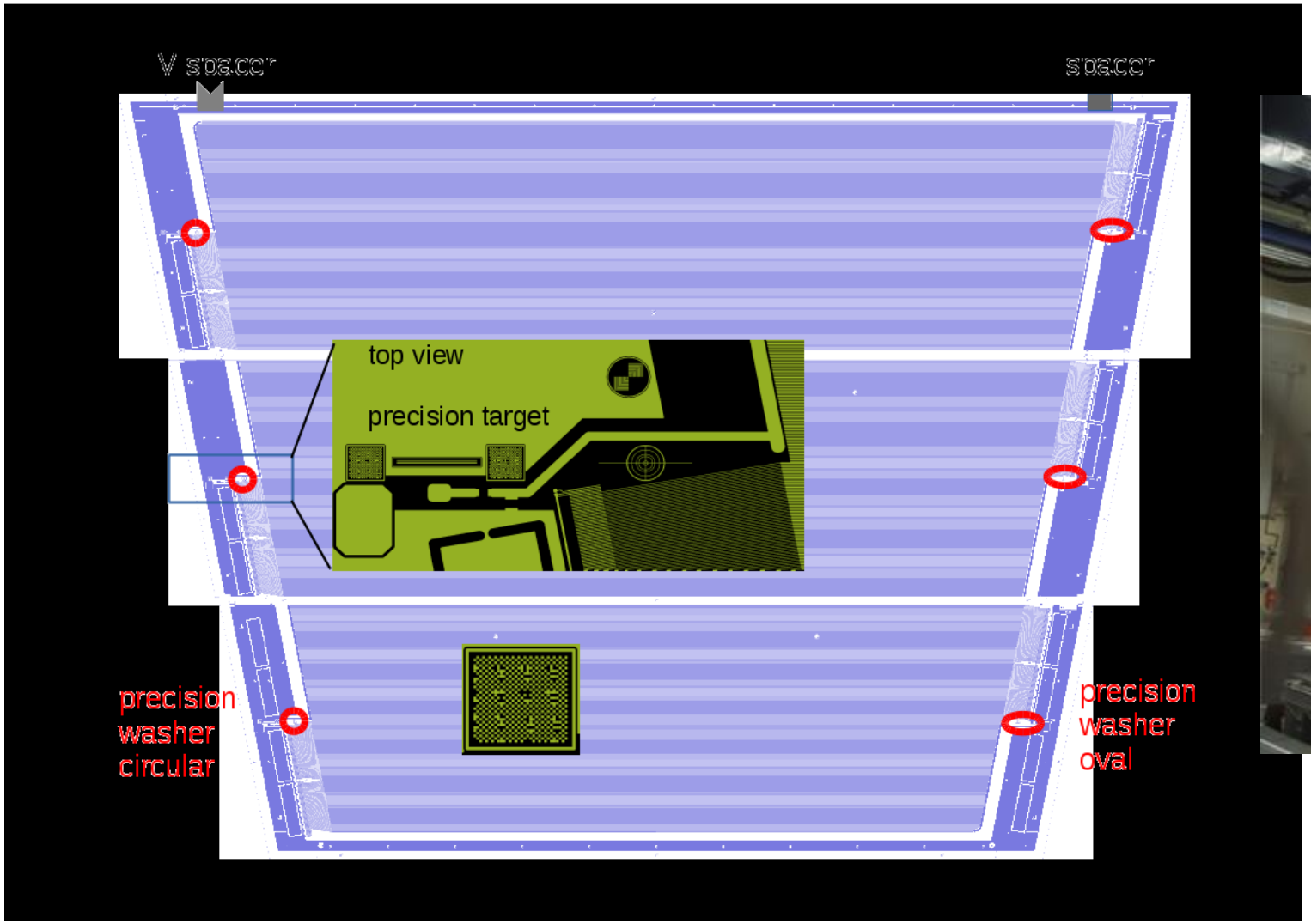
# GBT-SCA

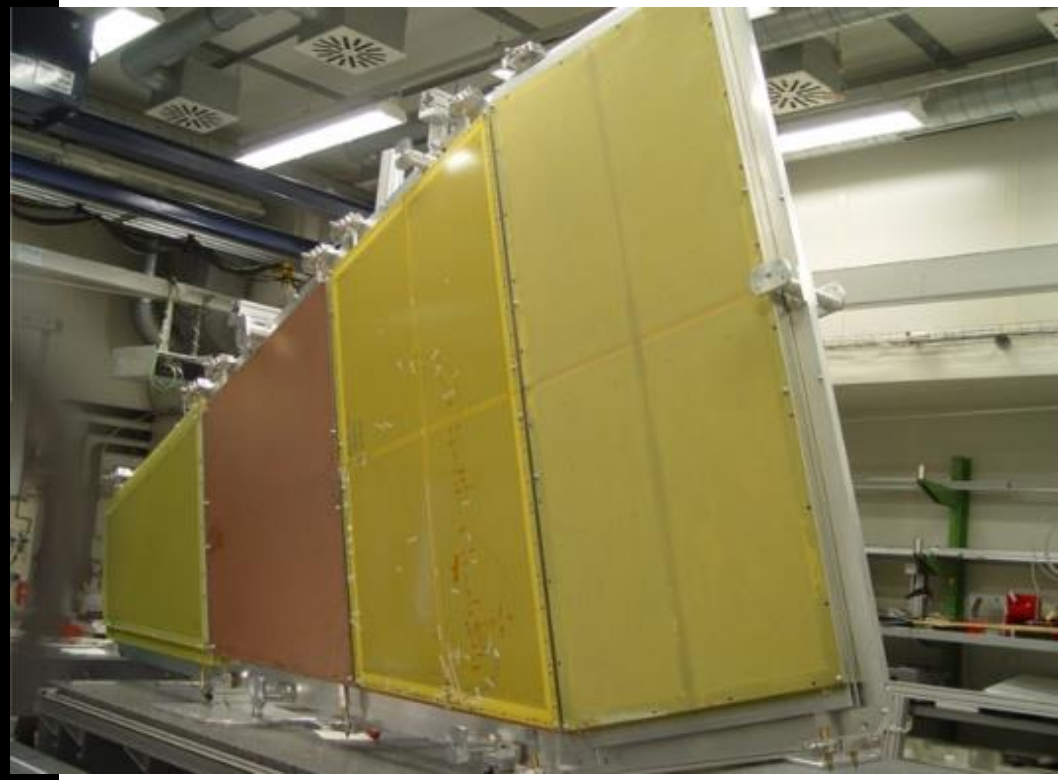



Taken by GBT-SCA manual

# MMs detector

MMs PCB layout

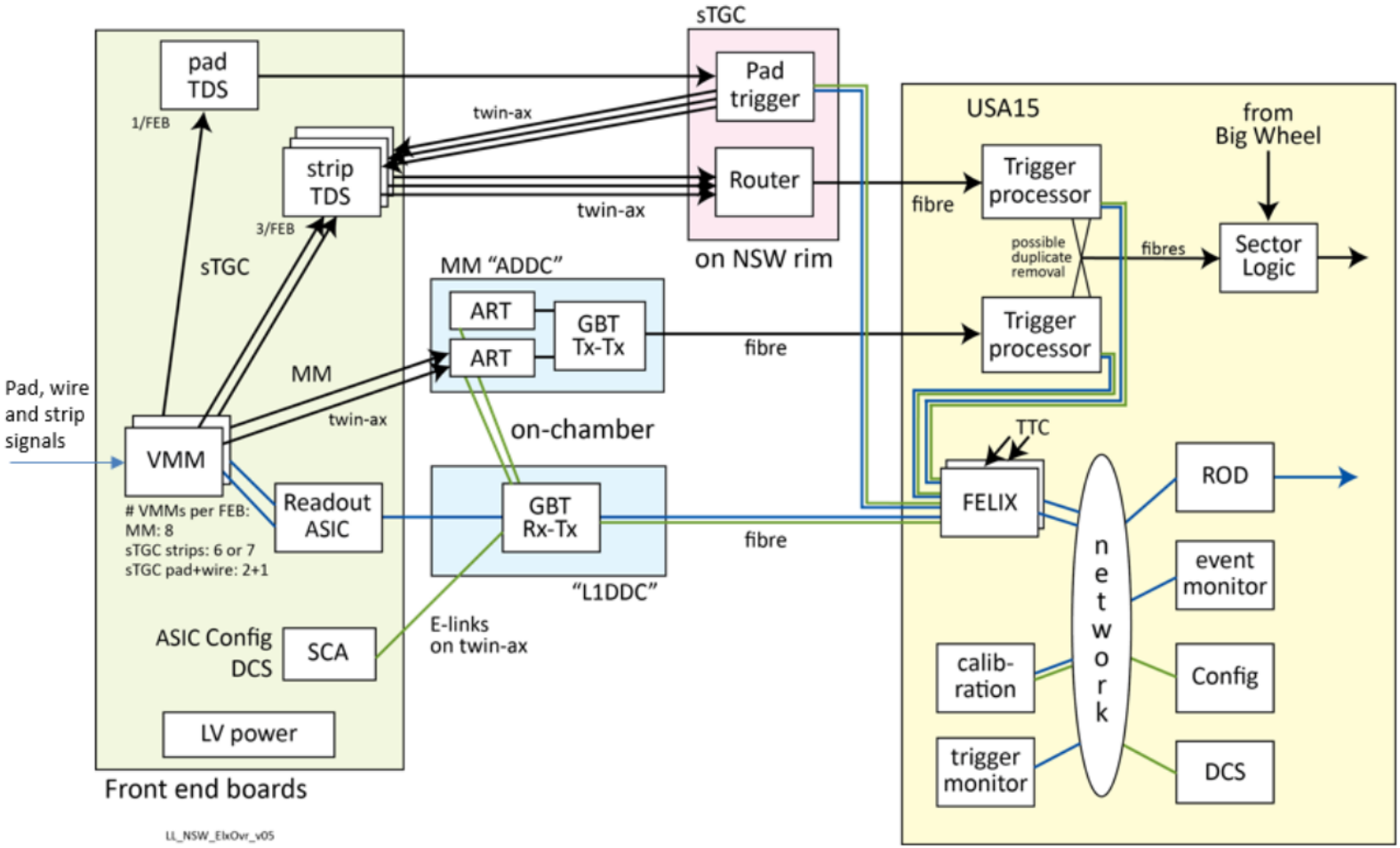


Constructed MMs plane (Large Module)

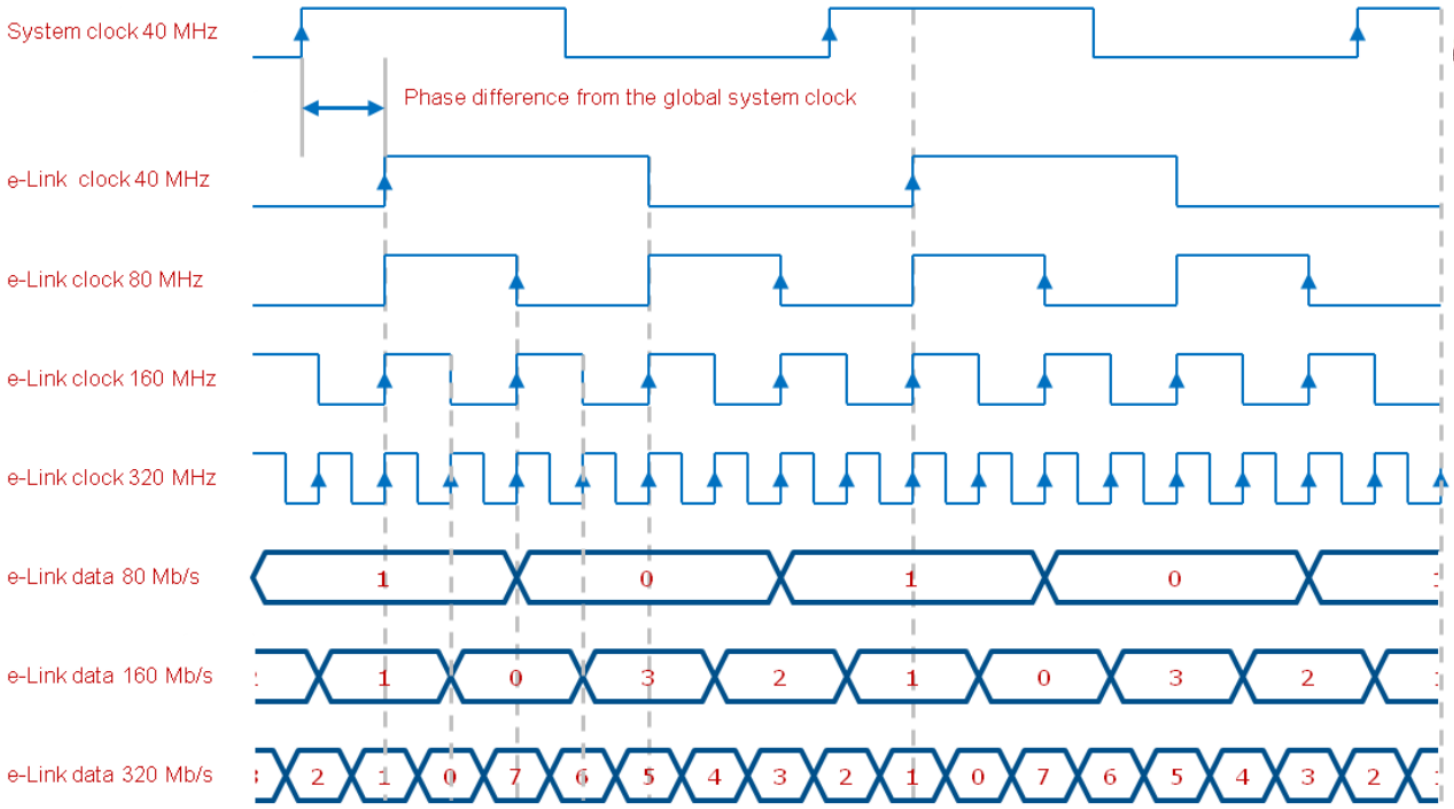
# sTGC trigger

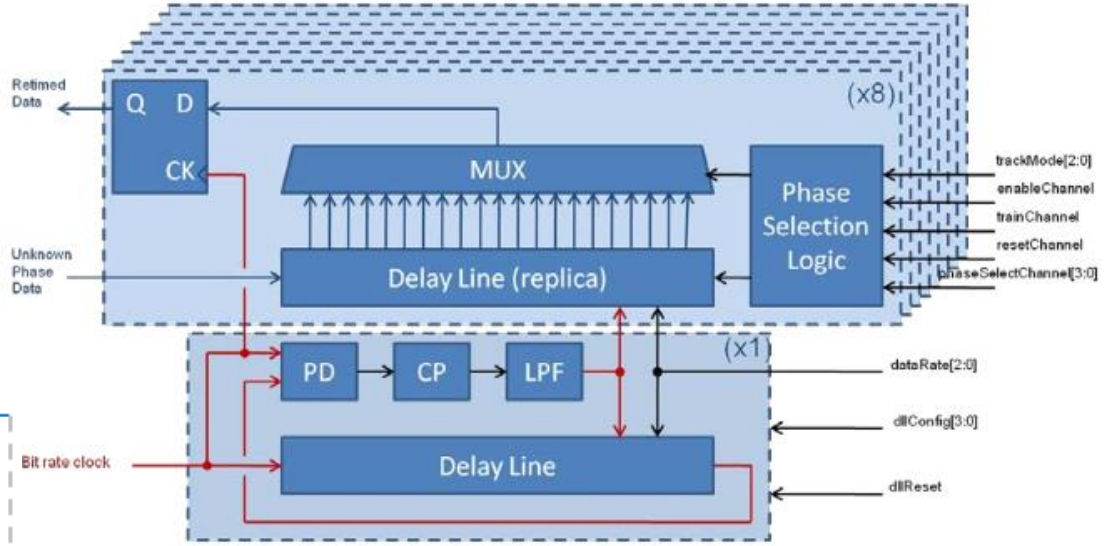
- The digitized signal (time and amplitude) from FEs is sent to the pTDS where the strips are buffered and tagged with the BCID
- Pad signals are sent to the pad trigger logic, which identifies a track
- The candidate geometrical coordinates together with its corresponding BCID are sent to the front-end sTDS
- The sTDS then transmits the strip charges, BCID, band-ID, and ϕ-ID
- Router handle all incoming traffic from the TDS chips
- Signals are sent by fiber to track finding processors at USA15 where centroids and track segments are calculated and sent to sector logic to be combined with candidate tracks from the Big Wheel



# E-Link clocks

Clock and data-down relation




Data phase aligner for the data-up

Figures taken from GBTX manual

# Overall scheme

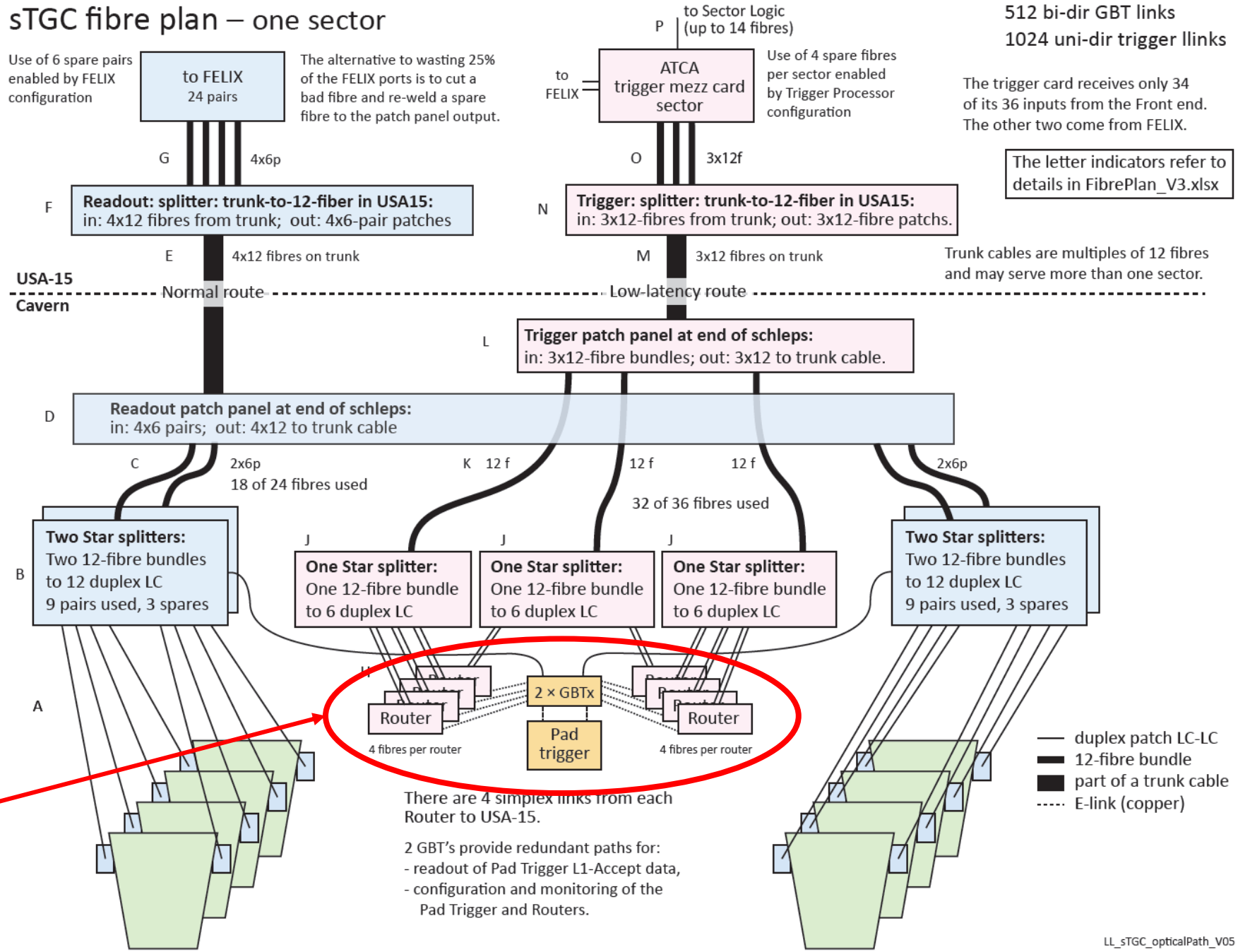
Rim electronics – 10 boards

- 8 Routers
- 1 PAD trigger
- 1 RIM-GBT

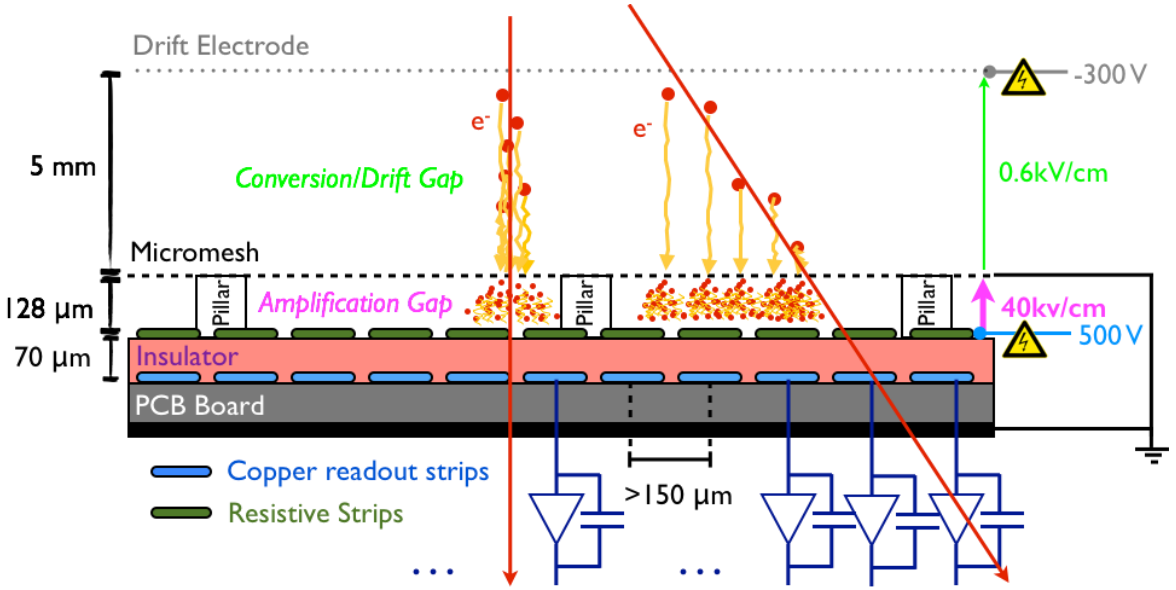
RIM-GBT

- Transmits
  - configuration data and clock to SCA
  - BC clock to FPGA
  - Configuration data to FPGA
  - Any additional data to FPGA
- Receives
  - monitoring data from SCAs
  - Data from the FPGA

RIM boards



# Operation principle MMs and sTGC




MM detector principle

Micromegas – 2.097.152 channels

-Strip pitch: 450 µm for Large Module (LM), 425 µm for Small Module (SM)

-Readout Strips: 300 µm, Resistive Strips: 250 µm

-Data rates: LM – 7.99 Gbps/plane, SM – 4.39 Gbps/plane

sTGC – 331.744 channels

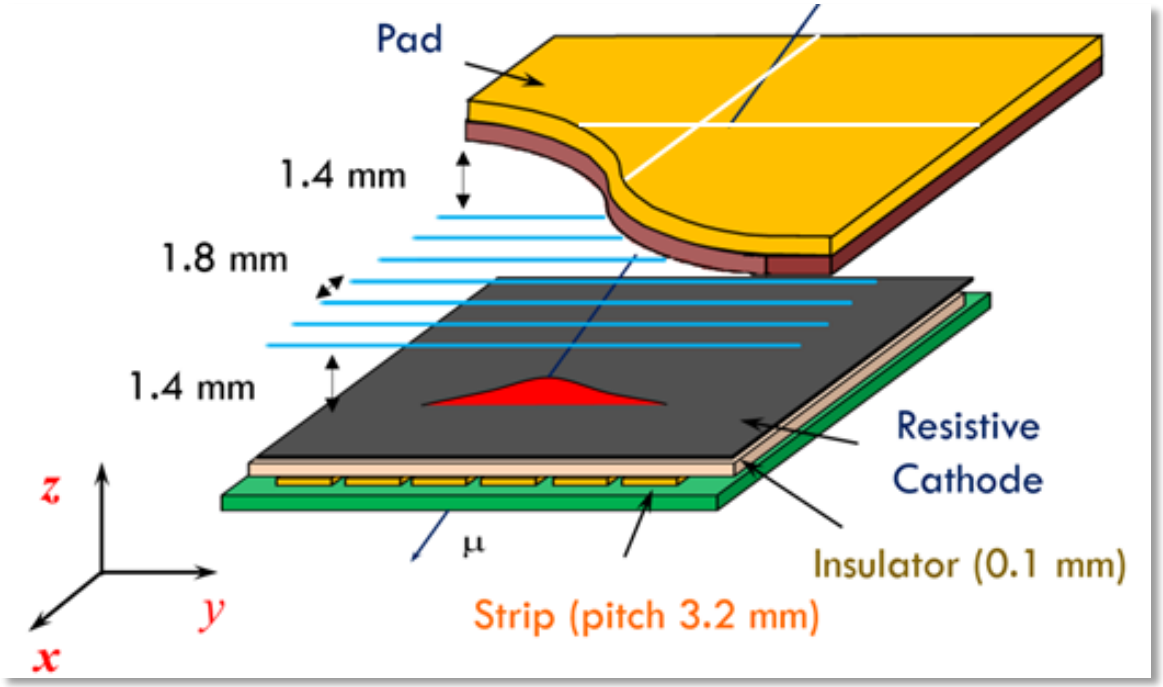
-Wires: 50 µm, pitch 1.8 mm

-Strips: pitch 3.2 mm

-Data rates:

-Strips: LM – 1.77 Gbps/plane, SM – 1.14 Gbps/plane

-Pads & Wires: LM – 1.04 Gbps/plane, SM – 632 Mbps/plane




sTGC detector principle