A high throughput ADC system for the PROMETEO test-bench of the ATLAS Tile Calorimeter

Matthew Spoor

matthew.spoor@cern.ch

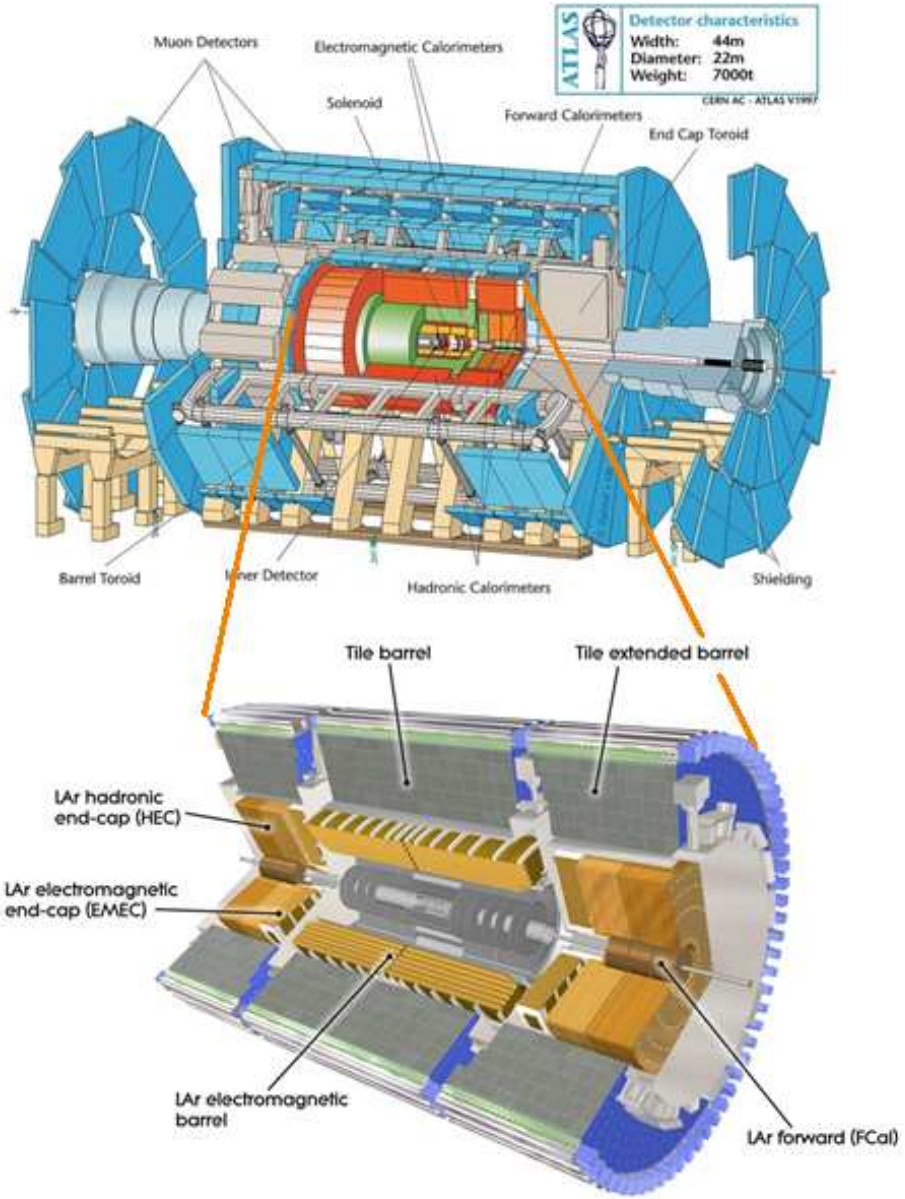
University of the Witwatersrand, SA

HEPP, Febuary 2016

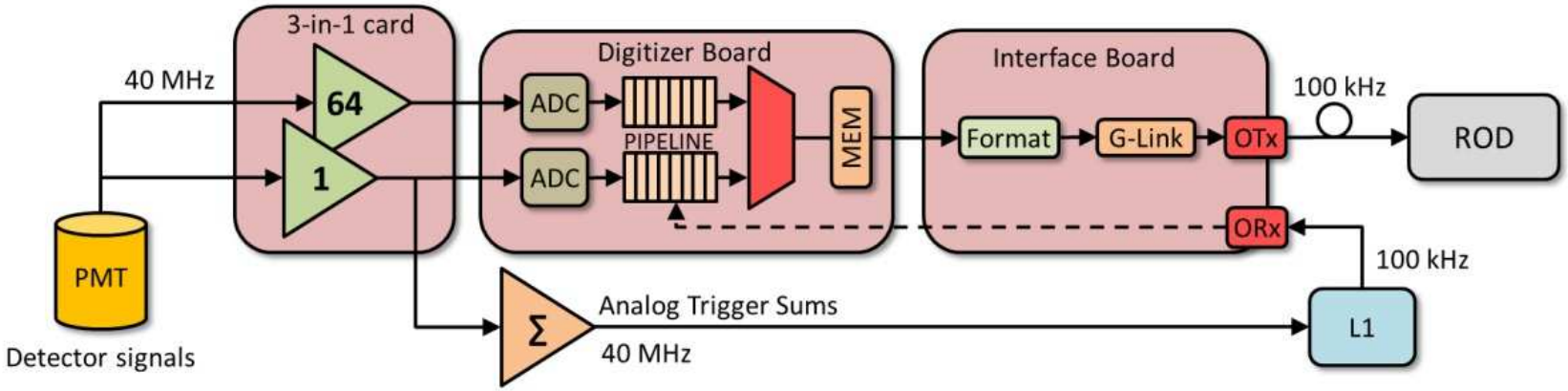
Outline

ATLAS Tile Calorimeter

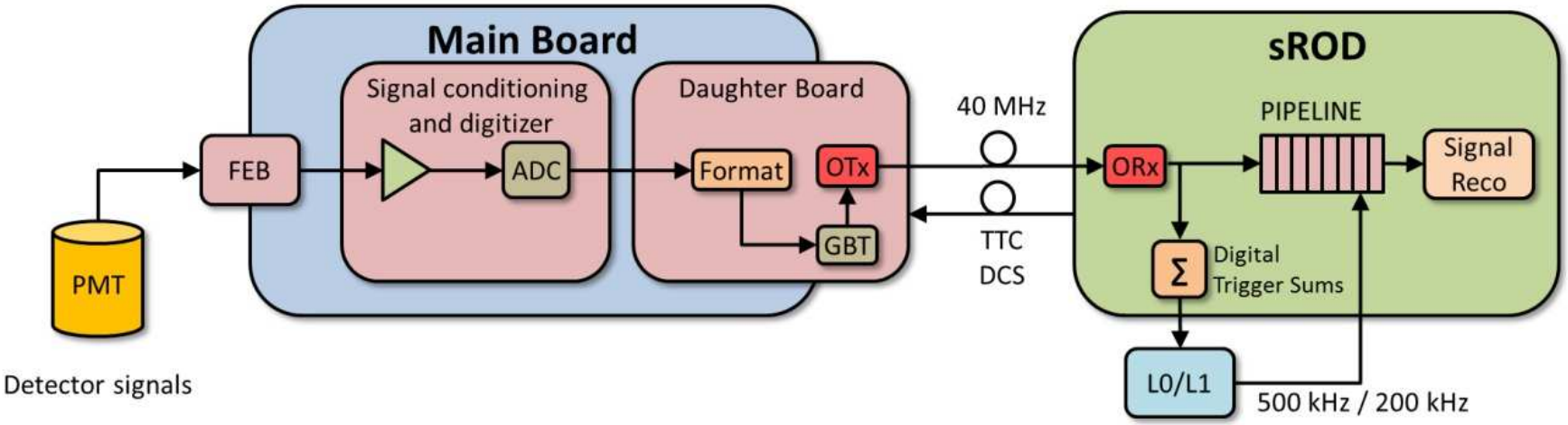
- General purpose particle detector (Proton-Proton)
- 40 MHz collision rate
- Millions of readout channels
- Petabytes of data generated a second



Phase II Upgrade - TileCal readout electronics



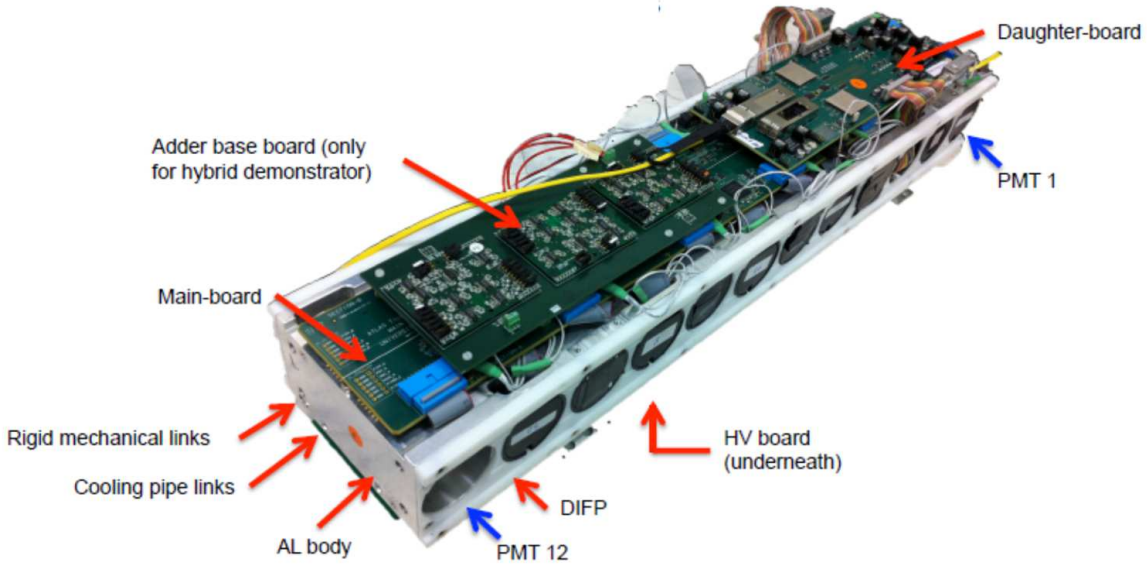
Present front-end electronics.



Equivalent Phase-II upgrade electronics.

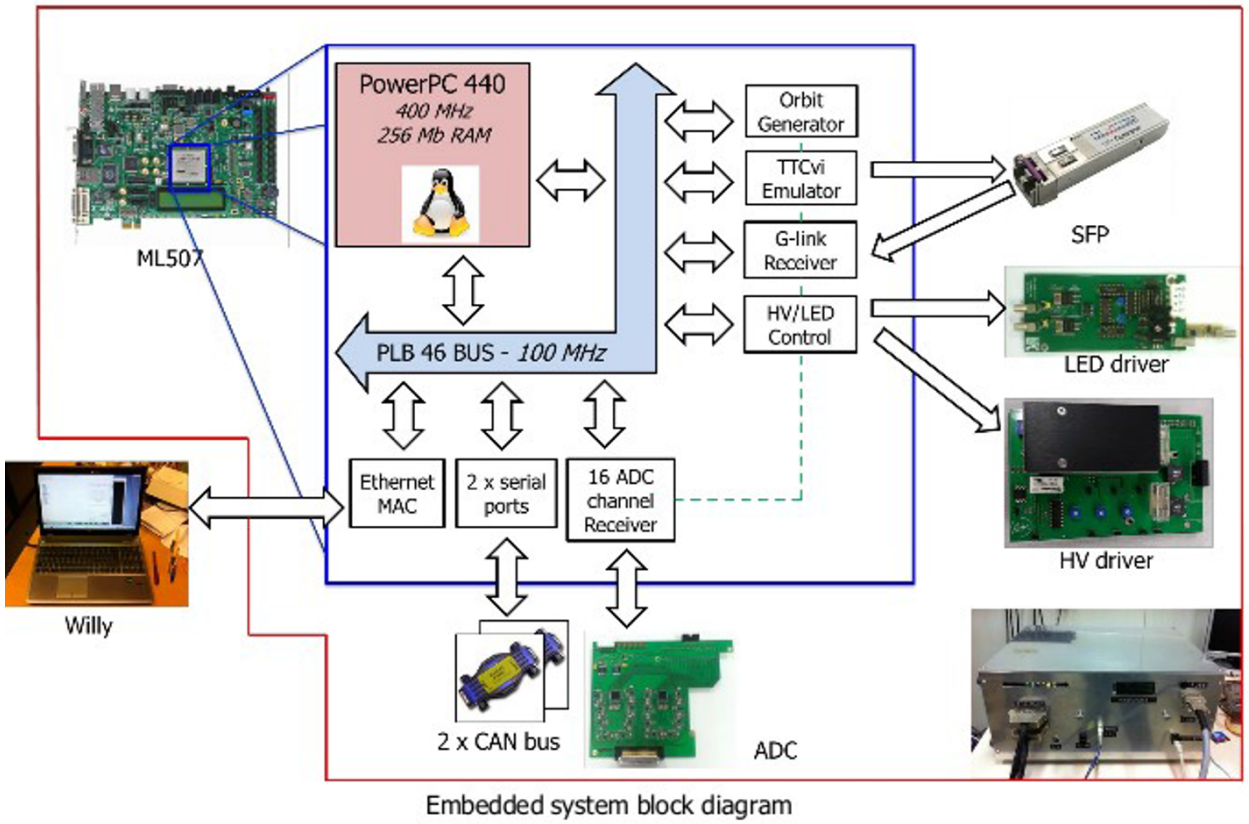
Hybrid Demonstrator

- Validation of the new readout architecture, trigger system interfaces.
- Divides each TileCal module into 4 separate mini-drawers.
- Mini-drawer: Mainboard, Daughterboard, 12 PMTs, HV card and Adder board
- Compatible with old architecture.



Mini-Drawer.

MobiDICK test-bench

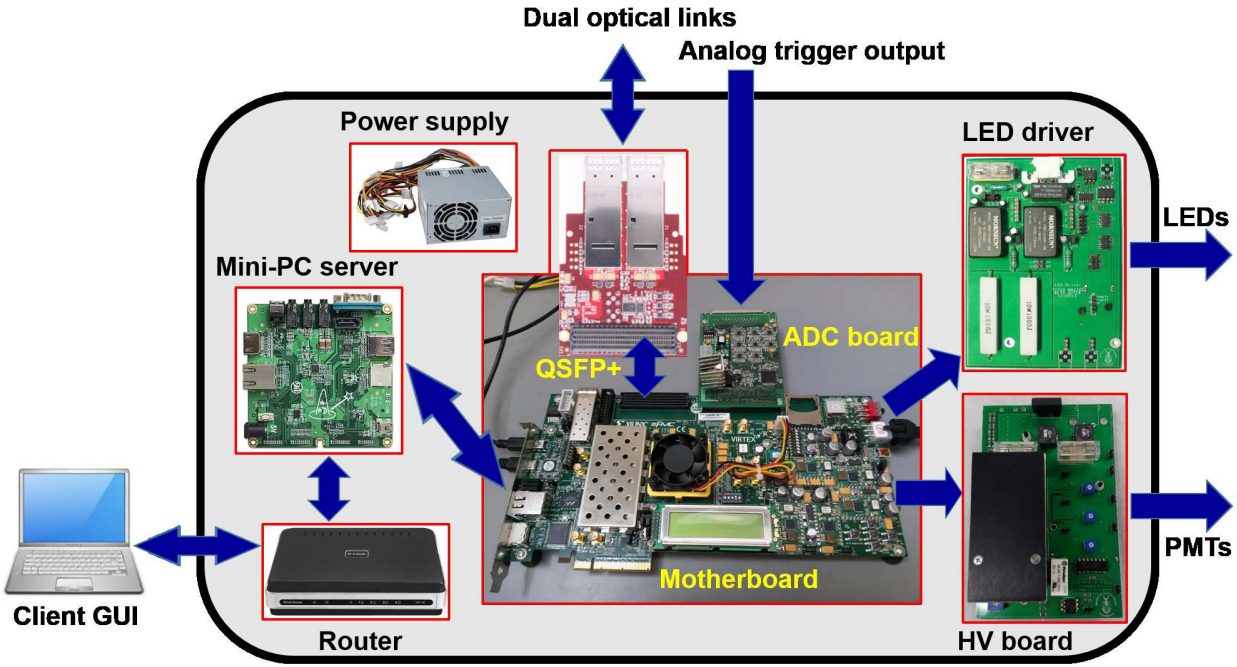


Embedded system block diagram

Design of PROMETEO.

- Main board: Xilinx ML507 evaluation board
- Recording data after L1 trigger @ 100 kHz
- Using slow canbus to control 3in1 cards and HV in each PMT
- Server running on PPC, connects to client via Ethernets

PROMETEO test-bench



Design of PROMETEO.

- Main board: Xilinx VC707 and QSFP+ to transfer data through FMC connectors at 40 MHz
- Bandwidth upgrades from 640 Mbps/s to 40 Gbps
- Full compatibility to sROD in the TileCal, sharing the main board
- Removed Canbus dongles
- Using IP bus protocol, firmware manipulated directly by client via ethernet

PROMETEO test-bench: Requirements

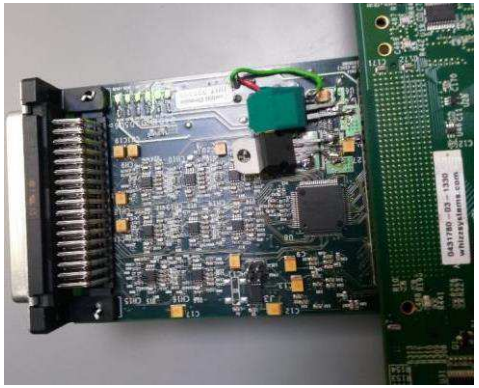
- Conceptual design requirements for PROMETEO:
  - read-out data from 12 PMTs at the LHC bunch crossing frequency
  - assess the quality of data in real-time
  - be self-contained and portable
  - be low-cost and scalable for network usage

- PROMETEO has been designed to perform the following tests:
  - Charge Injection System (CIS) Noise/Linearity
  - Integrator Noise/Linearity
  - Pedestal Noise/Linearity
  - High Voltage (HV) Stability/Linearity

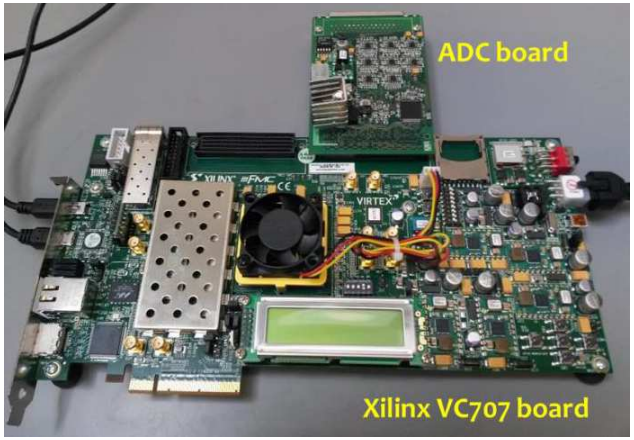
ADC FMC Trigger Board

Aim: Develop, test and validate a new ADC board for PROMETEO

- Redesign ADC PCB: smaller and VC707 compatible
- Troubleshoot and fix board prototypes
- Complete redesign of firmware
- Perform validation testing



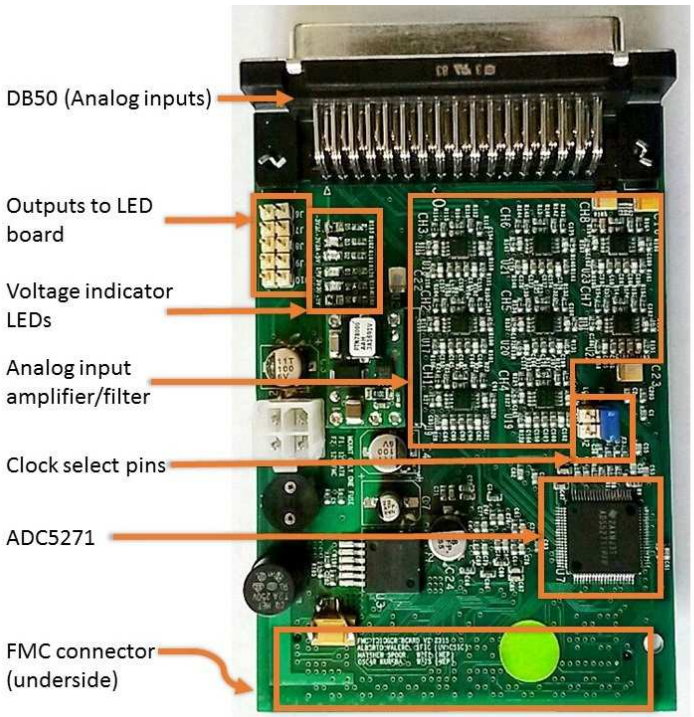
ADC v1 Prototype.



ADC connected to the VC707 through FMC.

ADC FMC Trigger Board

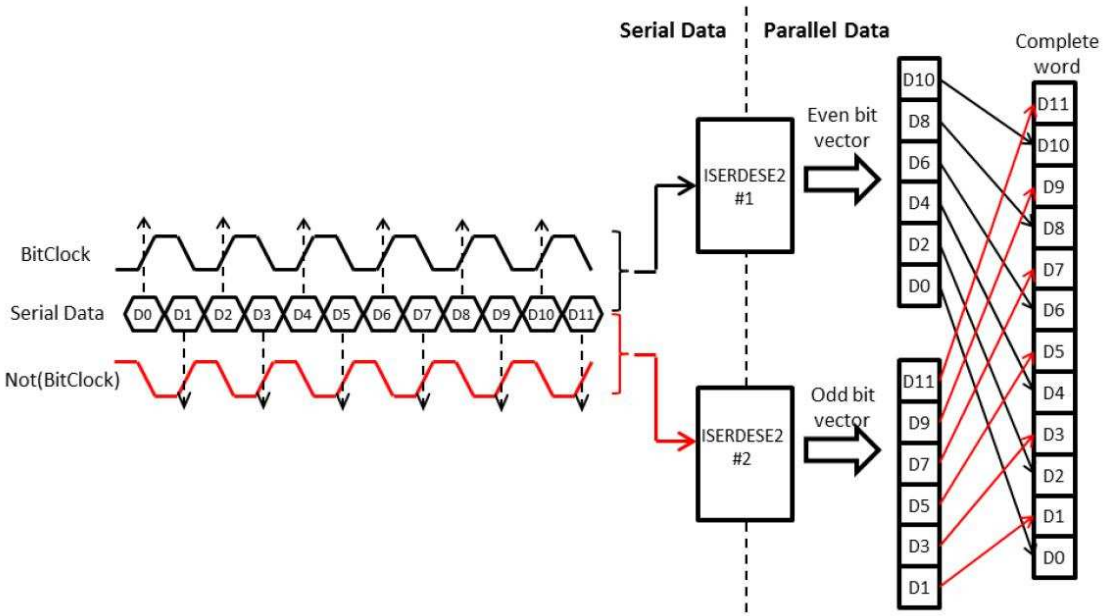
- Part of the PROMETEO:
  - Test the adder cards in the hybrid demonstrator drawer
  - Digitizes analog signals coming from the Hadron and Muon trigger cables
- Hardware specifications
  - Based on the MobiDICK ADC board design
  - FPGA Mezzanine Card (FMC) format
  - 2 x Texas Instruments ADS5271
    - 8 ADC channels per ADC
    - Up to 50 MSPS, 12 bit
  - DB50 connector
  - Status: V1 produced and tested + V2 Produced, final testing



ADC Trigger Board V2

Firmware

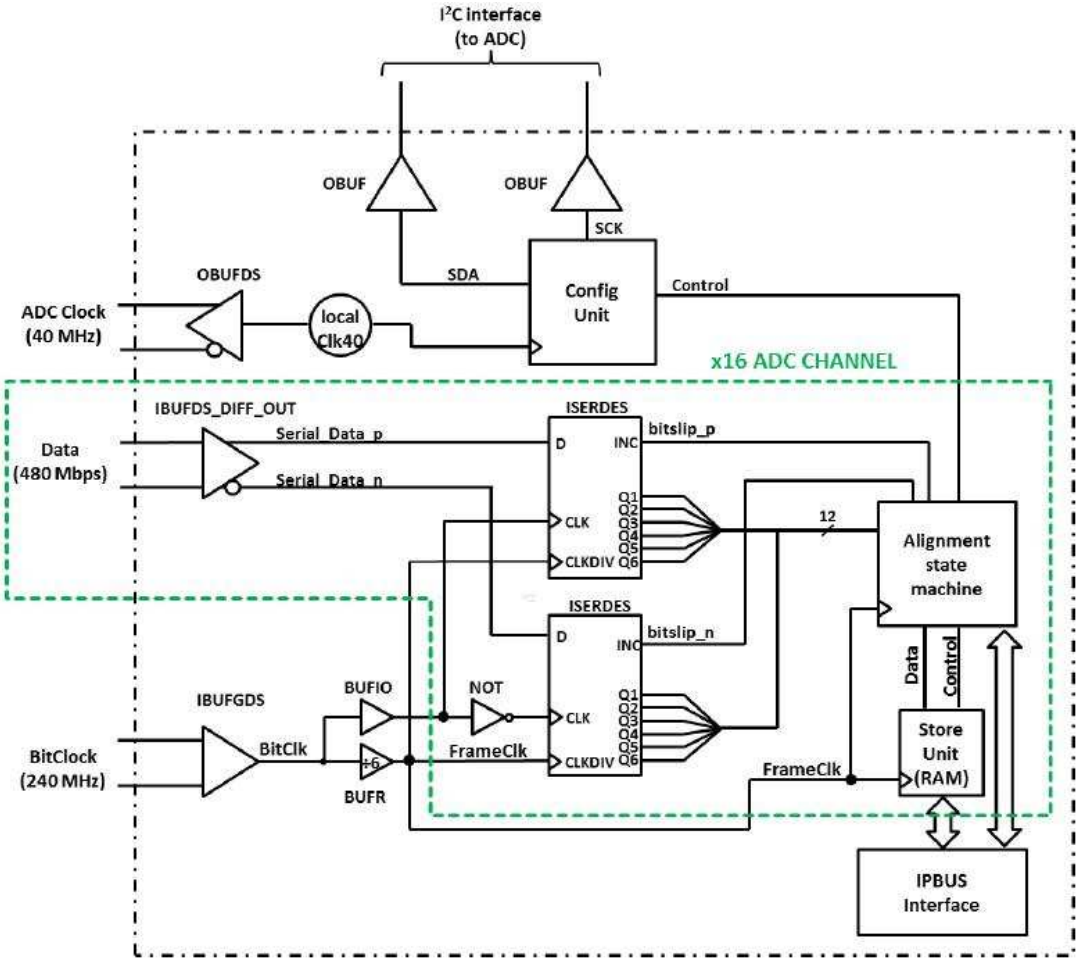
- Firmware Requirements:
  - Deserialisation of 16 ADC channels using regular IO pins
    - 480 MSPS (12 bits x 40 MHz)
    - Total of 7.68 Gbps
  - Configuration of the ADC (I2C interface)
  - Storage in FIFO memories or IPBus registers
  - Status: Under development
- ADC readout cell
  - Two ISERDESE2 blocks: Single Data Rate, 6 bits
  - Latching positive and negative data ports independently



ADC readout cell

Complete Architecture

- Modules that are needed:
  - 16 x ADC readout cell
  - configuration unit
    - I2C interface
  - Send 40 MHz Clock (From ADC)
    - ADC and FPGA firmware running in the same clock domain
  - FIFO memories or IPBUS memories
  - State machines
    - Word and Bit Alignment
    - Control and Data Flow

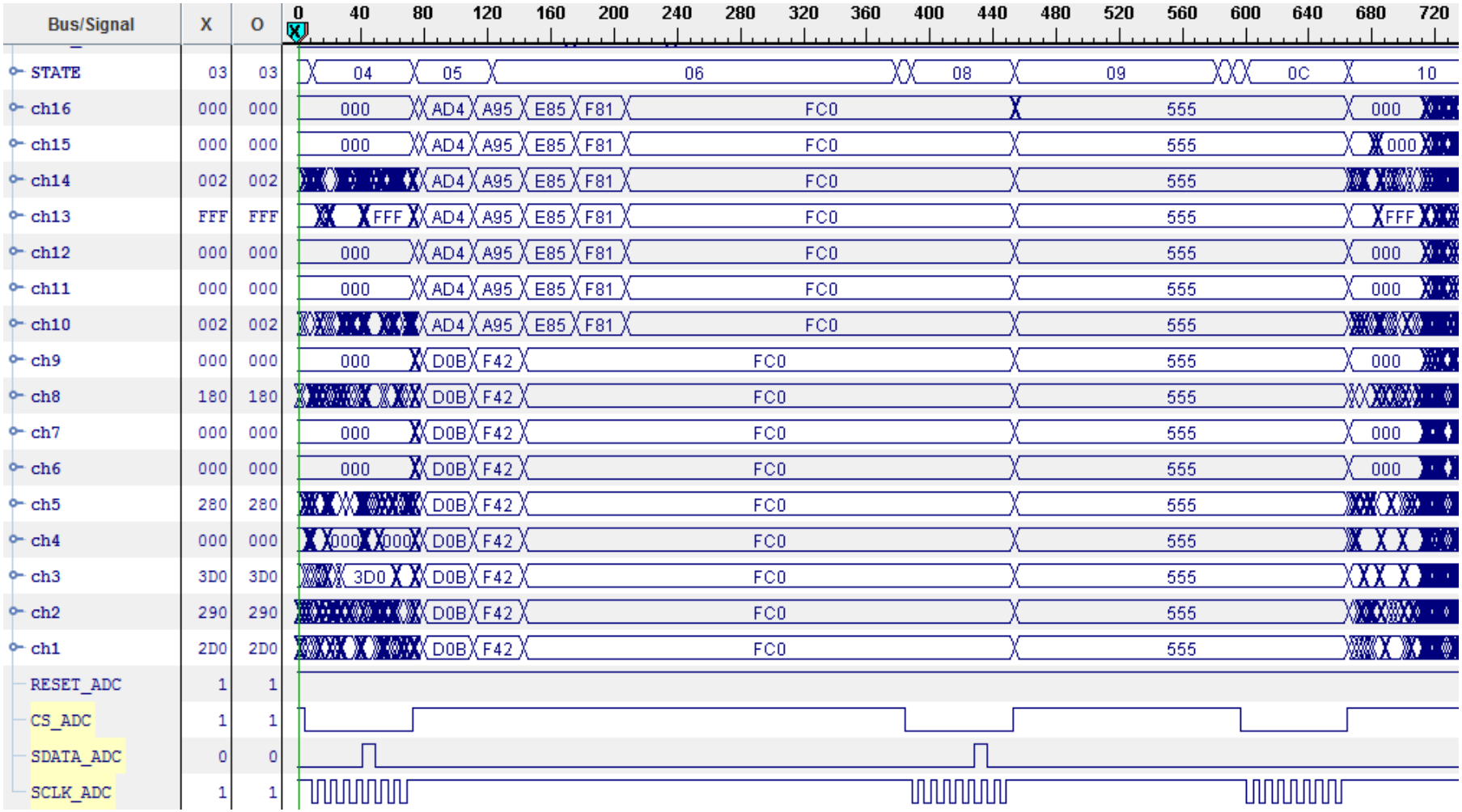


FPGA firmware layout

Alignment Simulation

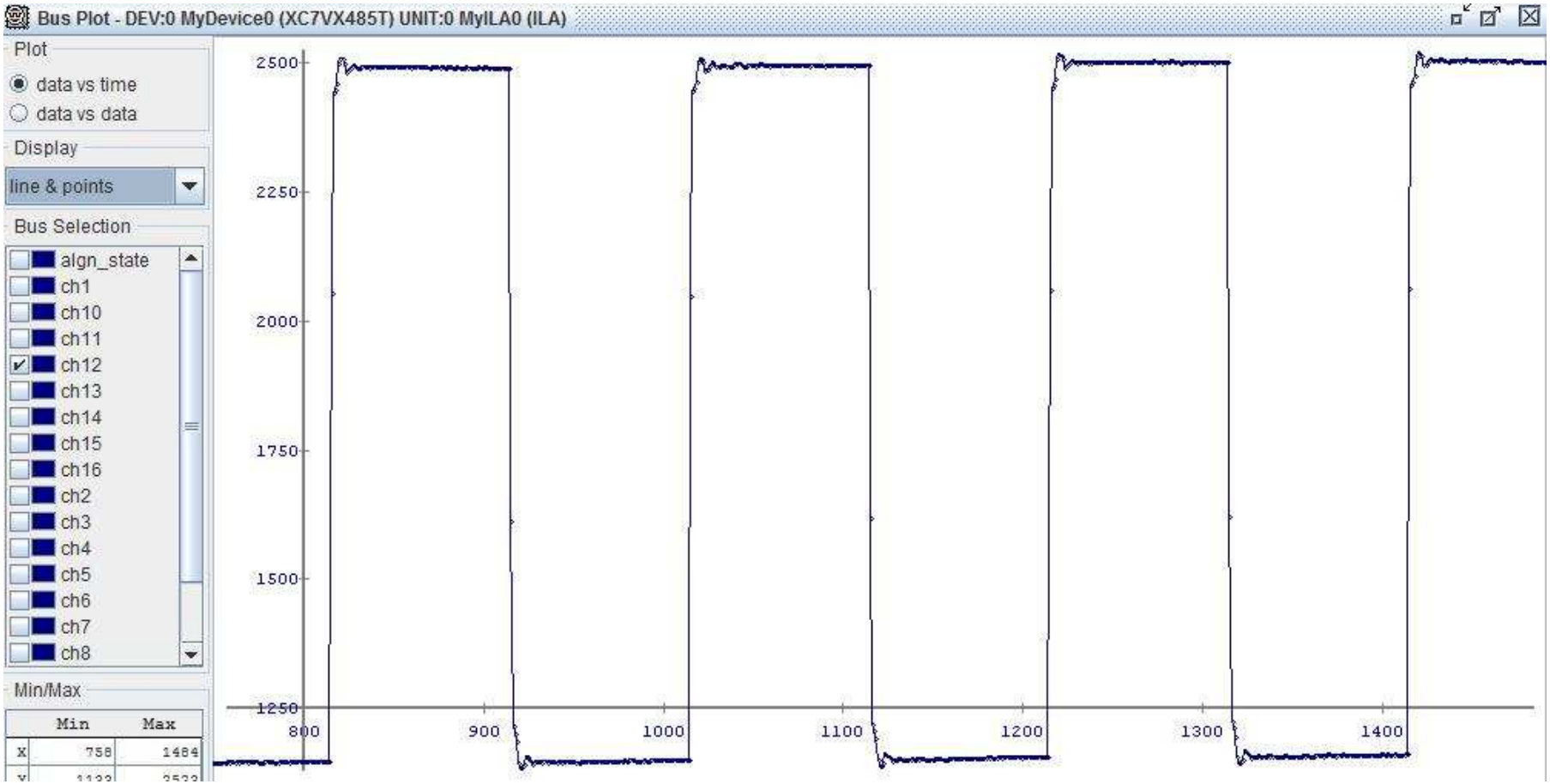
Data alignment simulation

ADC Setup



ADC setup and data readout

Analog testing



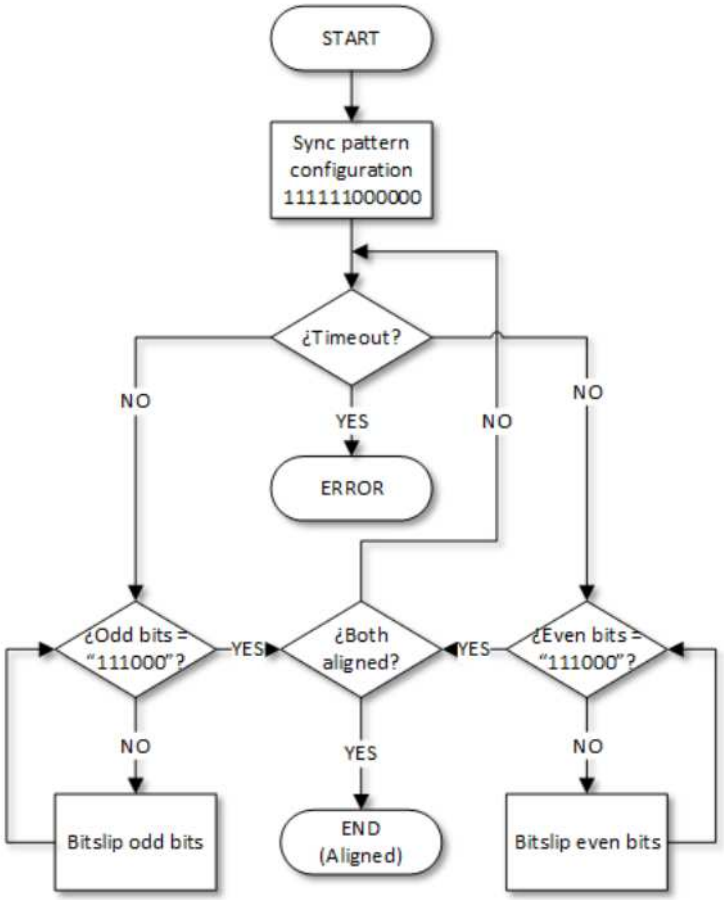
200KHz 0.9-1.9V, Analog input

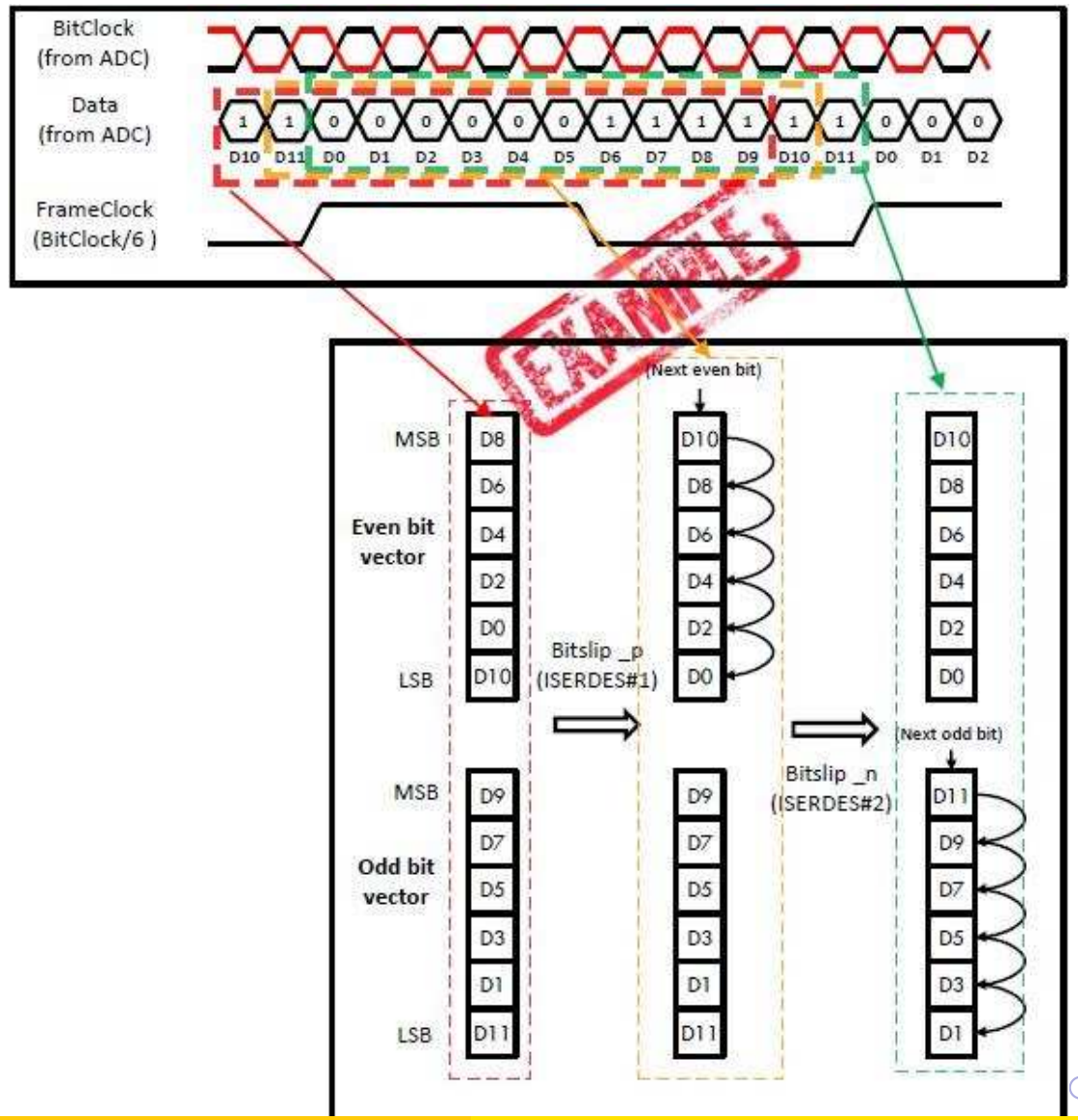
Status of the ADC board

- PCB
  - x2 V2.0 ADC boards manufactured in SA last year
  - Has undergone testing at WITS and CERN
  - **Functional!**
  - To be installed in a PROMETEO system later this month
  - x6 boards to be manufactured (x4 Prometeo Systems, x2 backup)
- Firmware
  - Majority of firmware completed
  - Still needs IPbus module
  - Additional functionality to be added (Custom ADC configurations)
  - Needs to be integrated into SROD firmware

Word Alignment state machine

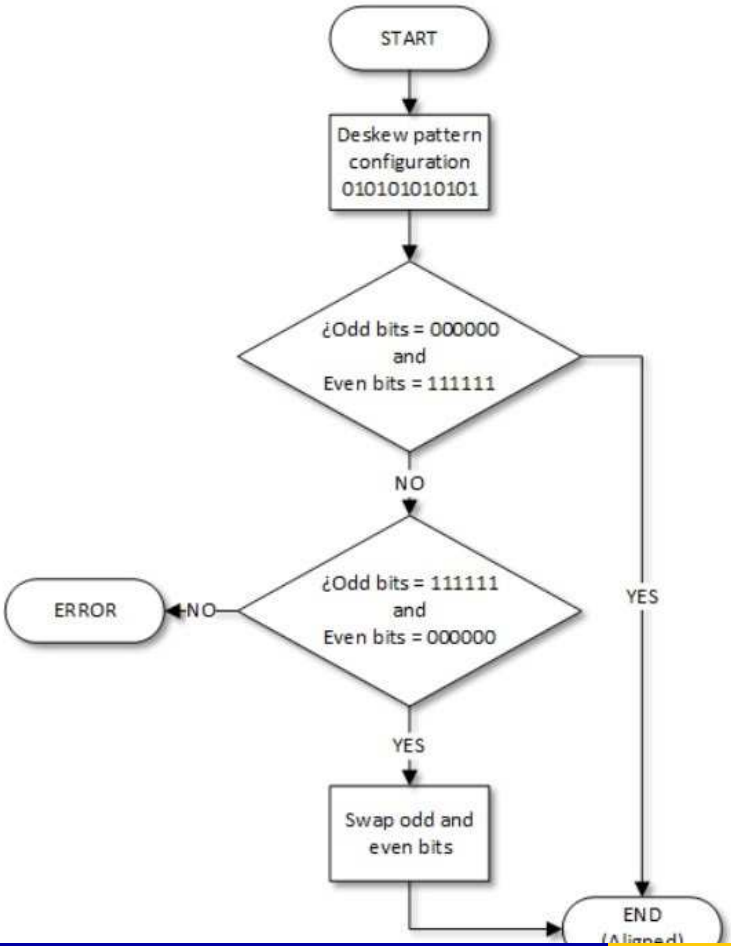
- Detect word boundaries

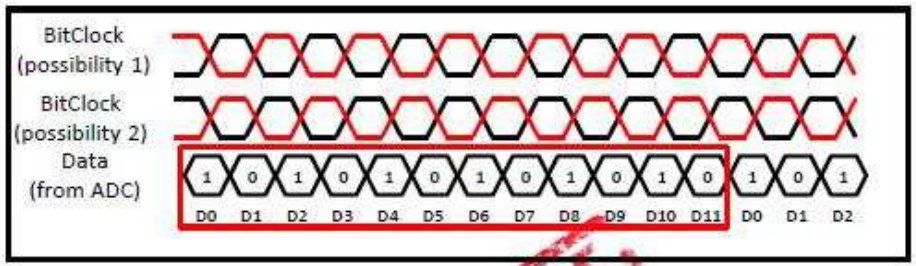


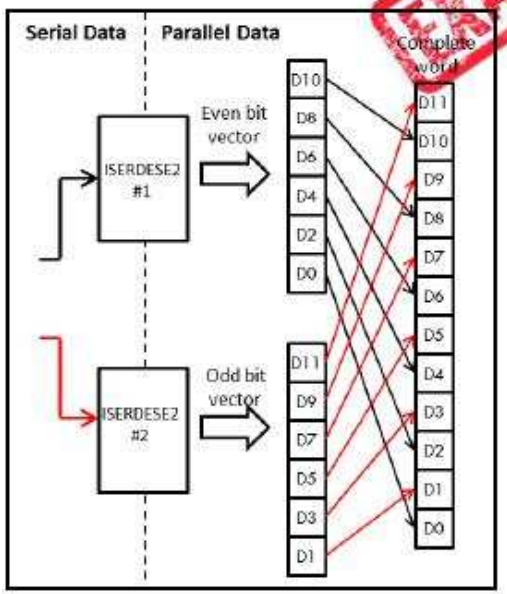


Bit Alignment state machine

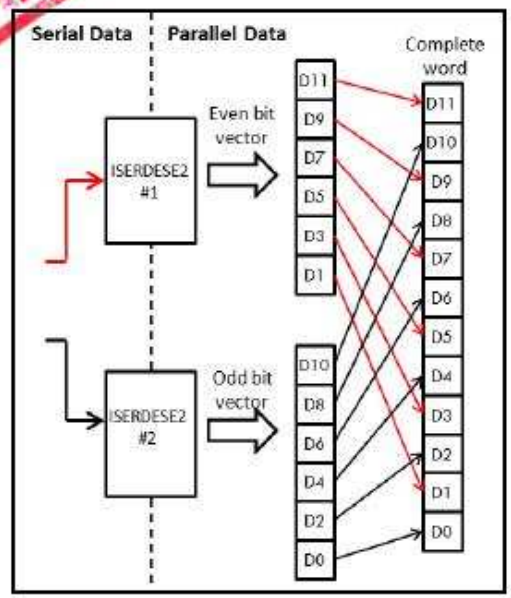
- No guarantee that positive data will be registered with rising clock edge and negative data the falling clock edge







No swap



Odd and Even bits swapped