The Run 3 and 4 Trigger Systems

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Run3 and 4 scenarios

Performance Projections up to HL-LHC:

This presentation tries to explain how we may overcome current technical limits in the (trigger system of the) LHC experiments.
Run3 challenges

• On top of many detector upgrades:
  • **ATLAS and CMS** will face event rates and pile-up levels much higher than the original design values.
    • Trigger adapts to the new environment by:
      • increasing resolution
      • increasing granularity
      • performing pile-up subtraction
      • improving muon system
      • introducing track finding
      • increasing complexity of Global Trigger selections.
    • keeping low energy thresholds, most useful to do physics with electro-weak scale particles.
  • **ALICE**, requiring a large sample of events recorded for high precision measurements of rare probes at low Pt:
    • will readout all Pb-Pb interaction at 50 kHz
  • **LHCB** need for improving statistics by increasing luminosity to \(2 \times 10^{33} \text{ cm}^{-2} \text{s}^{-1}\):
    • will improve efficiency and trigger algorithms by
      • using data from every bunch crossing
      • building a software trigger
  • Extensive electronics upgrades needed by all experiments:
    • Substantial increase in bandwidth and processing requirements.
CMS Trigger Phase I Upgrade

- CMS decision for early upgrade in 2013-2015

**Upgraded System Architecture**

- ECAL energy
- HF energy
- HCAL energy
- CSC Hits
- RPC Hits
- DT Hits
- CuOF
- HO HTR
- MPC
- Mezz
- LB
- CPPF
- TwinMux
- Micro-Global Muon Trigger
- DeMux
- Layer-1 Calo
- Layer-2 Calo

**Calorimetry**

**Global trigger**

**Muons**

The existing Level-1 trigger system of CMS. Candidate trigger objects from calorimeter systems (left) and muon detectors (right) are combined and forwarded to the Global Trigger, which calculates the trigger decision and sends out “Level-1 Accept” signals to read out the complete CMS detector at a maximum rate of 100 kHz.

The existing Level-1 Trigger can only use part of the detector information (see figure 2). Data from the three muon detector systems (Drift Tubes (DTs), Cathode Strip Chambers (CSCs) and Resistive Plate Chambers (RPCs)) and the calorimeters (the electromagnetic calorimeter (ECAL), the hadronic calorimeter (HCAL) and the forward hadronic calorimeter (HF)) are available at reduced precision for the L1 decision while information from the silicon tracker (pixels and strips) is read out only in case of a positive Level-1 decision and therefore available only at the High-Level Trigger.

Data from the calorimeters are combined in the electronics of the “Regional Calorimeter Trigger (RCT)” and the “Global Calorimeter Trigger (GCT)” and forwarded to the “Global Trigger (GT)”. Muon candidates are calculated by separate Track Finder electronics for DTs and CSCs and by a Pattern Comparator system for the RPCs. These muon candidates are merged by the “Global Muon Trigger (GMT)”, which sends the four best muon candidates to the Global Trigger. The GT calculates a maximum of 128 trigger paths (“Algorithms”), which can consist of single trigger objects or of combinations of several muon and/or calorimeter objects. Topological conditions (such as differences in the coordinates $\phi$ (azimuth) and $\eta$ (pseudorapidity)) can also be applied at this level. Algorithms can be enabled, disabled or prescaled by a constant factor and are then combined in a “Final OR”. The “Trigger Control System (TCS)” checks if all parts of the CMS detector are ready to receive a trigger signal and if there are no other reasons why the trigger decision should be suppressed, and in this case sends out an L1A signal via the “Trigger, Timing and Control (TTC)” system of CMS to all components of the detector. This triggers the readout of all detector data and the transfer to the computer farm of the High-Level Trigger.
CMS Calo Trigger for Run2 and Run3

- increased resolution of detector information entering trigger
- higher trigger tower granularity, selection on cluster shape of e/ gamma, tau objects
- event by event pile-up subtraction

- seamless coverage of detector by time-multiplexed architecture (new trigger paradigm)
- modular electronics (μTCA format) based on large FPGA and many 10 Gb/s links (up to 144 RX/TX on MP7).

Time-Multiplexed Calo Architecture

- Each card spans 8 out of 72 towers in φ and 1/3 of η.
- 18 cards, each receiving 60 links at between 5.0 Gbps & 6.6 Gbps of Calorimeter data.

Hardware Processor Platforms

- MP7 (calo Layer-2, BMTF, GMT, GT)
  - 144Tx/Rx 10Gb/s optical links
  - V7 690 FPGA
- CTP7 (calo Layer-1)
  - 67Tx, 48Rx 10Gb/s optical links, backplane IO
  - V7 690 FPGA
- MTF7 (Endcap, overlap track finders)
  - Large input IO (84 Rx 10Gb/s links)
  - Large 1GB LUT in external RAMs
- All boards in microTCA format
  - Common interface to DAQ, timing, etc
  - Modular design with optical IO for max. flexibility
  - microTCA telecoms format chosen to give access to commercial infrastructure components
CMS Muon Trigger for Run2 and Run3

- PhaseI upgrades foresee new endcap stations (CSC+RPC 4th) and CSC ME1/1 with increased granularity
- Muon trigger moves:
  - from:
    - muon candidates from sub-detectors and late merging
  - to:
    - muon tracks combining regional information from all detectors present in that region

- **better muon pT resolution** to avoid trigger rate blowup
- **better muon track-finding algorithms**, including in overlap regions
CMS trigger in Phase-I

- Many Phase-I trigger upgrade items have been already successfully deployed. Successful new developments:
  - Mass deployment of MicroTCA electronics (not likely for Run4).
  - Parallel operation of new and legacy systems.
  - Introduction of time-multiplexed architecture (possible adoption in Run4 by ATLAS).
  - Common approach on handling of large firmware projects common tool (SWATCH) to handle: architecture, simulation, test, deployment.

- Run3 will see additional muon coverage and additional Global trigger algorithms.
  - Aim for 100 kHz Level-1 trigger rate in Run2.
Similarly to CMS, ATLAS has improved its trigger in preparation for Run2, anticipating deployment of some Phase-I systems.

Improved filter, BCID-dependant pedestal subtraction

Fake muon rate reduction in $1.0 < |\eta| < 1.3$ using Tile Calorimeter

Event selection based on event topology

Fast Tracker: see next slides
FTK architecture

Phase-I Upgrade anticipated to Run2

The Fast Tracker feeds HLT with full scan tracking at 100 kHz ($p_T > 1$ GeV)

Combination of ATCA and VME cards

- 8192 ASICs (65nm)
- 1 billion patterns
- ~2000 FPGAs
- Thousands of I/O links up to 10 Gb/s

Feb 29th, 2016
A. Annovi - LHCC review
FTK HW arriving at CERN

FTK full scan tracking at 100 kHz.
Reconstruct up to $O(30M)$ track/s
2016 goal: commission barrel only system

AM06: 65nm $\sim 160mm^2$
Working at 100 MHz (nominal speed)
- Now: package more for this summer
- July: produce more AM06 for next year

FTK Input and Output cards fully produced
Now: being installed and commissioned

Core processing cards produced or in production soon
- July 2016: 12.5% processing power installed
  - Barrel only system
- April 2017: 25% processing power installed
  - Full coverage
- **2018: full system installed**
  - Full coverage & full processing power

10/32 modules already installed and operated in 2015
Phase-I upgrades foresee:
- having a powerful L1Calo using increased granularity to achieve better isolation
- keeping low energy thresholds;
- the Muon Endcap Trigger will suppress fake rate using New Small Wheel detectors;

It will be achieved with:
- an upgraded L1Trigger: a real-time, low latency path using:
  - Multi-Gbps (6.4-12.8 Gbps) optical IOs
  - Algorithms implemented in large FPGAs
  - ATCA (VME) boards hosting multiple interconnected FPGAs using Multi-Gbps links.
- Example: jFEX:
  - ATCA board, 5 FPGAs
  - 240 x 11.2 (6.4) Gbps inputs,
  - 48 x 11.2 (6.4) Gbps Outputs,
  - 120 x 11.2 (6.4) Gbps inter-FPGA connections.
The L1Calo upgrade will use improved segmentation supercell data, and implement three “Feature Extractors” (FEX’s) which will process the supercell data. The eFEX will identify electrons and photons, the jFEX will identify standard jets, do calculations of MET, HT, and the gFEX will identify large-R jets, do calculations of MET, HT. Prototypes available for gFEX, eFEX and support modules
ATLAS Phase-I Muon Trigger

Fake rate reduction in the forward region using the New Small Wheel detector

- NSW Electronics comprises
  - 4 custom ASICs: VMM, ROC, TDS, ART
  - 4 custom on-detectors boards (FEBs, ADDC, L1DDC)
- Trigger electronics on-detector (rim)
- Trigger processor in USA15
- New Sector Logic and New Muon to Central Trigger Processor Interface

New Endcap Sector Logic prototype available

Endcap muon trigger algorithm

Level1 Trigger fake fake rejection

6 optical outputs (6.4 Gbps) from NSW SFP with GTX RX in FPGA
- 6 optical outputs for other detectors SFP with GTX RX
- 2 optical outputs (6.4 Gbps) to MuCTP1 SFP with GTX TX

First version of prototype boards came in October.
LHCB Upgrade

• Upgrade philosophy (foreseen in LS2, for Run3)
  • Remove existing L0 hardware trigger
  • Readout all detector data @ 40 MHz
  • Triggering is 100% in software running in PC farm

Upgrade architecture

• Data compression on front-end driven by link cost:
  • 15000 links needed (4.8 Gb/s)
• Baseline choice for backend electronics is PCIe format.
LHCB Upgrade R&D

- Heavy use of flash-based FPGAs for on-detector readout and trigger (not all on software?) processing:
  - example below: Calorimeter
- Common readout board based on PCIe.

Calorimeter (PMTs)

- 8000 PMTs connect to ICECAL chip in 0.35 um. Final prototype OK.
- FPGAs for digital processing (FLASH): 4 for ADC data processing 1 for trigger algorithm both transmitted to PC farm

Common ‘readout’ board

- Generic FPGA-based hardware for different tasks:
  - PCIe40
  - Challenges: new & complex FPGA power & cooling
  - See talk by J-P. Cachemiche on Thursday

Different firmware flavours

- ‘TELL40’ for Data
- ‘SOL40’ for Controls
ALICE Upgrade in LS2

- High precision measurements of rare probes at low pT cannot be selected with a trigger:
  - factor 100 gain in statistics reading out all Pb-Pb interactions at 50 kHz.
  - online data reduction necessary reconstructing clusters and tracks, no filtering.

Upgrade architecture overview

Development of a Timing and Trigger Distribution system based on GBT + PON

Development of a Common Readout Unit (CRU)

Legacy systems integrated into continuous readout
CRU performs data compression:

- Example: TPC cluster finder in FPGA.
  - from 160 Gb/s to < 80 Gb/s
Run4 Challenges

• Need to target operations of CMS and ATLAS up to $7.5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ with a $\mu$ of 200 collisions per bunch crossing.

• To fully explore the EW scale trigger thresholds should remain comparable to what they are in Run2.

• Trigger and DAQ Upgrades are necessary: in addition to Detector Upgrade it is necessary to readout the largest possible subset of data at 40 MHz:
  • Higher granularity, early access to full calorimeter data
  • Tracker becomes crucial
  • Additional detectors improving Muon Trigger Pt resolution
  • Large processing power and bandwidth for data treatment in off-detector electronics.

• Different approaches chosen by CMS and ATLAS.
CMS in Phase II

• On top of new Tracker, Calorimeter (improved S/N and time resolution) and High Granularity Endcap Calorimeters, new forward Muon detectors up to eta 3-6:
  • Track information will be used in the trigger (self-seeding):
    • Tracker FE identifies high transverse momentum stubs.
    • Latency 12.5 µs, 750 kHz rate, HLT output 7.5 kHz

pT>2 GeV @ 40 MHz

Trigger/DAQ Architecture

• L1-Trigger
  • 12.5 s latency, 750 kHz accept rate at 200 PU (see next slide)

• Trigger timing, throttling and control
  • High bandwidth bi-directional link allowing trigger information to steer readout

• DAQ
  • Similar event builder, HLT & storage as present
  • Increase bandwidth - 800 links x 100 Gbps to provide 30 Tbps throughput at 30% occupancy

• HLT
  • Processing power scales as PU x L1 rate ≈ 52 wrt Run 2 at 200 pileup - need to develop improved software using new computing technics beyond gain at constant resources
  • HLT rejection 1/100 (as current system)

F. Meijer's presentation
Global trigger correlates L1Tracks with (ele, mu, …) objects identified by L1Calo and L1Muon who combine information from all detectors.

- Muons improve pT resolution
- Electrons match L1Track with e/g candidate: ID
- Tracker-based isolation improves for electrons and muons
- Taus identification improves with track+calo
- Multi object trigger improves by requiring objects from same vertex.
CMS R&D for Phase II

- Formidable technical challenges from L1 track finding:
  - Data rates > 50-100 Tb/s
  - Occupancy and combinatorics: O(10^4 hits/BC) at μ = 200
  - Latency 4+1 μs for tracking

- Three R&D projects ongoing

• Goal: demo 1 geometric/time slice of the full system
  - Target resolution: 6 mrad φ, 0.0012 q/pT
  - Mock-up future, larger FPGAs w/ >1 daisy-chained boards

• TMT / Hough: Demonstrator
  - Demo uses Imperial MP7 (μTCA)
    - Virtex 7 690T, 0.94 Tbps FP I/O
    - 6x12 channel miniPOD, 11.3 Gbps / link
  - Expertise from CMS Phase-1 Calo trigger system presently a single track finding board and a data source
    - Running both pipelined and systolic HT firmware implementations

• Using Wisconsin CTP7 (μTCA) boards for the demonstration
  - Used in the CMS Phase-1 Calo trigger
  - Virtex-7 690 FPGA
  - Zynq SoC with dual Cortex-A9 ARM
  - GTH: 80 RX & 61 TX
  - 3 CTP7 boards are used as sector boards, 1 CTP7 handles sending input stubs and receiving output tracks
  - AMC13 card is used for central clock distribution

• Tracklet Hardware
  - Tracklet demonstrator @ CERN

• Split detector into trigger "towers", nominally 48 (6 η x 8φ)
  - 3 types of towers (barrel, endcap, hybrid)

• The AM + FPGA Approach
  - Utilize modern, high-speed ATCA backplane
    - Nominally 1 shelf per tower, 1 mezzanine per BX

= ATCA shelf

PRB(oard)

PRM(ezzanine)

AM

Tracklet demonstrator @ CERN

CTP7
Split L0/L1 architecture. L0 latency similar to current L1 system.

- L0 based on Phase-I L1Calo and new L0Muon Trigger
- L1 latency longer (60 $\mu$s) uses L1Track AM-based track finder (2-4 GeV PT), driven by L0 Regions of Interest
- L1Global trigger based on L1Track and full-calorimeter data and L0Muon

Option for transmitting all data off-detector at L0 rate of 1 MHz. Need for bandwidth and Event Storage.

Need factor 100 of rate reduction in Event Filter.
ATLAS in Phase II

- **L0Muon** uses information from precision muon chambers (MDT)
- **L0Calo** will use new digital signals from Tile and New Forward calorimetry.
- **L1Track** trigger receives ITk data from regions pointed by ROIs defined by L0 and finds tracks above 4 GeV.
  - Factor 5 reduction for MU20 and EM18 with >95% efficiency
  - Track Z0 resolution better than 10mm
  - Needs regional readout and pattern recognition to fit within 15µs (L0/L1 scheme)
  - Processing by next generation Associative Memory + FPGA.
ATLAS in Phase II

- L1Global processes full granularity calorimeter, L1Tracks and L0Muon information.
  - Time multiplexed architecture.
- Event Filter input rate increases to 400 kHz (1MHz in single-level architecture)
  - hardware-based full event tracking (FTK++)
    - multi-threading, seamless integration of offline algorithms
- General Purpose Graphical Processors (GPGPU) of FPGA.
- In single-level architecture accelerated regional track processing

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ATLAS Phase II trigger upgrade

Overview

40 Event Processor time-multiplexed system, better than 0.1% dead time at 1 MHz

Receives
- calorimeter information from every cell
- L0Muon objects
- Level-1 tracks

Input up to 8 events in parallel each taking 2 \( \mu \)s to arrive

Linear processing of calorimeter data on arrival

Iterative processing for calorimeter jets and \( \gamma > 6 \) \( \gamma \)

RoI processing for e, \( \gamma \), \( \tau \)

Global and topological selections
- tracks vital for taus and pileup suppression
Summary

• Not a simple job to give justice to such an enormous effort like designing, building and operating LHC trigger systems in 23 slides.

• Keywords appearing in Run3 systems: new trigger architectures like Time Multiplexing, Topological Triggers, modular electronics μTCA, ATCA, based on Large FPGAs, hosting O(100) links running at 4.8-12.4 Gb/s. Readout boards based on PCIe. First deployment of online data reduction (and calibration). Timing and trigger distribution based on PON+GBT.

• Status: already deployed (CMS) or at full-functional prototype stage (others)

• Keywords for Run4 are: self-seeded (CMS) or seeded (ATLAS) tracker systems, full event readout at 400-750 KHz-1MHz. HLT need for large input bandwidth and very performant storage handler. HLT profiting from hardware-based processing, AMs, FPGAs and GPGPUs.

• Many ongoing R&D projects ongoing.
Backup
Single hardware level architecture

Event Filter now delivers a factor 100 reduction down to output rate of 10 kHz

Naively a factor 2.5 larger than in two level system, at least 10 times larger than Phase I

EF Track regional tracking processor alongside FTK++ full event tracking

Data to DAQ/Event Filter

Data Input to Trigger

Trigger Signals: L0

Trigger Data to Readout

Output 10 KHz