The Run 3 and 4 Trigger Systems

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many thanks to contributors from ACES 2016 Workshop
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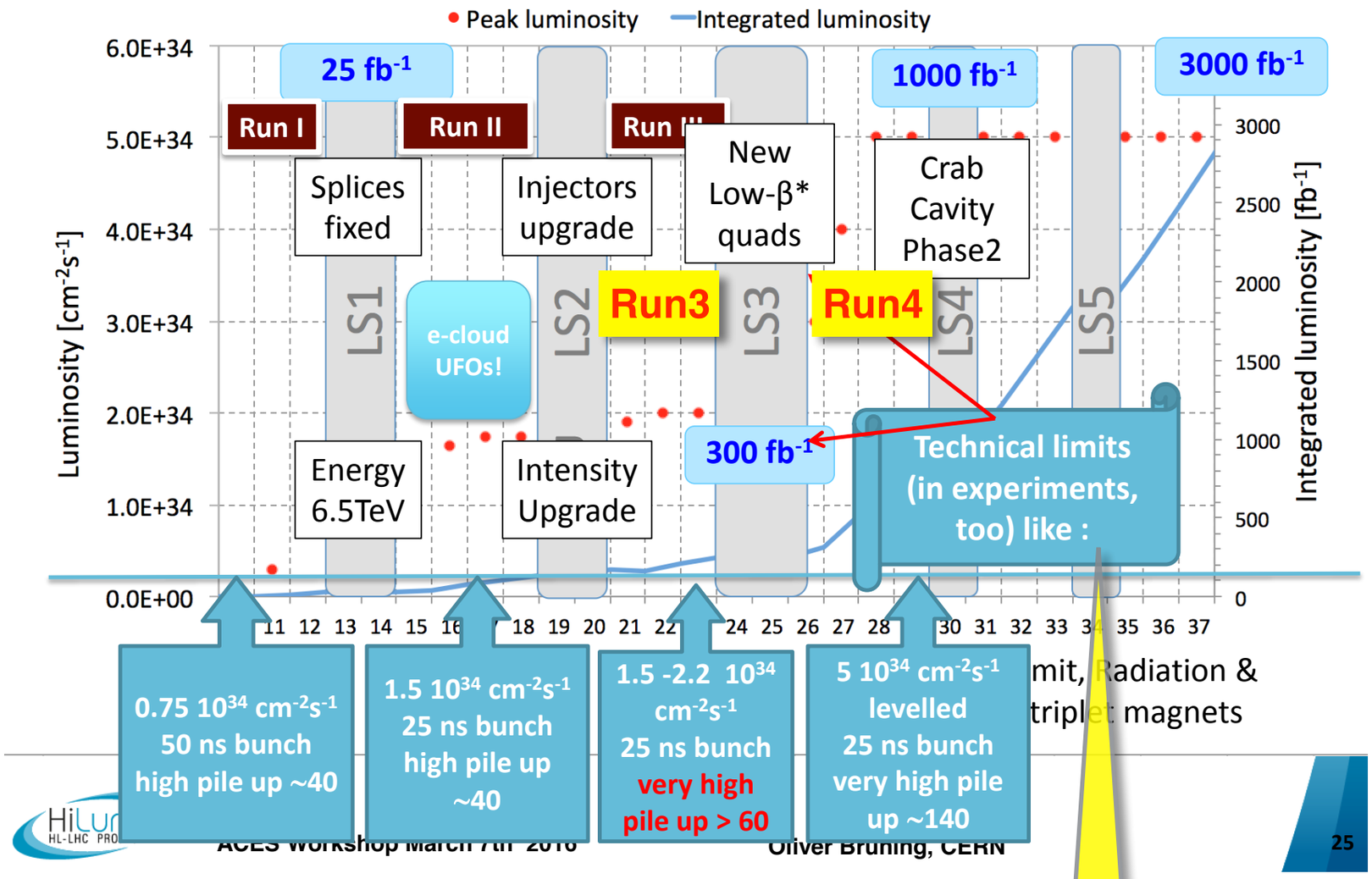
Run3 and 4 scenarios

Performance Projections up to HL-LHC:



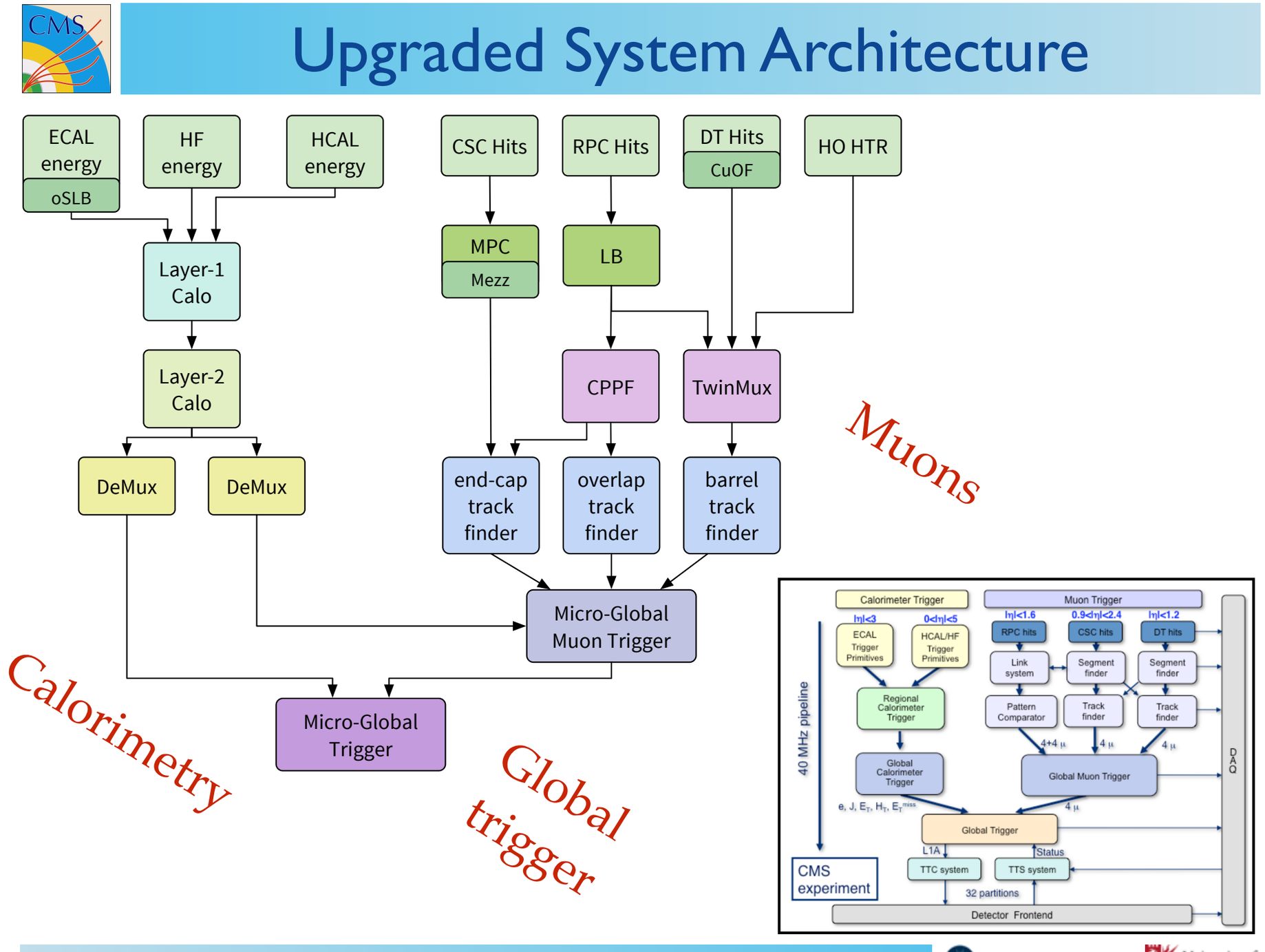
This presentation tries to explain how we may overcome current technical limits in the (trigger system of the) LHC experiments.

Run3 challenges

- On top of many detector upgrades:
- **ATLAS and CMS** will face event rates and pile-up levels much higher that the original design values.
  - **Trigger adapts to the new environment by:**
    - **increasing resolution**
    - **increasing granularity**
    - **performing pile-up subtraction**
    - **improving muon system**
    - **introducing track finding**
    - **increasing complexity of Global Trigger selections.**
      - **keeping low energy thresholds, most useful to do physics with electro-weak scale particles**.
- **ALICE**, requiring a large sample of events recorded for high precision measurements of rare probes at low Pt:
  - **will readout all Pb-Pb interaction at 50 kHz**
- **LHCB** need for improving statistics by increasing luminosity to 2×10^{33} $cm^{-2} s^{-1}$:
  - **will improve efficiency and trigger algorithms by**
    - **using data from every bunch crossing**
    - **building a software trigger**
- Extensive electronics upgrades needed by all experiments:
  - Substantial increase in bandwidth and processing requirements.

CMS Trigger PhaseI Upgrade

- **CMS decision for early upgrade in 2013-2015**

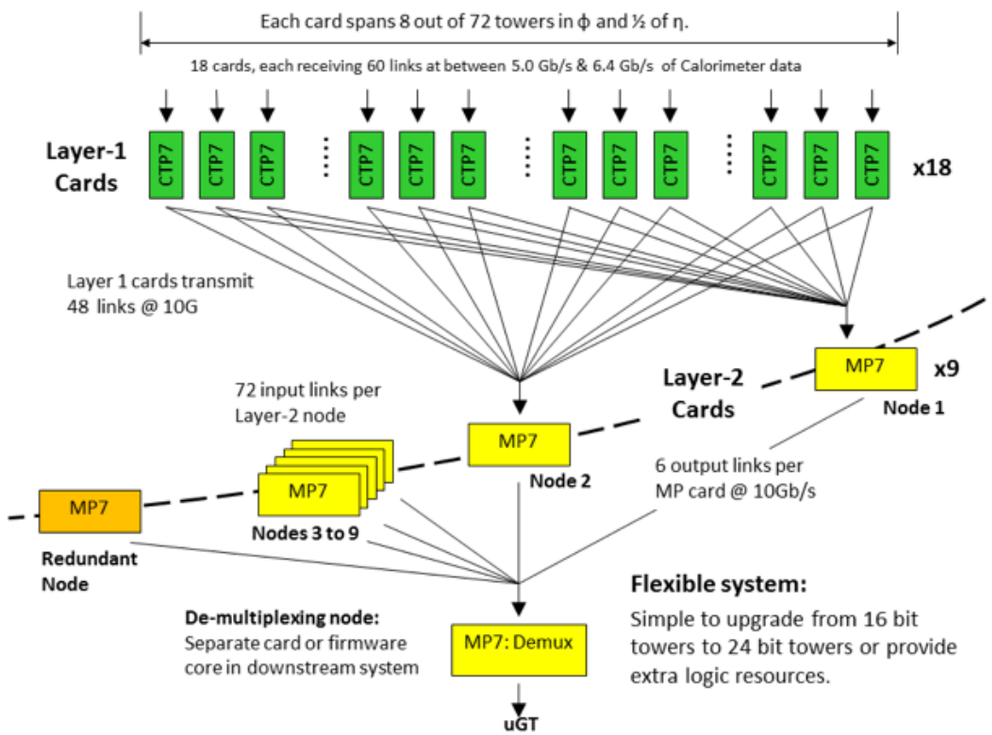


CMS Calo Trigger for Run2 and Run3

- increased resolution of detector information entering trigger
- higher trigger tower granularity, selection on cluster shape of e/gamma, tau objects
- event by event pile-up subtraction

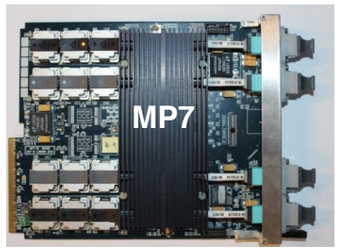
- **seamless coverage of detector by time-multiplexed architecture (new trigger paradigm)**
- **modular electronics (*μ*TCA format) based on large FPGA and many 10 Gb/s links (up to 144 RX/TX on MP7).**

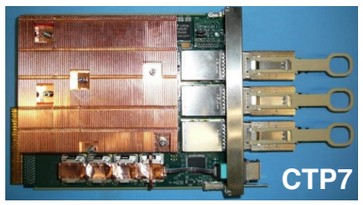
Time-Multiplexed Calo Architecture

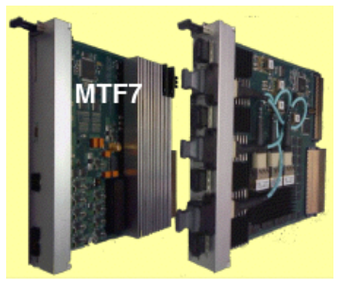


Hardware Processor Platforms

- MP7 (calo Layer-2, BMTF, GMT, GT)
  - 144Tx/Rx 10Gb/s optical links
  - V7 690 FPGA
- CTP7 (calo Layer-1)
  - 67Tx, 48Rx 10Gb/s optical links, backplane IO
  - V7 690 FGPA
- MTF7 (Endcap, overlap track finders)
  - Large input IO (84 Rx 10Gb/s links)
  - Large 1GB LUT in external RAMs
- All boards in microTCA format
  - Common interface to DAQ, timing, etc
  - Modular design with optical IO for max. flexibility
  - microTCA telecoms format chosen to give access to commercial infrastructure components

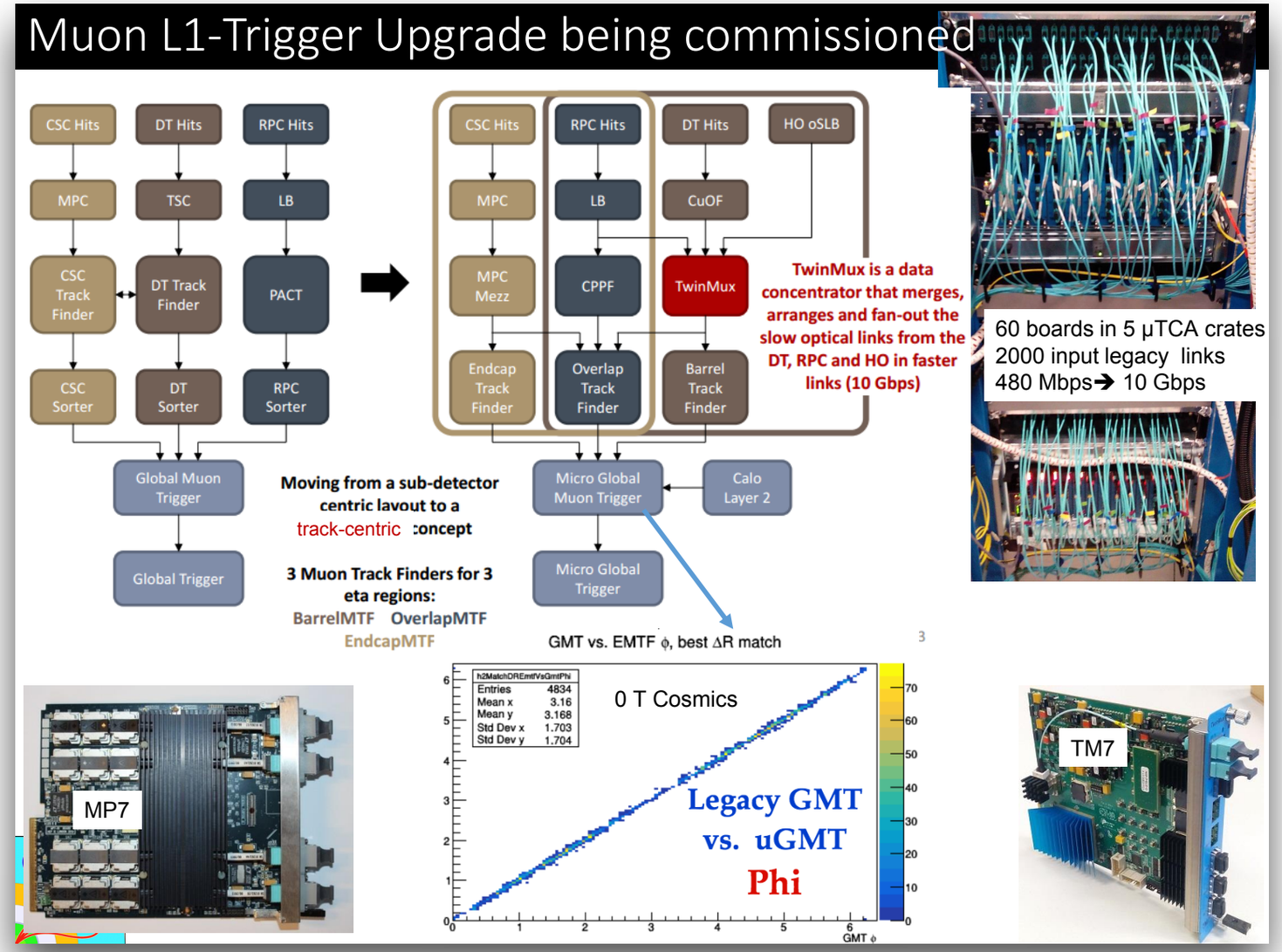






CMS Muon Trigger for Run2 and Run3

- Phase1 upgrades foresee new endcap stations (CSC+RPC 4th) and CSC ME1/1 with increased granularity
- Muon trigger moves:
  - **from:**
    - **muon candidates from sub-detectors and late merging**
  - **to:**
    - **muon tracks combining regional information from all detectors present in that region**



- **better muon pT resolution** to avoid trigger rate blowup
- **better muon track-finding algorithms**, including in overlap regions

CMS trigger in Phase-I

- **many Phase-I trigger upgrade items have been already successfuly deployed. Successful new developments:**
  - mass deployment of MicroTCA electronics (not likely for Run4).
  - parallel operation of new and legacy systems.
  - introduction of time-multiplexed architecture (possible adoption in Run4 by ATLAS).
  - Common approach on handling of large firmware projects common tool (SWATCH) to handle: architecture, simulation, test, deployment.
- **Run3 will see additional muon coverage and additional Global trigger algorithms.**
  - Aim for 100 kHz Level-1 trigger rate in Run2.

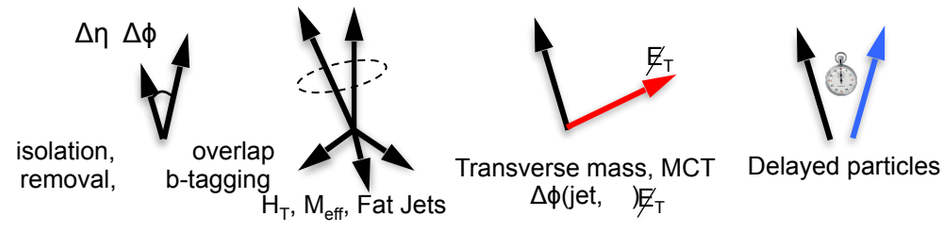
ATLAS Trigger and DAQ in Run2

- **Similarly to CMS, ATLAS has improved its trigger in preparation for Run2, anticipating deployment of some Phase-I systems**

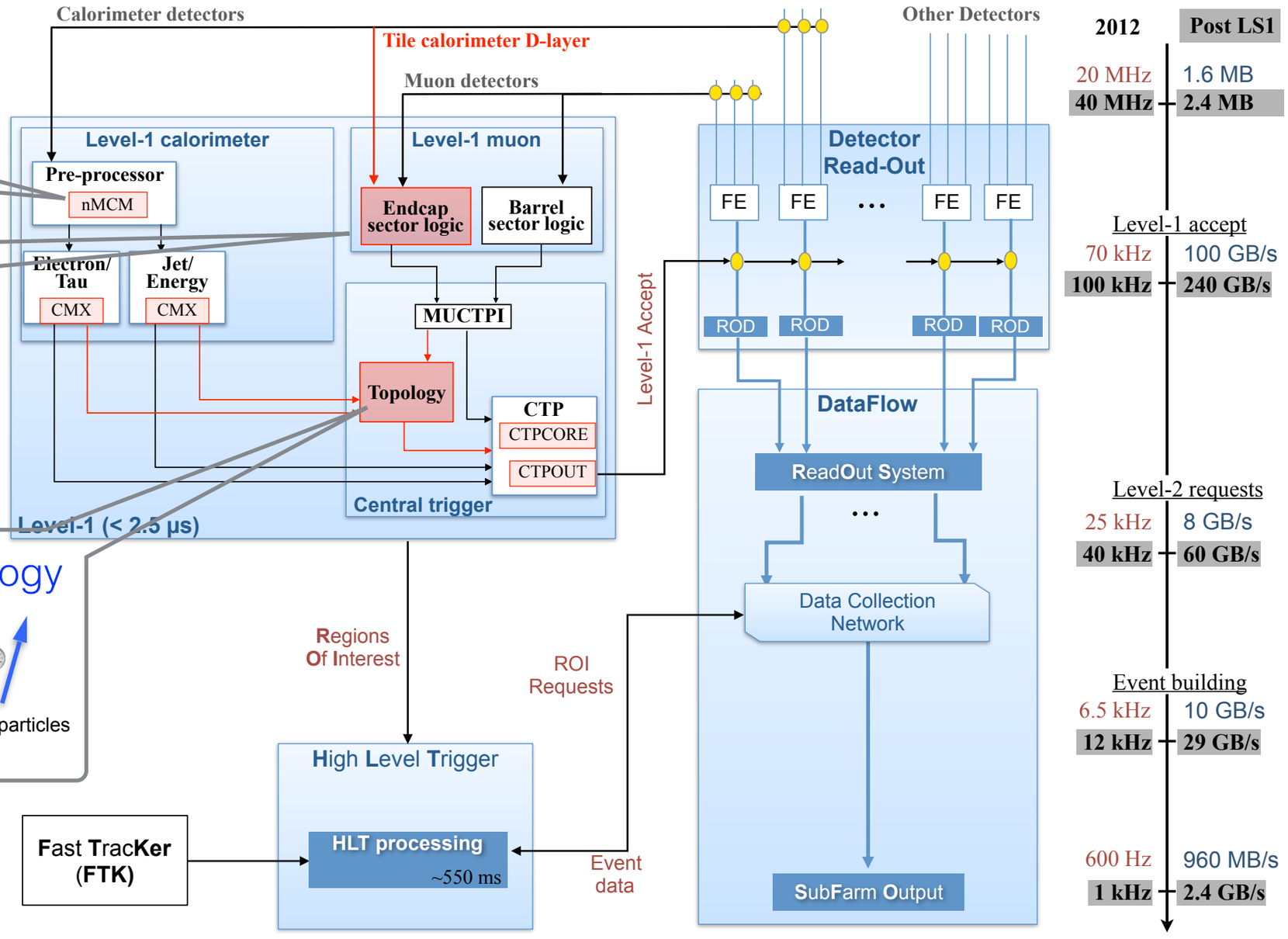
Improved filter, BCID-dependant pedestal subtraction

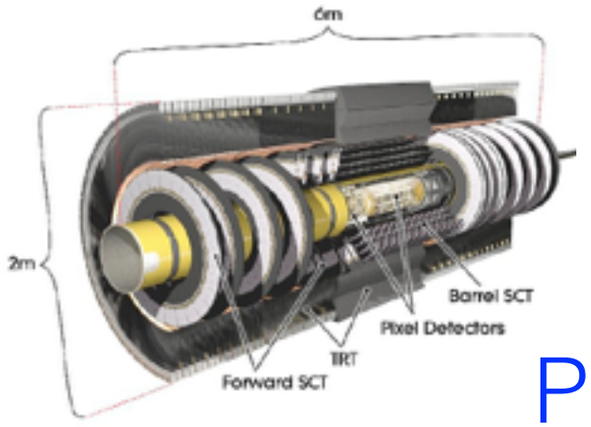
Fake muon rate reduction in 1.0 < |eta| < 1.3 using Tile Calorimeter

Event selection based on event topology



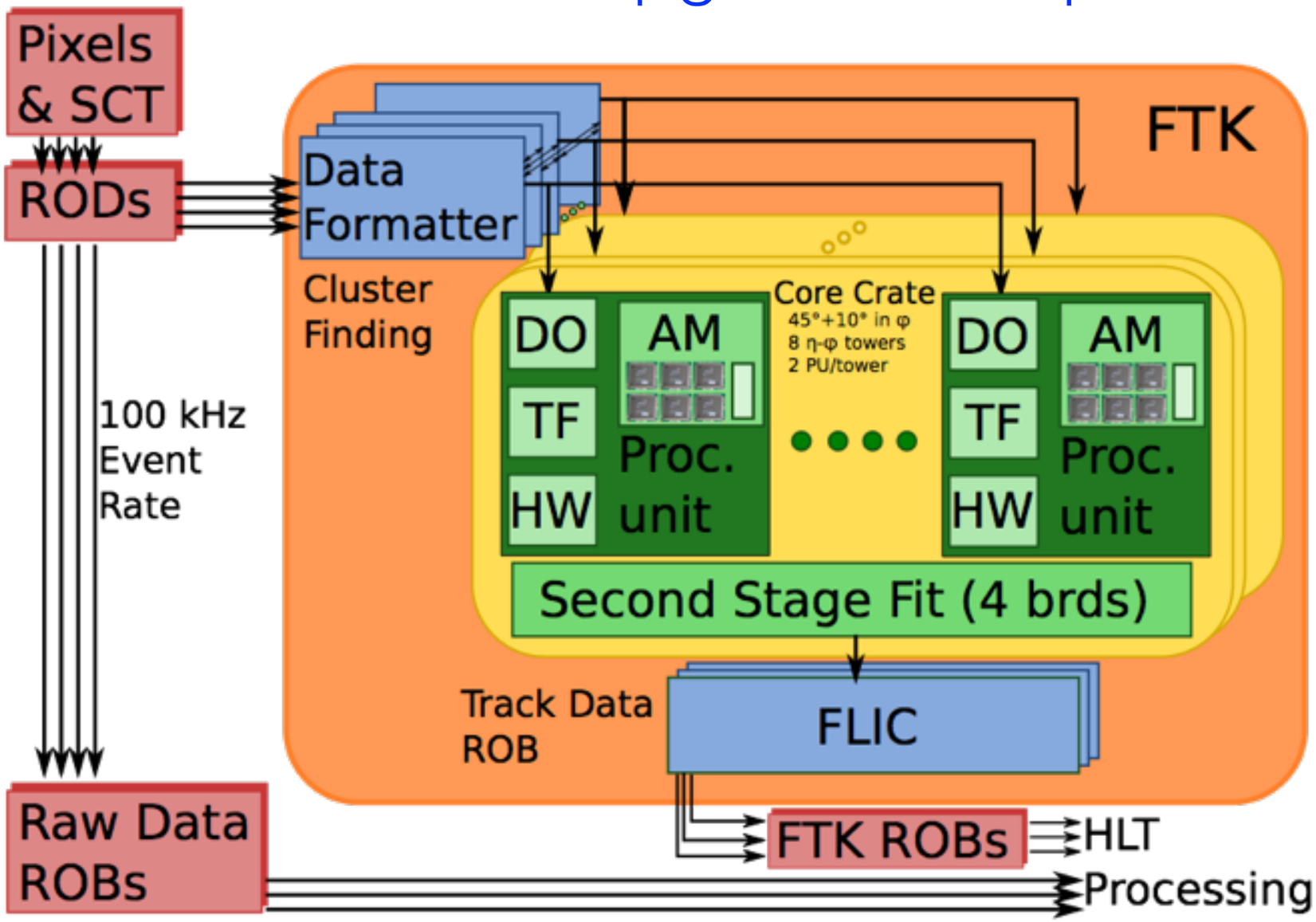
Fast Tracker: see next slides





FTK architecture

Phase-I Upgrade anticipated to Run2



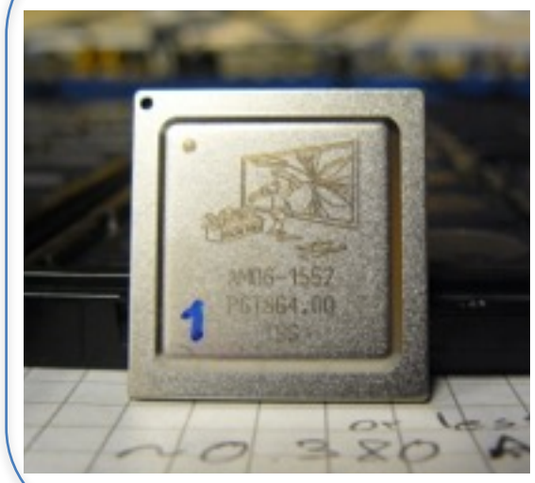
The Fast Tracker feeds HLT with **full scan tracking at 100 kHz (p_T > 1 GeV)**

Combination of ATCA and VME cards

- 8192 ASICs (65nm)
  - 1 billion patterns
  - ~2000 FPGAs
  - Thousands of I/O links up to 10 Gb/s

FTK HW arriving at CERN

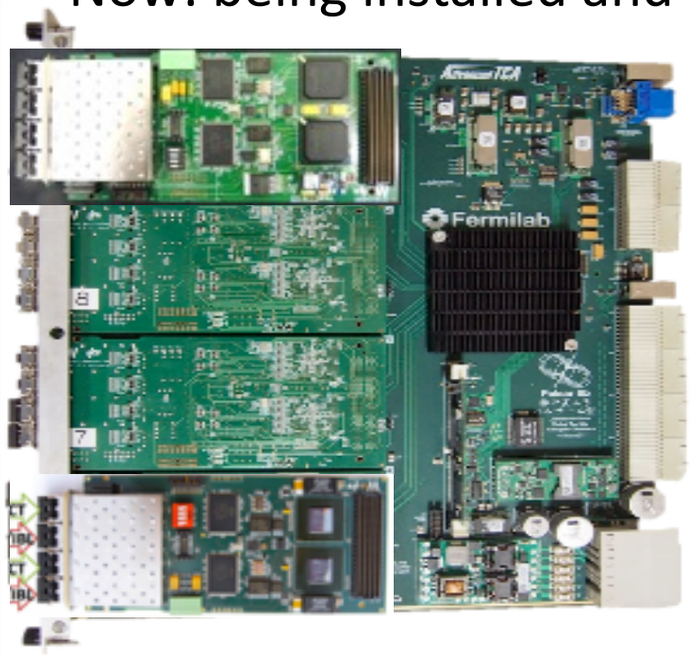
FTK full scan tracking at 100 kHz.
Reconstruct up to O(30M) track/s
2016 goal: commission barrel only system

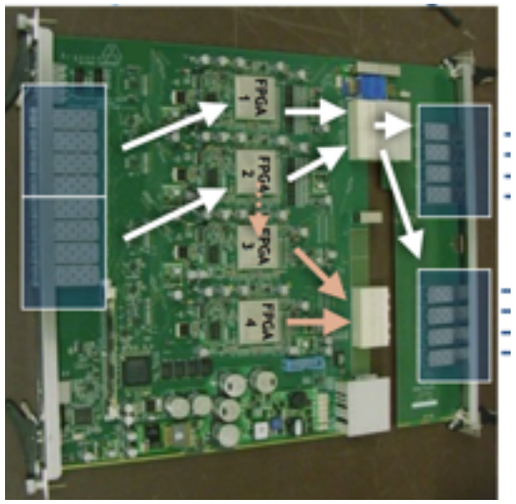


AM06: 65nm ~160mm^2
Working at 100 MHz
(nominal speed)

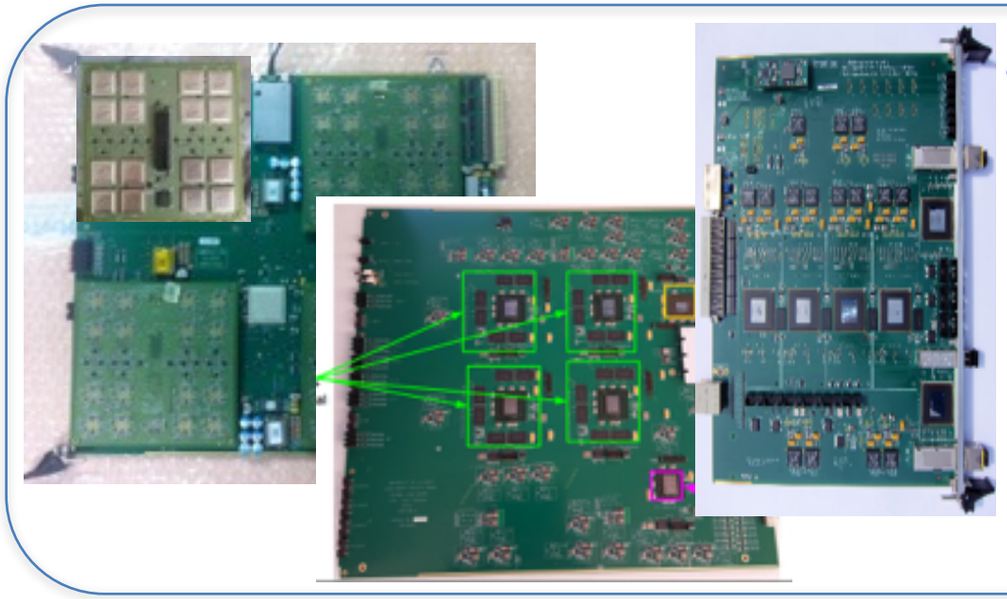
- Now: package more for this summer
- July: produce more AM06 for next year

FTK Input and Output cards fully produced
Now: being installed and commissioned





10/32 modules already
installed and operated in 2015



- Core processing cards produced or in production soon
  - July 2016: 12.5% processing power installed
    - Barrel only system
  - April 2017: 25% processing power installed
    - Full coverage
  - **2018: full system installed**
    - Full coverage & full processing power

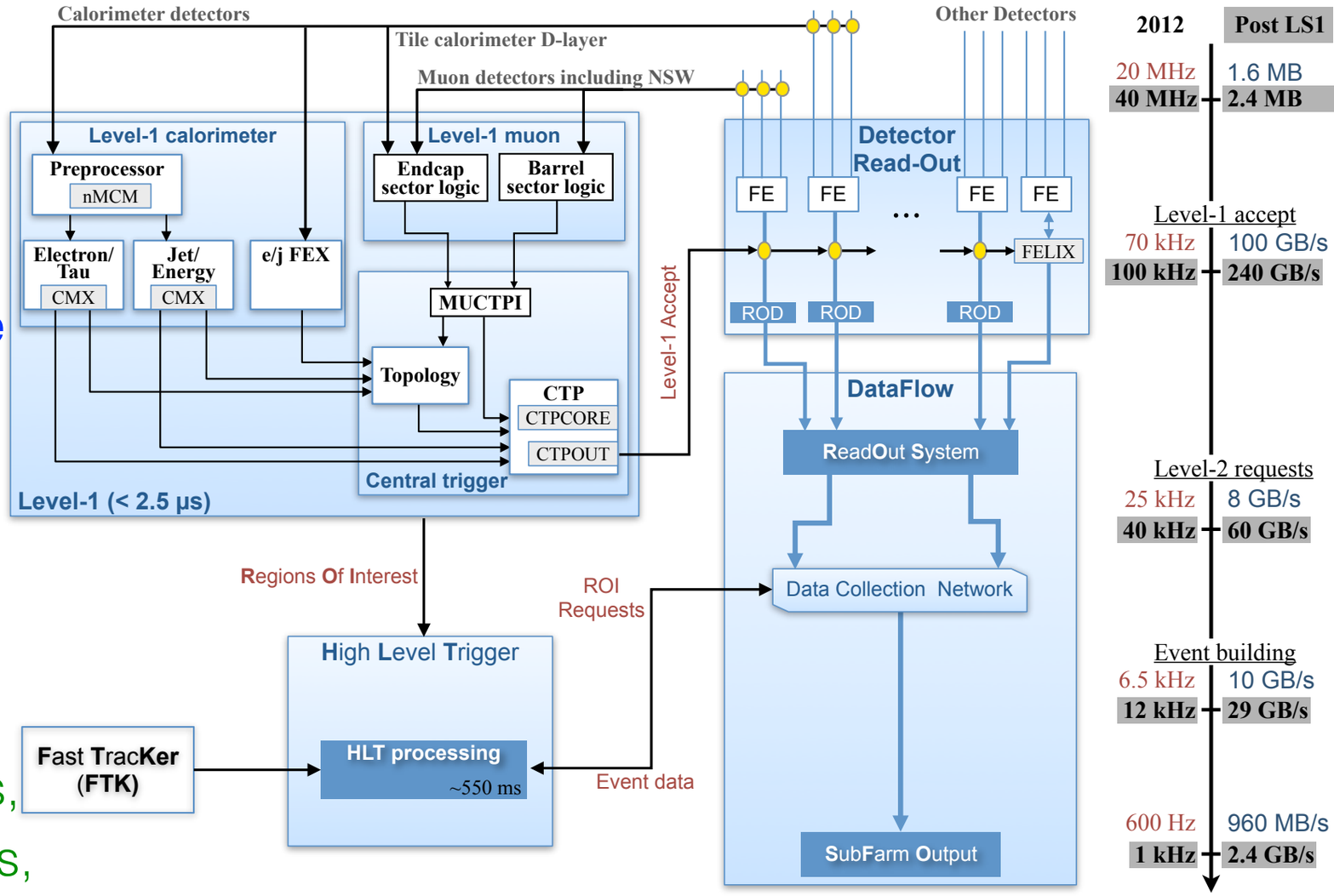
ATLAS Trigger and DAQ after Phase-I upgrade

Phase-I upgrades foresee:

- having a powerful L1Calo using increased granularity to achieve better isolation
- keeping low energy thresholds;
- the Muon Endcap Trigger will suppress fake rate using New Small Wheel detectors;

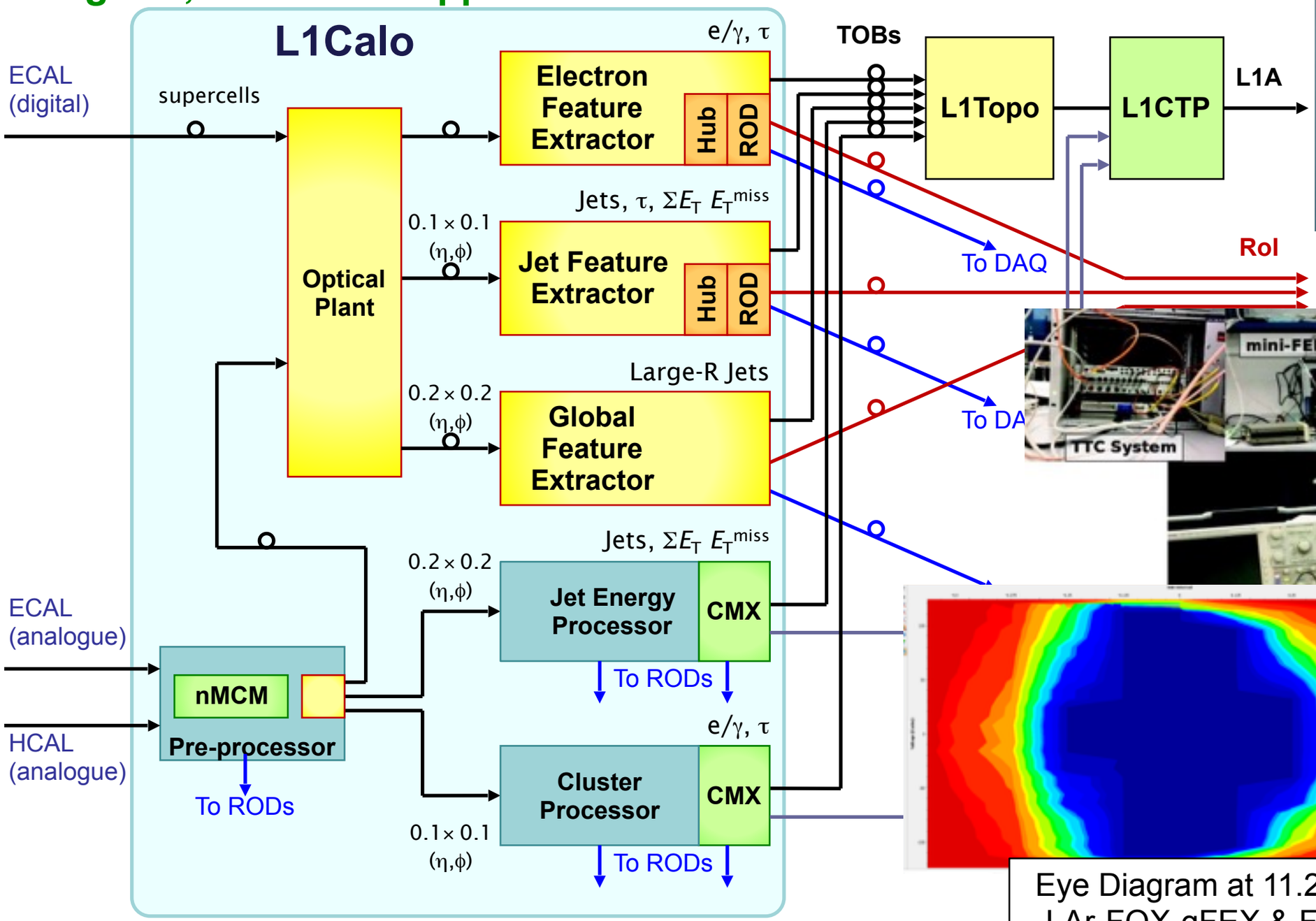
It will be achieved with:

- an upgraded L1Trigger: a real-time, low latency path using:
  - Multi-Gbps (6.4-12.8 Gbps) optical IOs
  - Algorithms implemented in large FPGAs
- ATCA (VME) boards hosting multiple interconnected FPGAs using Multi-Gbps links.
- Example: jFEX:
  - ATCA board, 5 FPGAs
  - 240 x 11.2 (6.4) Gbps inputs,
  - 48 x 11.2 (6.4) Gbps Outputs,
  - 120 x 11.2 (6.4) Gbps inter-FPGA connections.

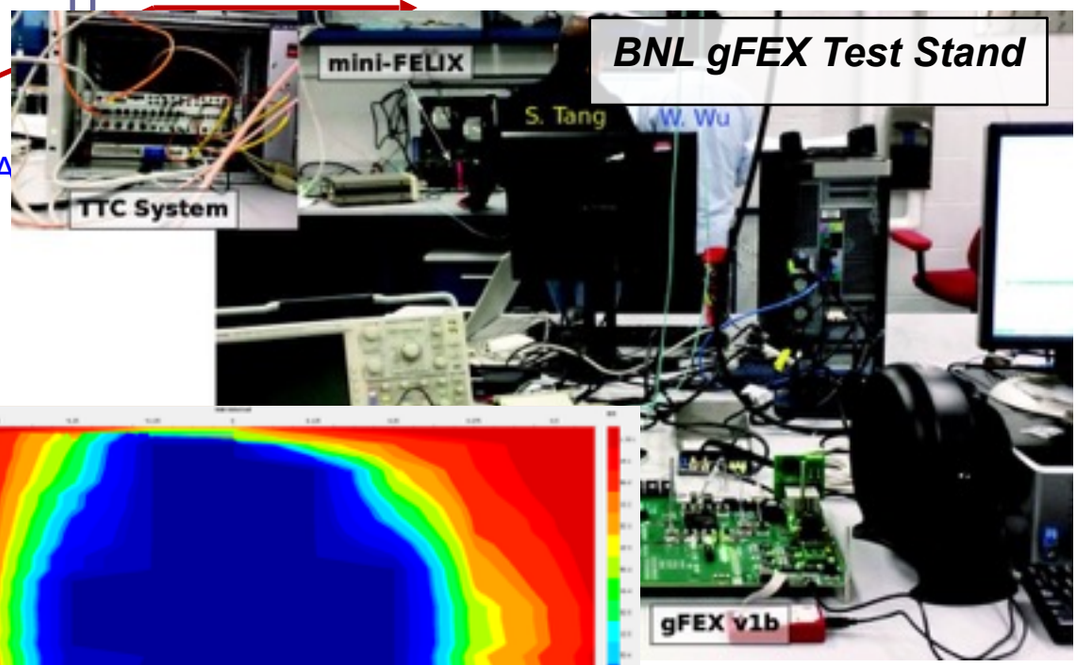


L1Calo Phase-I Upgrade

The L1Calo upgrade will use **improved segmentation supercell data**, and **implement three "Feature Extractors" (FEX's)** which will process the supercell data. The eFEX will identify electrons and photons, the jFEX will identify standard jets, do calculations of MET, HT, and the gFEX will identify large-R jets, do calculations of MET, HT. **Prototypes availablee for gFEX, eFEX and support modules**



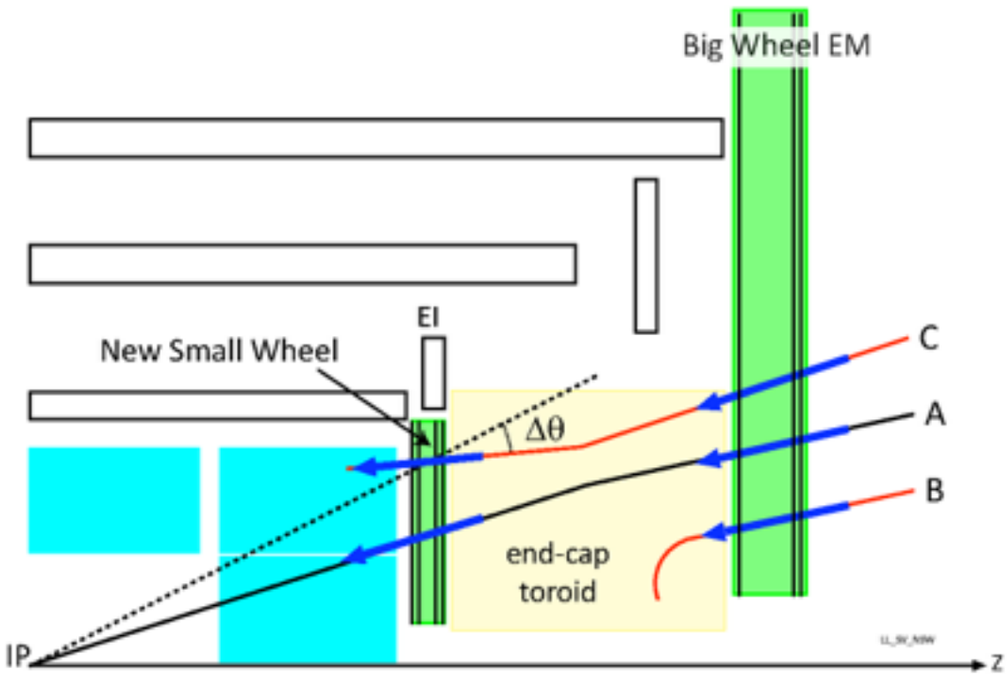
eFEX Prototype



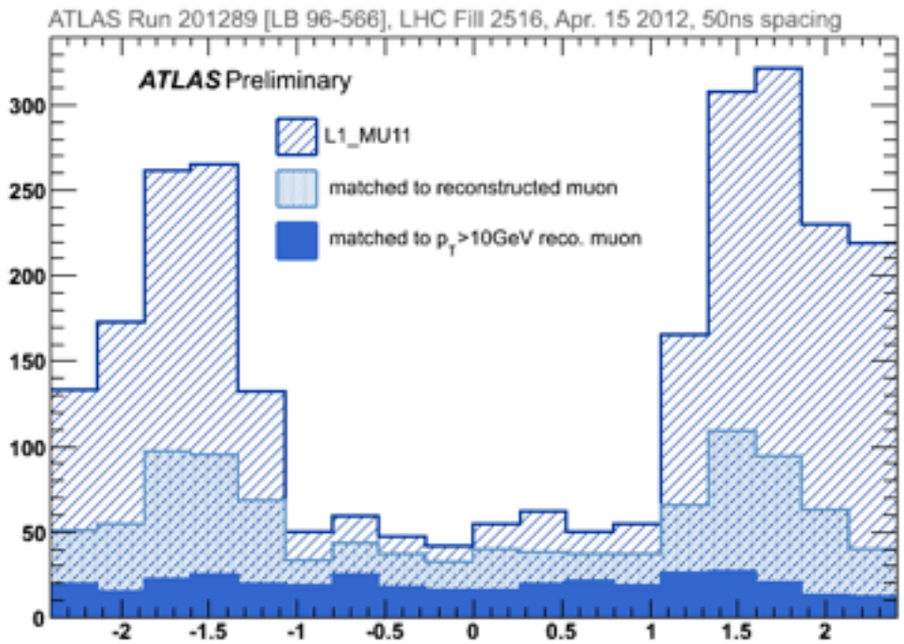
Eye Diagram at 11.2 Gb/s
LAr-FOX-gFEX & FELIX

ATLAS Phase-I Muon Trigger

Endcap muon trigger algorithm



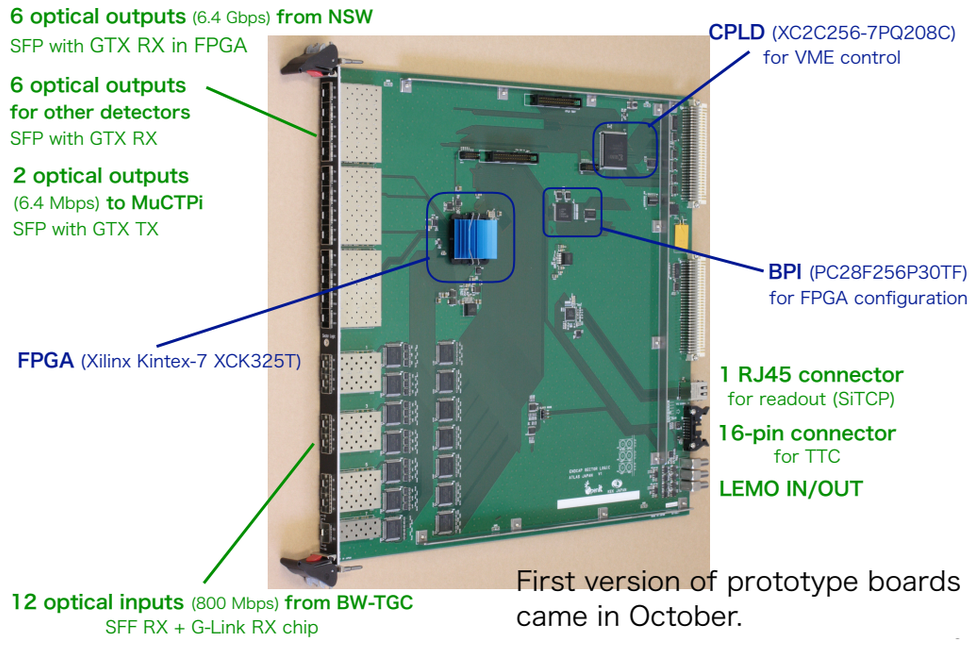
Level1 Trigger fake rejection



Fake rate reduction in the forward region using the New Small Wheel detector

- NSW Electronics comprises
  - 4 custom ASICs: VMM, ROC, TDS, ART
  - 4 custom on-detectors boards (FEBs, ADDC, L1DDC)
  - Trigger electronics on-detector (rim)
  - Trigger processor in USA15
- New Sector Logic and New Muon to Central Trigger Processor Interface

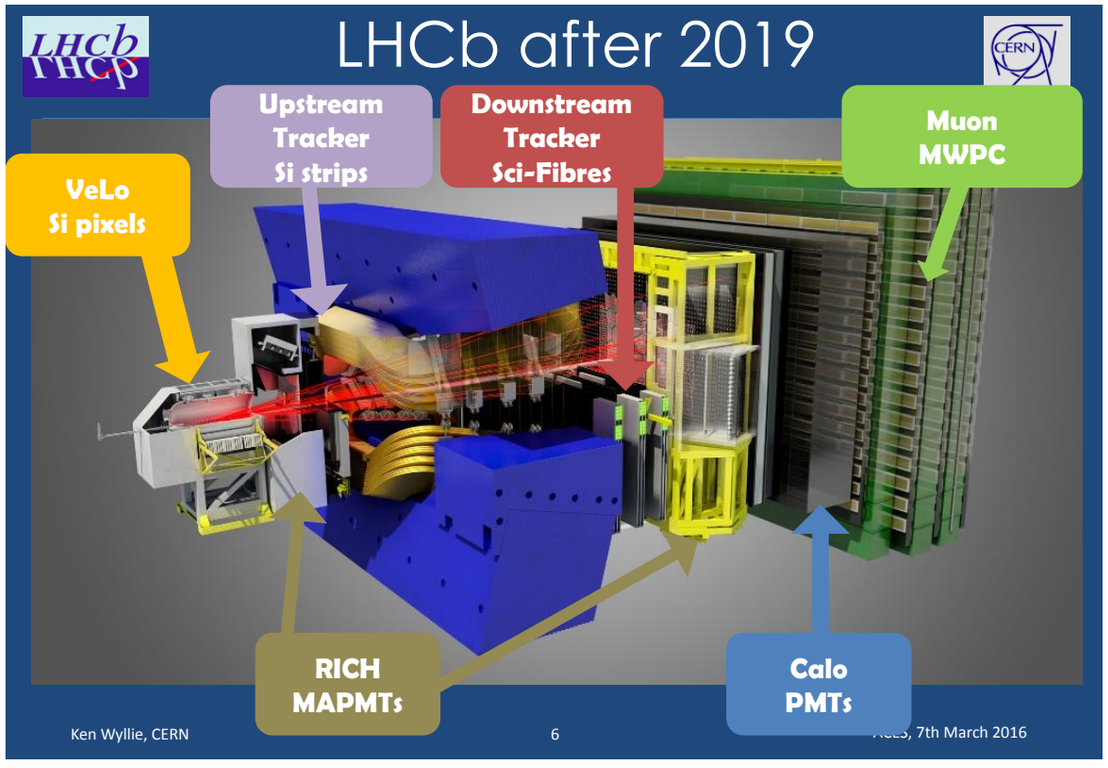
New Endcap Sector Logic prototype available

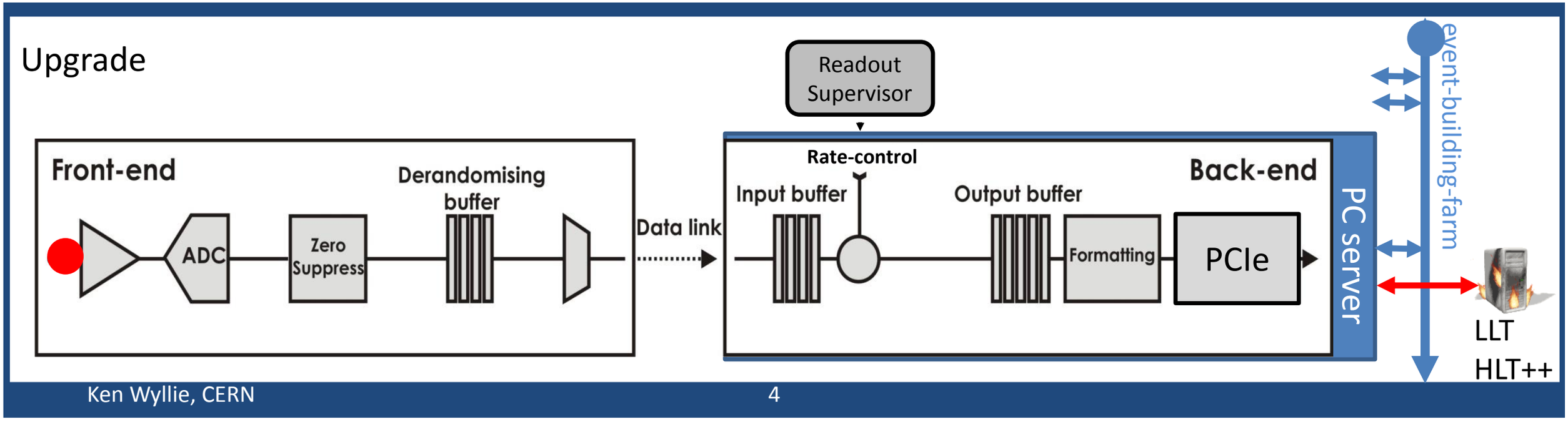


First version of prototype boards came in October.

LHCB Upgrade

- Upgrade philosophy (foreseen in LS2, for Run3)
  - **Remove existing L0 hardware trigger**
  - **Readout all detector data @ 40 MHz**
  - **Triggering is 100% in software running in PC farm**

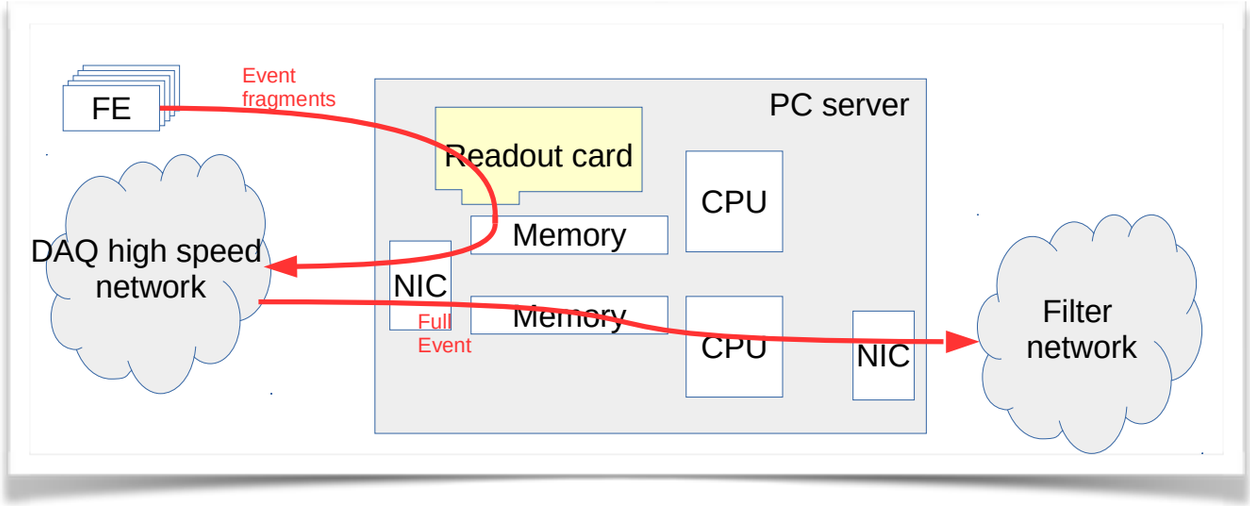




- **Data compression on front-end driven by link cost:**
  - 15000 links needed (4.8 Gb/s)
- **Baseline choice for backend electronics is PCIe format.**

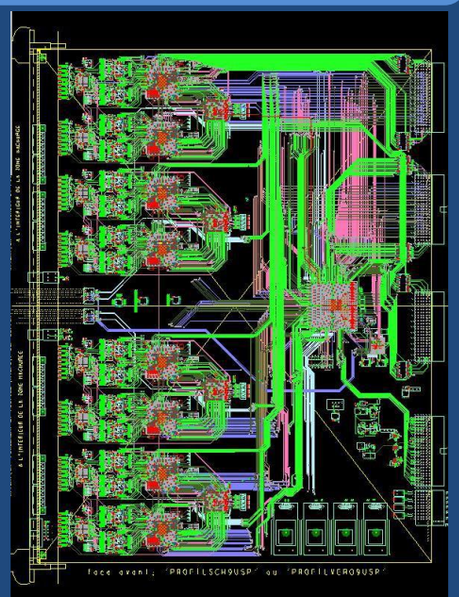
LHCB Upgrade R&D

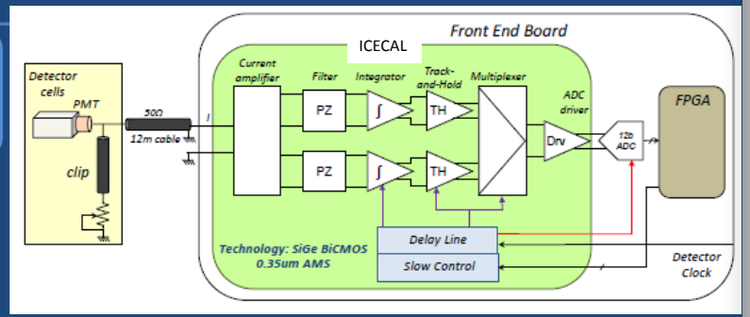
- Heavy use of flash-based FPGAs for on-detector readout and trigger (not all on software ?) processing:
  - example below: Calorimeter
- **Common readout board based on PCIe.**



Calorimeter (PMTs)

8000 PMTs connect to ICECAL chip in 0.35 um.
Final prototype OK.





FPGAs for digital processing (FLASH):
4 for ADC data processing
1 for trigger algorithm
both transmitted to PC farm

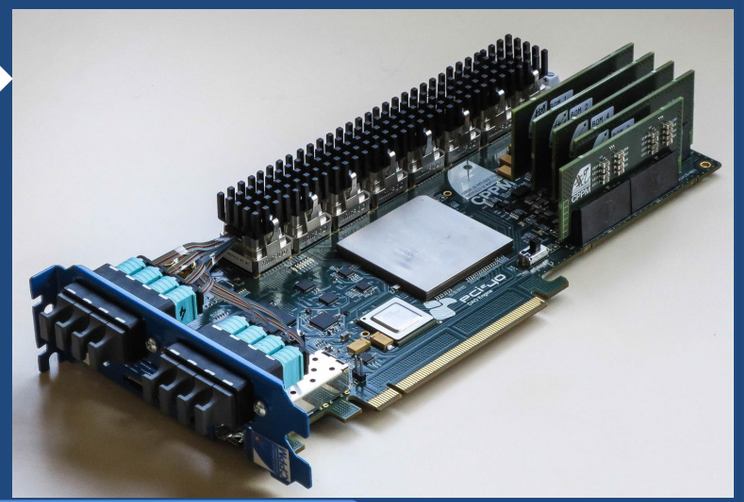
Common 'readout' board

Generic FPGA-based hardware for different tasks:

PCIe40

Challenges:
new & complex FPGA
power & cooling

See talk by J-P. Cachemiche on Thursday



Different firmware flavours

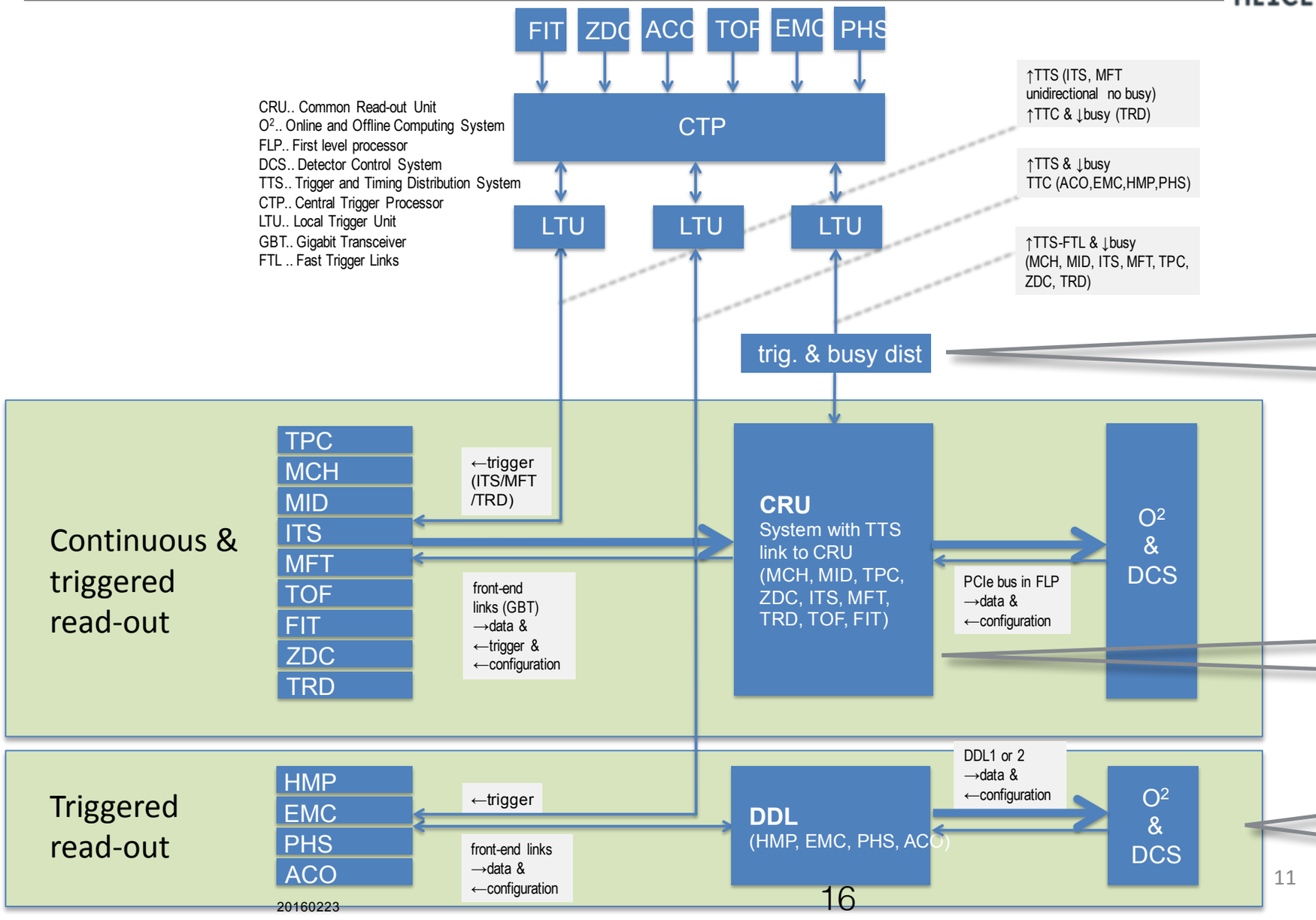
'TELL40' for Data

'SOL40' for Controls

ALICE Upgrade in LS2

- High precision measurements of rare probes at low pT cannot be selected with a trigger:
  - **factor 100 gain in statistics reading out all Pb-Pb interactions at 50 kHz.**
  - **online data reduction necessary reconstructing clusters and tracks, no filtering.**

Upgrade architecture overview



Development of a Timing and Trigger Distribution system based on GBT + PON

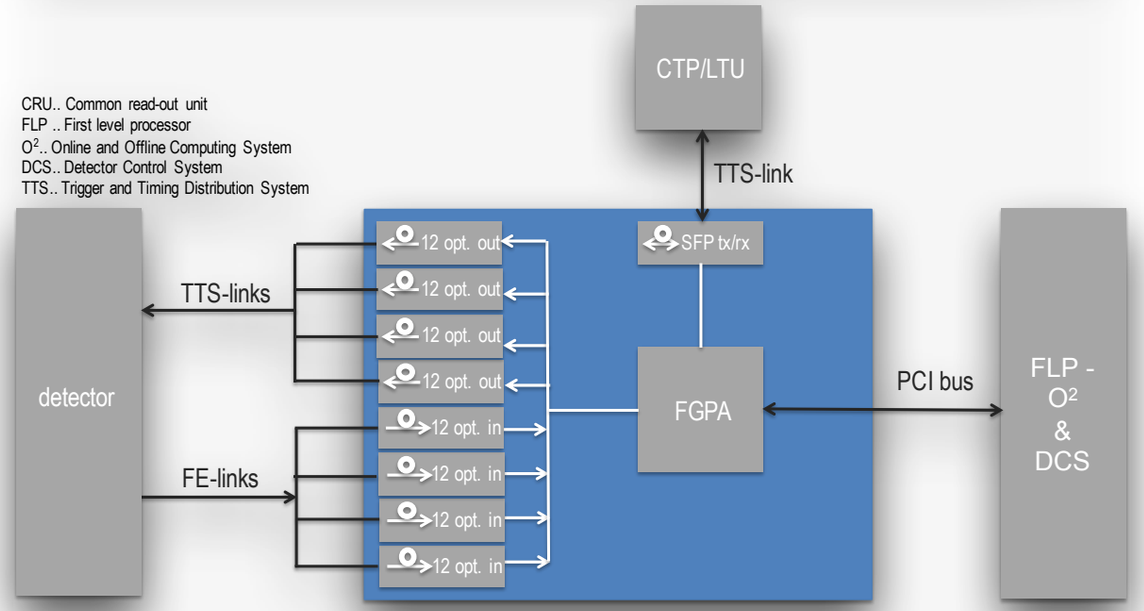
Development of a Common Readout Unit (CRU)

Legacy systems integrated into continuous readout

ALICE Upgrade R&D

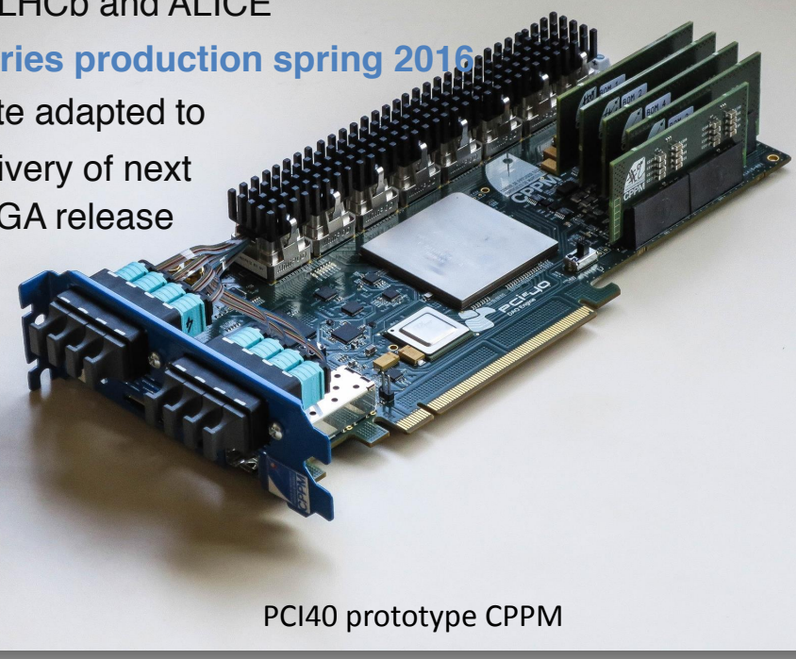
Common readout unit (CRU)

CRU.. Common read-out unit
FLP .. First level processor
O^2.. Online and Offline Computing System
DCS.. Detector Control System
TTS.. Trigger and Timing Distribution System



Common read-out unit – PCI40

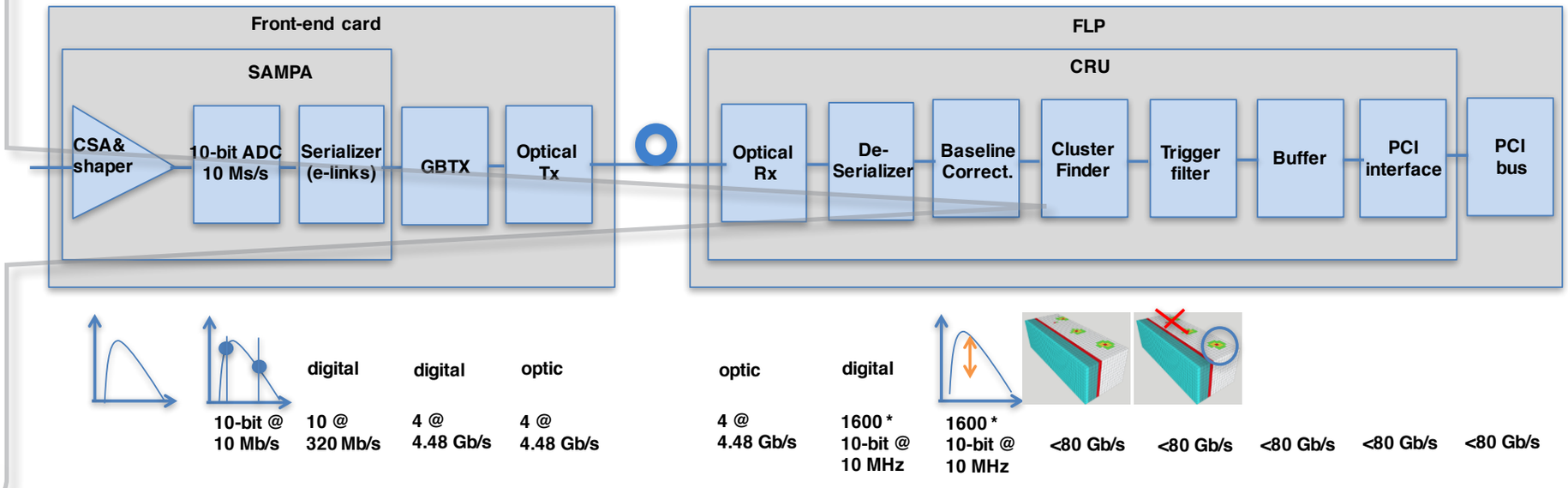
- **PCI40 (LHCb) prototype exists**
  - Main functionality tested by LHCb and ALICE
- **Pre series production spring 2016**
  - Date adapted to
  - delivery of next FPGA release



PCI40 prototype CPPM

CRU performs data compression:

- **Example: TPC cluster finder in FPGA.**
  - **from 160 Gb/s to < 80 Gb/s**



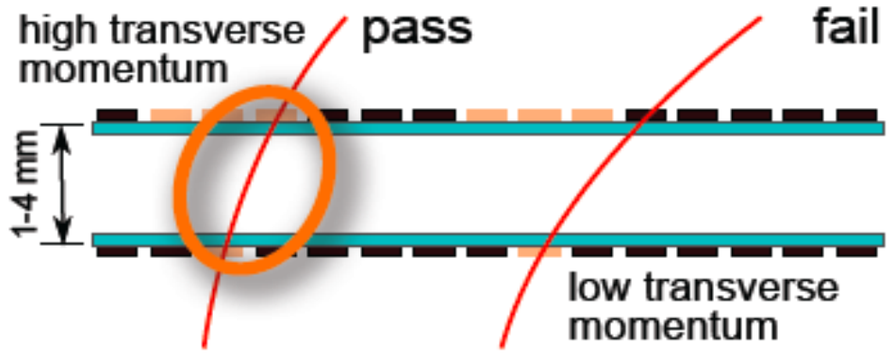
Run4 Challenges

- Need to target operations of CMS and ATLAS up to 7.5 x 10^{34} $cm^{-2}s^{-1}$ with a μ of 200 collisions per bunch crossing.
- To fully explore the EW scale trigger thresholds should remain comparable to what they are in Run2.
- Trigger and DAQ Upgrades are necessary: **in addition to Detector Upgrade it is necessary to readout the largest possible subset of data at 40 MHz:**
  - **Higher granularity, early access to full calorimeter data**
  - **Tracker becomes crucial**
  - **Additional detectors improving Muon Trigger Pt resolution**
  - **Large processing power and bandwidth for data treatment in off-detector electronics.**
- Different approaches chosen by CMS and ATLAS.

CMS in Phase II

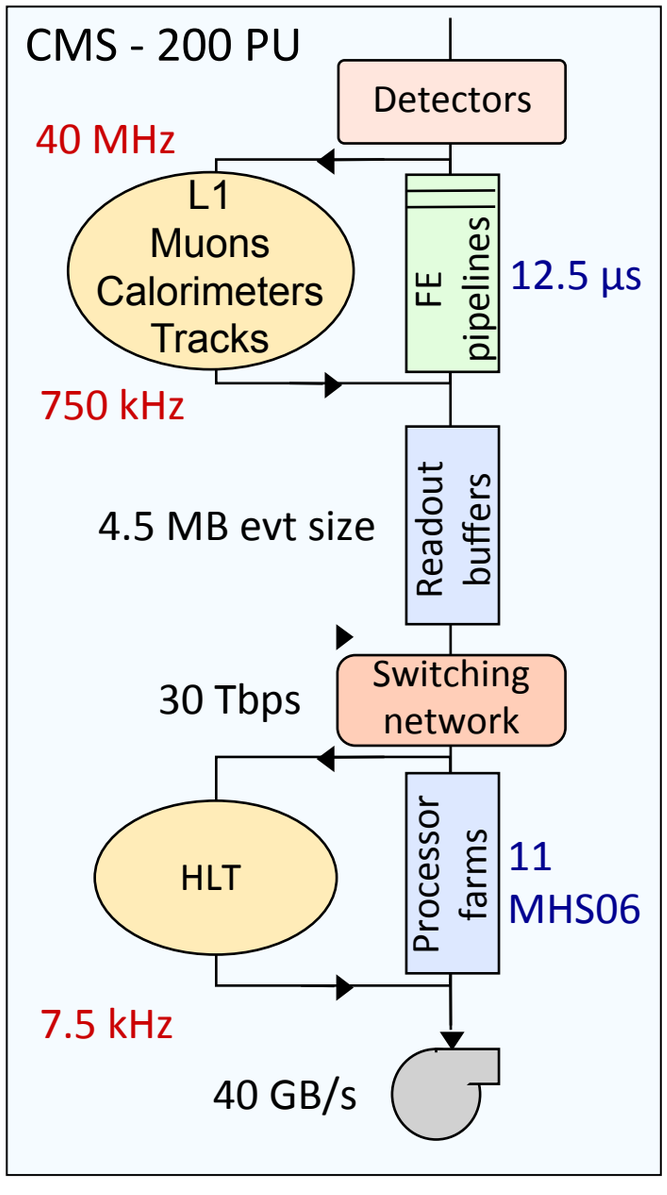
- On top of new Tracker, Calorimeter (improved S/N and time resolution) and High Granularity Endcap Calorimeters, new forward Muon detectors up to eta 3-6:
  - **Track information will be used in the trigger (self-seeding):**
    - **Tracker FE identifies high transverse momentum stubs.**
- **Latency 12.5 *μ*s, 750 kHz rate, HLT output 7.5 kHz**

pT>2 GeV @ 40 MHz



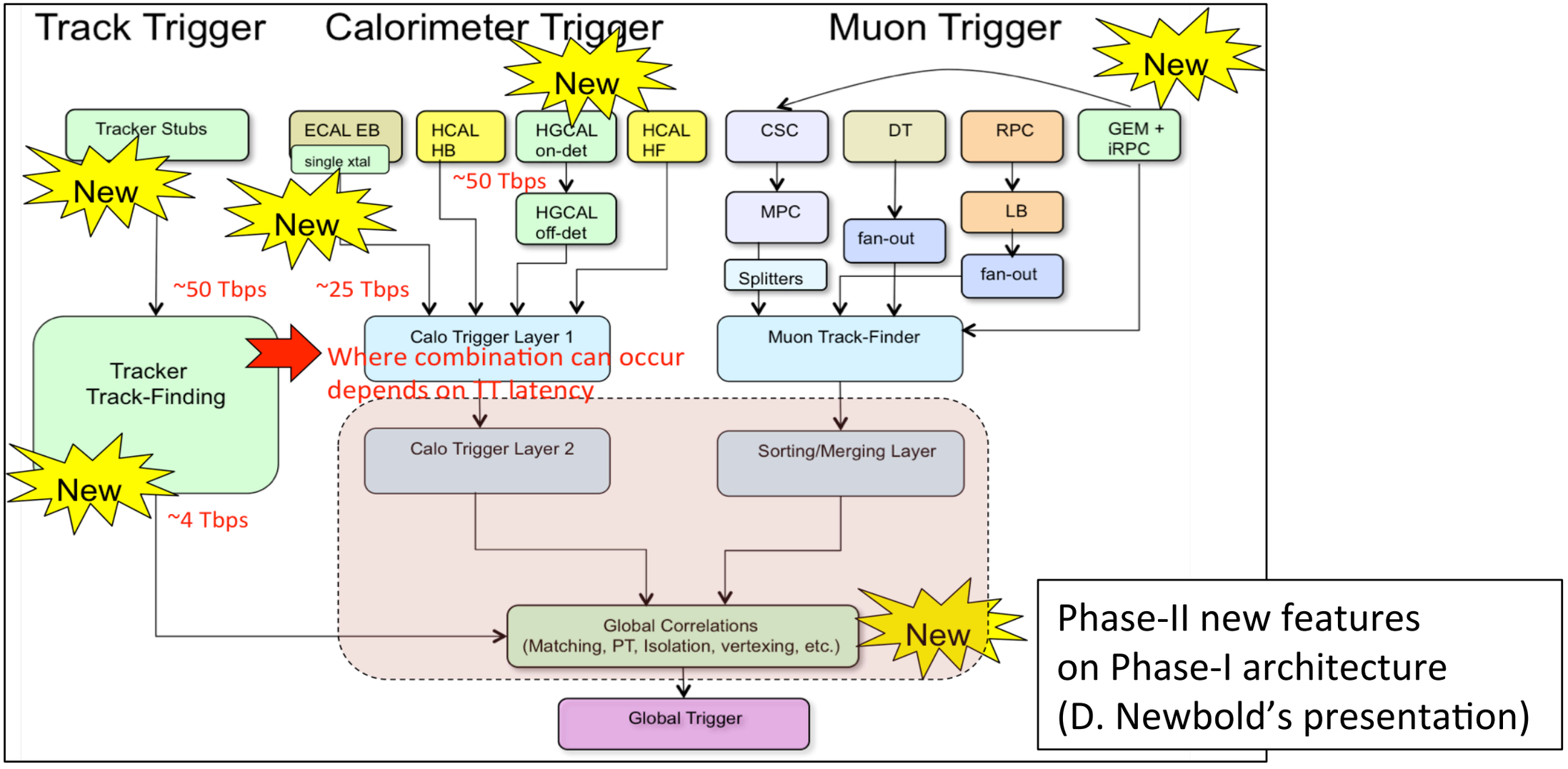
Trigger/DAQ Architecture

- L1-Trigger
  - 12.5 s latency, 750 kHz accept rate at 200 PU (see next slide)
- Trigger timing, throttling and control
  - High bandwidth bi-directional link allowing trigger information to steer readout
- DAQ
  - Similar event builder, HLT & storage as present
  - Increase bandwidth - 800 links x 100 Gbps to provide 30 Tbps throughput at 30% occupancy
- HLT
  - Processing power scales as PU x L1 rate ≃ 52 wrt Run 2 at 200 pileup - need to develop improved software using new computing technics beyond gain at constant resources
  - HLT rejection 1/100 (as current system)



F. Meijers's presentation

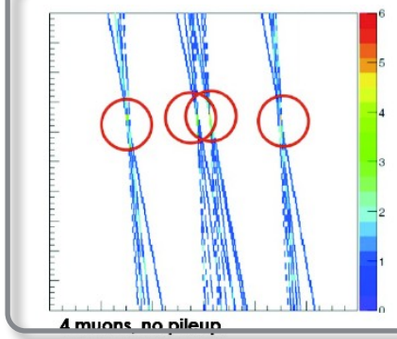
CMS Phase II architecture



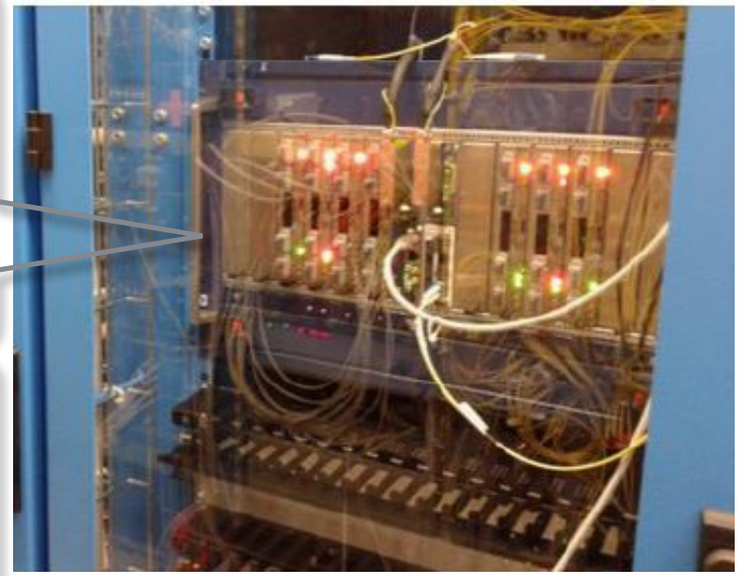
- **Global trigger correlates L1Tracks with (ele, mu, …) objects identified by L1Calo and L1Muon who combine information from all detectors.**
  - **Muons improve pT resolution**
  - **Electrons match L1Track with e/g candidate: ID**
  - **Tracker-based isolation improves for electrons and muons**
  - **Taus identification improves with track+calo**
  - **Multi object trigger improves by requiring objects from same vertex.**

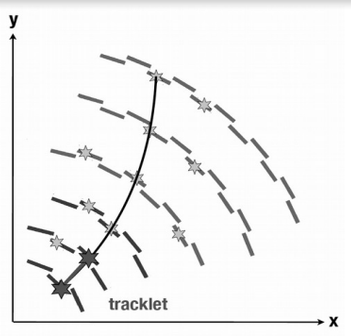
CMS R&D for PhaseII

- **Formidable technical challenges from L1 track finding:**
  - Data rates > 50-100 Tb/s
  - Occupancy and combinatorics: O(104 hits/BC) at μ = 200
  - Latency 4+1 μs for tracking
- **Three R&D projects on-going**

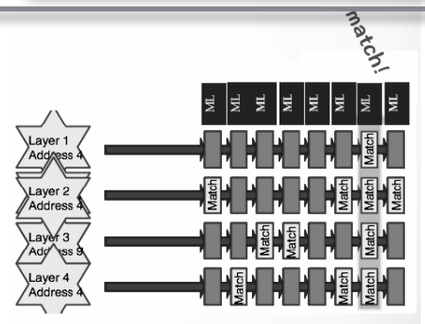


TMT Hough

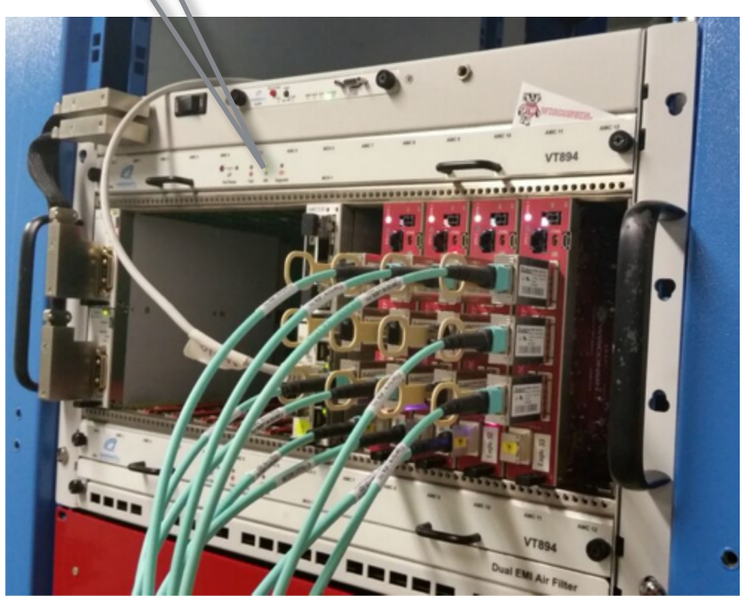




Tracklet

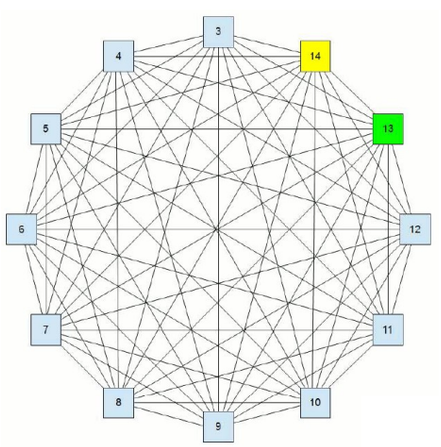


AM+FPGA



CTP7

Tracklet demonstrator @ CERN



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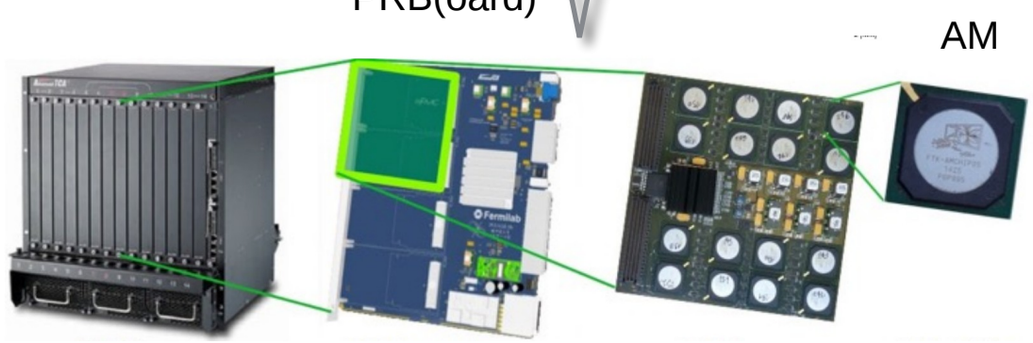


ATCA shelf

PRM(ezzanine)

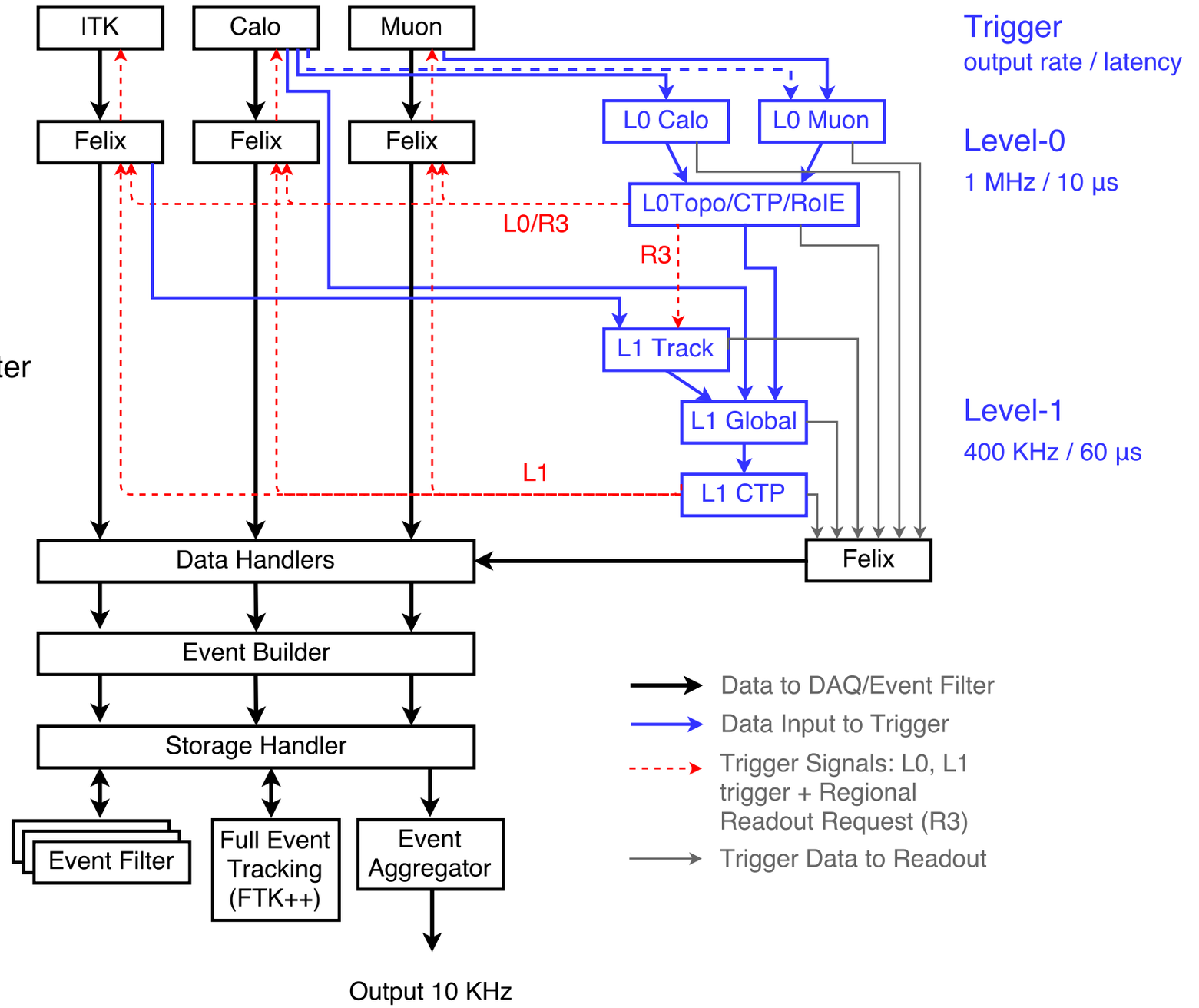
ATLAS

- **Split L0/L1 architecture. L0 latency similar to current L1 system.**

- L0 based on Phase-I L1Calo and new L0Muon Trigger

- **L1 latency longer (60 μs) uses L1Track AM-based track finder (2-4 GeV PT), driven by L0 Regions of Interest**

- L1Global trigger based on L1Track and full-calorimeter data and L0Muon



Option for transmitting all data off-detector at L0 rate of 1 MHz. Need for bandwidth and Event Storage.

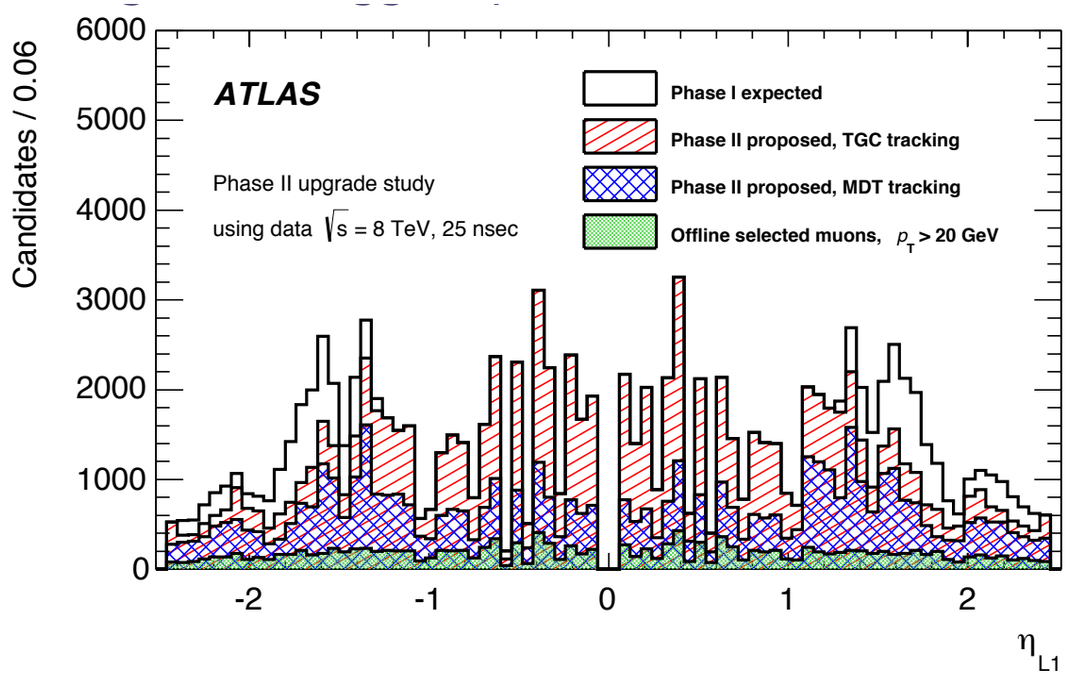
Need factor 100 of rate reduction in Event Filter.

ATLAS in PhaseII

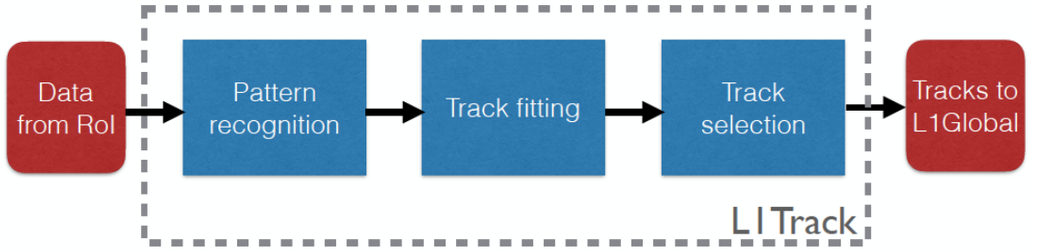
- **L0Muon uses information from precision muon chambers (MDT)**

- **L0Calo will use new digital signals from Tile and New Forward calorimetry.**

- **L1Track trigger receives Itk data from regions pointed by ROIs defined by L0 and finds tracks above 4 GeV.**



Input rate: 1MHz
Regional readout
(max 10% of ITk)



- Factor 5 reduction for MU20 and EM18 with >95% efficiency

- Track Z0 resolution better than 10mm

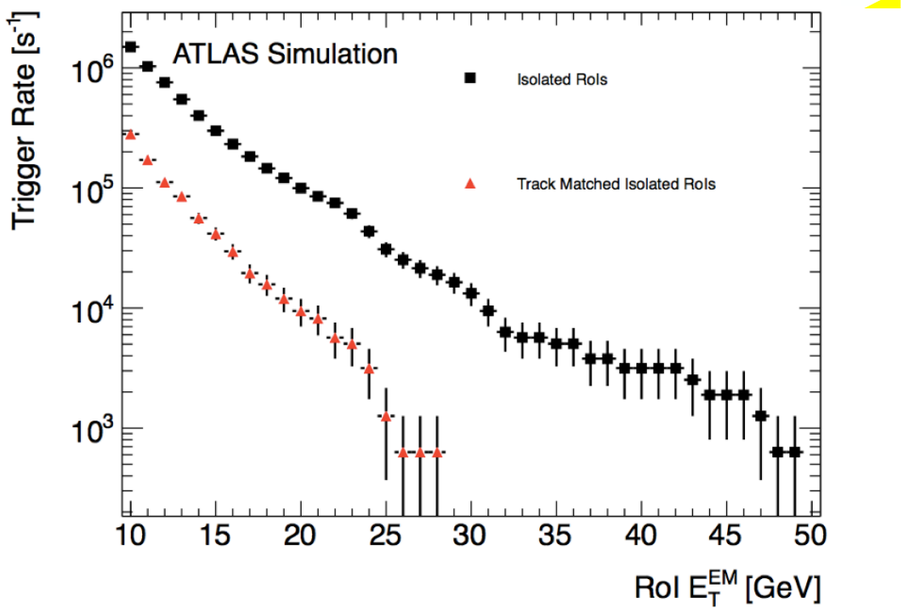
- needs regional readout and pattern recognition to fit within 15μs (L0/L1 scheme)

  - **processing by next generation Associative Memory + FPGA.**

Associative memory pattern bank

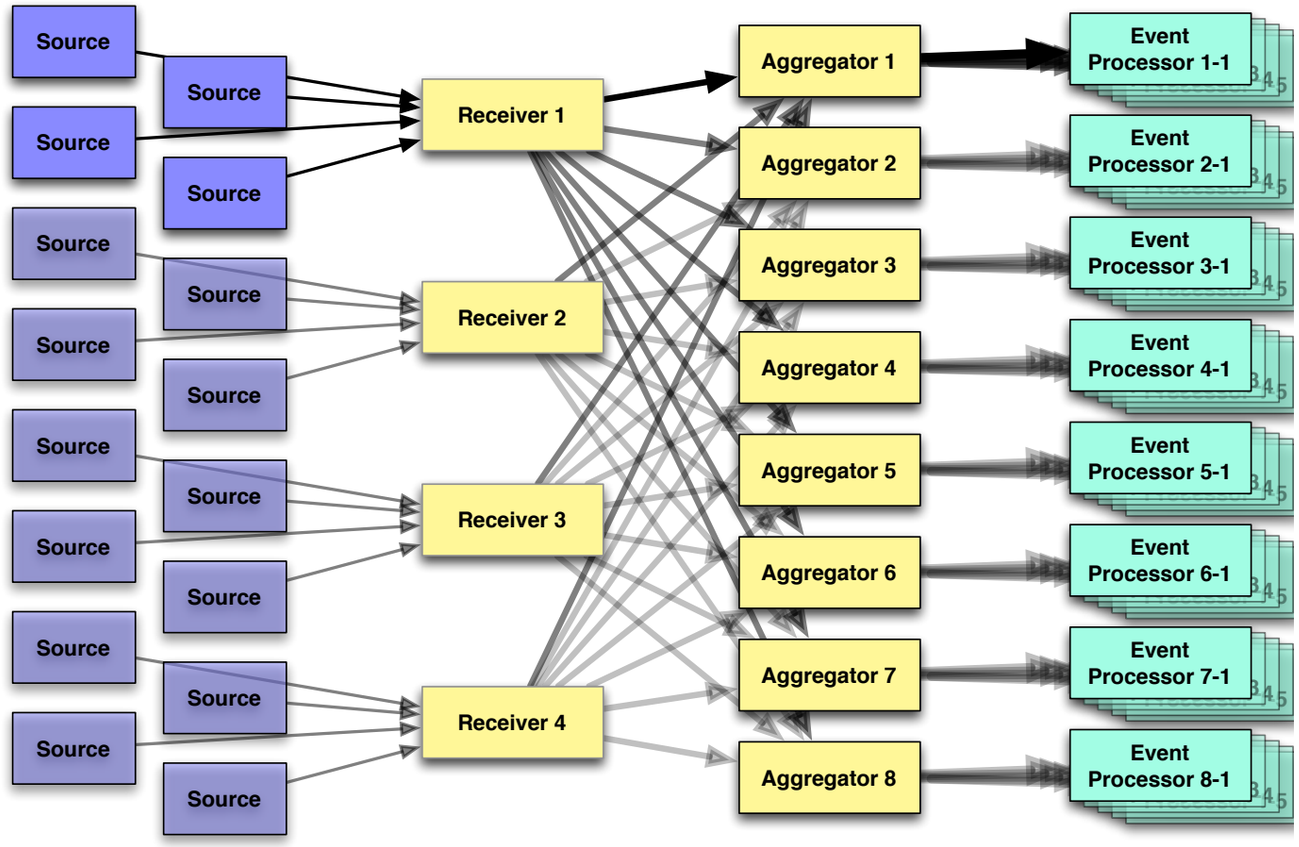
Linearised track-fit, suitable for FPGA

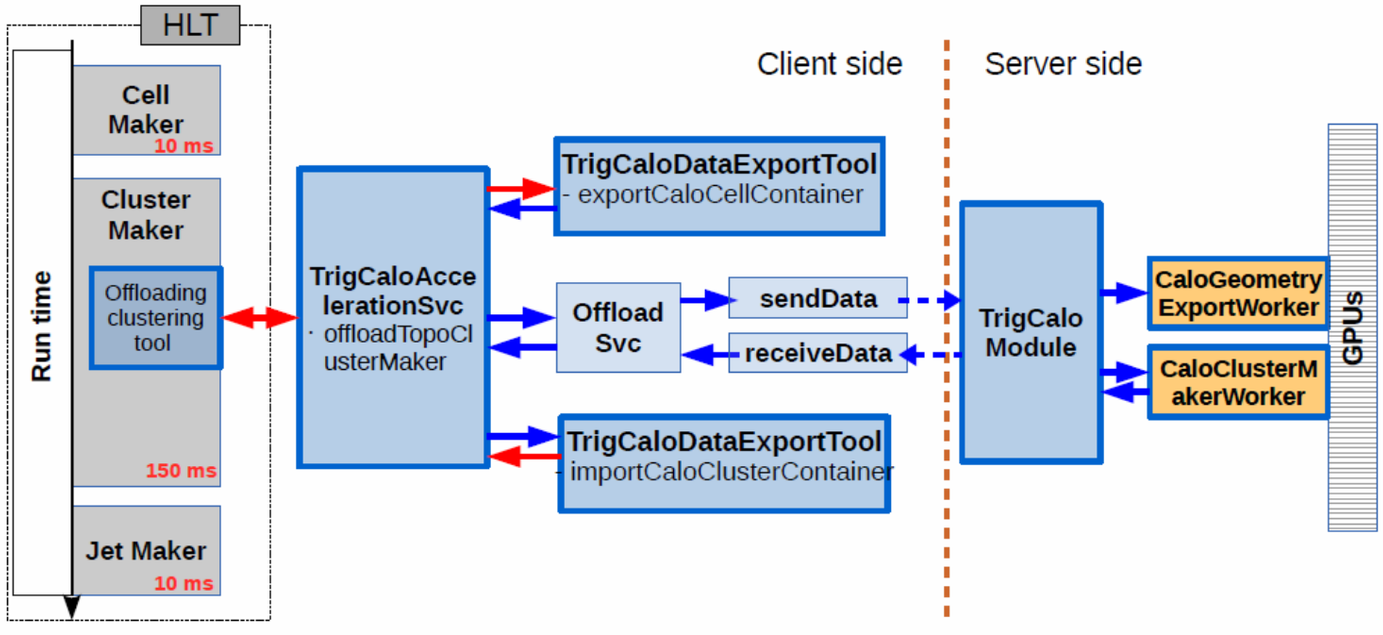
Based on either track-quality criteria, or track properties



ATLAS in PhaseII

- **L1Global processes full granularity calorimeter, L1Tracks and L0Muon information.**
  - Time multiplexed architecture.
- **Event Filter input rate increases to 400 kHz (1MHz in single-level architecture)**
- **hardware-based full event tracking (FTK++)**
- multi-threading, seamless integration of offline algorithms
- **General Purpose Graphical Processors (GPGPU) of FPGA.**
- **In single-level architecture accelerated regional track processing**





Summary

- **Not a simple job to give justice to such an enormous effort like designing, building and operating LHC trigger systems in 23 slides.**

- **Keywords appearing in Run3 systems**: new trigger architectures like **Time Multiplexing**, **Topological Triggers**, **modular electronics** µTCA, ATCA, **based on Large FPGAs, hosting O(100) links running at 4.8-12.4 Gb/s**. **Readout boards based on PCIe**. **First deployment of online data reduction** (and calibration). **Timing and trigger distribution based on PON+GBT**.
  - Status: already deployed (CMS) or at full-functional prototype stage (others)

- **Keywords for Run4 are**: **self-seeded (CMS) or seeded (ATLAS) tracker systems**, **full event readout at 400-750 KHz-1MHz. HLT need for large input bandwidth and very performant storage handler**. **HLT profiting from hardware-based processing, AMs, FPGAs and GPGPUs.**
  - Many ongoing R&D projects ongoing.

Backup

ATLAS single-level Trigger Architecture