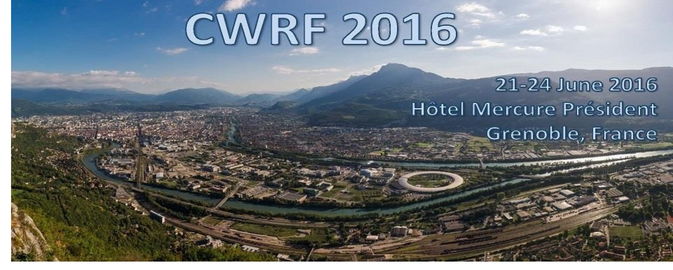

ADVANCED LOW LEVEL RF SYSTEM FOR IFMIF AND LIPAC PARTICLE ACCELERATORS

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Introduction

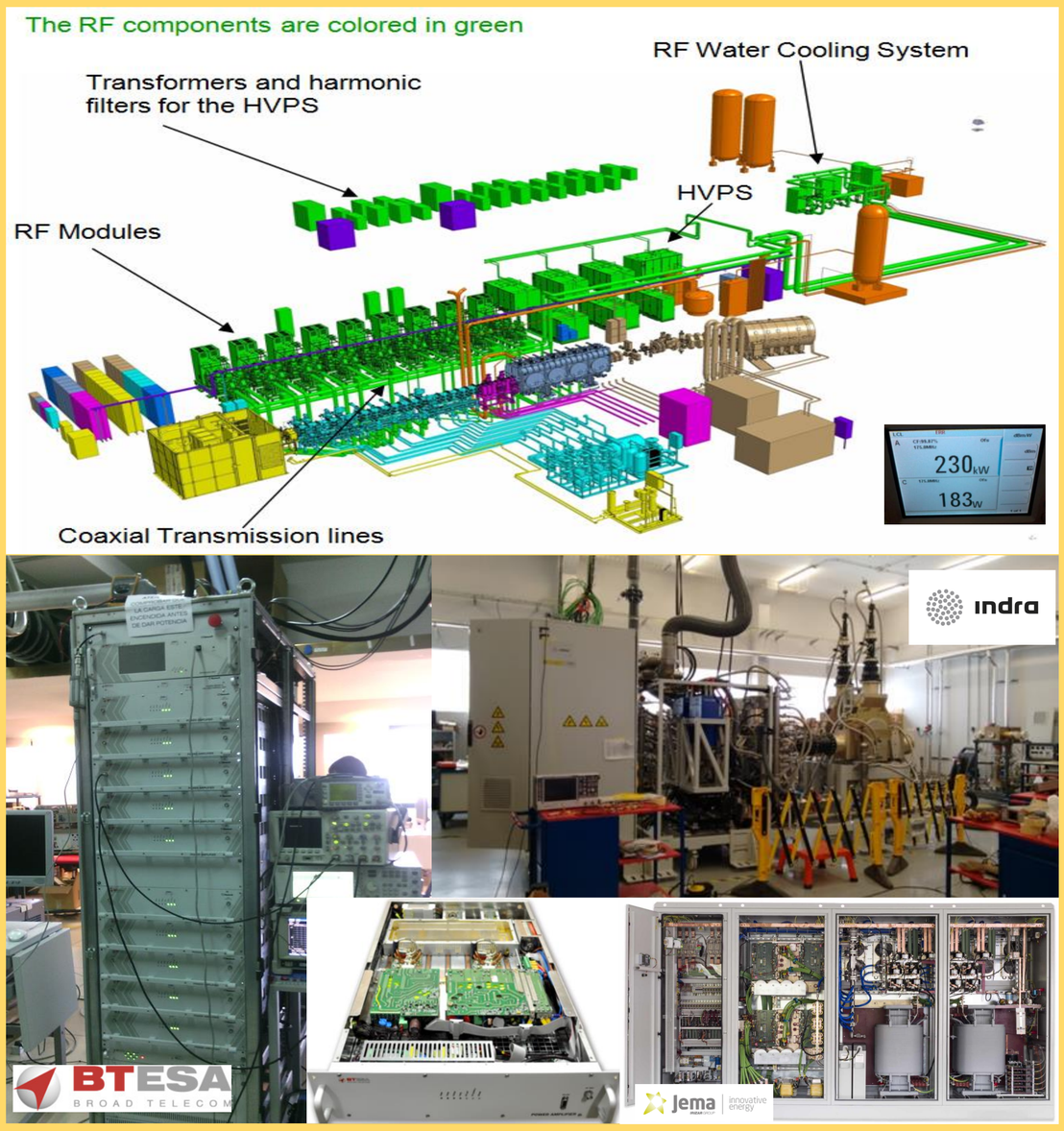
The IFMIF/EVEDA Accelerator Prototype (LIPAc) is currently under construction in Rokkasho (Japan). LIPAc will generate a 9 MeV deuteron beam at 125 mA current with a 100% of duty cycle, and it will serve to validate the final IFMIF accelerator concept. CIEMAT (Spain) and its partner companies and institutes are in charge of integrating the IFMIF/EVEDA Radiofrequency (RF) Power System. Very high availability, high performance, and easy maintainability are the main objectives for this development. Dealing with such a challenging goals has required successive improvements in the reference design. One of these innovative improvements is the **FleXible Low Level RF** system **(XLLRF**) , which is presented in this poster.

The XLLRF, a Fully Digital LLRF

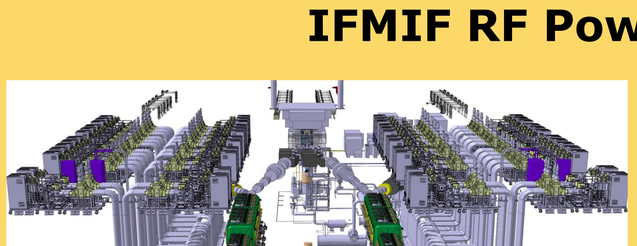
LIPAc and IFMIF accelerators beams will manage the world's highest deuteron current and space charge. The management of these challenging characteristics requires innovative solutions. This innovation leads to a high level of uncertainty on how to match the system specifications and thus a flexible and reconfigurable high performance LLRF is required. LLRF systems are usually devoted to the closed loop regulation of the accelerating cavities voltage signal. These systems use to be analog or digital-analog, since they use, at least, analog front-ends for intermediate frequency (IF) conversion before or after digitalization. However, the LIPAc/IFMIF flexible LLRF System (called XLLRF), developed by CIEMAT and SEVEN SOLUTIONS, is an innovative fully digital system. No analog frequency conversion is performed, which increases the measurement bandwidth and simplify the analog front-end design. This LLRF also integrates White Rabbit (WR) protocol for timing synchronization (sub-nanosecond) and Master Oscillator distribution. The first prototypes have been tested with the full power LIPAc RF amplifier chains performing better than expected.

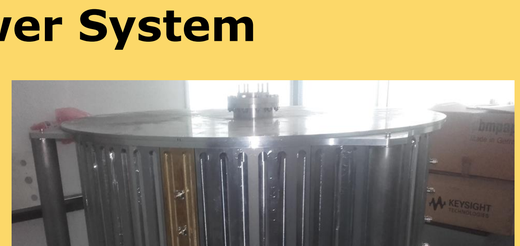
LIPAc RF Power System

The LIPAc RF Power system consists of:
1. Eight 200 kW Tetrode based RF chains for feeding the RFQ.
2. Eight 105 kW Tetrode based RF chains for feeding the Super Conducting Linac.
3. Two 16 kW SSPA RF chains for feeding the bunching cavities of the MEBT.
4. Twelve 400 kW, 13 KV DC Power Supplies (HVPS).



IFMIF RF Power System





Matrix Combiner & SSPA

The current reference design for the IFMIF RF Power System is based on High performance SSPA and Matrix Combiners (under test). This new solution will take advantage of the flexibility of the fully digital XLLRF.

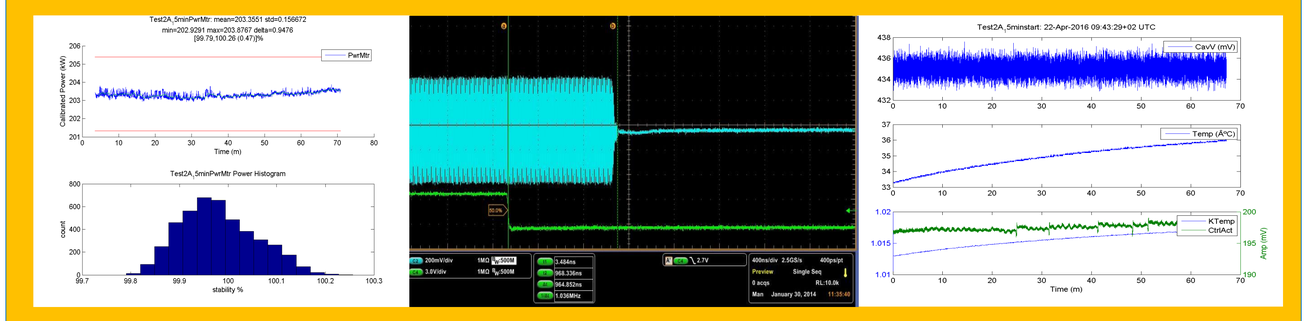
Main Characteristics of the XLLRF

Hardware description

The LLRF module is a compact and fully integrated system. It is based on a modular design, where the different boards can be easily extracted and substituted in order to improve the availability. A flexible and complete user interface eases the setting, commissioning and maintenance tasks.

Main Functionalities

- Cavity field amplitude and phase control (feedback loop). Stability req. < 1%.
- Accelerating cavity tuning: manual and automatic.
  - Mechanical Tuning: step motor control
  - Frequency tuning: modulation of RF frequency to avoid power reflection. (freq. ± 300kHz)
- Cavity/coupler conditioning: manual and automatic.
- Continuous wave and pulsed operation modes.
- Feed-forward loop: cavity pre-filling, beam loading compensation.
- Fast Interlocks control (Emergency stop less than 3usec for a 230 kW output).
- Time and Clock distribution by White Rabbit Technology:
- Signal diagnostics and remote data access.
- Fast data logger for post mortem analysis.
- Automatic start-up.
- Master-slave feedback loop (RFQ): to operate several RF chains as an unique chain.
- Temperature dependence compensation.



Advantages

- Fully digital LLRF: Direct digital synthesis and direct digital sampling (high speed DACs and ADCs). Neither external front-end nor IF are used for frequency conversion.
- Modular design with all functionalities integrated in the same module.
- Flexible, reconfigurable, and customizable system.
- Fully digital signal processing. Flexible nominal frequency without hardware modifications.
- The use of White Rabbit technology (CERN) for time and clock distribution:
  Clock RMS jitter < 1ps & sub-nanosecond accuracy
- EPICS ready technology.
- Use of advanced FPGA technology (Xilinx Virtex-6).
- Configurable Analog Input module to receive different input signal levels: variable ADC range and attenuators, inputs with amplifiers.

All this characteristics traduce in a very flexible and reconfigurable system, where many improvements and modifications can be performed without HW changes, just via firmware: new functionalities, improved and faster control loops, operation frequency migration, fast and efficient frequency modulation, etc.

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