CMOS detectors for ILC: radiation hardness

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XII Meeting of the Spanish Network for future linear colliders

from Monday, 25 January 2016 at **08:30** to Tuesday, 26 January 2016 at **16:00** (Europe/Zurich)

CIEMAT
Avenida Complutense 40 Madrid 28040 España

Summary

- Hybrid vs CMOS detectors:
  What's He Got That I Ain't Got?
- Depleted CMOS and strip readout
- Radiation hardness (beyond ILC needs) of depleted CMOS
- Conclusions

Hybrid detectors

See: N. Wermes, arXiv:1509.09052v1, 30 Sep 2015

Advantages:

Both parts (sensor and RO chip) can be **optimized separately**

Sensor: radiation hardness

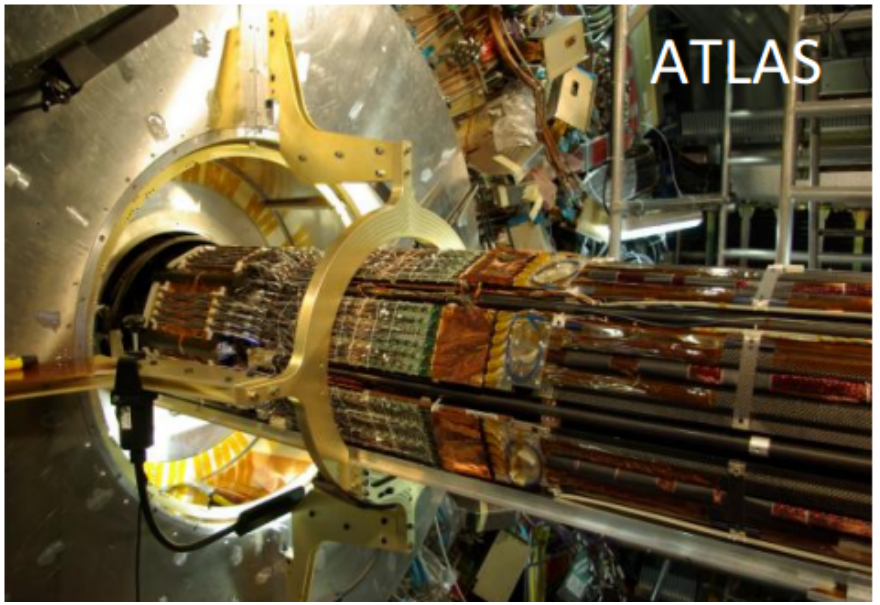
RO chip: allows for **complex signal processing**:

- Digest & process high rates (~Mhz/mm2)
- Zero supression
- Storage of hits during decision time (L1 latency)

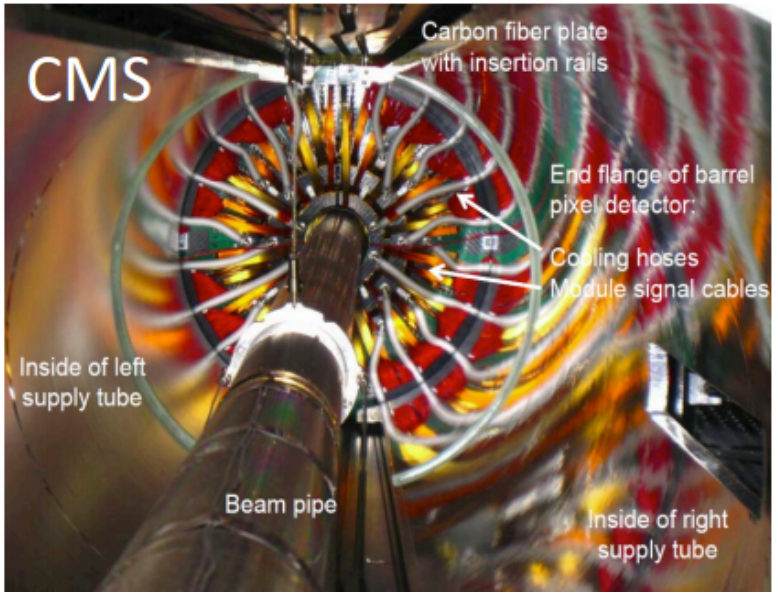
Disadvantages:

1) Large **material budget** (~3% X_0 in ATLAS& CMS) due to:
sensor, RO chip, flex capton, support, cooling, services.

2) **Module** production: bump bonding and flip chipping is complex and expensive



all based on
"Hybrid Pixels"



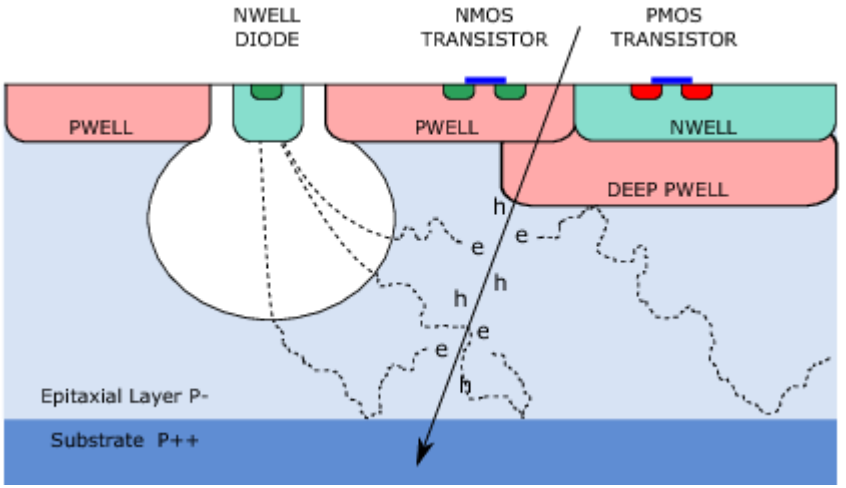
CMOS

Advantages

1) **Low cost**, as long as **standard commercial** process not modified
2) Monolithic: avoids hybridization, mechanically simpler, large **area (stiching)**
3) Smaller pixel size achievable (not limited by BB size)
4) They can be thinned down to 50 μm

Disadvantages (of MAPs, triple well MAPS, INMAPs...)

1) Industry does not care about particle detection (except photons)
2) Limited **radiation hardness** if charge is collected by **diffusion**
   (they use cheap low resistive substrates)
3) Normally “simpler” RO (MAPs do not allow PMOS transistors): signal is **multiplexed**



More info: ILC Detector Baseline Design report

CMOS for ILC

- CMOS detectors are **no strangers** to ILD:
  - Present in **VTX** detector
  - Present in 2 first **endcaps** of forward tracking
  - They are not the only detectors considered: **FPCCD** and **DEPFETs** are other candidates

- **CMOS** and in general, undepleted MAPs, are **enough** for **ILC** needs:

  - Bunch structure (1 ms long bunch train at 5 Hz) is "slower" than charge collection by diffusion (~μs)

  - Very modest radiation environment (compared to LHC): **1kGy and 10^{11} n_{eq}/cm^2/yea**

  - Sensors with similar needs already used in running experiments. Example:

    STAR experiment (@RHIC)
    AMS 350 nm, pitch 21 μm, 400 Ωcm, T=35 ºC, 200 μs,
    $3 \cdot 10^{12}$ n_{eq}/cm^2 and 150 kRad
    ALICE ITS
    Tower Jazz 0.18 μm, 20-40 μm epi layer, >1 kΩcm, **700 kRad/10^{13} n_{eq}/cm^2**

- These devices **collect charge by diffusion**.

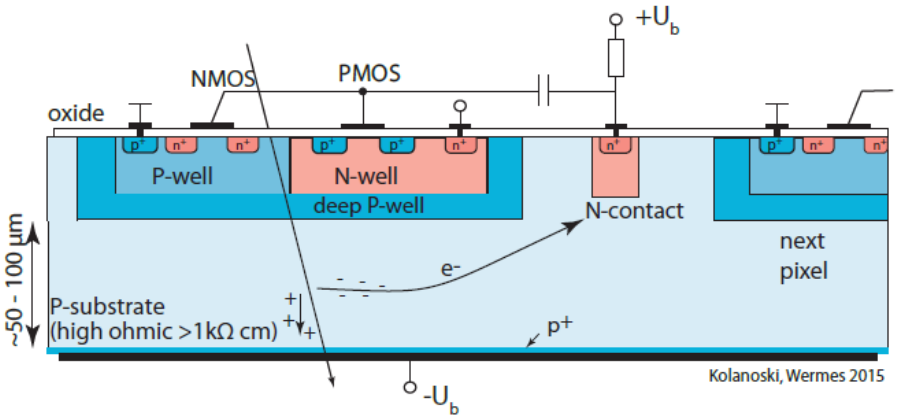
LHC upgrade is working in a **new** (in HEP) family of **CMOS** devices that LC community could benefit from ...

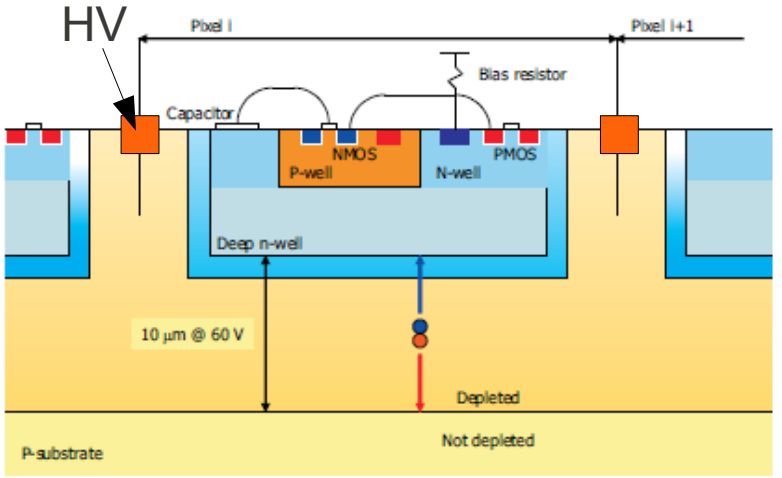
(Partially) Depleted CMOS

- **Radiation Hardness:** Drift as charge collection mechanism → deplete bulk
- **Cost:** Stick to commercial CMOS technology

$$d \sim \sqrt{\rho \cdot V}$$

HR-CMOS

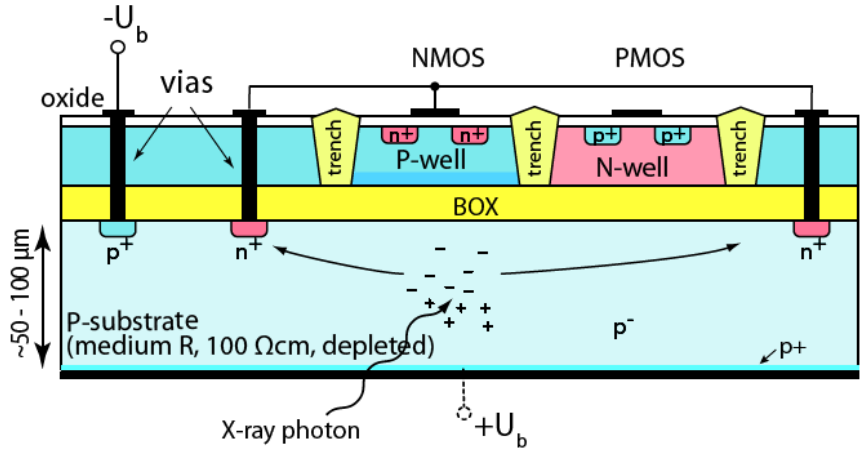




HV-CMOS

Note: a bit "oldish" classification. Now measuring what is the optimal choice for ρ·V

CMOS on SOI



ATLAS HV/HR-collaboration
HVCMOS: [2015 JINST 10 C05021]
HRCMOS: [JINST 10 (2015) 02, P02013]
SOI: [NIM A796 (2015) 8]

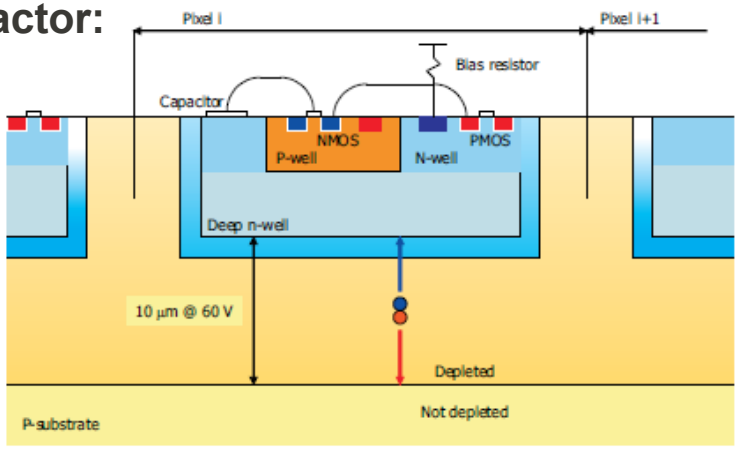
HVCMOS

• IFCA (within RD50 collaboration) involved in radiation hardness studies of these devices

• Uses **commercial** high-voltage (≤120V) CMOS technology (used in industry as HV switches). This HV is applied to a **low resistivity substrate** (ρ~10 Ω ·cm)

Expected **10 μm depletion at 100 V** → Charge can be collected **by drift**
Expected **900 e-h pairs** → built-in **preamp** is needed

• To avoid damage to transistors both, **NMOS and PMOS** are **"embedded"** in a **Deep N Well (DNW)** . Any complex signal processing can be implemented inside. The DNW works both as a substrate for transistors and as the signal collection region. **Nearly 100% fill factor:**



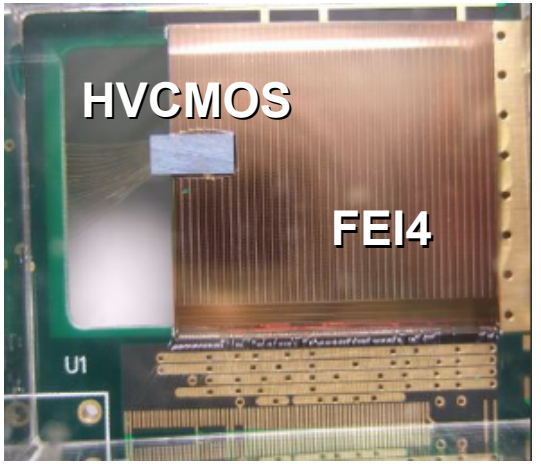
– Charge carriers do not have to travel long before being collected → **reduced trapping** impact.
<u>We need to quantify this radiation hardness</u>

– Capacitance due to big collecting region increases noise of CSA

• Two development strategies:

1) **Conservative**: drop in replacement of current sensors. Build preamplifier in sensor chip and capacitively couple to RO chip. CCPD (Capacitively Coupled Pixel Detector) concept

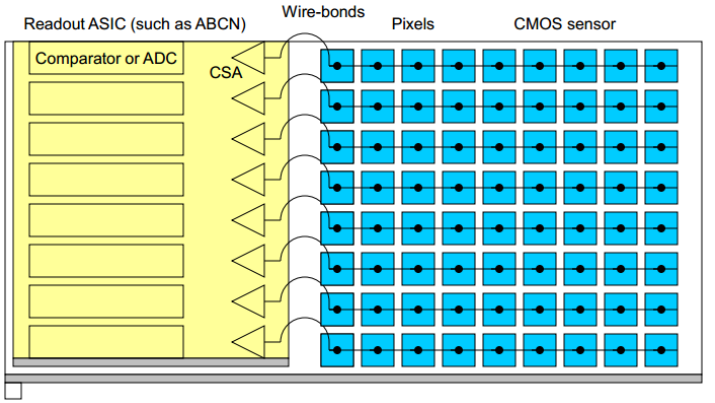
2) **Liberal:** Go fully monolithic and totally replace RO chip



HVCMOS strip readout (pixelated strips)

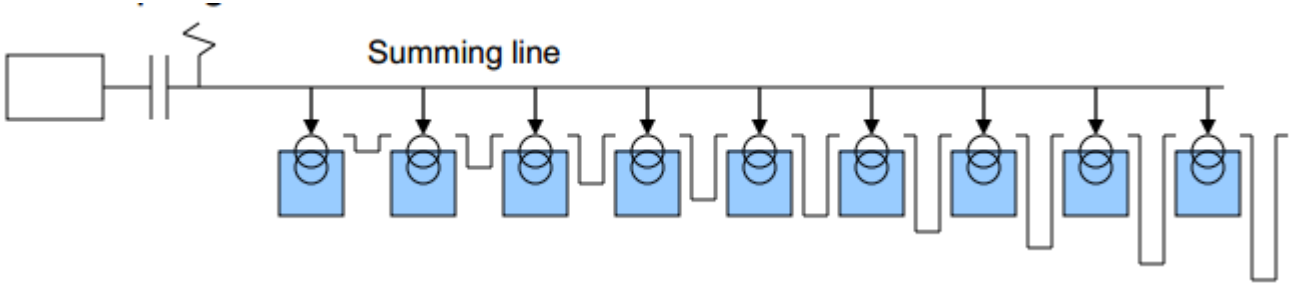
• A standard **strip** sensor can be **replaced** with an HVCMOS detector segmented into **long pixels**, e.g., 40 μm × 800 μm (ATLAS case) .

• Detector can be connected to **existing readout chip** (one-to-one strip sensor replacement)



• Large area CMOS sensors can be produced by **stitching** several 2cm x 2cm wafer reticles

• **2D position information**: every pixel generates a digital current pulse with unique amplitude



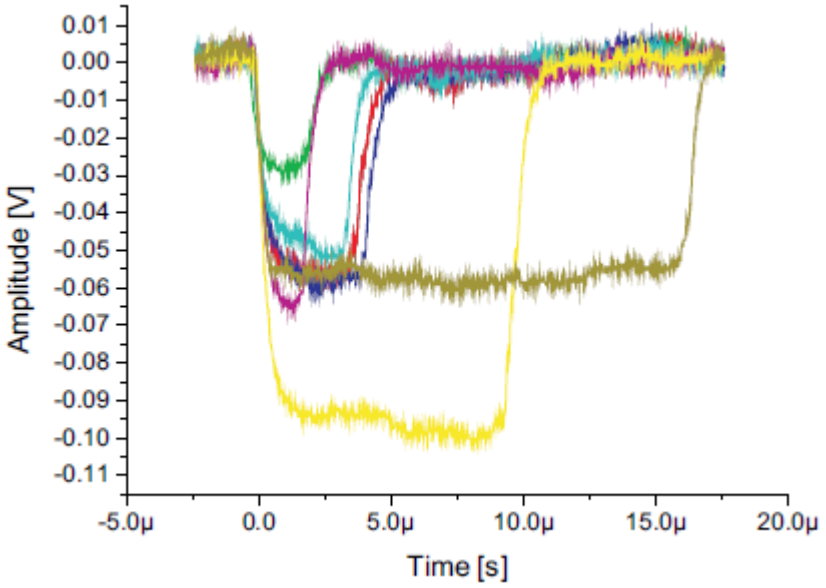
Pixel output current sources biased by z-dependent bias voltage

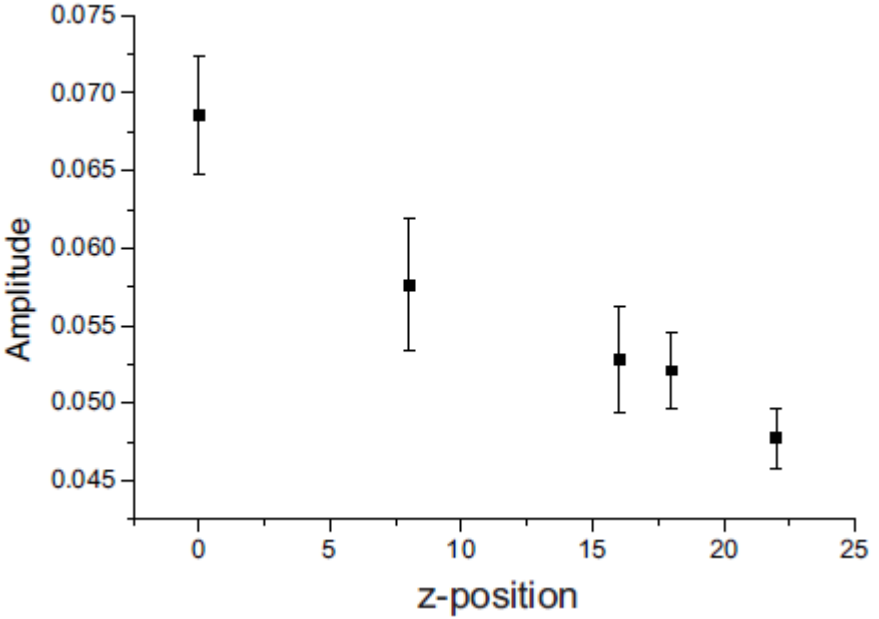
• Prototypes:

- **Demonstrator** (ams 180 nm) [I. Peric, PoS(Vertex 2012)021]
- [2015] Small test detector HVStrip in 350nm AMS technology (ATLAS upgrade)

• **Power** consumption per pixel including a CSA and a comparator ~7μW

HVCMOS strip readout





Pulse height discrimination

No strip readout chip used. Measurements directly in an oscilloscope

^{55}Fe **source measurements**: **Z-dependent bias** is used.

Amplitude variations due to current source mismatch and noise

Pulse width proportional to the charge measured by the integrated CSA

Measured output signal amplitude as the function of pixel-position.

Signal amplitudes are Z-dependent and fluctuate from hit to hit.

I. Peric, PoS(Vertex 2012)021

HVCMOS radiation hardness

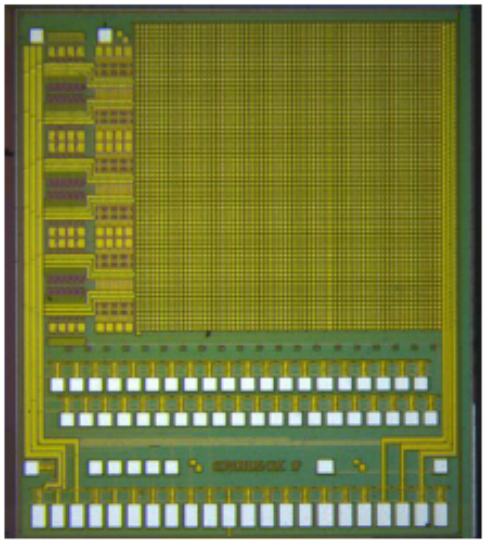
M. Fernandez et al, JINST paper (approved for publication)

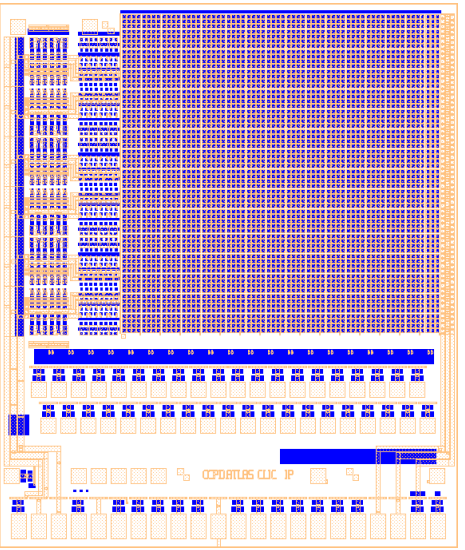
- Contributed by **IFCA-UC**, together with **CERN-SSD** within **RD50** collaboration
- Charge collection studied using dedicated diode conceived for **edge-TCT** measurements

Neutron (Lbj)	1	7	20
Protons (PS)	1.4	3.7	6.9

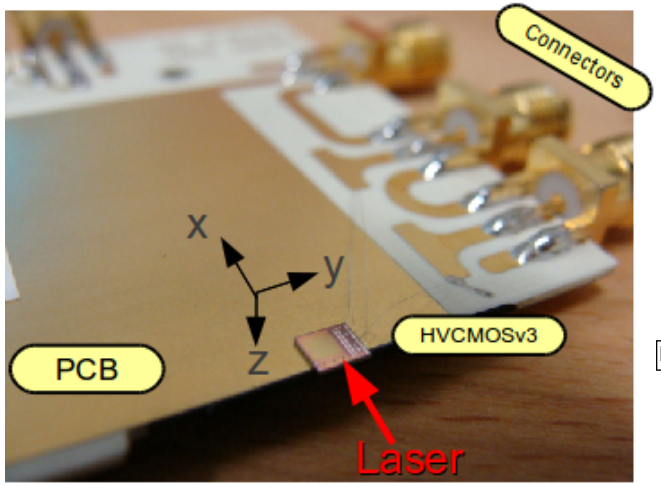
$\times 10^{15}\ n_{eq}/cm^2$

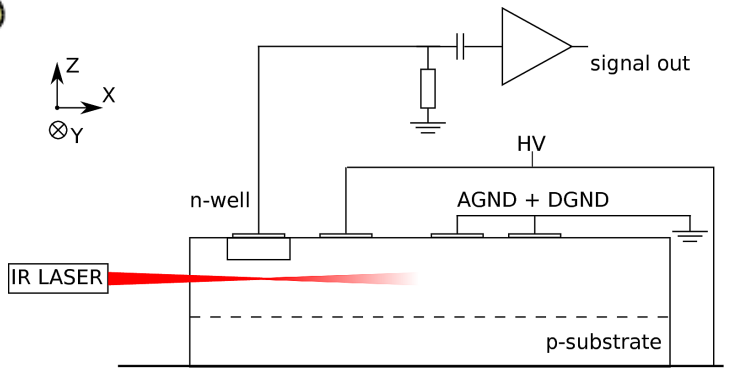
ILC needs: $10^{11}\ n_{eq}/cm^2/year$

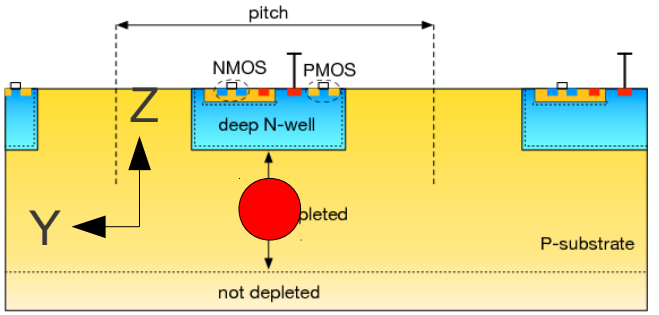




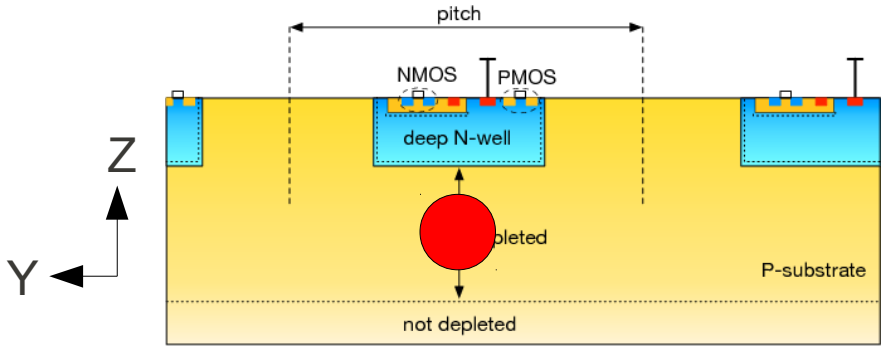
- **Edge-TCT:** PCB, HVCMOS biasing, measurement sketch

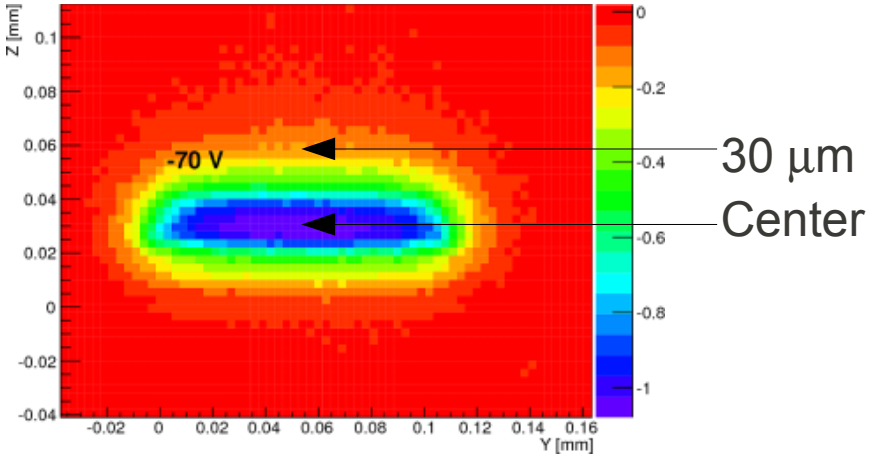


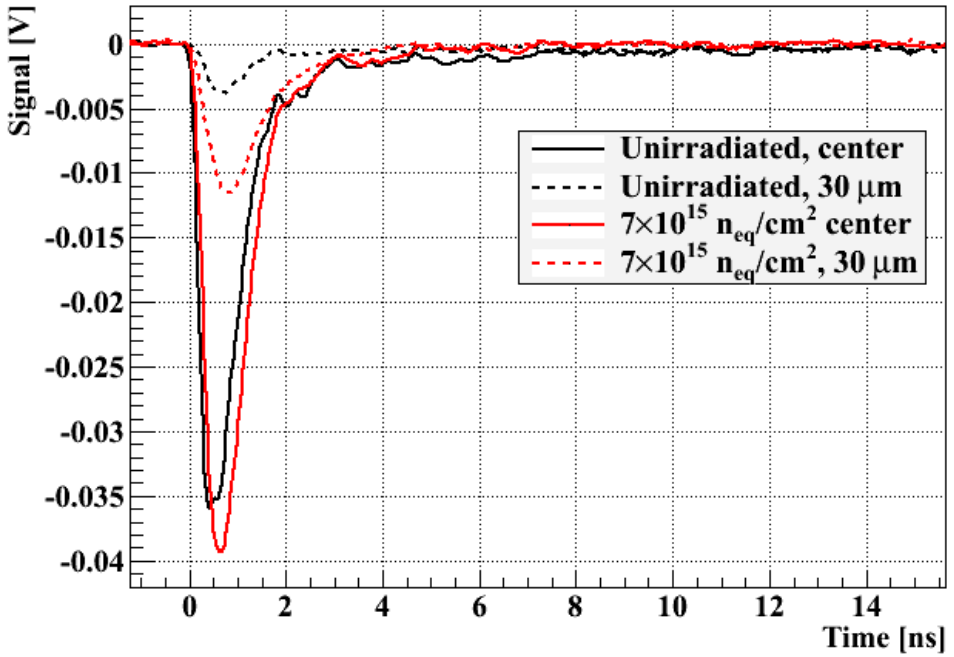


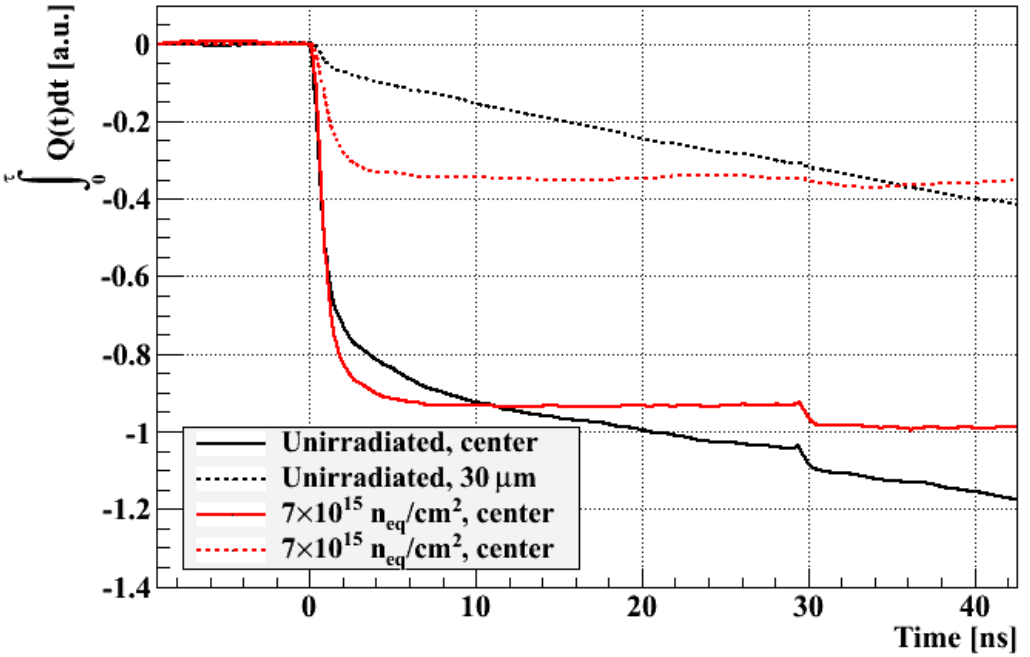


HVCMOS: radiation hardness





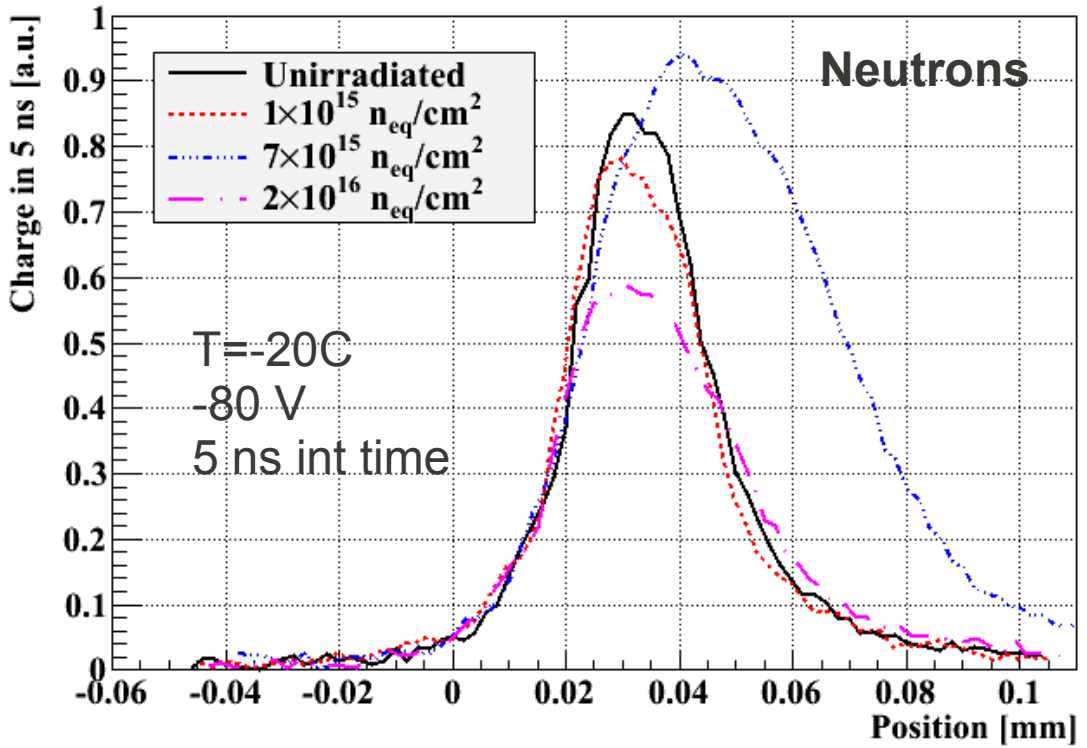


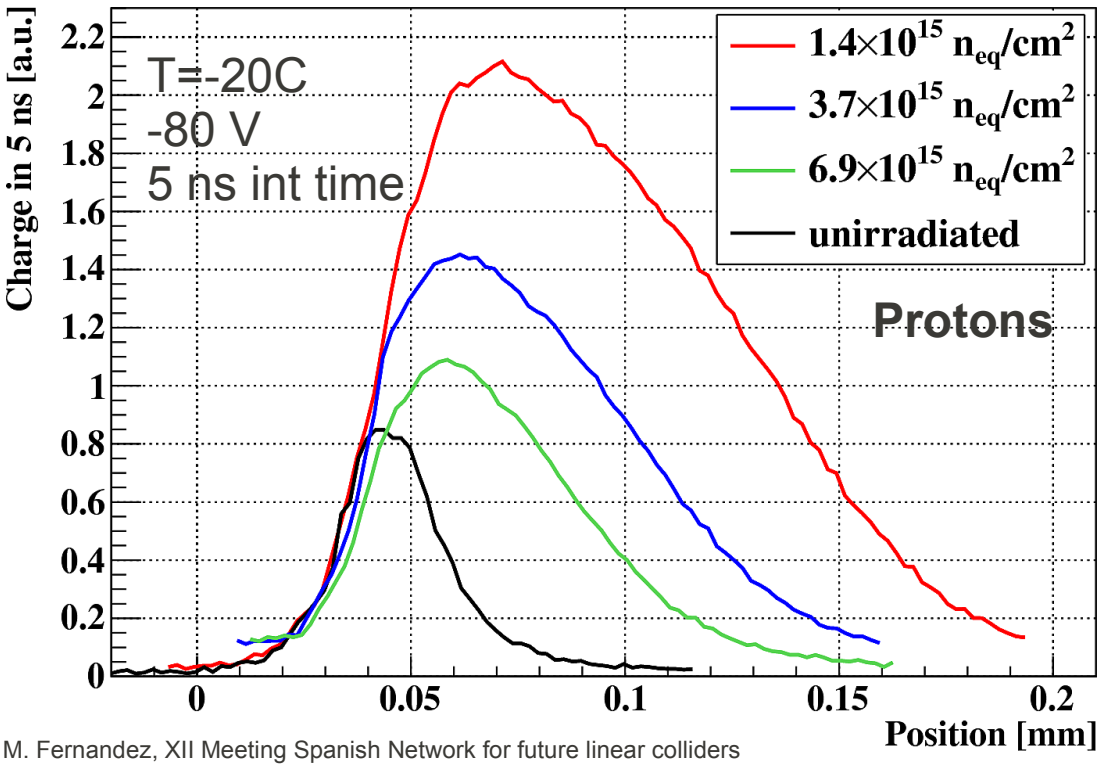


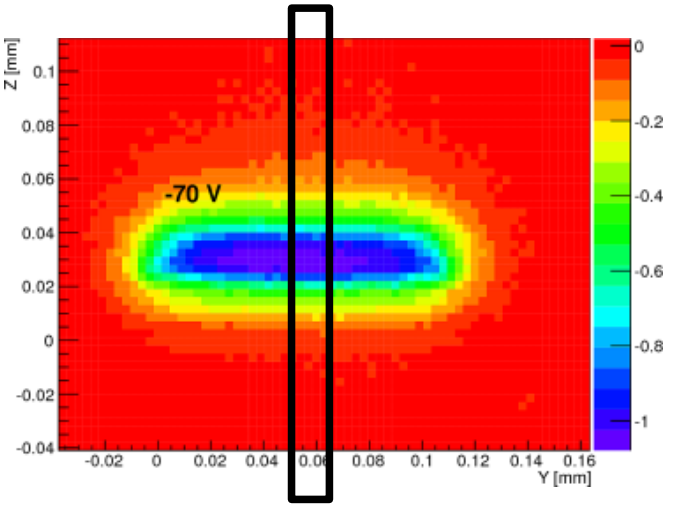
- Transients at the center of the diode and 30 µm below it.
- Fast collection → Seems like drift

- Running charge: accumulated charge as a function of integration time
- Distinct signature of diffusion is unveiled

HVCMOS: charge profiles







- Collected charge profiles Q(z)
  FWHM of profiles → Depletion depth

Neutrons:

Unirrad & 1e15 very similar

Deepest depletion for 7e15 n_{eq}/cm^2

Protons:

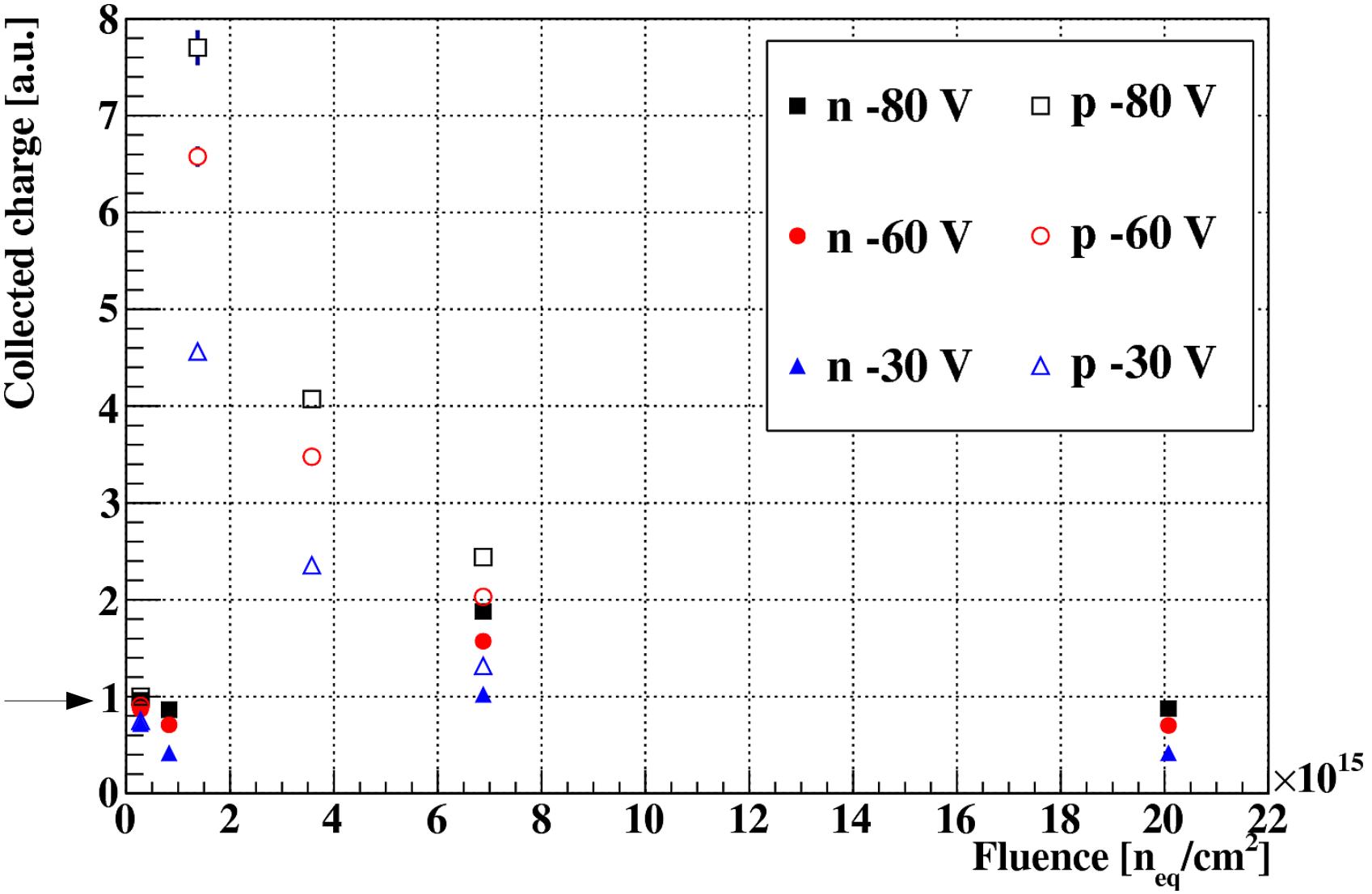
More charge collected for any fluence

Deepest depletion for 1.5e15 n_{eq}/cm^2

Note: Laser power variation 1% (RMS)

Mind different scales!

Collected charge (neutrons and protons)

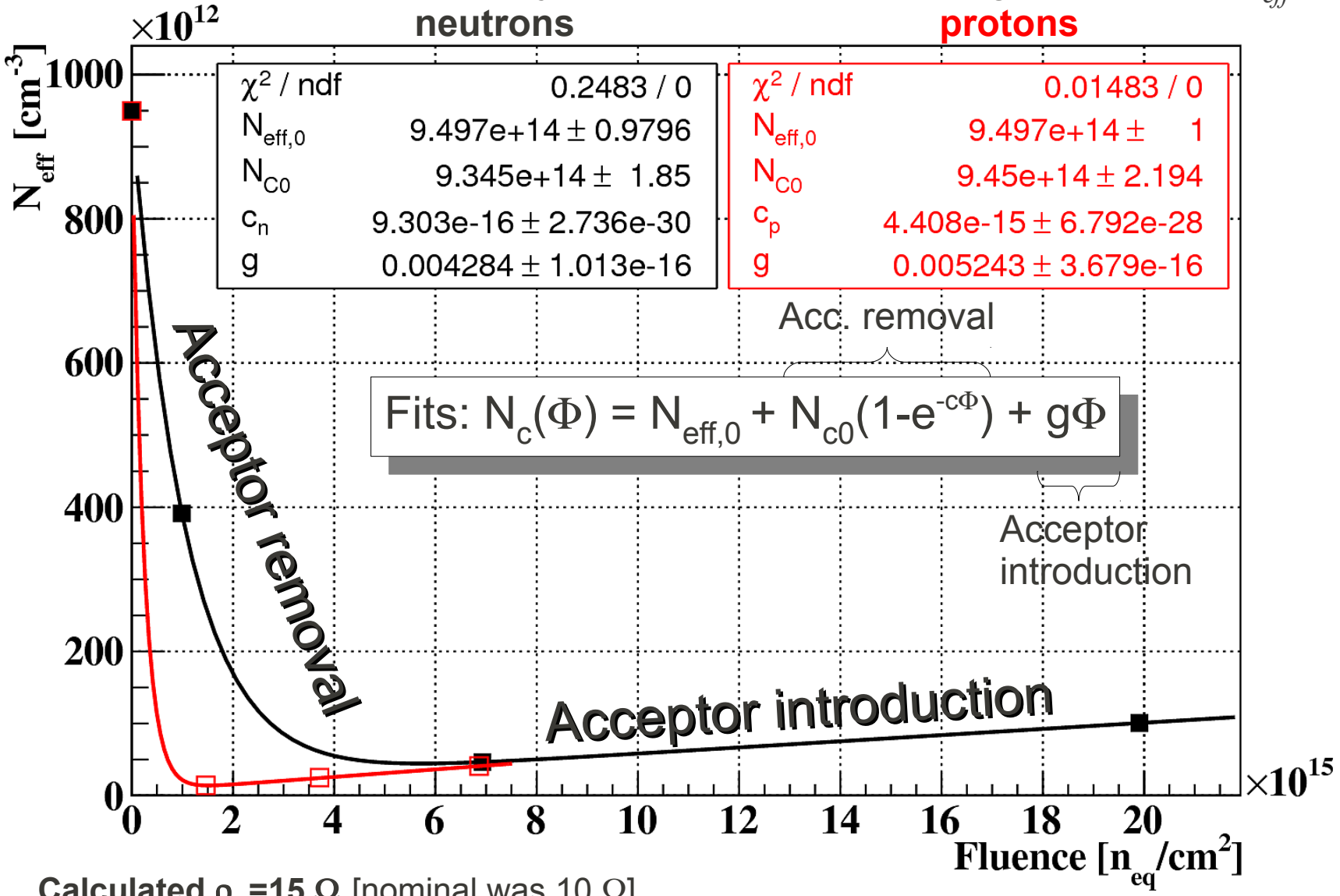


Charge of unirradiated at 80 V is **defined** as **1**

- **More charge** collected in **irradiated** detectors due to increased depletion depth
- Showing collected charge (at the center of the detector) in **5 ns**, over **200 µm**
- **Fluence range 1-1.5 $\times 10^{15}$ n_{eq}/cm^2,** very fast increase of collected charge

Space charge (neutrons and protons)

- Doping concentration: $N_{eff} = N_{donor} - N_{acceptor} \sim - N_{acceptor}$
- It can be estimated (abrupt junction) from width of charge profiles: $N_{eff} = \frac{2\epsilon\epsilon_0}{q \cdot FWHM^2} V$



Calculated ρ_0=15 Ω [nominal was 10 Ω]

Conclusions

Instituto de Física de Cantabria

• Growing surface of tracking systems, complexity of hybridization, cost of traditional hybrids, material budget... make monolithic solutions very attractive.
Large area+low cost → makes them excellent candidates to populate (outer strip) trackers

• Rad. hardness of vertex&tracker for ILC does not lead R&D.
Undepleted MAPS → slow
HVCMOS → Rad hard and fast (for ILC)

LC community can benefit from developments for HL-LHC

• HVCMOS ATLAS-collaboration demonstrated strip readout prototype
Strips mimicked daisy chaining "long pixels"
2D information by amplitude encoding

• HVCMOS radiation hardness tested until 2×10^{16} n_{eq}/cm^2
– Unexpected effect observed: acceptor removal
– For the first time observed, the collected charge bigger than unirradiated!
– Irradiation of low resistivity substrates seem to have benefitial effect in:
- Charge collection
- Depletion depth
– After 2×10^{16} n_{eq}/cm^2 detector performance very similar to unirradiated

BACKUP

HVCMOS

the deep n-well has two roles:
signal collecting region
substratefor PMOS transistors placed in it.

Usually the PMOS transistor substrate (n-well) is connected to the positive supply voltage which makes its potential stable. Here we cannot bias the n-well in this way because the signal charge would be absorbed by the positive supply. The n-well has to be ”floating” (biased using high resistance). Electrons collected by the n-well cause a small voltage drop in it. The n-well is coupled to the input of the pixel amplifier. The amplifier amplifies the signal and restores the original n-well voltage.

- Power for VTX and tracking will benefit from low duty cycle (power pulsing possible).

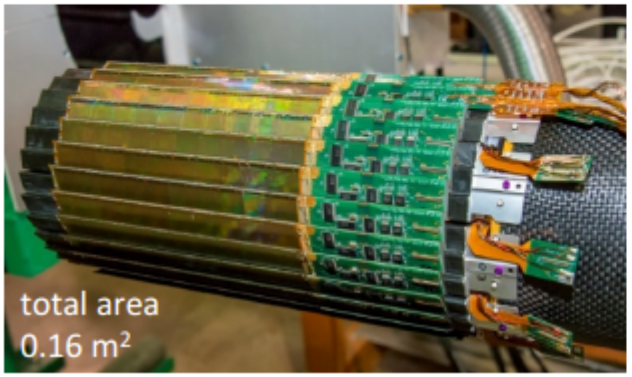
  Example: 130 μW/mm^2 barrel of SiD
  Air cooling envisaged (due to low mass needed for the system 0.15%X_0/layer)

(Semi)-Monolithic Pixel Detector Projects

universitätbonn

STAR / RHIC

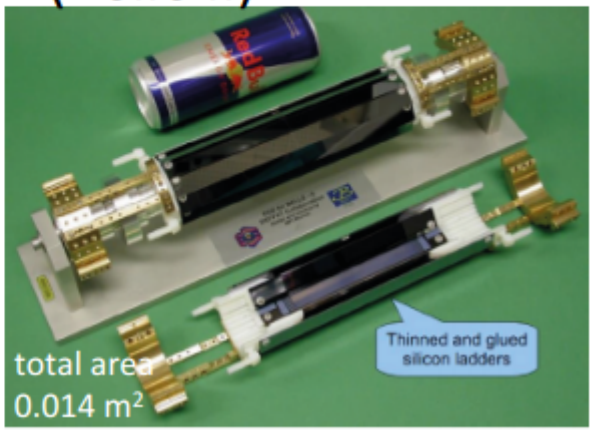
MAPS



in operation since 2014

(Belle II)

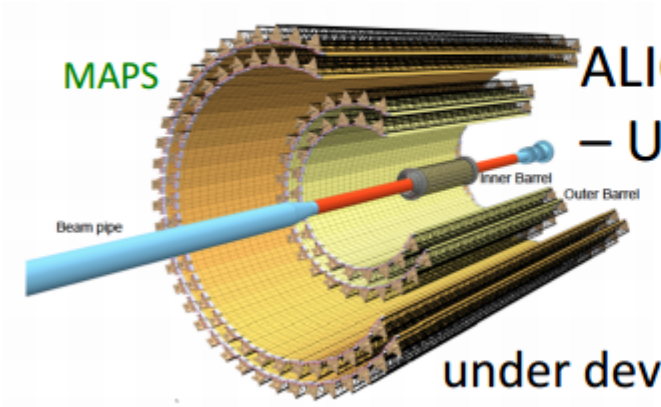
DEPFET



in production for 2017

ALICE – Upgrade

MAPS

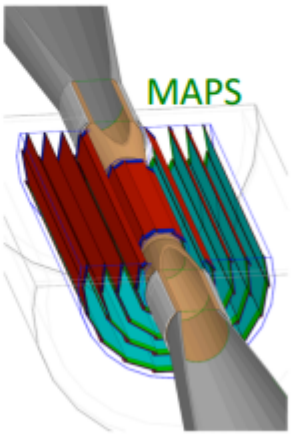


total area
~10 m²

under development
target: 2018

ILC

MAPS

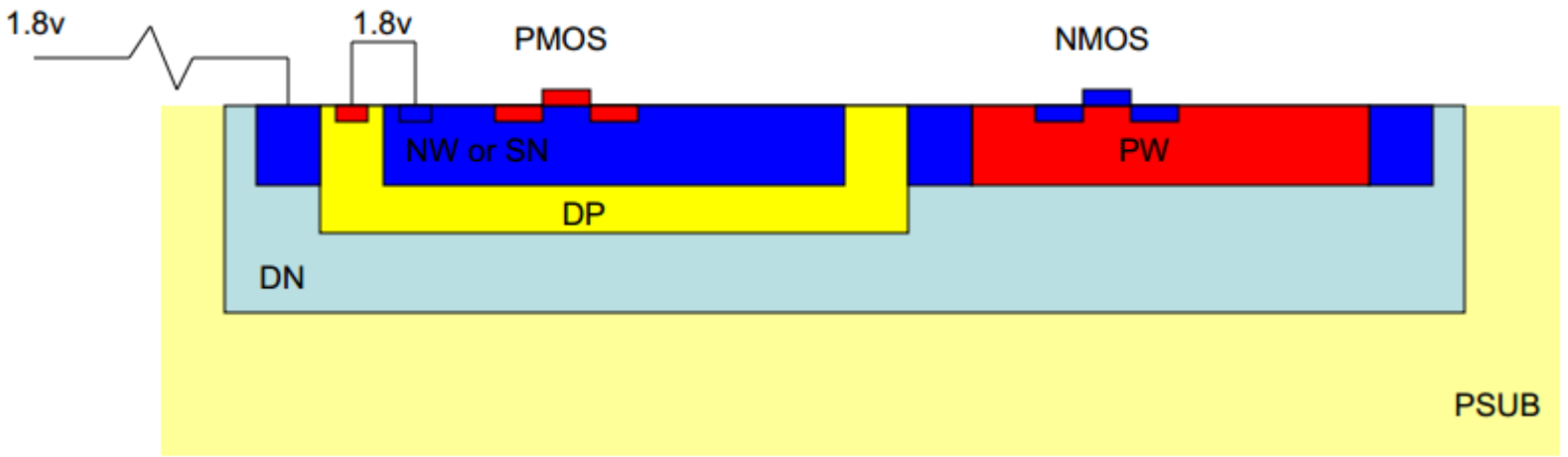


total area
? m²

current baseline

Technology issues – crosstalk

- Capacitive feedback into the sensor (n-well)
- Many important circuits do not cause problems: charge sensitive amplifier, simple shaper, tune DAC, SRAM but…
- "Active" (clocked) CMOS logic gates and sometimes comparators cause large crosstalk
- Possibility 1: Implement the circuits only using NMOST: effects on radiation tolerance, layout area, power consumption, etc.
- Possibility 2: Place the active digital circuits on the chip periphery or on separate chip.
- Possibility 3: Isolate PMOST from n-well using an additional standard technology feature – the deep P-well – we still haven't tested it…



SID Vertex requirements

ILC TDR, pg: 63 The time structure and low radiation background in the
ILC provides an environment which allows us to consider very light, low power detector structures. The bunch structure, with a 1 ms long bunch train at 5 Hz, enables power pulsing of the electronics, providing a power saving of a factor of 50-100 for front-end analog power. Goals:

• Hit resolution better then 5 μm in the barrel
• Less than 0.3% radiation length per layer. For a device with less than 0.3% radiation length per layer air cooling appears
to be the only viable low-mass sensor cooling technique
• Average power less than 130 μW/mm2 in the barrel
• Single bunch time resolution (¥ 300-700 ns)

These requirements then drive the design of the vertex system. The 5 μm resolution implies a pixel size of 17 μm, larger if charge sharing is used to improve the resolution. Some CMOS MAPS devices, which collect charge by diffusion rather than drift, can utilise larger pixels because diffusion naturally spreads the charge.

SID Vertex Baseline

the vertex detector for SiD is proposed to be an all-silicon structure in a barrel-disk geometry. The vertex barrel and inner endcaps have ~ 20 x 20 μm pixels. The pixel size increases to ~ 50 x 50 μm2 for the forward tracker disks. The total area of the vertex barrels is 1.63x 105 mm2 (1m2=1e6 mm2) and is 0.59◊105 mm2 for each set of 4 inner pixel disks and 1.96◊105 mm2 for each set of 3 forward pixel disks.

SID Sensor technology

3D integrated sensors and readout chips [66], Silicon-on-insulator (SOI) [67], Monolithic Active Pixels (MAPS) [68, 69], hybrid pixels [70, 71], and DEPFETs [72]. All of these technologies have the capability of delivering sensors less than 75 μm thick with 5 μm hit resolution and low power consumption.

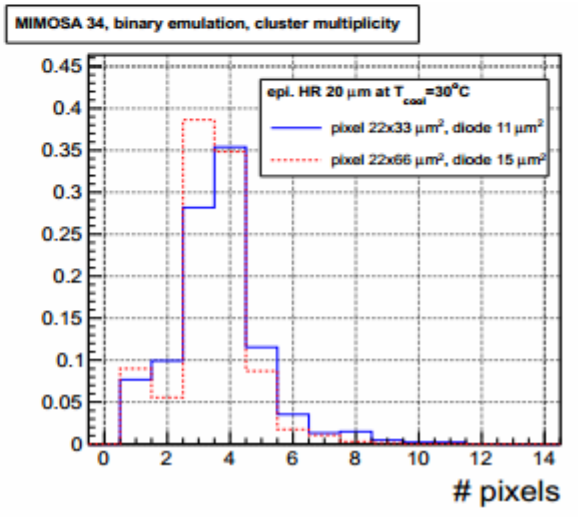
Comments on ILD Vertex Detector Requirements

- Expected N(hits)/cm^2/BX at 500 GeV & 1 TeV with anti-DID, for each ILD-VXD layer (DBD) :

Layer	1	2	3	4	5	6
0.5 TeV	6.3±1.8	4.0±1.2	0.25±0.11	0.21±0.09	0.05±0.03	0.04±0.03
1 TeV	11.8±1.0	7.5±0.7	0.43±0.13	0.36±0.11	0.09±0.04	0.08±0.04

- Occupancy in L1 and L2 :
  - L1 : 17 μm ×17 μm pixels (cluster mult. $\simeq$ 5)
    Pixel occ. at 500 GeV $\simeq 10^{-4}$/BX $\Rightarrow$ 10^{-2}/50 μs
  - L2 : 17 μm ×102 μm pixels (cluster mult. $\simeq$ 3)
    Pixel occ. at 500 GeV $\simeq 2\times10^{-4}$/BX $\Rightarrow$ 10^{-3}/2.5 μs
  - 1 TeV : twice higher occupancy
  - Luminosity upgrade : 4 times higher occupancy
  - Large uncertainties (MC stat., anti-DID uncertainty, etc.)

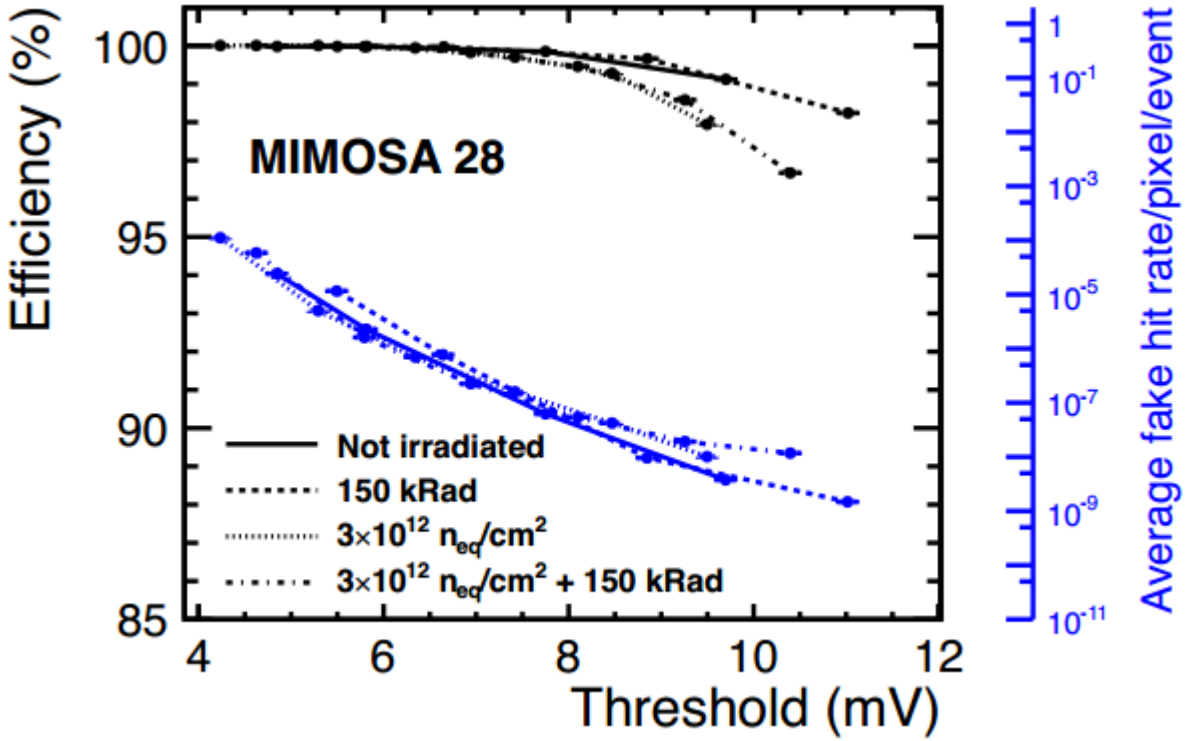
$\Rightarrow$ **Safety margins required on param. governing occupancy**



Submission Oct. 2015: AMS CMOS demonstrator chip (CCPD) in 350 nmtechnology (different waferresisJviJes: 20 – 1000 Ωcm) received back: End of 2015

The vertex detector is realised as a multi-layer pixel-vertex detector (VTX), with three super-layers
each comprising two layers, or a 5 layer geometry. Whilst the underlying detector technology has not yet been decided, the VTX is optimised for point resolution and minimum material thickness.
A system of silicon strip and pixel detectors surrounds the VTX detector. In the barrel, two layers of silicon strip detectors (SIT) are arranged to bridge the gap between the VTX and the TPC.
In the forward region, a system of two silicon-pixel disks and five silicon-strip disks (FTD) provides low angle tracking coverage. A distinct feature of ILD is a large volume time projection chamber (TPC) with up to 224 points per track.
Outside the TPC a system of Si-strip detectors, one behind the end-plate of the TPC (ETD) and one in between the TPC and the ECAL (SET), provide additional high precision space points

The required radiation tolerance follows entirely from the beam related background (i.e. beamstrahlung) (see section5.5.6), which is expected to affect predominantly the innermost layer. The requirements for the total ionising dose and the fluence amount respectively to about 1kGy and 10^11 neq/cm2 per annum.



Measured variations of the m.i.p. detection efficiency and fake hit rate (fraction of pixel noise fluctuations above threshold) of the STAR sensor as a function of the discriminator threshold, before and after irradiation (150kRad,3x1e12 neq/cm2) at a coolant temperature of 30C.

Fpg. 205: TD using CMOS pixelated strips could avoid stereo-angle modules (radial resolution of O(100 μm)). To achieve a precise measurement of the longitudinal impact parameter the radial segmentation of the innermost disks is crucial. Due to their higher occupancy, the first two disks are implemented using highly granular pixel detectors. three technologies are under consideration: CPS, CCD and DEPFET.
With the current design one disk of the FTD strip system will use less than 200 W of power during electronics-on time, or less than 40 W on average.