

Status of the readout electronics for the Silicon micro-strip detector of the ILD concept

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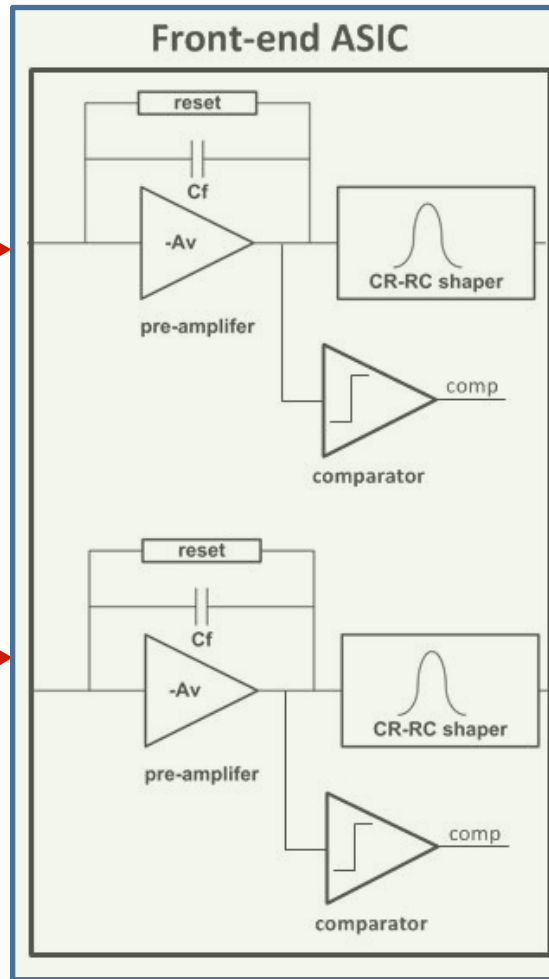
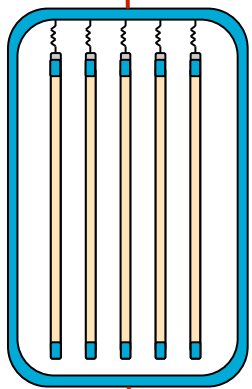
Outline

- Starting point
- Front-end ASIC
 - Noise analysis
 - CSA
 - CSA + Shaper
 - ASIC
- Test plan
- Conclusions

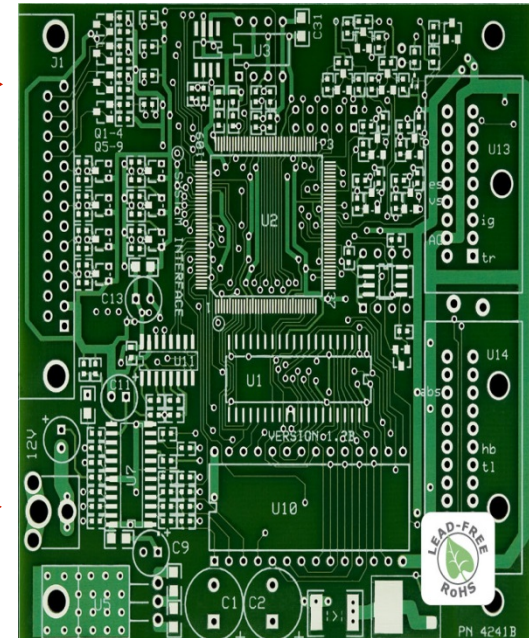
Starting point

μ strips

- Standard
- Resistive
- Gain



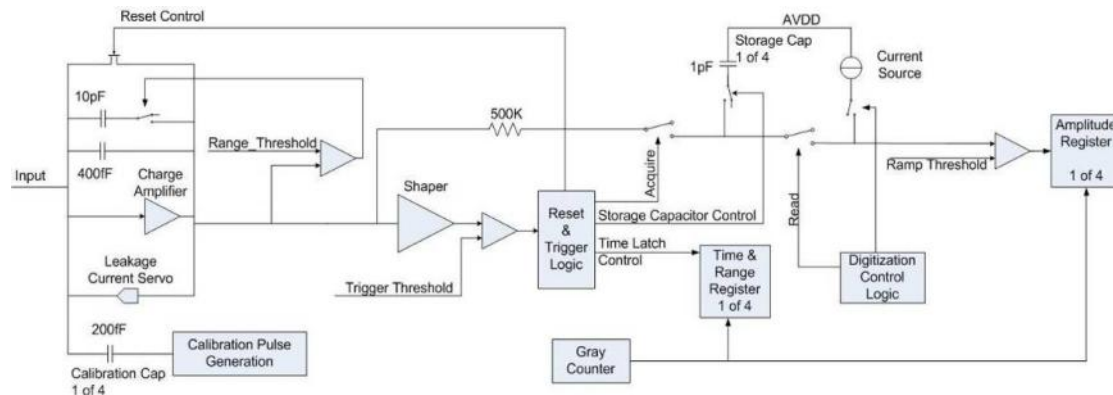
Digitalization



To DAQ

KPiX ASIC: generic R&D toward system-on-chip designs

- 32×32 array = 1024 channels
- Designed to be
 - bump-bonded to a Si sensor, or
 - bumped to a hybrid for large area detectors (RPC's, GEM's, etc)



Block diagram of a single channel

For each channel of the system-on-chip

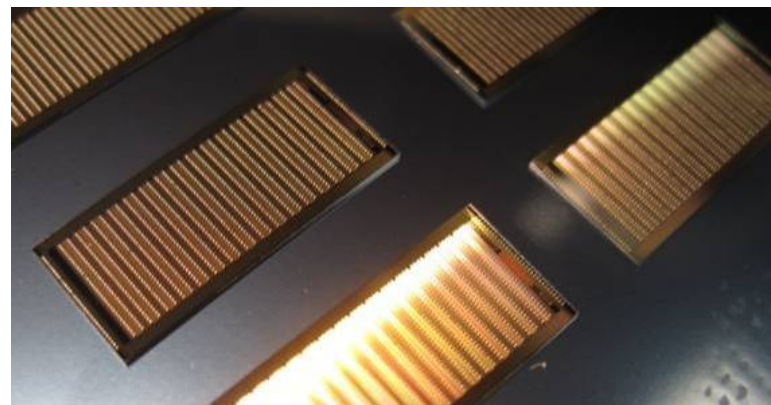
- » 4 samples per train with individual timestamps
- » auto-triggering
- » internal per-channel 13-bit ADC
- » automatic range switching for large charge depositions (10pC)
- » bias current servo for DC coupled sensors
- » power cycling: power down during inter-train gaps (20 uW avg for ILC time structure)
- » built-in calibration
- » nearest neighbor trigger ability
- » high-gain feedback capacitor for tracker application
- » dual polarity for GEM and RPC applications
- » external trigger for test beam

Digital IP core with serial data IO (only 4 signals)

0.25µm TSMC

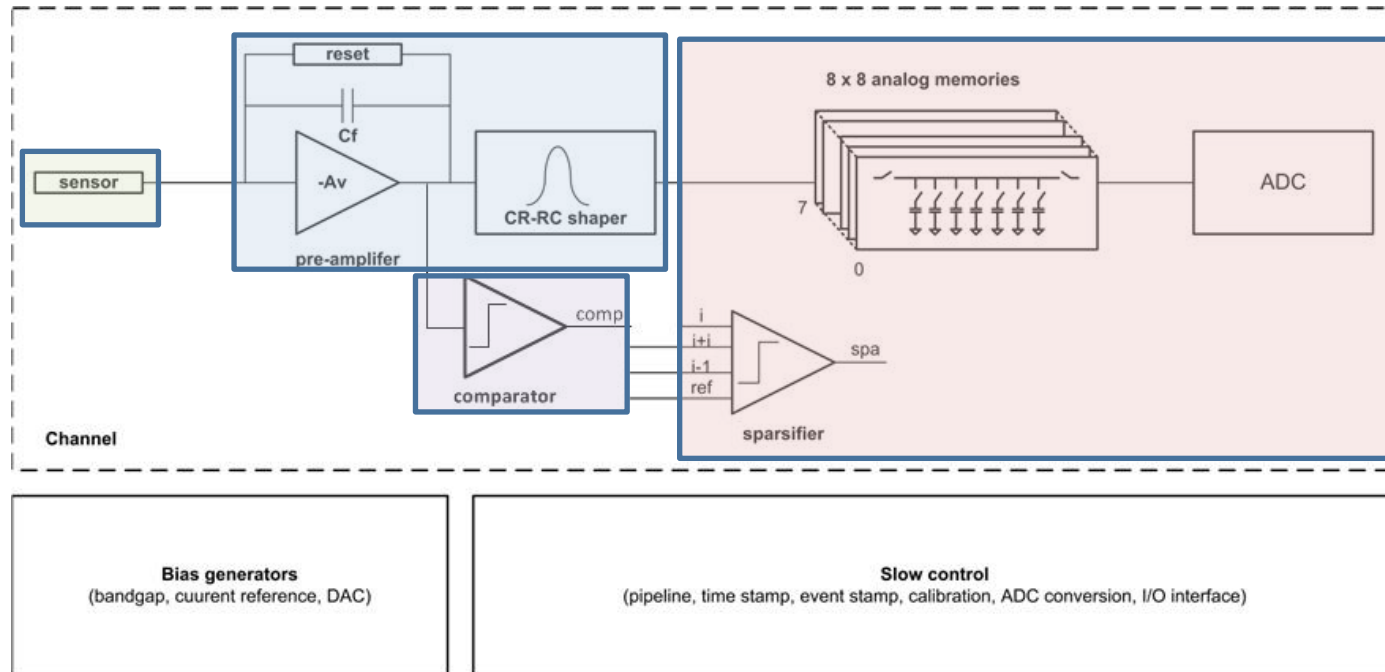
Collaboration: SLAC, UCSC, U. of Oregon, UC Davis

KPiX, An Array of Self Triggered Charge Sensitive Cells Generating Digital Time and Amplitude Information, D. Freytag, G. Haller, et al. SLAC-PUB-13462, 2008. 4pp (IEEE NSS Oct 2008)
KPiX, an 1,024 cell ASIC, Design and Performance, accepted for presentation at NSS 2012



1024-channel KPiX

Front-end ASIC



- In progress
- To be designed
- Not included
- Sent to foundry

Front-end ASIC: Noise analysis (1)

$$ENC \approx (C_d + C_f + C_i) \cdot \sqrt{\frac{2}{3}kT \frac{1}{g_m} 1.57 \frac{e^2}{\pi q_e^2 \tau} + \frac{k_f}{C_{ox}^2 \cdot WL} \frac{e^2}{2q_e^2}}$$

EKV model

$$g_m = \frac{I_{ds}}{2nU_t} \cdot \frac{1 - e^{-\sqrt{IF}}}{\sqrt{IF}}$$

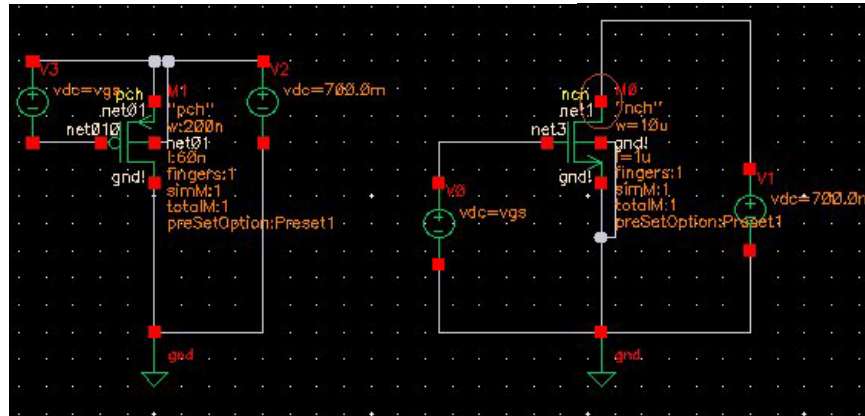
$$IF = \frac{I_{ds} \cdot L}{I_s^* \cdot W}$$

$$\lambda_E = \lambda \cdot L = \frac{I_{ds} \cdot L}{g_{ds}}$$

$$k_n = 2m^2 \cdot \frac{L}{W}$$

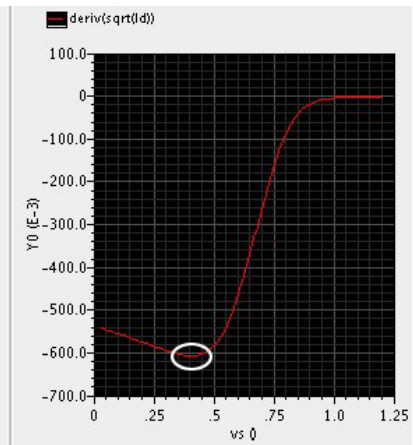
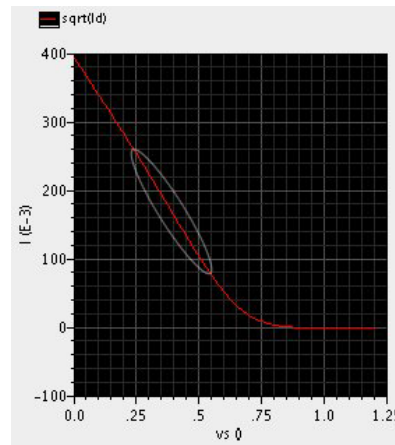
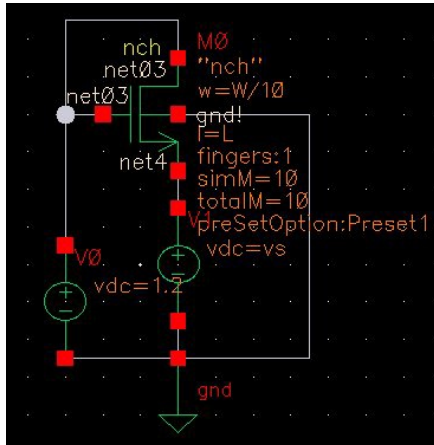
$$I_s^* = \left(-2 \cdot U_t \cdot \frac{d\sqrt{I_d}}{dV_s \text{ min}} \right)^2 \cdot \frac{L}{W}$$

$$n = \frac{I_s^*}{2 \cdot k_n \cdot U_t^2}$$



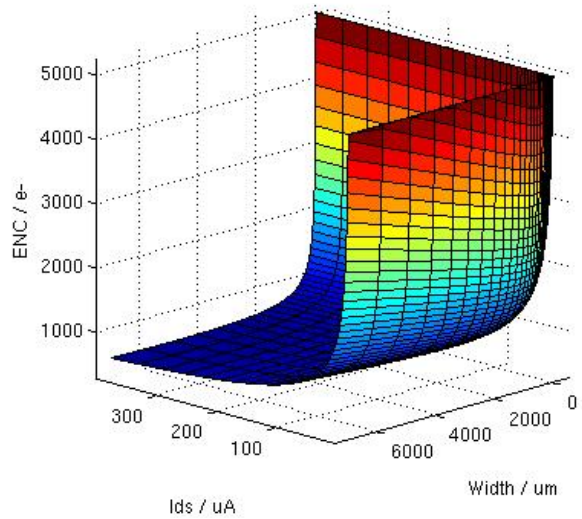
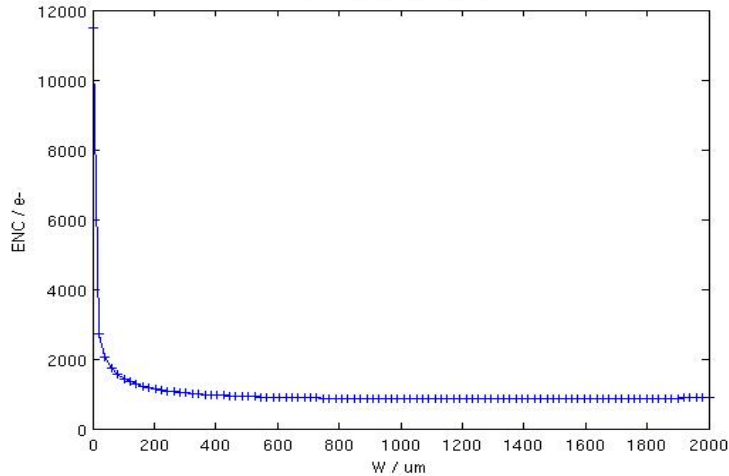
$K_p = 30.65 \mu\text{A}/\text{V}^2$
 $K_n = 141.10 \mu\text{A}/\text{V}^2$
 Values of I_s^* and λ_e are tabulated.

($I_s^* p = 95 \text{ nA}$; $I_s^* n = 420 \text{ nA}$)



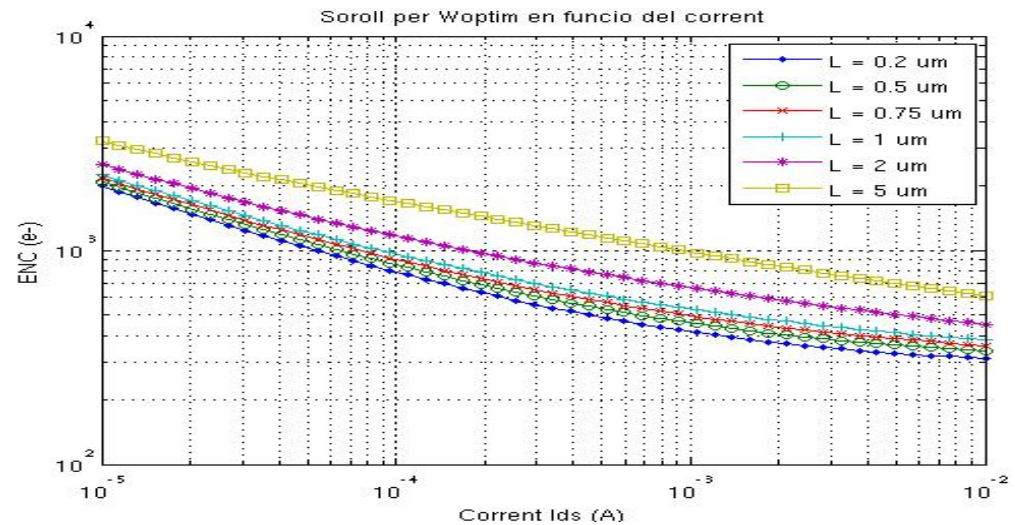
CSA: Input PMOS

Optimum width for a given L and Ids



L	Id _s	a	b	ENC 20pF	W _{optima}	Consum	IF
0.20 μm	100 μA	134e ⁻	32.8e ⁻	791e ⁻	2737 μm	120 μW	0.06
0.20 μm	200 μA	132e ⁻	24.8e ⁻	629e ⁻	3657 μm	240 μW	0.10
0.20 μm	300 μA	131e ⁻	21.3e ⁻	557e ⁻	4307 μm	360 μW	0.12
0.20 μm	500 μA	131e ⁻	17.8e ⁻	486e ⁻	5248 μm	600 μW	0.17
0.50 μm	100 μA	155e ⁻	35.0e ⁻	855e ⁻	1199 μm	120 μW	0.45
0.50 μm	200 μA	150e ⁻	26.7e ⁻	685e ⁻	1558 μm	240 μW	0.69
0.50 μm	300 μA	148e ⁻	23.1e ⁻	609e ⁻	1806 μm	360 μW	0.90
0.50 μm	500 μA	147e ⁻	19.4e ⁻	534e ⁻	2158 μm	600 μW	1.25
0.75 μm	100 μA	174e ⁻	36.7e ⁻	908e ⁻	860 μm	120 μW	0.96
0.75 μm	200 μA	167e ⁻	28.3e ⁻	732e ⁻	1097 μm	240 μW	1.51
0.75 μm	300 μA	164e ⁻	24.5e ⁻	653e ⁻	1258 μm	360 μW	1.98
0.75 μm	500 μA	161e ⁻	20.7e ⁻	574e ⁻	1482 μm	600 μW	2.80
1.00 μm	100 μA	193e ⁻	38.4e ⁻	960e ⁻	690 μm	120 μW	1.61
1.00 μm	200 μA	184e ⁻	29.8e ⁻	779e ⁻	867 μm	240 μW	2.56
1.00 μm	300 μA	180e ⁻	25.9e ⁻	698e ⁻	984 μm	360 μW	3.39
1.00 μm	500 μA	176e ⁻	22.0e ⁻	615e ⁻	1143 μm	600 μW	4.86

$$ENC \sim a + b \cdot Cd$$



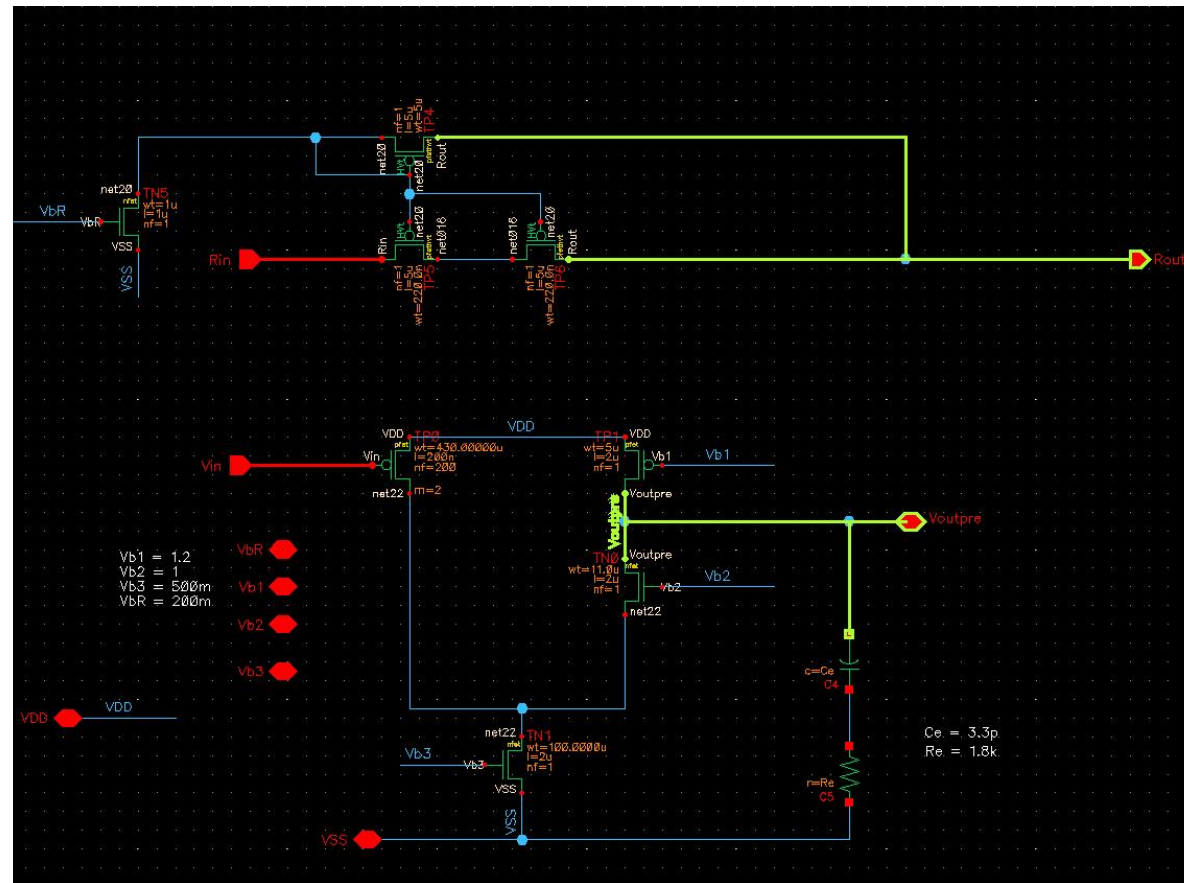
$$ENC = \sqrt{\frac{2}{3} kT \frac{1}{g_m} 1.57 \frac{C_t^2 e^2}{\pi q^2 \tau} + \frac{K_f}{C_{ox}^2 WL} \frac{C_t^2 e^2}{2q^2} + I_{leak} 1.57 \frac{e^2 \tau}{2\pi q} + \frac{kT}{R} 1.57 \frac{e^2 \tau}{\pi q^2}}$$

Hans-Günther Moser, "Silicon detector systems in high energy physics", 2009

Front-end ASIC: CSA

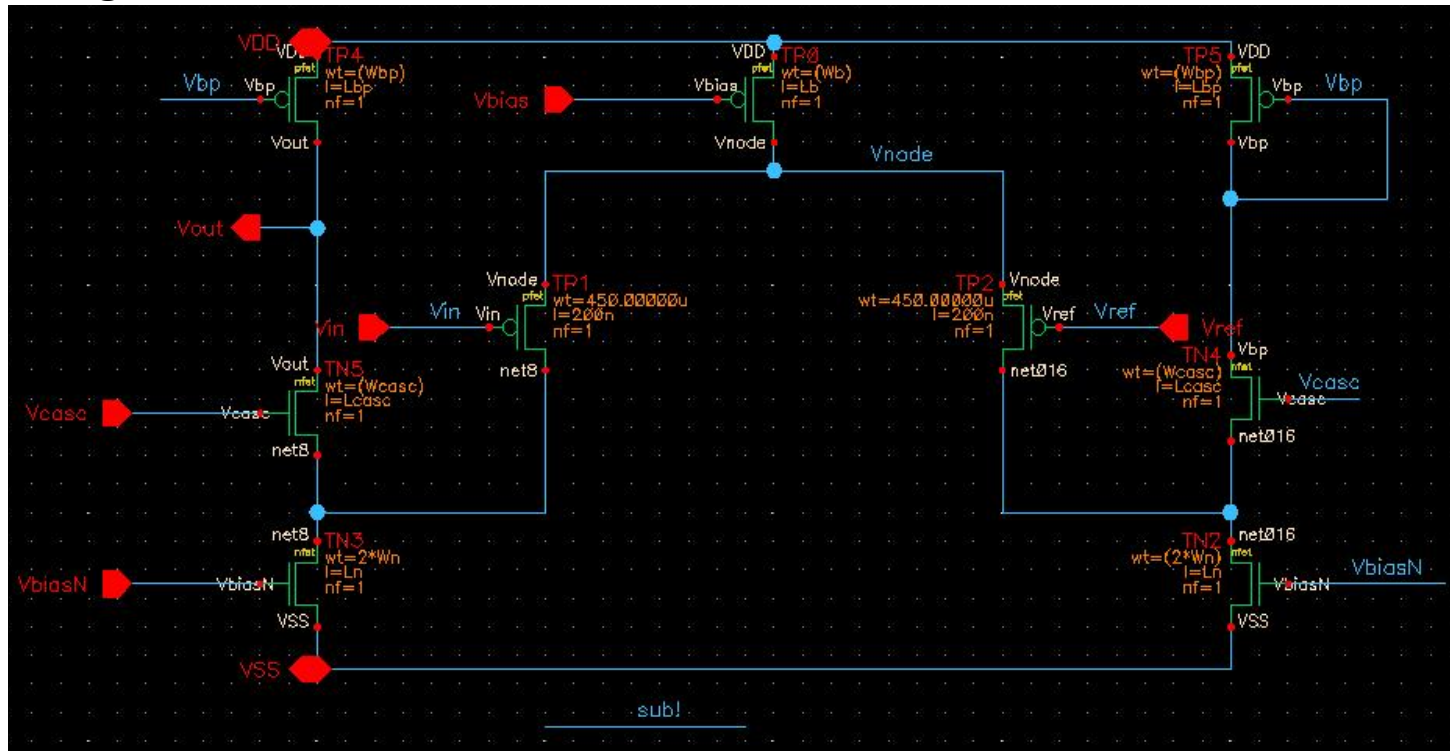
Pre-Amp design in AMS 180 nm

- Power supply: 1.8 V
- Power consumption < 120 μ W
- Scale: 40 MIP (1 MIP = 24000 e⁻)
- Amplifier:
 - Gain \sim 67,5 dB
 - GBW \sim 19,5 MHz
 - PM \sim 63 $^\circ$
- Main noise contribution of the circuit.
- Equivalent Noise Charge: ENC = a + b C_d (where C_d is the capacitor of the detector)
- Optimum L and I_{bias} to maintain the noise below 500 e⁻



Front-end ASIC: CSA differential

Pre-Amp design in AMS 180 nm



- Power supply: 1.8 V
- Power consumption: higher
- Scale: 100 MIP

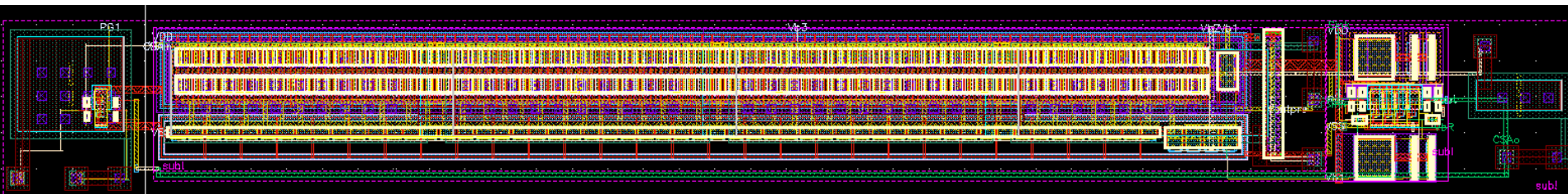
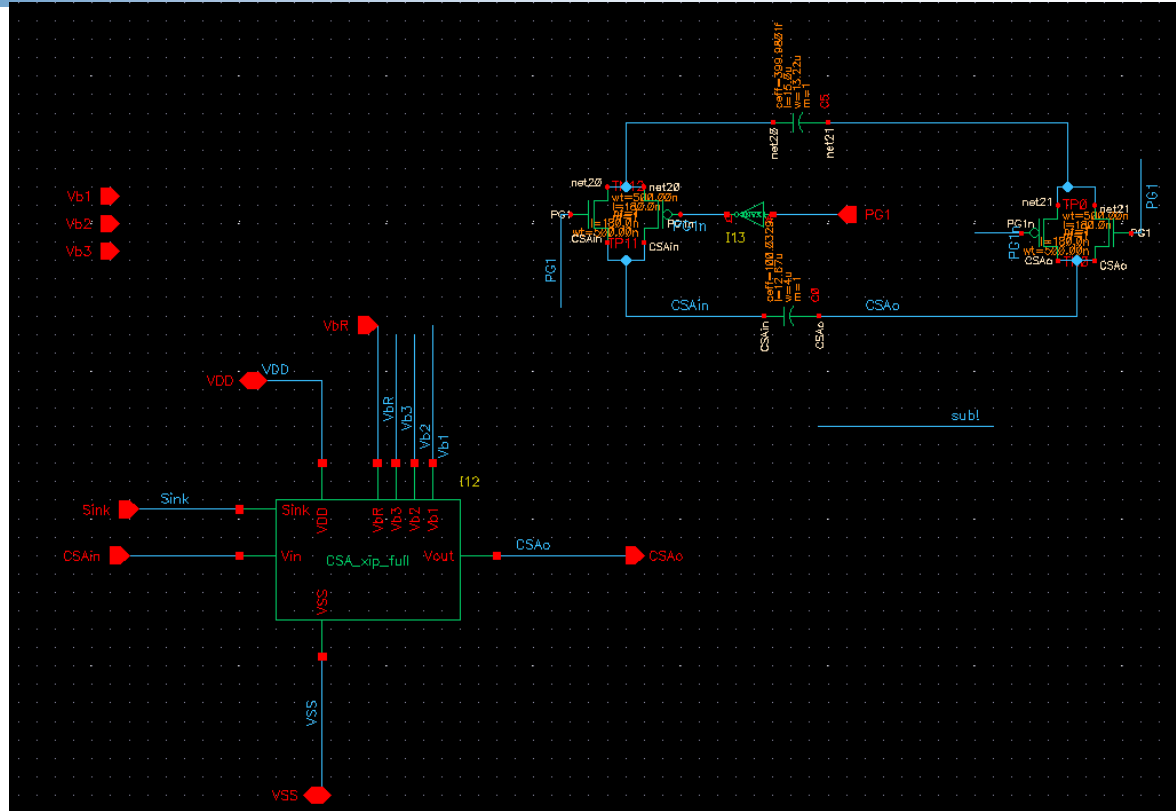
- Amplifier:

- Gain ~ 69 dB
- GBW ~ 79,5 MHz
- PM ~ 68°

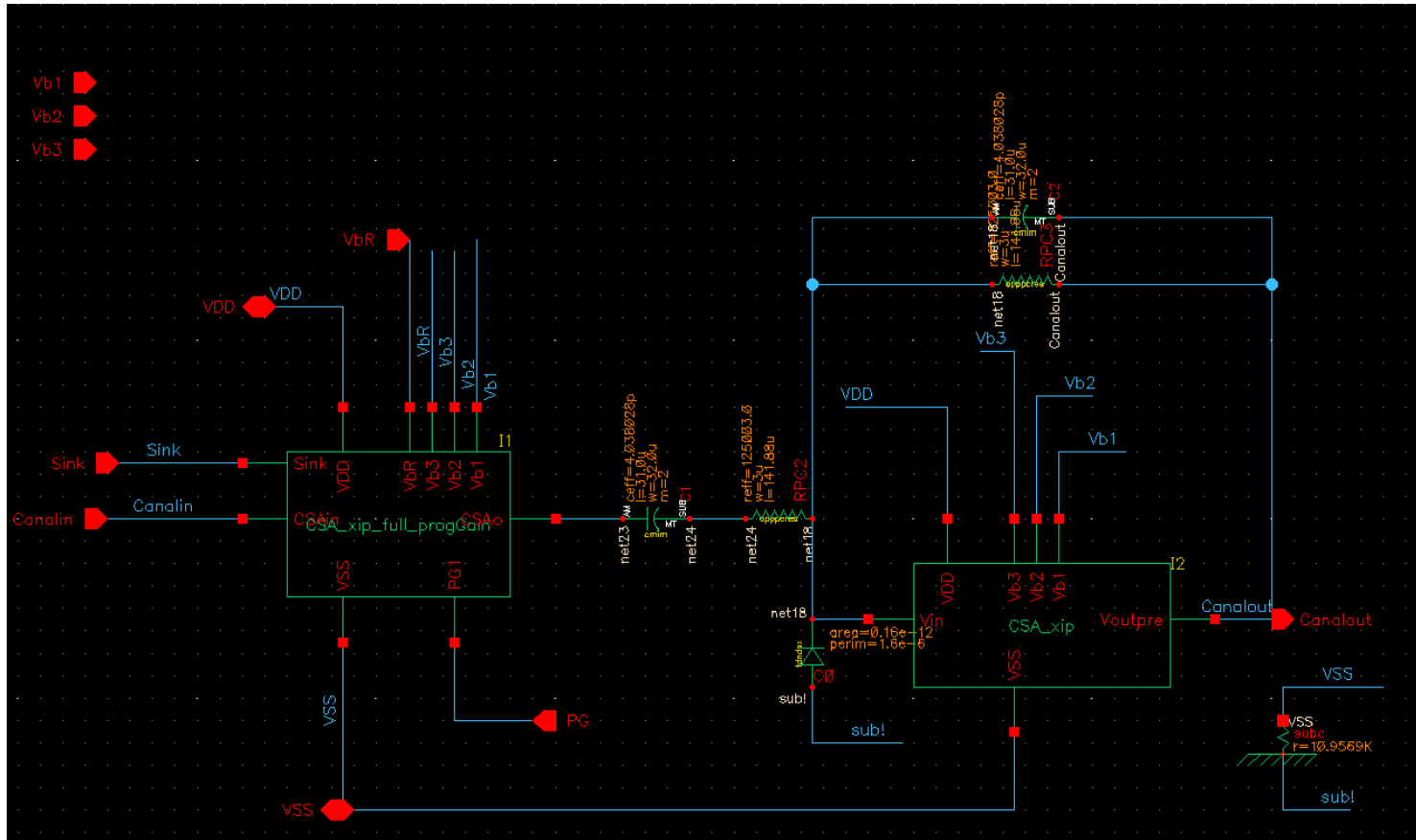
Front-end ASIC: CSA

Pre-Amp design in AMS 180 nm

- Programmable gain to reduce noise.
- Scale: 40 MIP (1 MIP = 24000 e-)
 - Gain 1: from 1 to 10 MIPs
 - Gain 2: from 10 up to 40 MIPs
- Layout: 220 μm x 25 μm

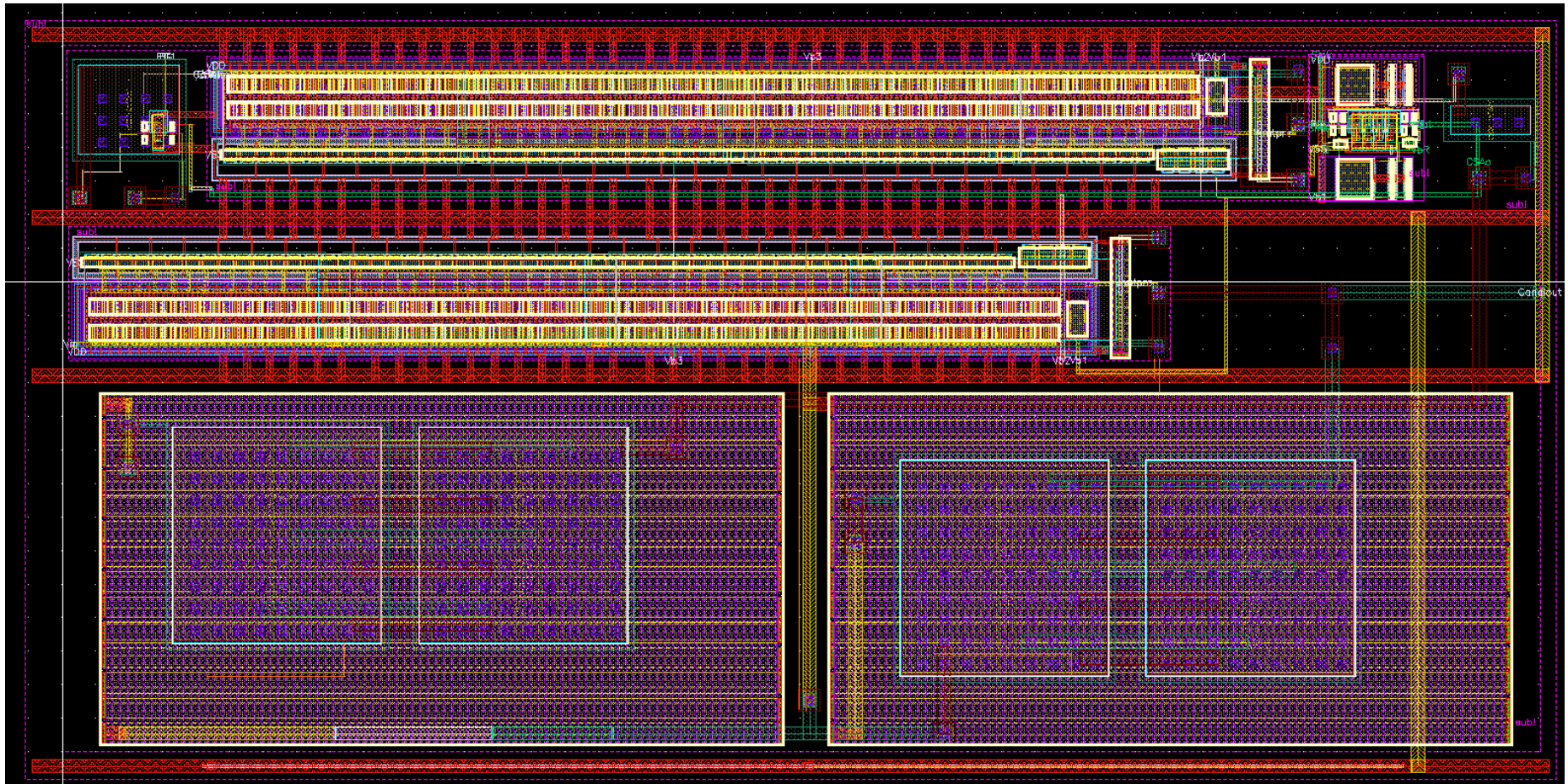


Front-end ASIC: CSA + Shaper



- No programmable shaping time
- 1 us shaping time

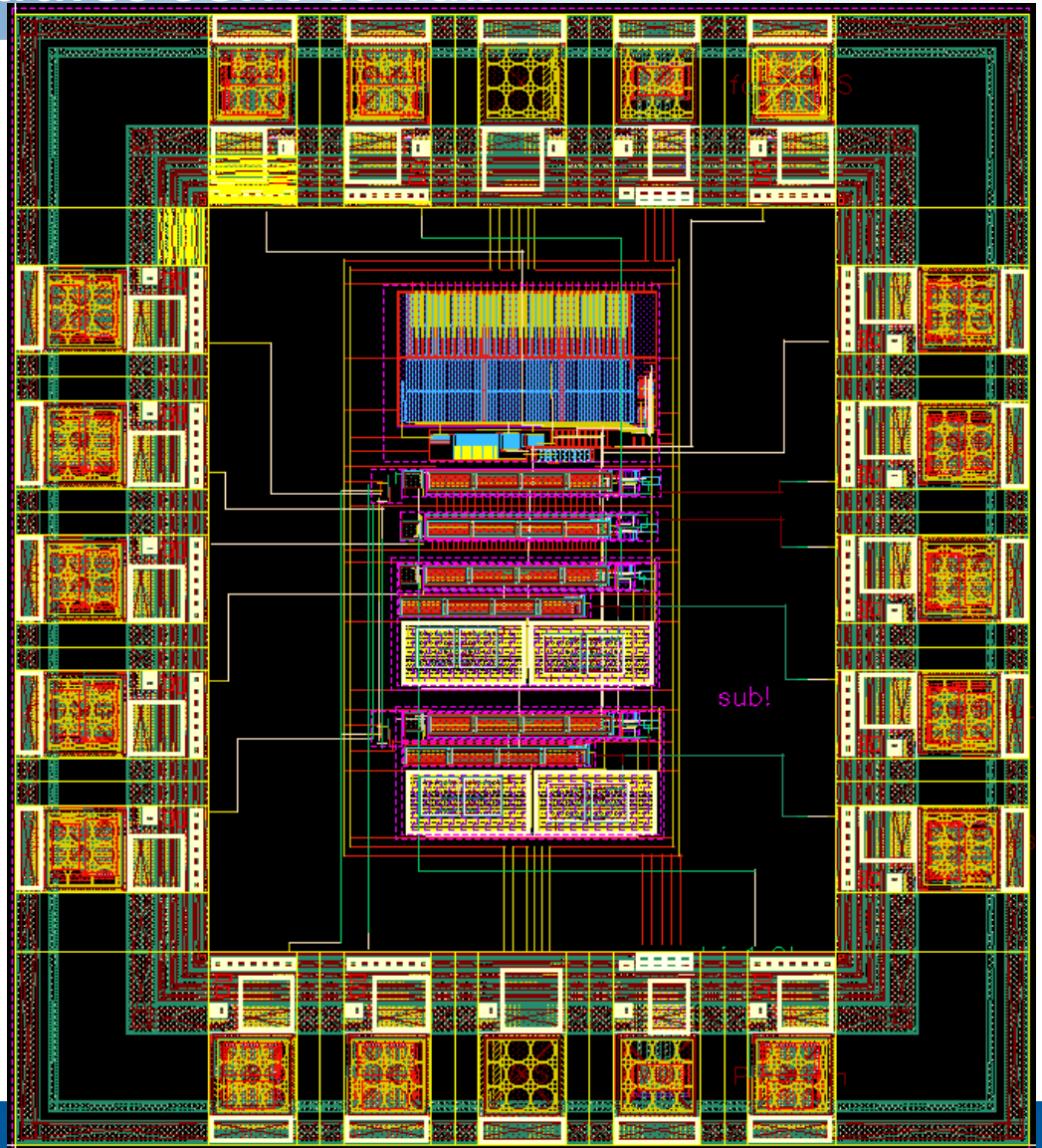
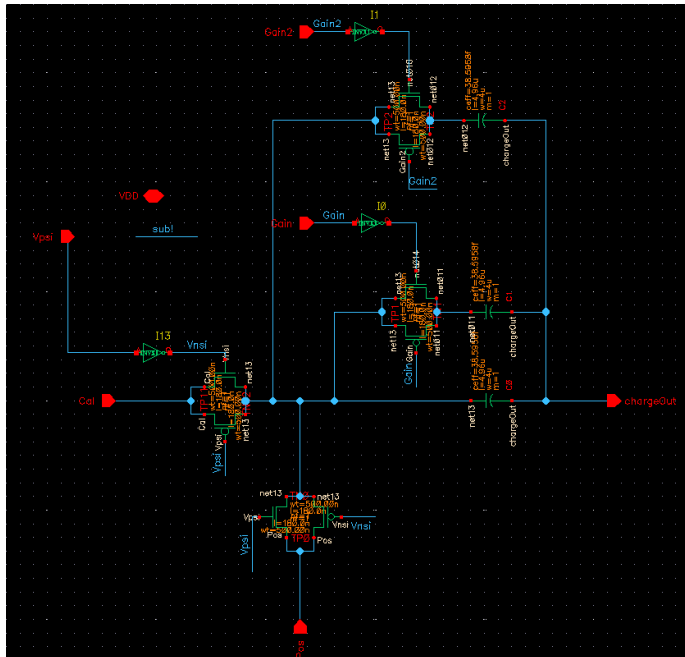
Front-end ASIC: CSA + Shaper



- 228 um x 112 um

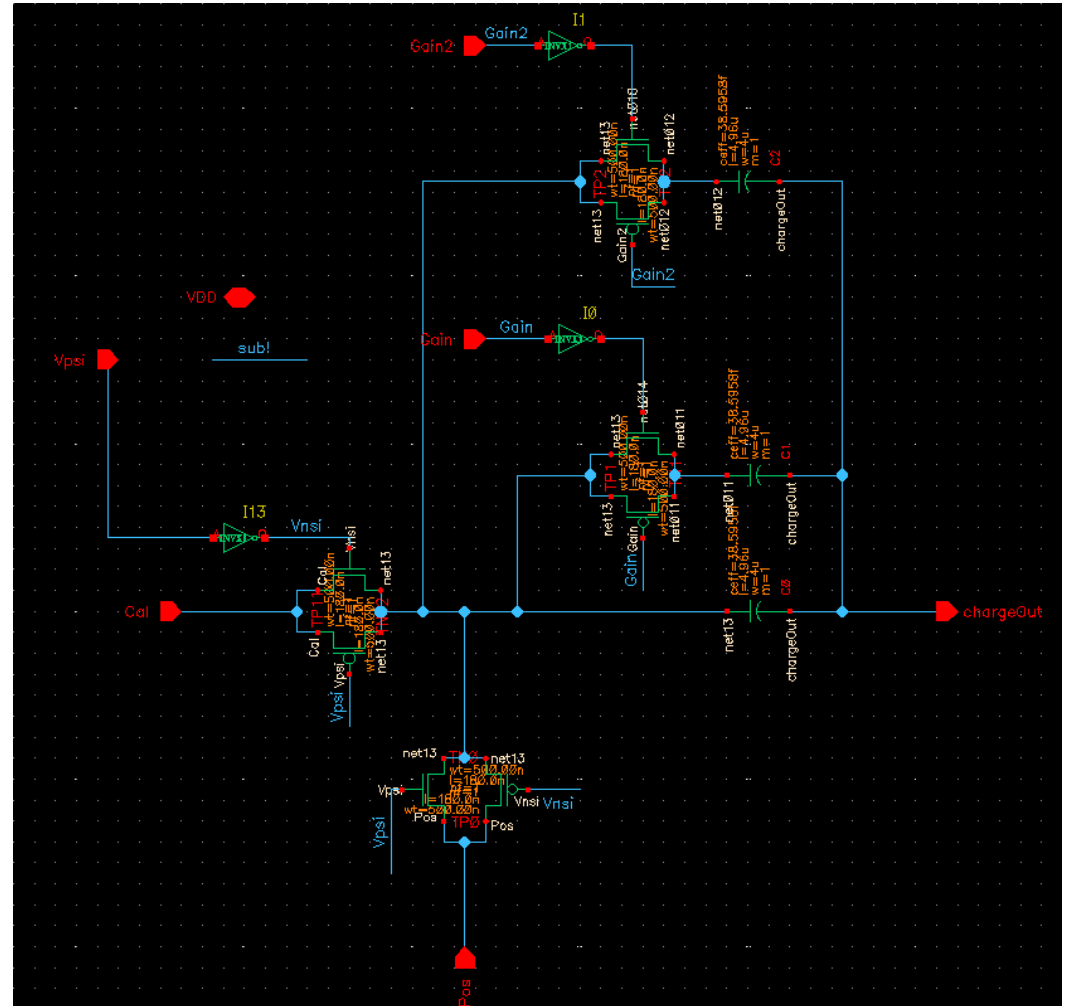
Front-end ASIC: Modules sent to fab

- 1 BIAS module
- 1 CSA
- 1 CSA + Shaper (channel)
- For test purposes:
 - 1 CSA + Charge Injection
 - 1 Channel + Charge Injection
- Size: 867 μm x 960 μm



Test plan: Calibration

- $Q_{cal} = C_{cal} * (V_{pos} - V_{cal})$
- C_{cal} :
 - 38.6 fF
 - 38.6 * 2 fF
 - 38.6 * 3 fF
- $V_{cal} = [1.8 \text{ V to } 0 \text{ V}]$
- $Q_{cal} = [0 \text{ fC to } 208.44 \text{ fC}]$
- 1 MIP $\sim 24000 \text{ e} \Rightarrow 3.86 \text{ fC}$



E. Beuville et al., "High Performance, Low-Noise, 128-Channel Readout Integrated Circuit for Flat Panel X-ray Detector Systems"

Test plan

- Test BIAS system
- Test of CSA + Charge Injection:
 - Test correct behavior of CSA
 - Find ENC at low gain
 - Find ENC at high gain
 - Dispersion from chip to chip
- Test of Channel + Charge Injection
 - Test correct behavior of the channel
 - Find ENC at the output of the shaper
 - Is shaping time correct ?
 - Dispersion from chip to chip
- Test with real sensors.

Conclusions

- **CSA can work with “source” or “sink” sensors.**
- **Similar noise but less power consumption than the work performed with TSMC 65 nm.**
- **For each switch noise increases, ENC with full gain near to 950 e.**
- **Study and design of a fast comparator. Has to be tested together with the resistive microstrip model.**
- **Need to adapt to DC sensors**