XII MEETING OF THE SPANISH NETWORK FOR FUTURE LINEAR COLLIDERS

DEPFET ACTIVE PIXEL DETECTOR

LC GROUP @ IFIC VALENCIA

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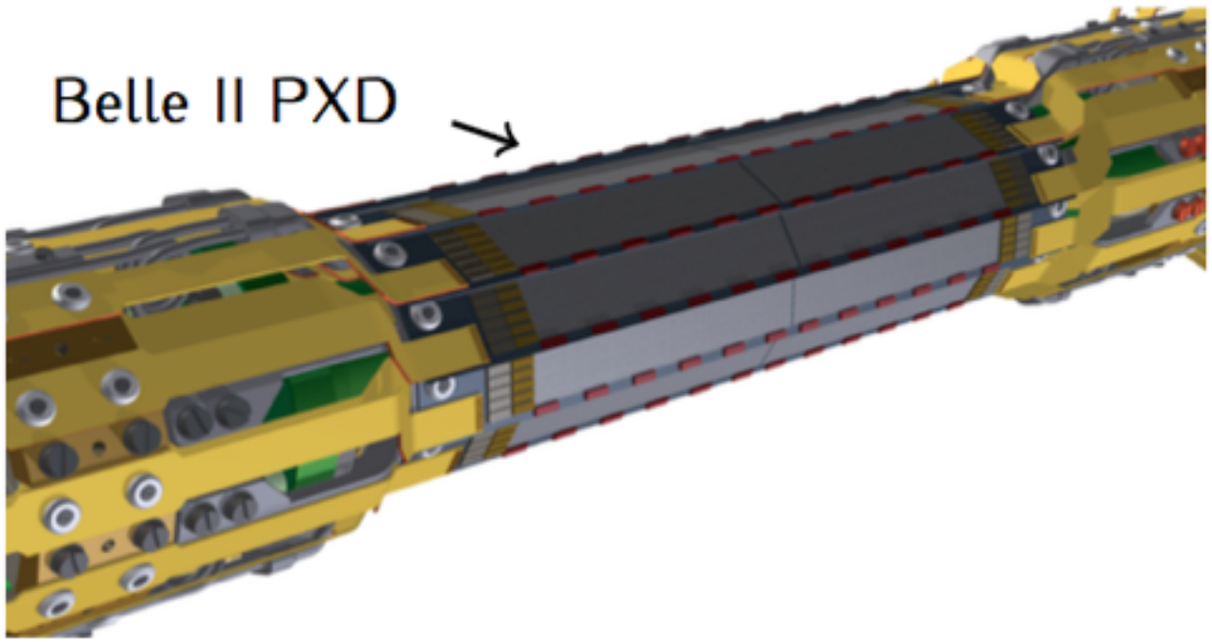
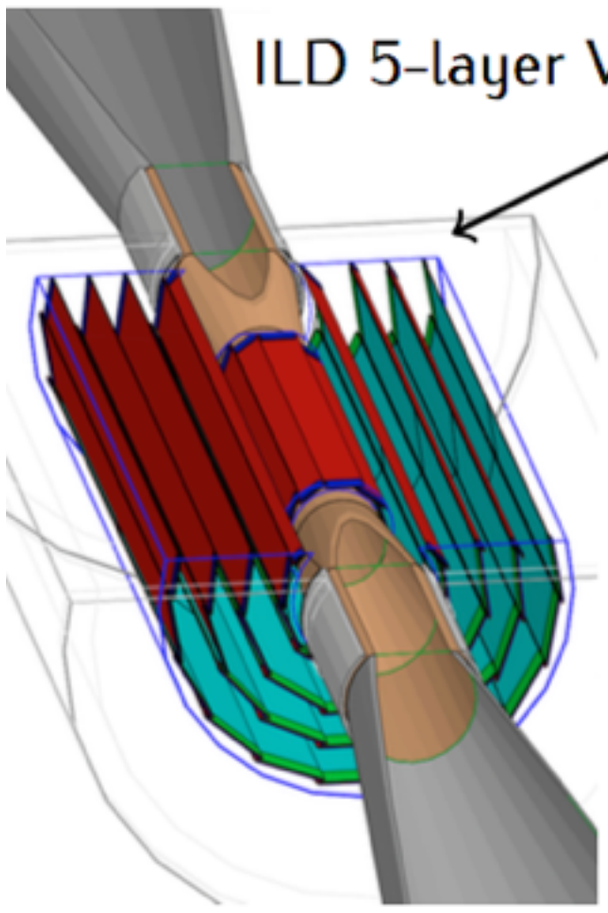
INTRODUCTION TO DEPFET PIXEL DETECTORS

The DEpleted P-channel Field Effect Transistor (or DEPFET) technology is one of the strongest candidates to be used as vertex detectors in the future accelerators due to its detection and amplification properties.

- It's the baseline pixel detector for Belle II at SuperKEKB.
- It's one of the strongest candidates for the ILD VXD at ILC.





	Belle II	ILD LOI 5-layer layout	
Radii	14,22	15, 26, 38, 49, 60	mm
Ladder length	90(L1), 122(L2)	123(L1), 250(L2-L5)	mm
Sensitive width	12.5(L1-L2)	13(L1), 22(L2-L5)	mm
Number of ladders	8, 12	8, 8, 12, 16, 20	
Pixel Size	50x50(L1), 50X75(L2)	20x20(L1-L5)	μm^2
Frame rate	50	20(L1), 4(L1-L5)	kHz

DEPFET PXD: VXD REQUIREMENTS

The requirements for both vertex detectors are quite similar. The DEPFET prototypes designed for the Belle II experiment are almost prototypes for the layers 1 and 2 of the ILD VXD.

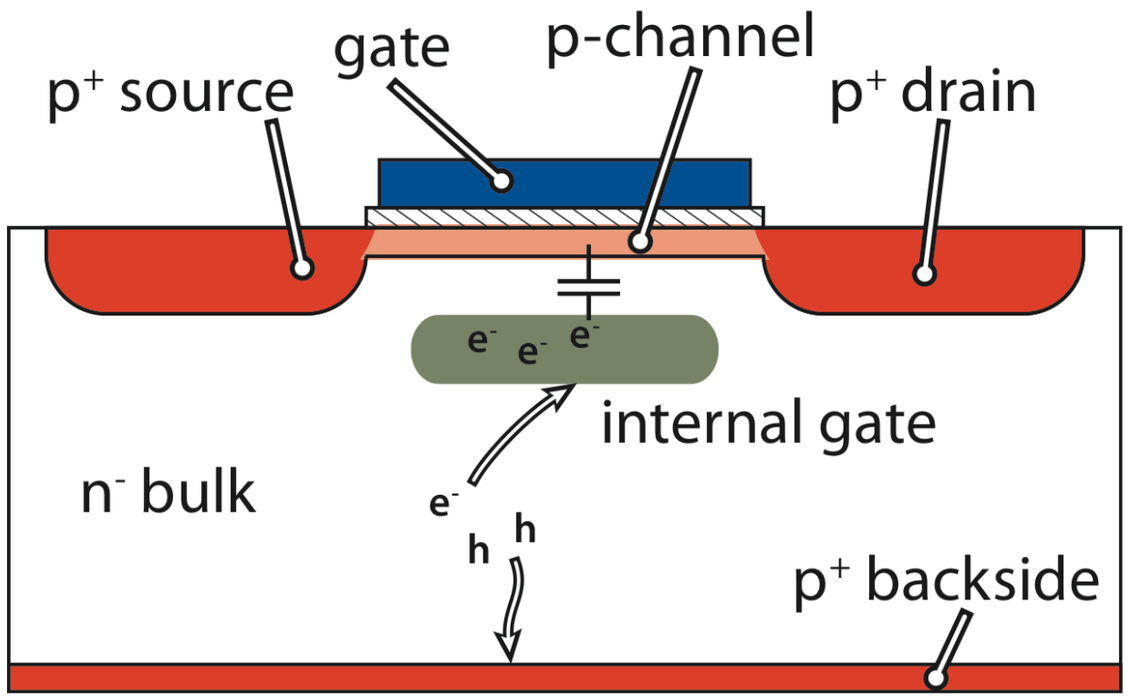
	Belle II	ILC
Occupancy	0.4 hits/μm^2/s	0.13 hits/μm^2/s
Radiation	2 Mrad/year	< 100 krad/year
Duty cycle	1	1/200
Frame time	20 μs (cont r.o. mode)	25-100 μs
Momentum range	Low momentum (<1GeV)	All momenta
Acceptance	17º-155º	6º-174º
Material budget	0.21% X_0 per layer	0.12% X_0 per layer
Resolution	15 μm (50x75 μm^2)	5 μm (20x20 μm^2)

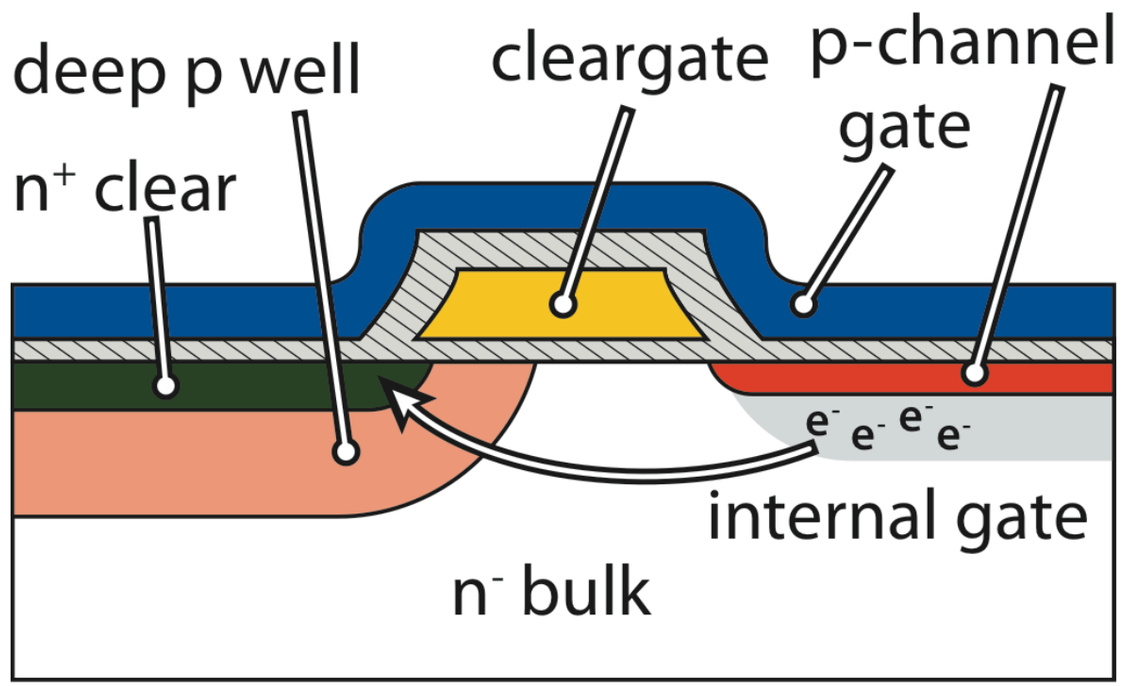
DEPFET PXD: PIXEL FUNDAMENTALS

- Each pixel consists of a p-channel FET integrated in a completely depleted bulk.
- The substrate is a n-type silicon bulk with a p^+ backside contact. With an additional n-doped implantation under the FET a potential minimum for the electrons is created under the FET gate (internal gate).
- The electrons created by the impinging particles gather in the internal gate, then the drain current in the FET is proportional to the electrons in the internal gate. This feature implies an internal amplification (g_q). This kind of measurement benefit from small intrinsic noise.

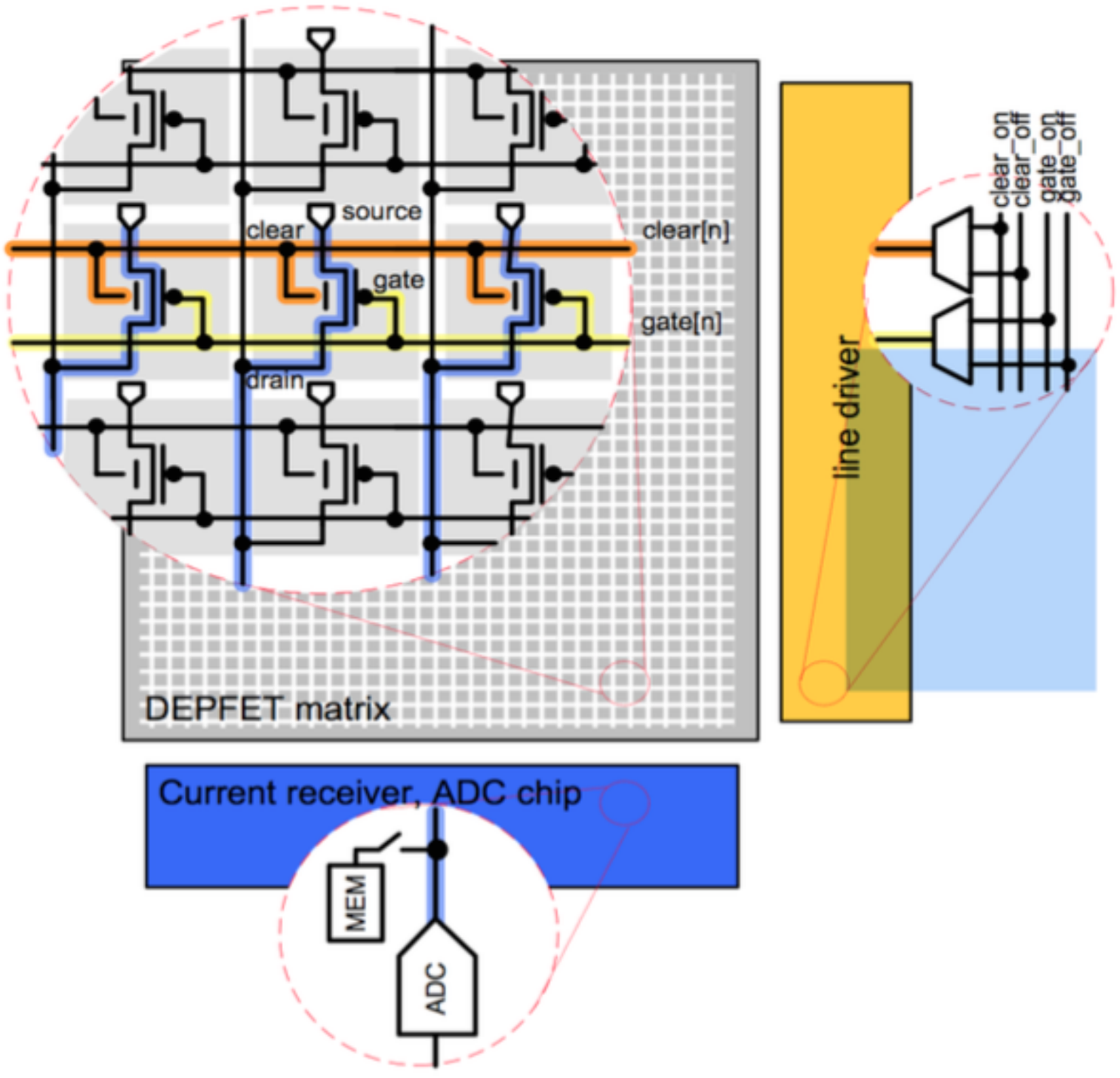
$$g_q = \frac{\partial I_{ds}}{\partial Q_{int}}$$

- In between measurements a clear mechanism allows the pixel to remove the electrons from the internal gate.





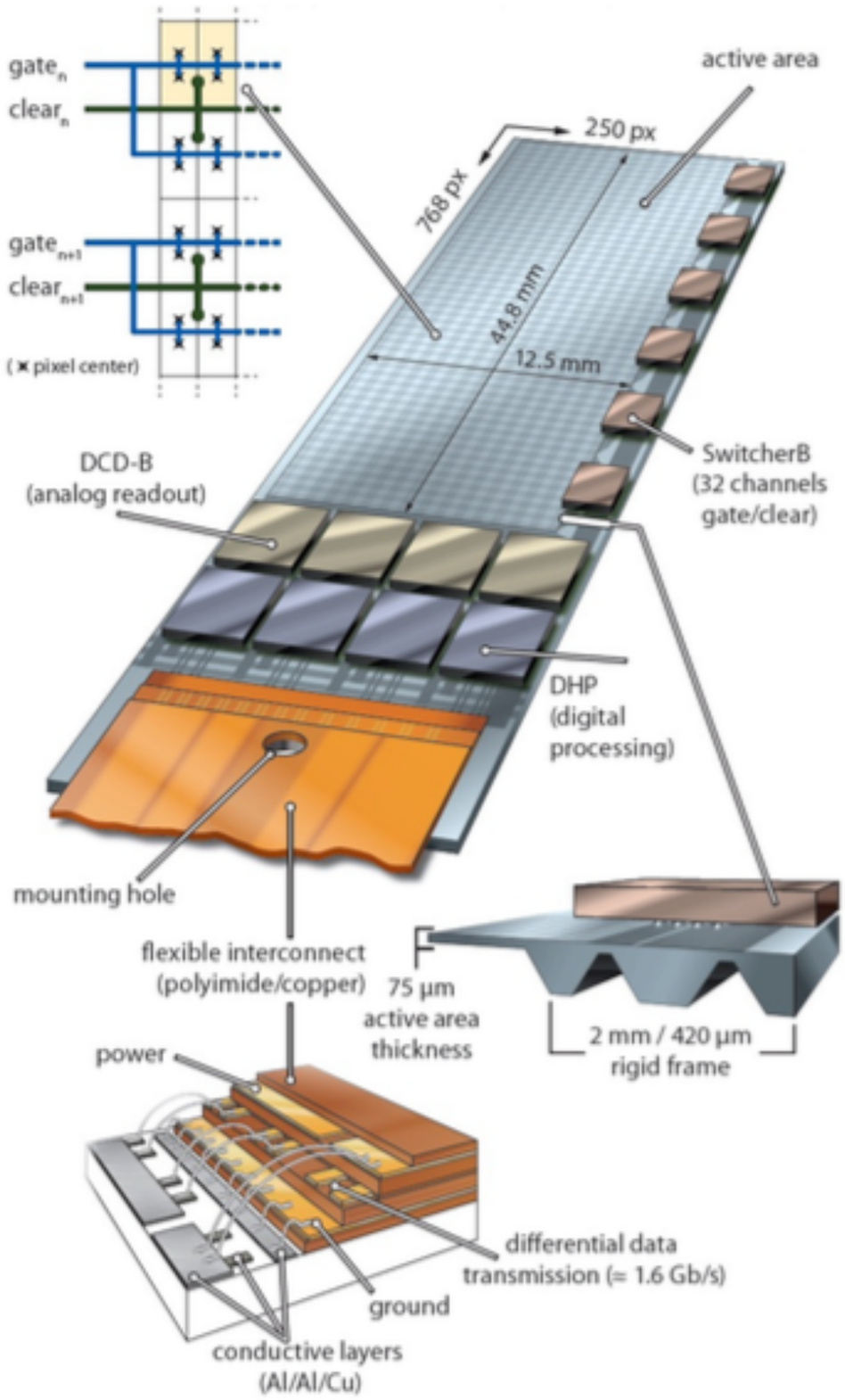
DEPFET PXD: PIXEL ARRAY



- Gate and Clear lines need switcher steering chips.
- Row-wise readout (with 4 rows at a time for Belle II - 20μs/frame).
- Long drain readout lines keep most of the material out of the acceptance region.
- All the sensor is sensitive to charge, but only activated rows consume power. This feature allows for a low power consumption of the PXD array.

DEPFET PXD: HALF LADDER

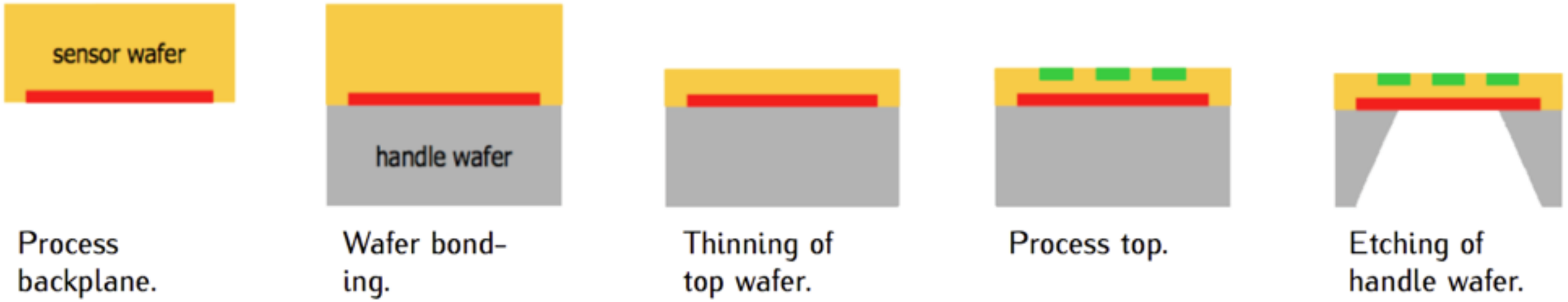
- **Switcher B (Row controller):**
  - Gate and Clear signals.
  - 32x2 channels
- **DCDB (Drain Current Digitizer):**
  - Analog frontend.
  - Amplification and digitation of drain signals.
  - 256 input channels - 8bit ADC/channel.
  - 92ns sampling time.
- **DHP (Data Handling Processor):**
  - First data compression.
  - Common mode and pedestal corrections.
  - Data reduction (Zero suppresion).
  - Timming and trigger control.



DEPFET PXD: PRODUCTION

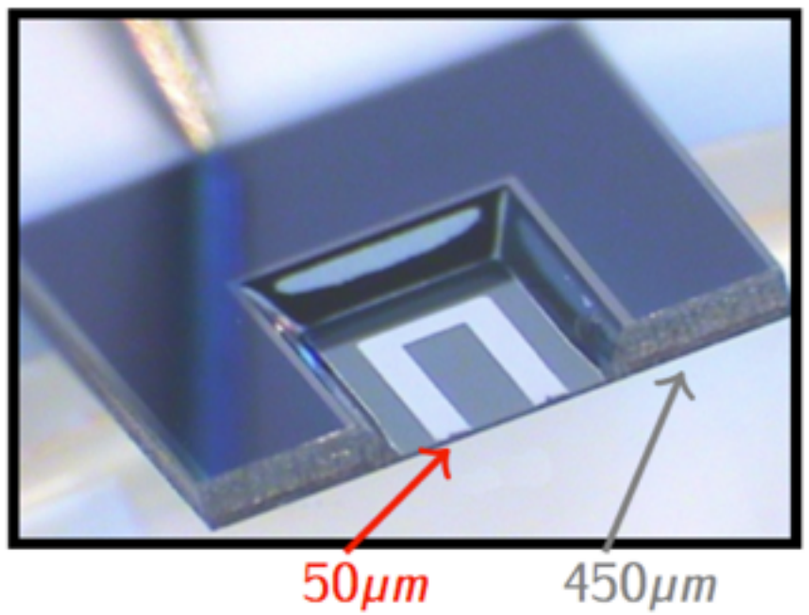
DEPFET production consist in a 90 steps process with 9 implantations, 19 litographies, 2 poly-layers, 2 alu-layers, one copper layer and one back side processing.

To achieve the low material budgets required by the experiments (0.21% X0 for Belle II and 0.15% for ILD) conventional thinning technologies were not an option. So a new thinning technique was developed for the DEPFET production.

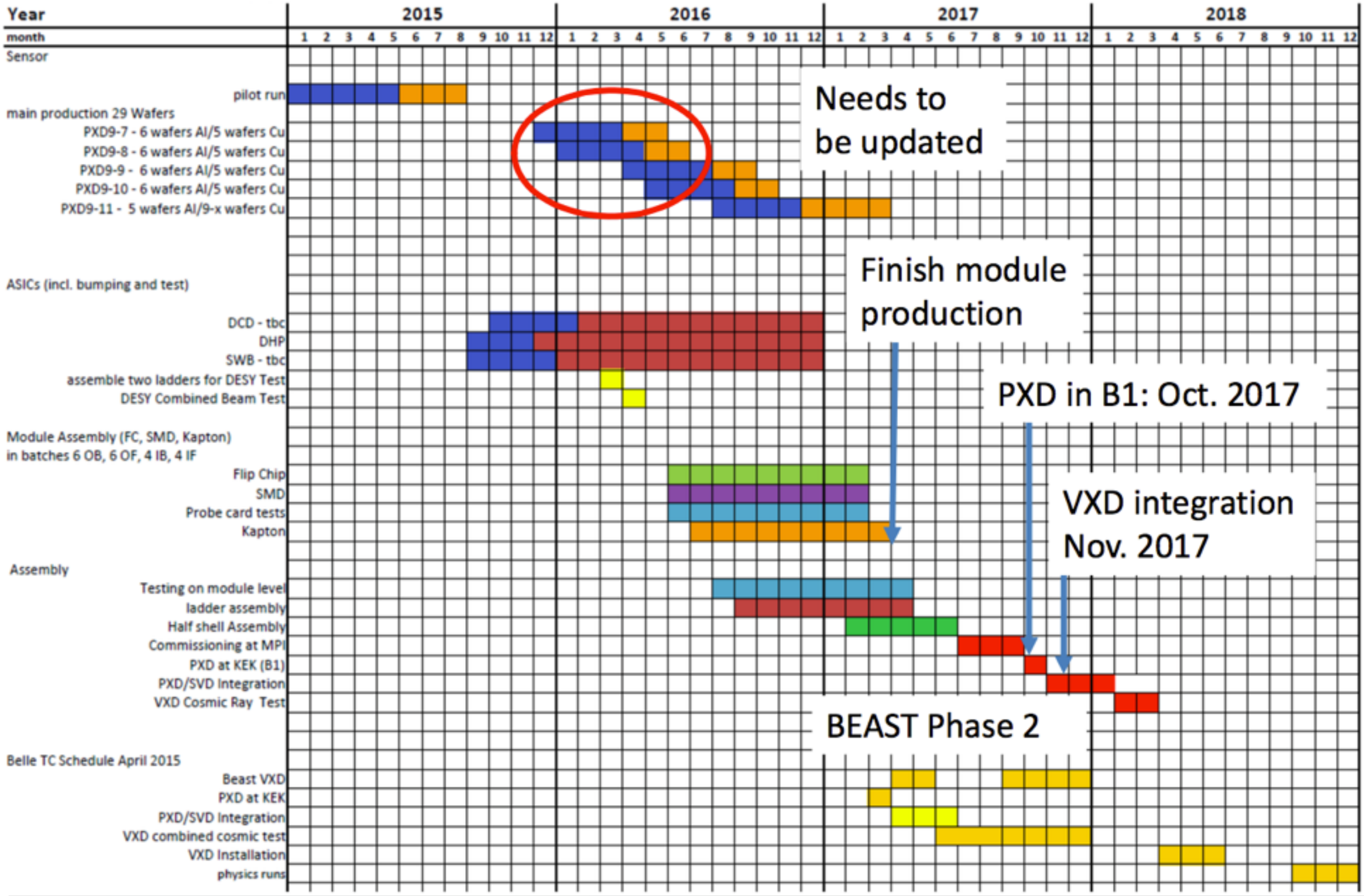


After the silicon doping, printing of the IC and thinning of the DEPFET matrix the module is finished by:

- Flip chip of the ASICs.
- Assembly of the SMDs.
- Attachment of the Kapton cable.



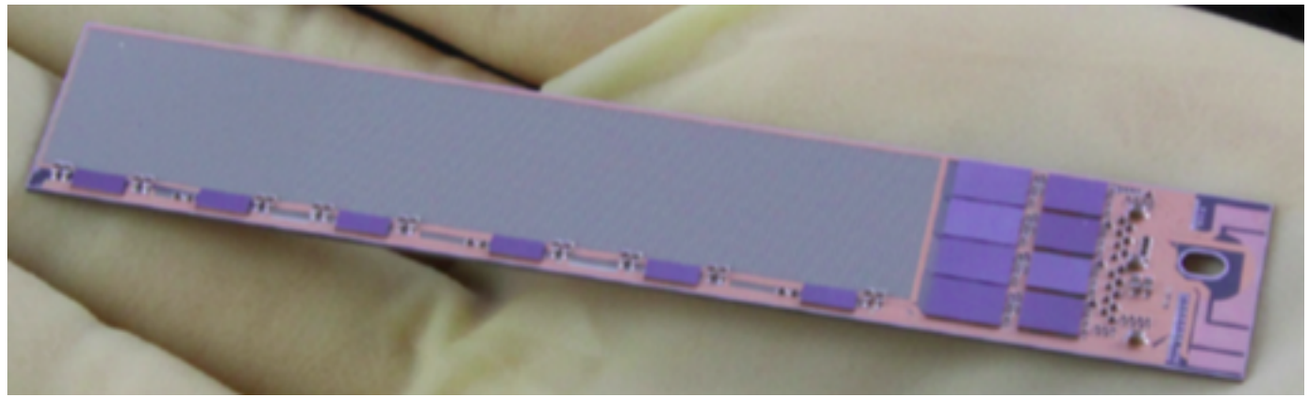
DEPFET PRODUCTION STATUS: CALENDAR



DEPFET PRODUCTION: ACTUAL STATUS

- The pilot run has been completed. Of 18 sensors (3 silicon wafers) 14 passed the electrical tests and are ready for the metallization steps.

- The first complete module has been produced from one of the pilot run sensors.



SEE C. KIESLING TALK @ 9TH VXD BELLE II WORKSHOP

- The final design for the DEPFET pixels (PXD9) has been tested in a test beam. Results show a higher than expected internal gain (g_q) of 740 ± 50 pA /e^-.

SEE B. SCHWENKER TALK @ 9TH VXD BELLE II WORKSHOP

DEPFET PRODUCTION: NEXT STEPS

- Latest versions of the ASICs submitted: DHPT1.1, SwitcherB, DCDB5. Further testing and optimization ongoing, final versions expected for summer 2016.

- A VXD combined test beam of 2 PXD + 4 SVD ladders (final sensors) will be performed in April. All the VXD readout chain, slow control, cooling and environmental sensors will be tested.

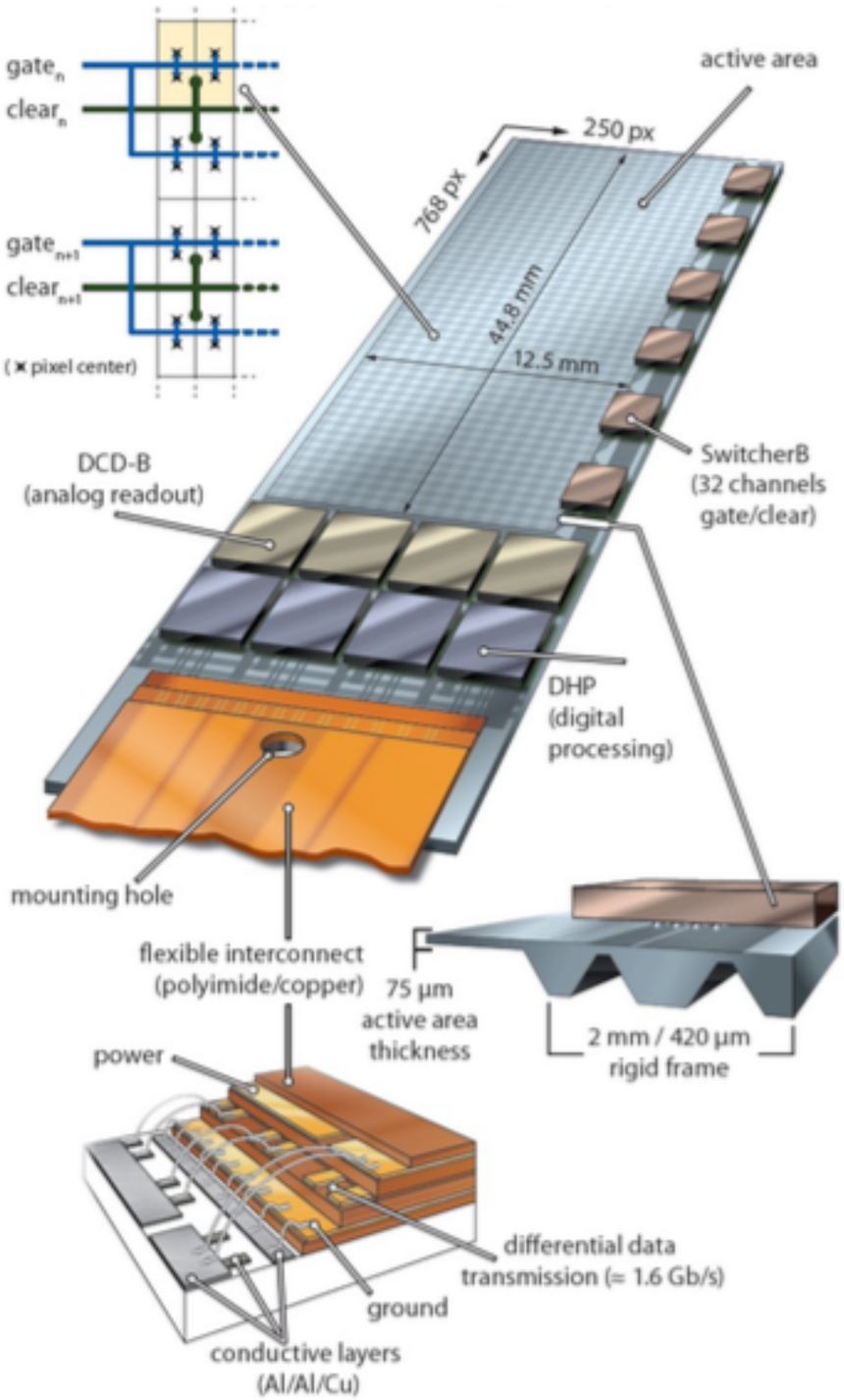
SEE C. MARIÑAS TALK @ 9TH VXD BELLE II WORKSHOP

- ASICs and SMD assembly to be performed by the second half of the year. Probe card tests will be performed to ensure proper assembly before Kapton cable attachment.

- Commissioning at MPI expected for early 2017. Final VXD integration expected for November 2017.

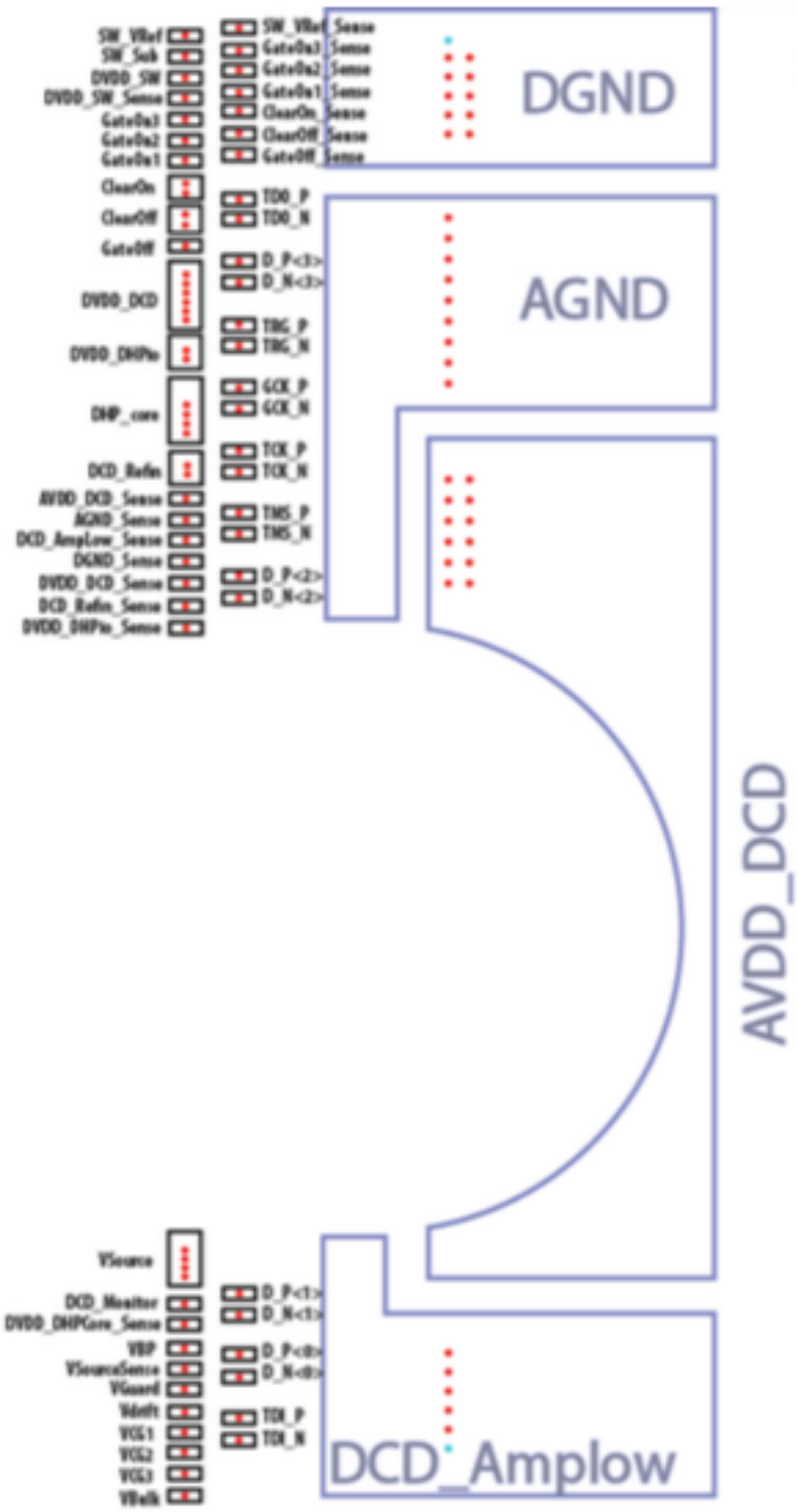
QUALITY CONTROL: PROBE CARD

- The DEPFET modules fully assembled will be attached to a kapton cable.
- After attaching the Kapton cable, reworking may be impossible.
- Pre-testing of the modules before the attachment is necesary.
- A needle card is required for this purpose.



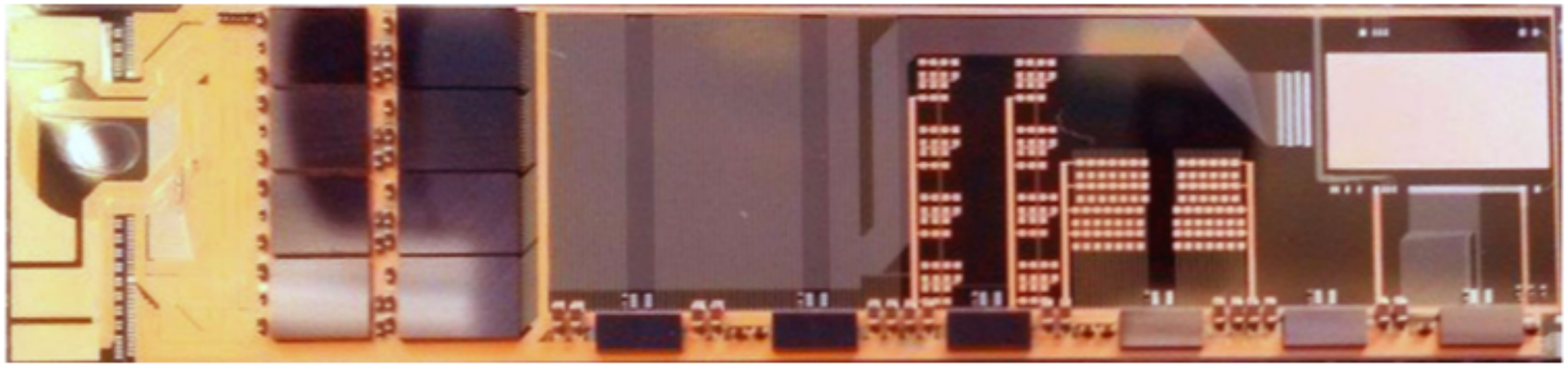
PROBE CARD: PXD9 LAYOUT

- **Pad distribution for PXD9:**
  - 59 small aluminium pads, 4 big copper pads.
  - 8 pads for high speed differential lines.
- **Design considerations:**
  - 114 needles (multiple needles for the big pads) are required.
  - PCB size is limited by connectors for power supply and infiniband.
  - Design priority: rather simple and passive PCB, minimizing the path length of the high speed signals.

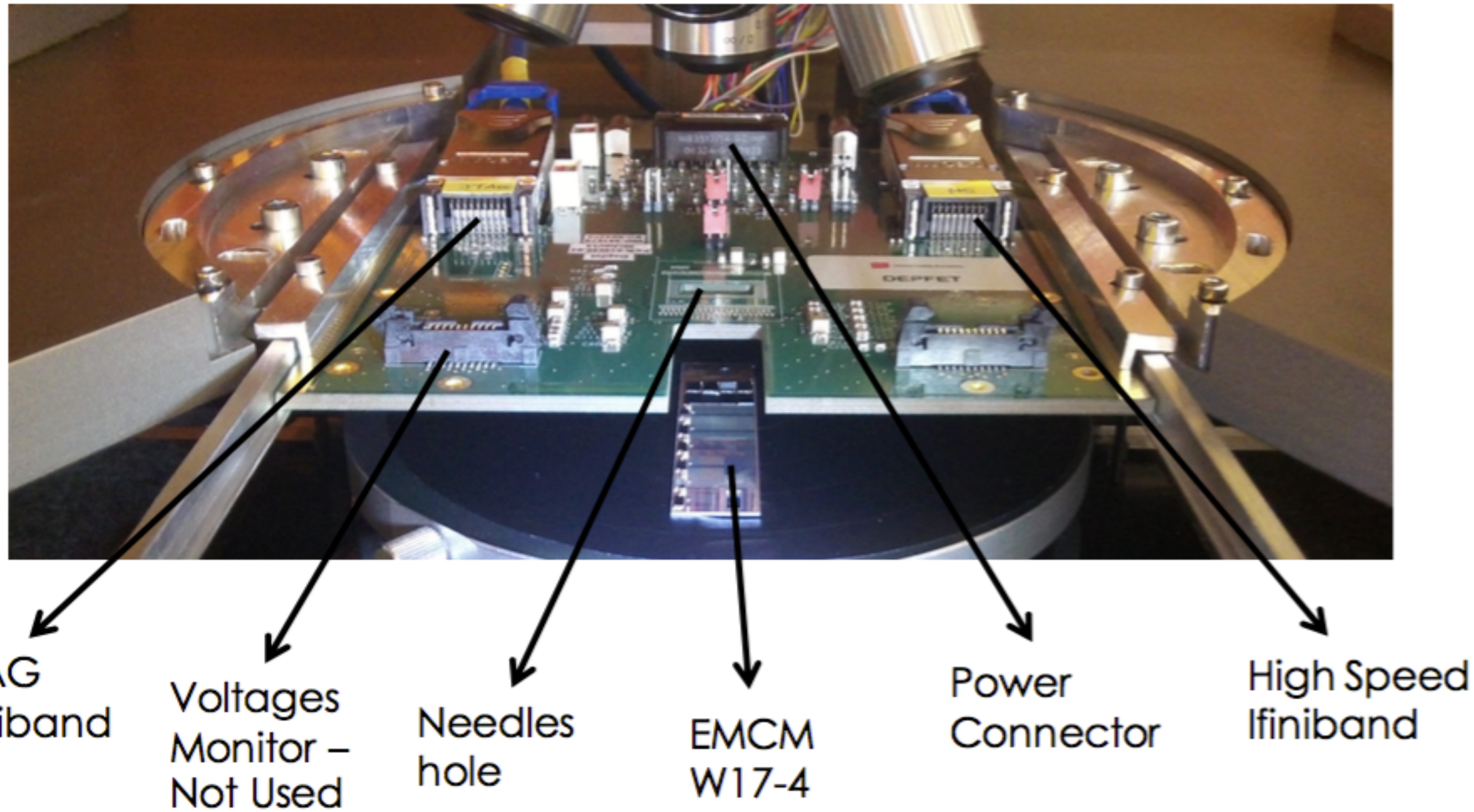


PROBE CARD: EMCM NEEDLE CARD

- **EMCM (electrical module without active area):**
  - A probe card for the EMCM has been built.
  - The results prove the feasibility of testing with a needle card.
  - The PXD9 pads layout is slightly different from the EMCM pads layout, a new needle card design is required.



PROBE CARD: EMCM SETUP



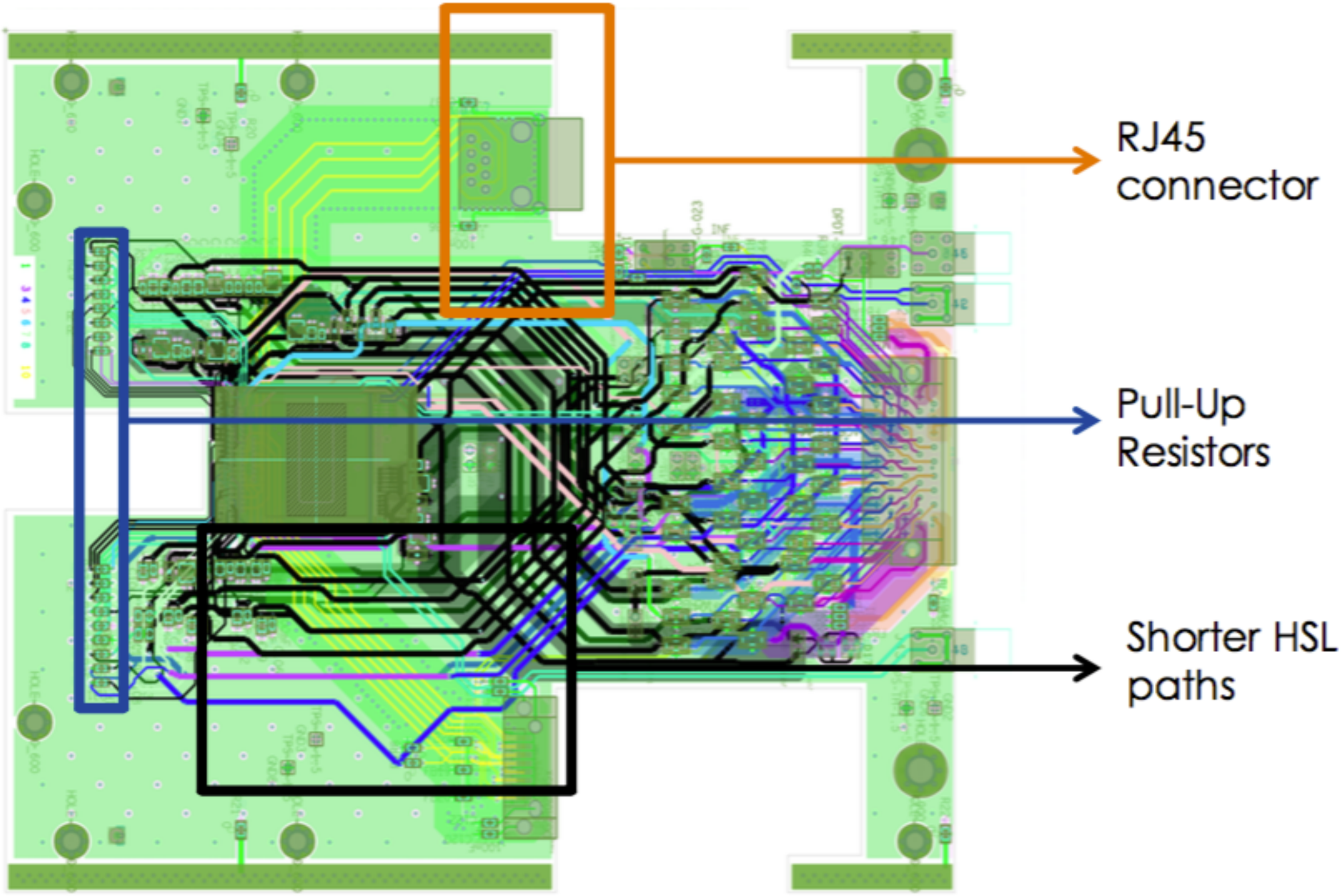
PROBE CARD: EMCM RESULTS AND SUMMARY

- **With the EMCM setup the following measurements were performed:**
  - Voltages applied and current consumptions measured for a populated EMCM.
  - Slow control and boundary scan:
    - Chips were configured.
    - Some parameters were write and read via JTAG.
    - The infrastructure and interconnection tests were performed.
  - A High speed link was established succesfully with the DHE software:
    - The quality of the signal was measured with an eye diagram.
    - The delay settings were optimized.
    - DCD pedestals were read.
- **These results indicate that if the contact between the needles and the modules pads is good enough, there is no problem to operate (and even get stable high speed links) the module with the probe card.**

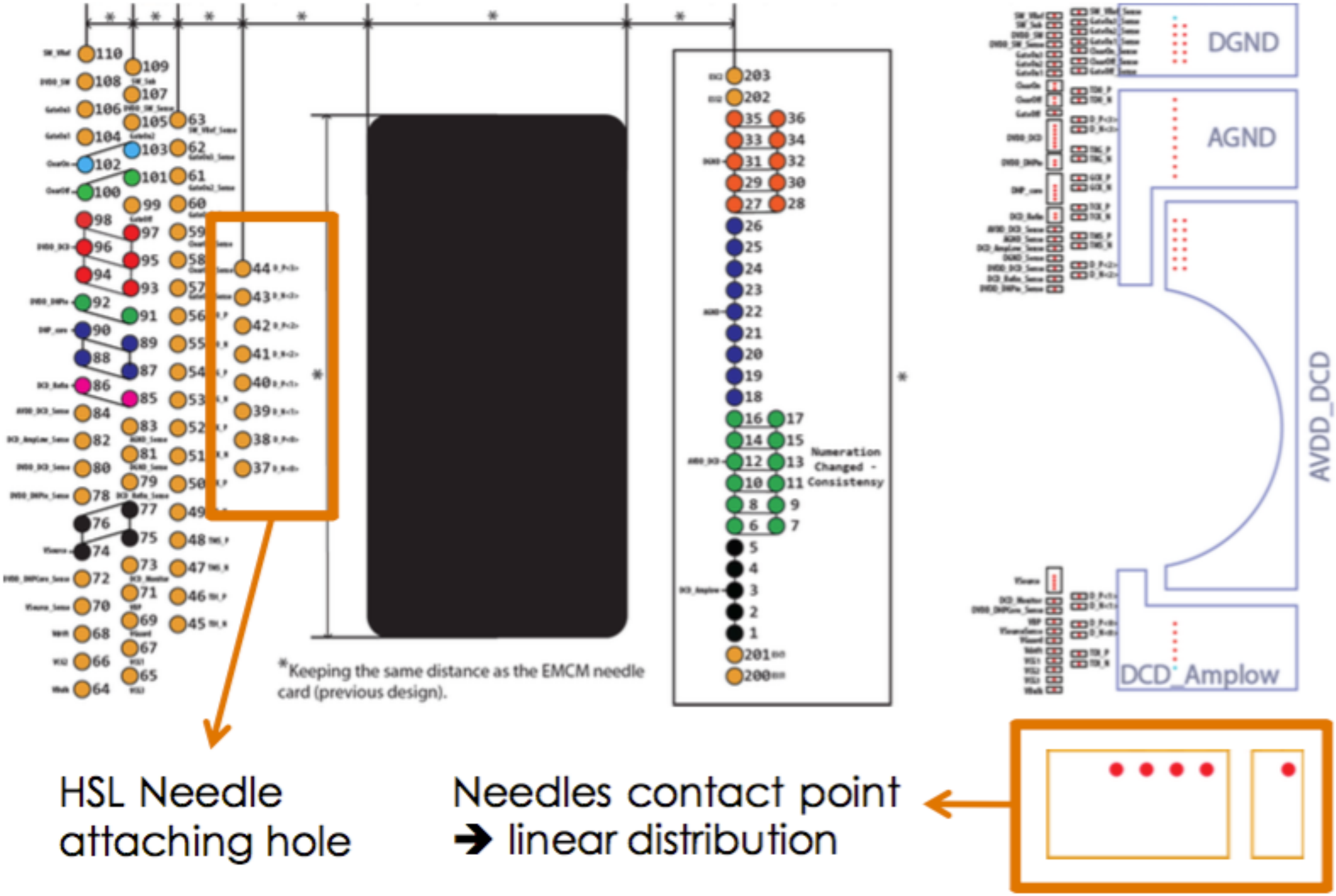
PROBE CARD: PXD9 DESIGN MODIFICATIONS

- **Needle card for PXD9 → two new designs are required:**
  - Design A: outer-bwd & inner-fwd → PCB fabricated.
  - Design B: outer-fwd & inner-bwd → Modifying PCB.
- **Adapt PCB to the new DHE → RJ45 added.**
- **High speed link optimization:**
  - Reduce length of HSL needles.
  - Reduce length of the HSL PCB paths.
- **To reduce pad damage → new needles contact distribution.**
- **To avoid unexpected overvoltage due to bad contacts in the needles of the sense lines → inclusion of pull-up resistors.**

PROBE CARD: PXD9 PCB A DESIGN



PROBE CARD: PXD9 NEEDLES A DESIGN



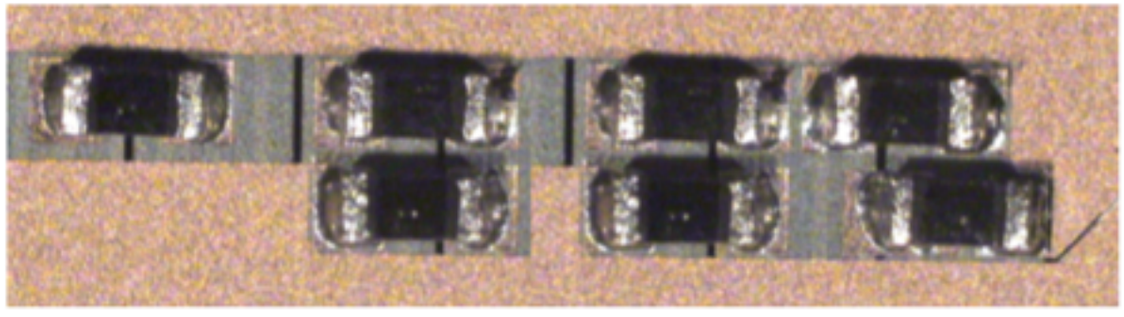
PROBE CARD: PROPOSED TESTING PROTOCOL

- **Based on the EMCM results a preliminary testing protocol is proposed:**

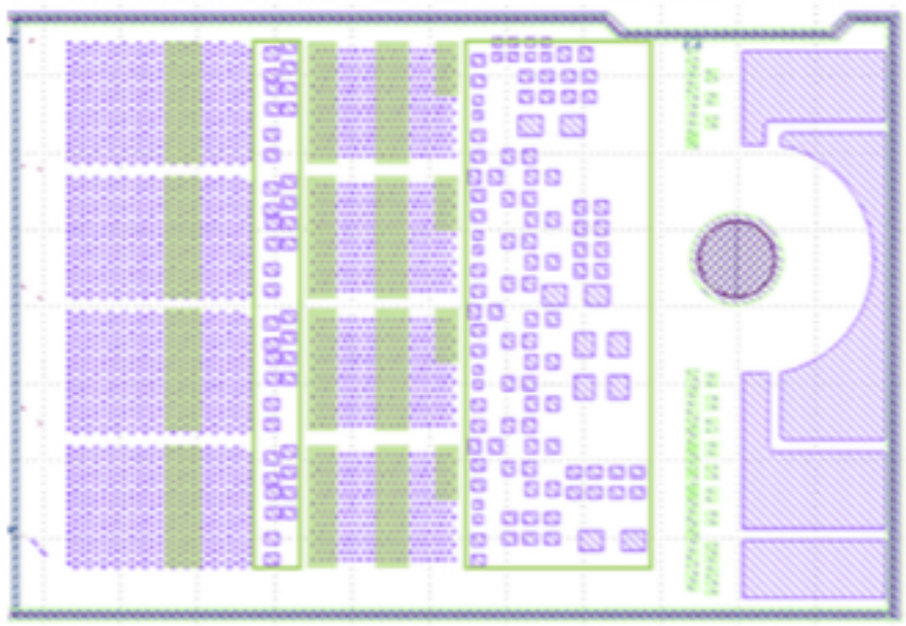
1. Visual inspection.
2. Check of voltages & currents.
3. Chip configuration: JTAG write & read.
4. Boundary scan.
5. High Speed Link stability.
6. Optimize DHP and DCDB interconnections.
7. Read DCDB pedestals.
8. Check of voltages & currents (Matrix).
9. Read Matrix pedestals.
10. Modification of Switcher sequence: matrix saturation.

TESTING PROTOCOL: VISUAL INS. & VOLTAGES

- **Visual inspection**
  - Visual inspection over SMDs and the rest of the components.



- **Check of voltages & currents.**
  - Proper connection between the power supply and the ASICS.
  - Check if the current consumption is within expected values.

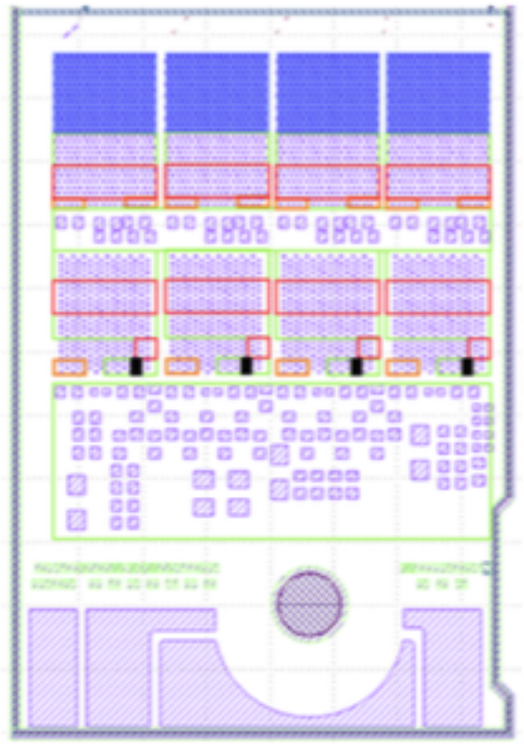


TESTING PROTOCOL: CHIPS, BS & HSL

- **Chip configuration: JTAG Write & Read:**
  - Use the automatic configuration script.
  - Change, write and read some parameters to test proper slow control connection and ASICs response.
- **Boundary Scan:**
  - Test proper boundary cell structure, chip ID & communication thorugh JTAG controller.
  - Check the digital connections between boundary cells.
- **High speed link stability:**
  - DHE software to establish the links and test the quality of data transfer connection.
  - If HSL can’t be established, use IBERT with a random pattern to debug.

TESTING PROTOCOL: DCDB & SWITCHERS

- **Optimization of the DCDB parameters.**
- **Read DCDB pedestals.**
- **Check Matrix voltages & currents.**
- **Read Matrix pedestals.**



- **Modification of Switcher sequence:**
  - Saturate the matrix removing the clean process to test the response of the matrix and the switcher sequence modification.

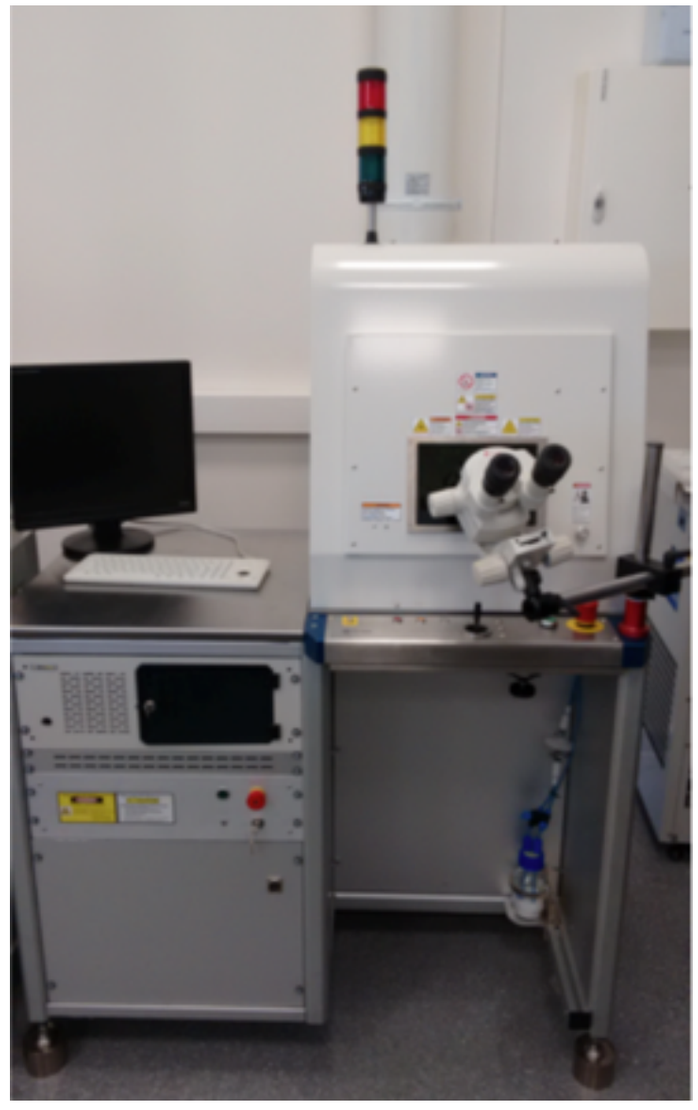
TESTING PROTOCOL: SUMMARY

- The pre-test of the modules, with the needle card is an important step to ensure the viability of a rework in case of ASIC problems.
- The EMCM tests prove its feasibility.
- The PCB design has been modified to suit the PXD9 pad layout A; improving the HSL stability and reducing the damage on the module pads. The PCB has been fabricated and is ready for the component assembly.
- A second design is required for the PXD9 pad layout B. The PCB modification is beign performed.
- With the testing protocol we can check that all the ASICs are working properly. Further studies are required to ensure the safety in all the steps.

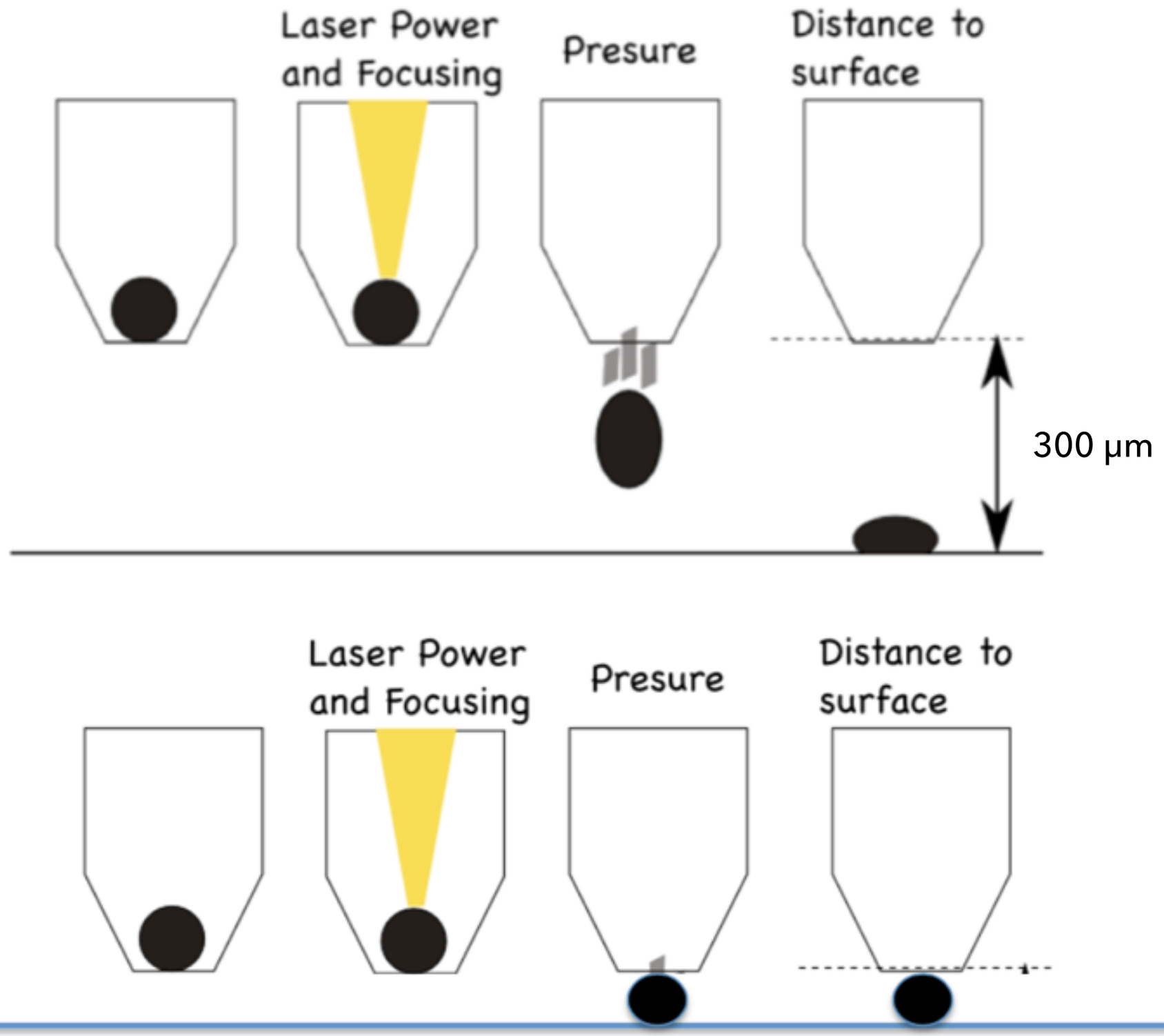
SEE M. BORONAT TALK @ 9TH VXD BELLE II WORKSHOP

SMD ASSEMBLY IN COLLABORATION WITH NTC

- A collaboration with the NTC (Nanophotonics Technology Center of the Polytechnic University of Valencia) was established to be a backup for the SMD assembly in the DEPFET modules production chain.
- In the first trials we realized that the current equipment used to place the welding balls to bond the SMDs couldn't perform the job succesfully.
- A new equipment with a more powerful laser and a different approach was bought to place the welding balls correctly.

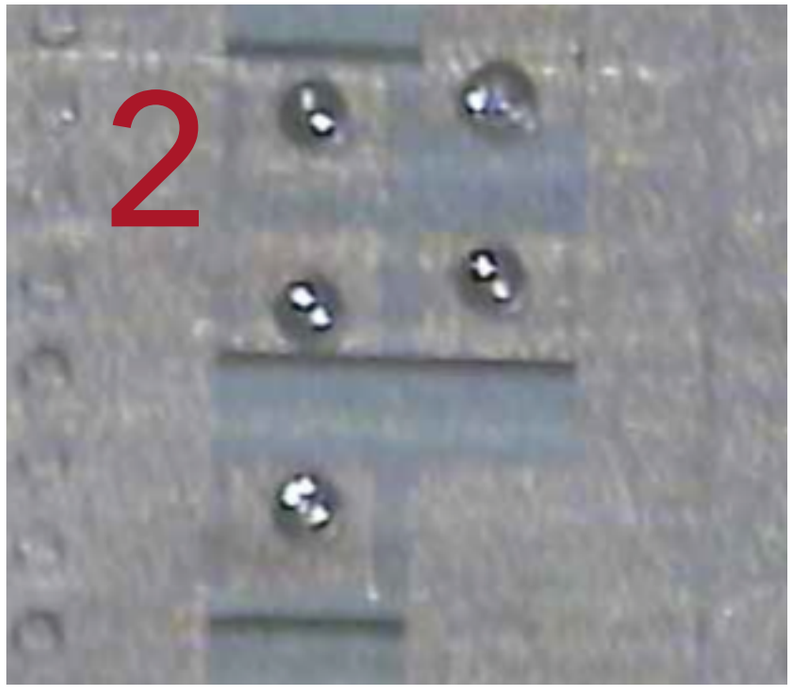


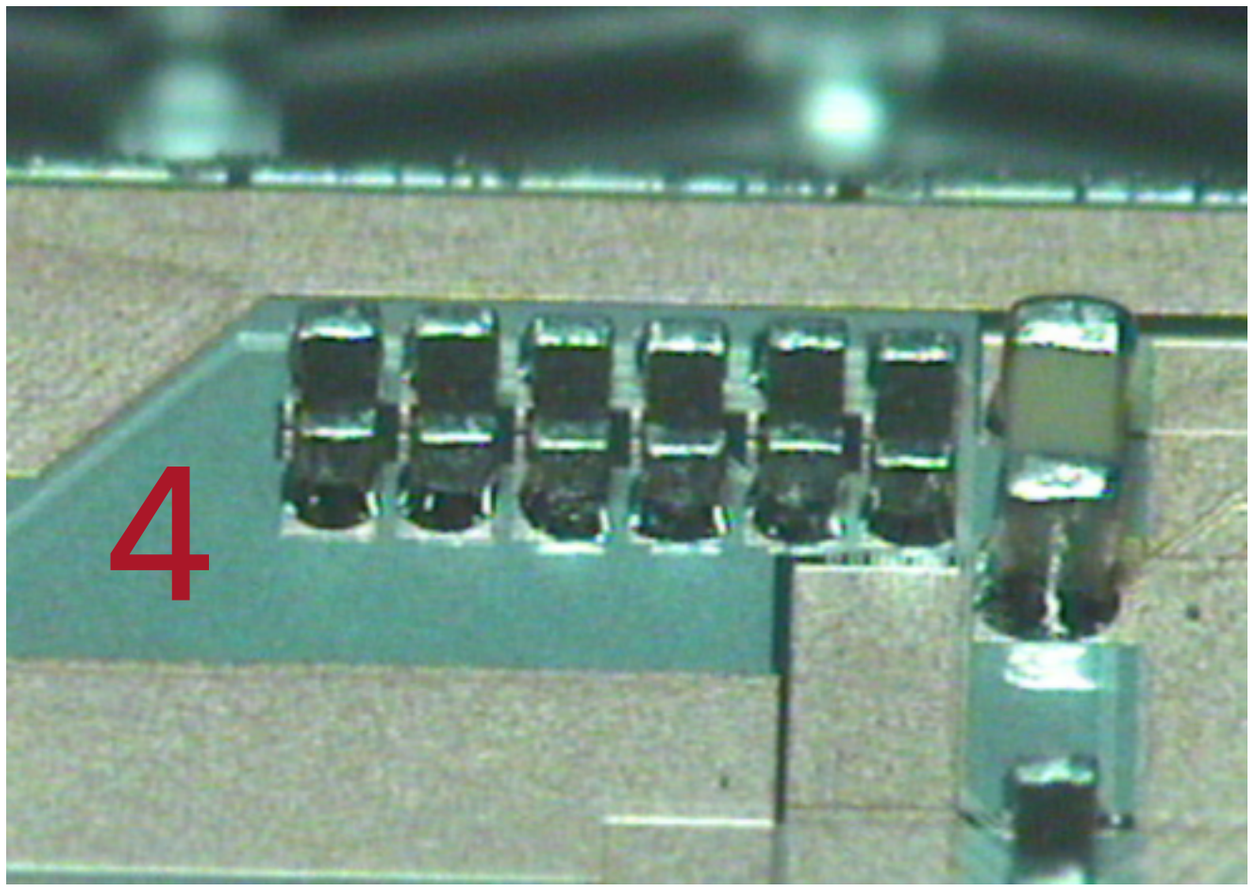
NTC SMD ASSEMBLY: NEW APPROACH

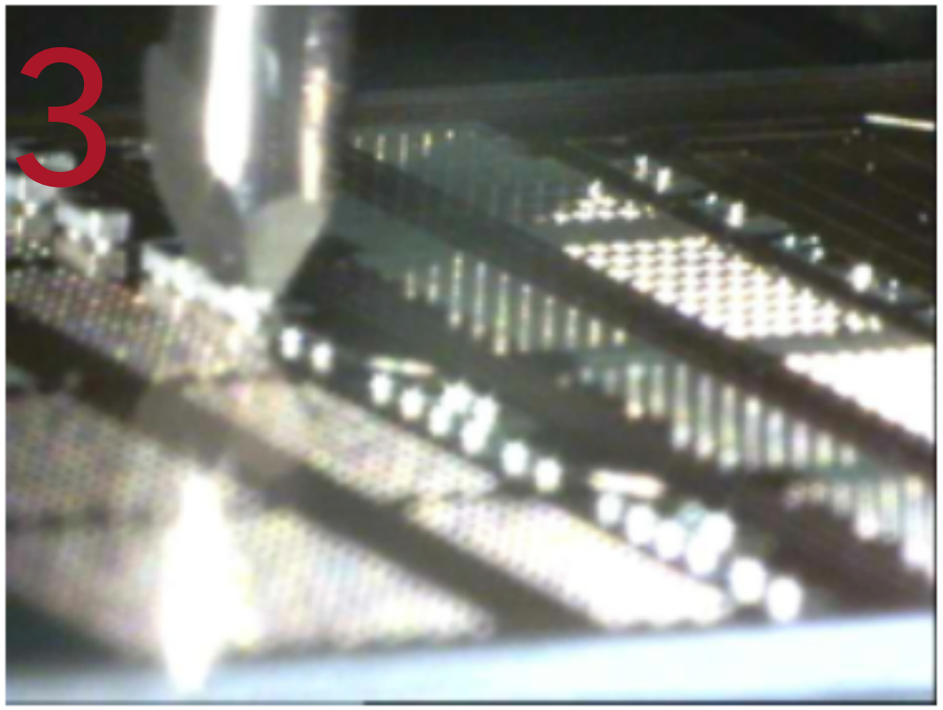


NTC SMD ASSEMBLY: PROCESS FLOW

1. Vacuum cleaning (ATV)
2. Sn63Pb37 Ball placement (Pactech)
3. SMDs tacking (Finetech)
4. Final Soldering (ATV)

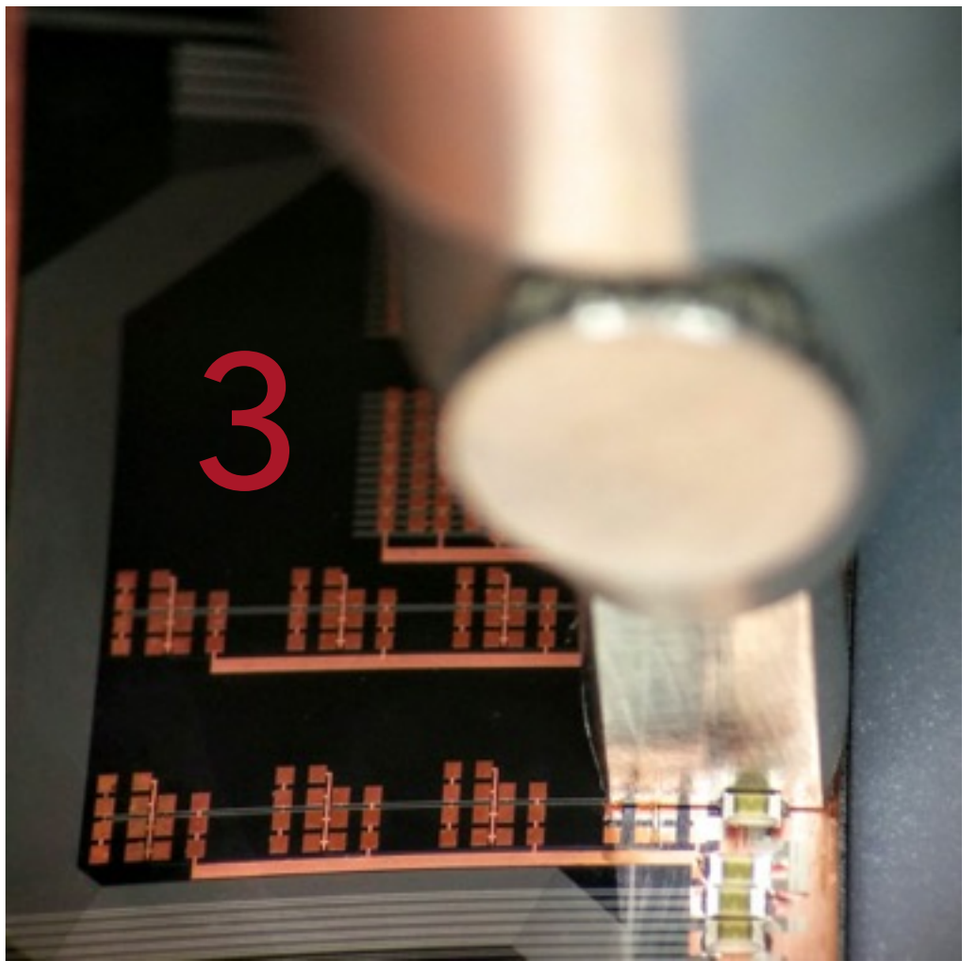


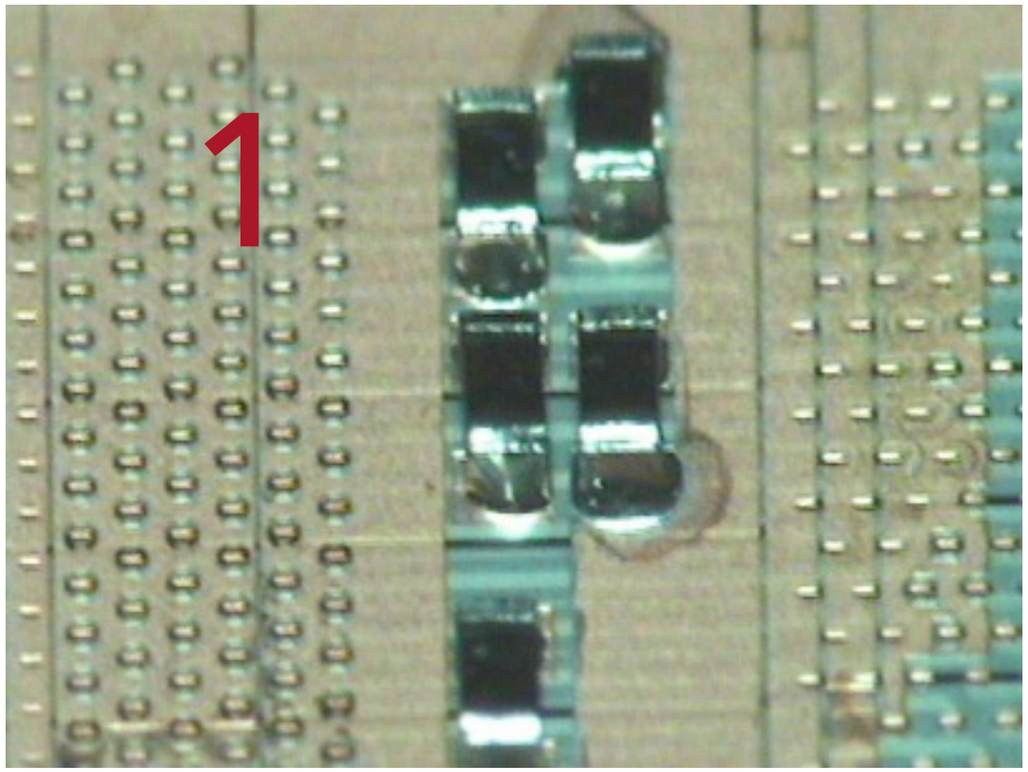


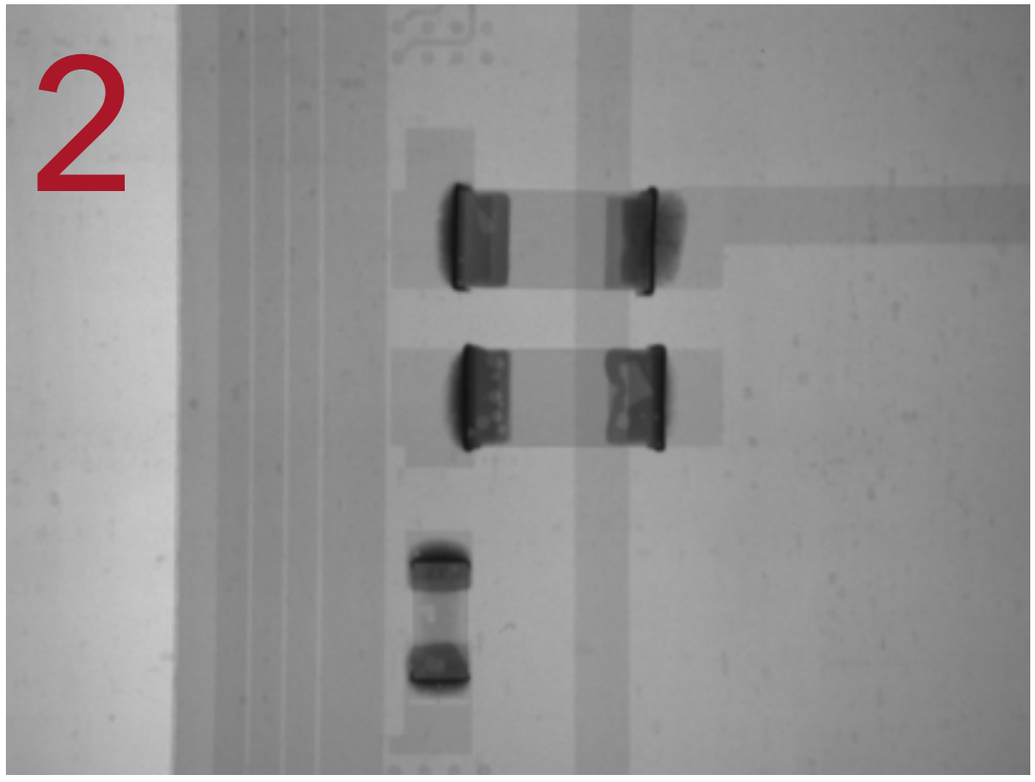


NTC SMD ASSEMBLY: QUALITY CONTROL @ IFIC

1. Visual inspection
2. X-Ray inspection
3. Shear test
4. Reports for each component







NTC SMD ASSEMBLY: RESULTS AND SUMMARY

- The process flow is complete. SMDs have been assembled succesfully. Further optimization of the process is beign performed.
- Quality control reports performed at IFIC found that the welding strenght was competitive with the main assembly centers.
- NTC has demonstrated its feasibility as a backup for the SMD bump bonding for the DEPFET modules.
- The DEPFET collaboration will keep sending the NTC material to mantain their backup capabilities.

CONCLUSIONS

- DEPFET module production is on track: good silicon wafer yields (14/18 sensors working properly), the first PXD9 complete module has been succesfully produced.
- IFIC contributes to the DEPFET collaboration in the module production by:
  - Proving the feasibility of probe card testing for an EMCM.
  - Designing the PCB and needles for the PXD9 A & B layouts of the probe card.
  - Proposing a testing protocol to check that the ASICs are working properly before attaching the Kapton cable.
  - Providing a backup for the SMD assembly in collaboration with NTC.

THANKS FOR YOUR ATTENTION

BACKUP

PROBE CARD: EMCM PCB DESING