

ATLAS New Small Wheel (NSW) small-strip Thin Gap Chamber (sTGC) simulation in Athena

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CAP Congress
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Outline



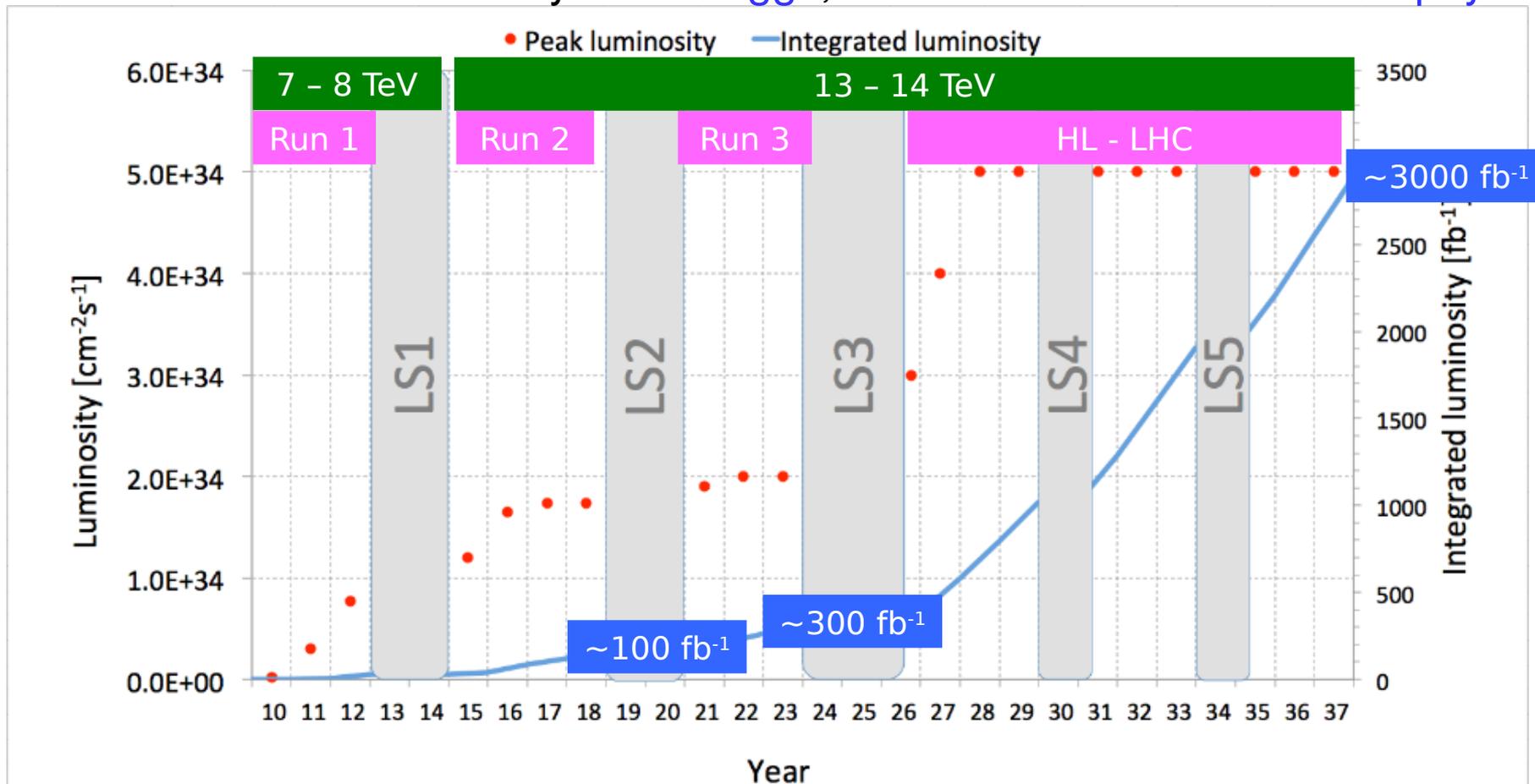
- Introduction
 - Motivation
- The New Small Wheel (NSW)
- The small-strip Thin Gap Chambers (sTGC)
 - Signal simulation (charge distribution)
 - Timing simulation
 - Deadtime (pile-up)
- Summary and Conclusion

Why Upgrade? Harsher Conditions at the LHC



Upgrade **ATLAS** to increase data acquisition **rate**

→ Accelerate the study of the **Higgs**, the **standard model** and **new physics**



Increased **Rate** due to higher **Luminosity**, more **Energy** and smaller **Bunch Spacing** (25 ns)

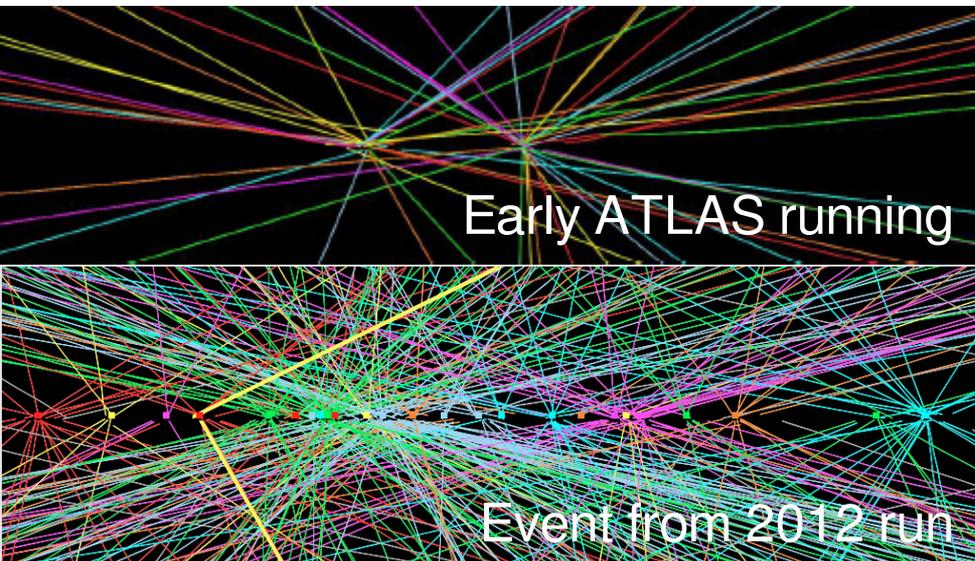
Collecting the data



ATLAS collision rate:

- Original: 25 every 50 ns
- Future: 50-100 every 25 ns

Collisions in one event in ATLAS



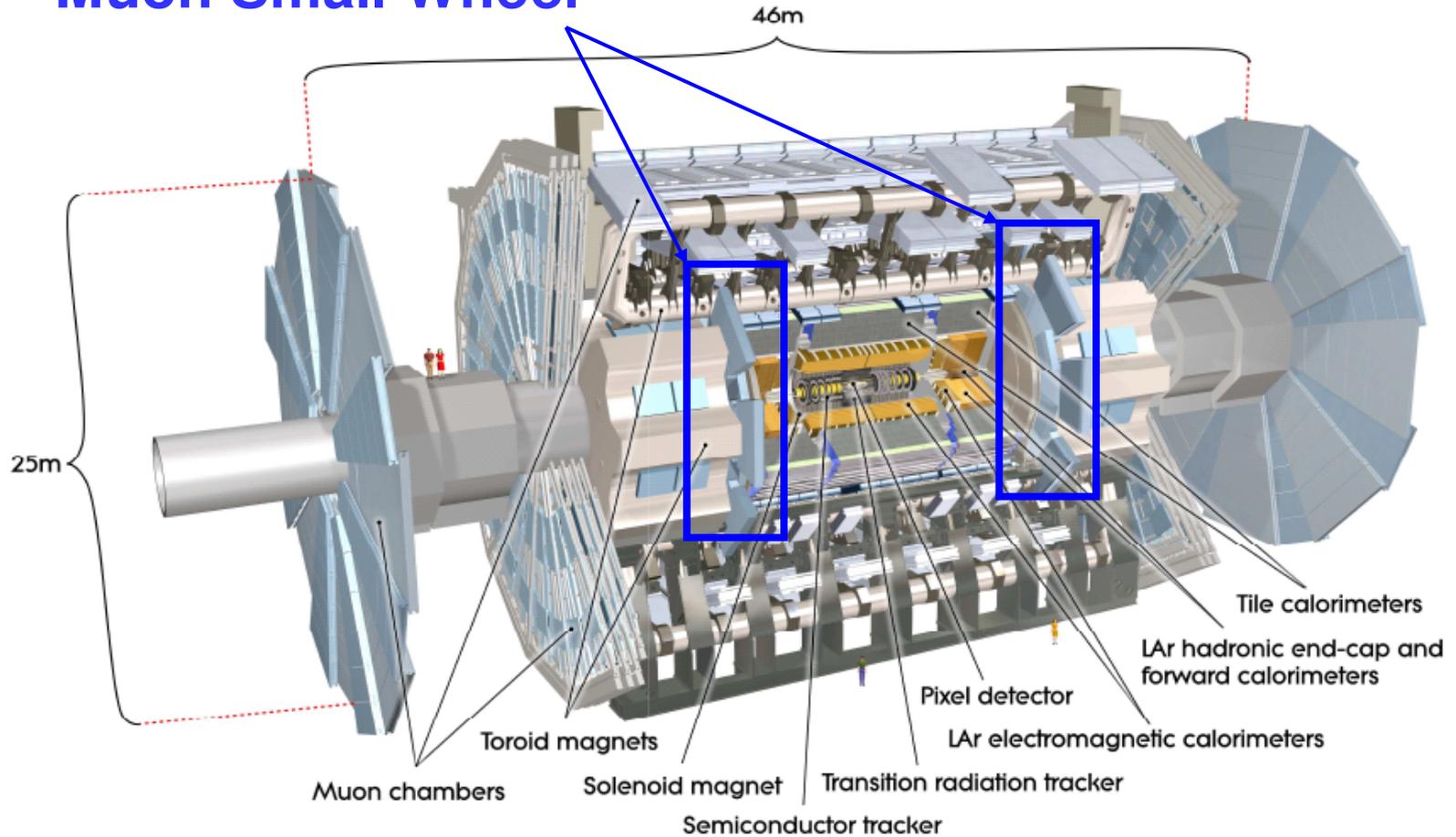
- With current **Muon Small Wheel** the **trigger cannot handle** Run 3 rate
- Key **trigger** selection looks for energetic **muons**
- **Trigger** designed for original luminosity of $1 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$
- The **High Luminosity LHC** trigger will need to handle luminosity of $5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$
- To collect interesting events we need to **enhance** ATLAS trigger capability

Run 3 will have even more collisions!

Small Wheel in ATLAS

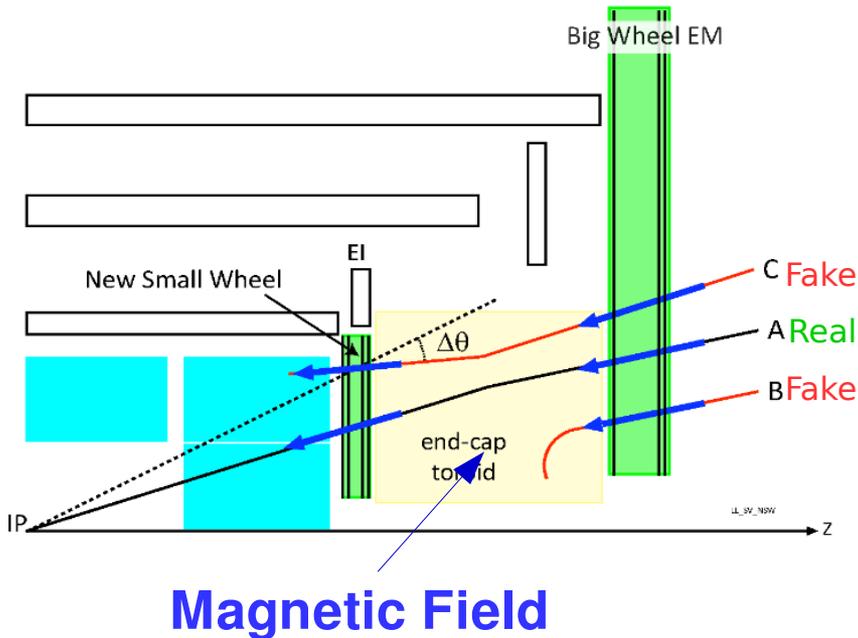


Muon Small Wheel



The **Small Wheels** are the most forward muon chambers → **highest event rate**

Why a New Small Wheel at ATLAS?

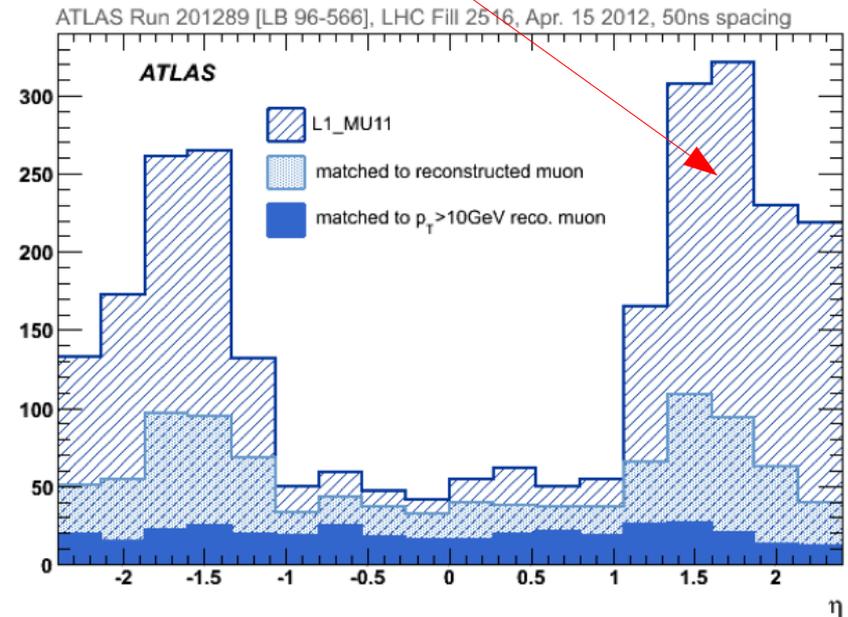


Magnetic Field

Current trigger relies mainly on the **Big Wheel**

Difficult to distinguish between **A, B** and **C** above

Fake muon triggers are **overwhelming** in the end cap regions



The **NSW** will simultaneously **improve tracking performance** and **reduce fake rate** by an order of magnitude

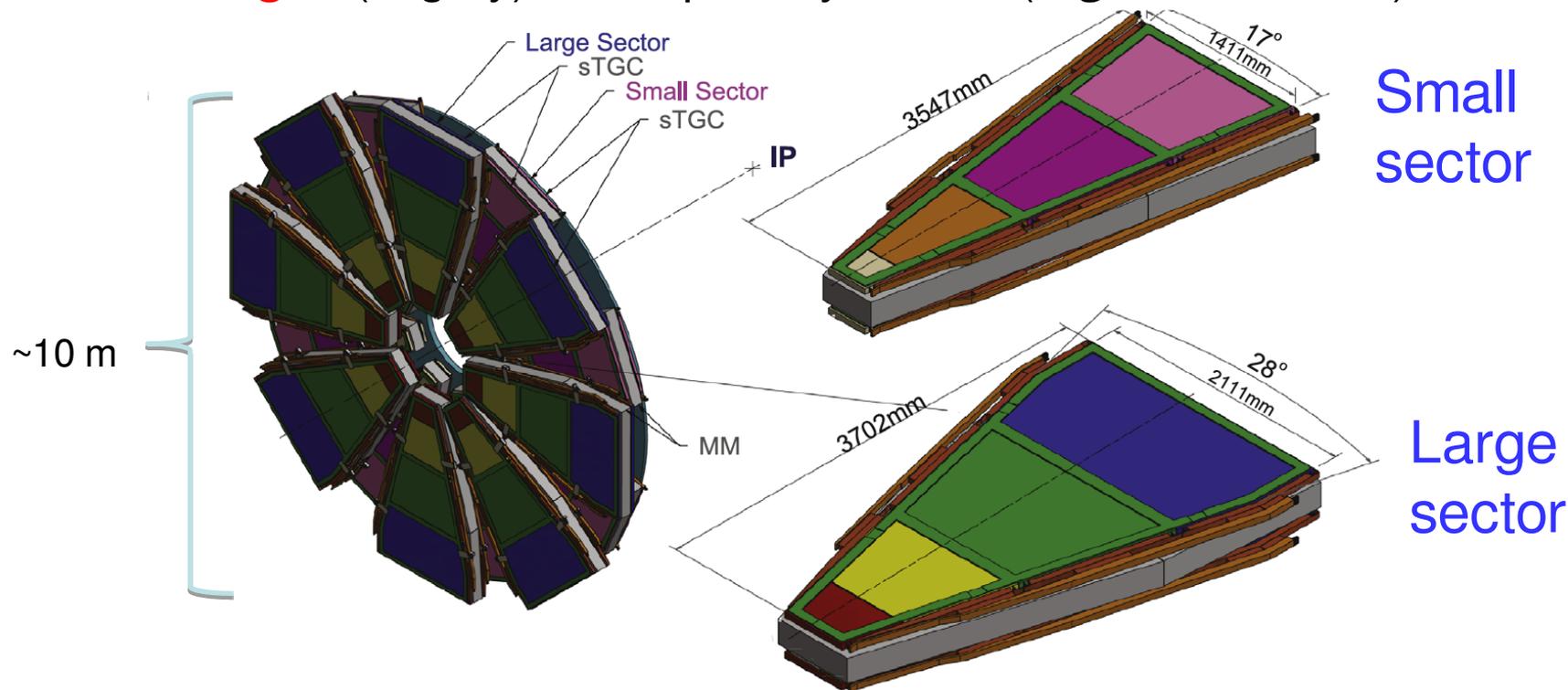
New Small Wheel Technologies



The **NSW** must provide angular resolution of <1 mrad or less to the IP, and so a spatial resolution of <100 μm per layer, in <1 μs

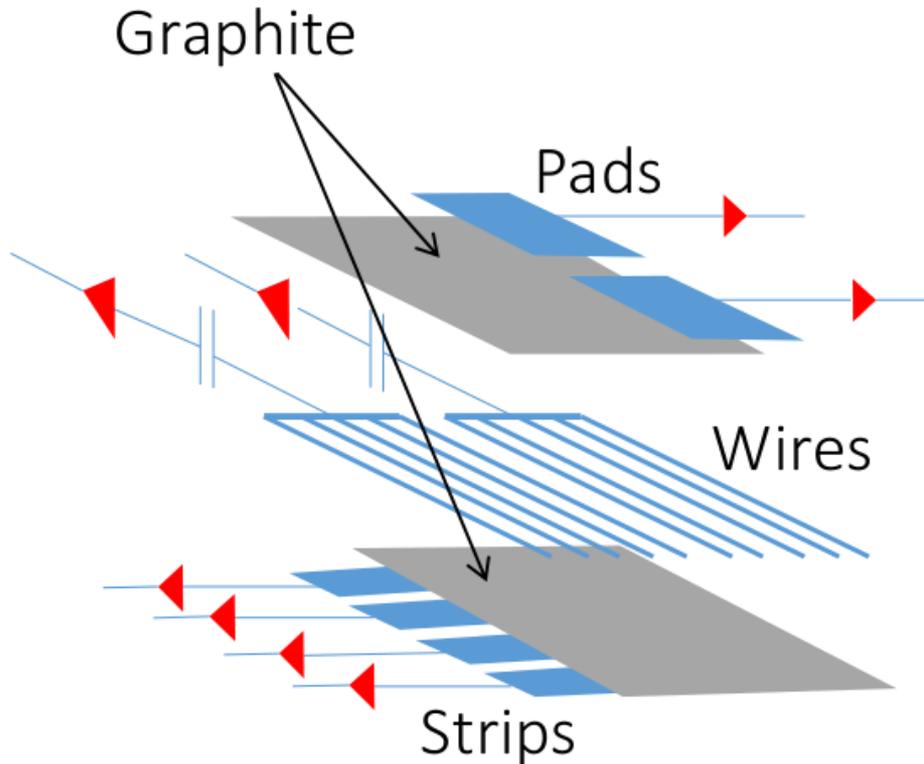
To satisfy the requirements, use two separate technologies:

1. **sTGC** (in color below) as the primary **trigger** (*very fast*)
2. **MicroMegas** (in grey) as the primary **tracker** (*high-resolution*)



sTGC's are the outer chambers \rightarrow longer lever arm \rightarrow better angular resolution

The small-strip Thin Gap Chamber (sTGC)



Gas: pentane / CO₂ (45% / 55% vol.)
2.8 mm gas gap

Anode: wires (at **2900 V**) **1.8 mm** pitch
Cathode: pads and strips, **3.2 mm** pitch

Resistive layer: mitigates 10kHz/cm²
rate protection against discharge

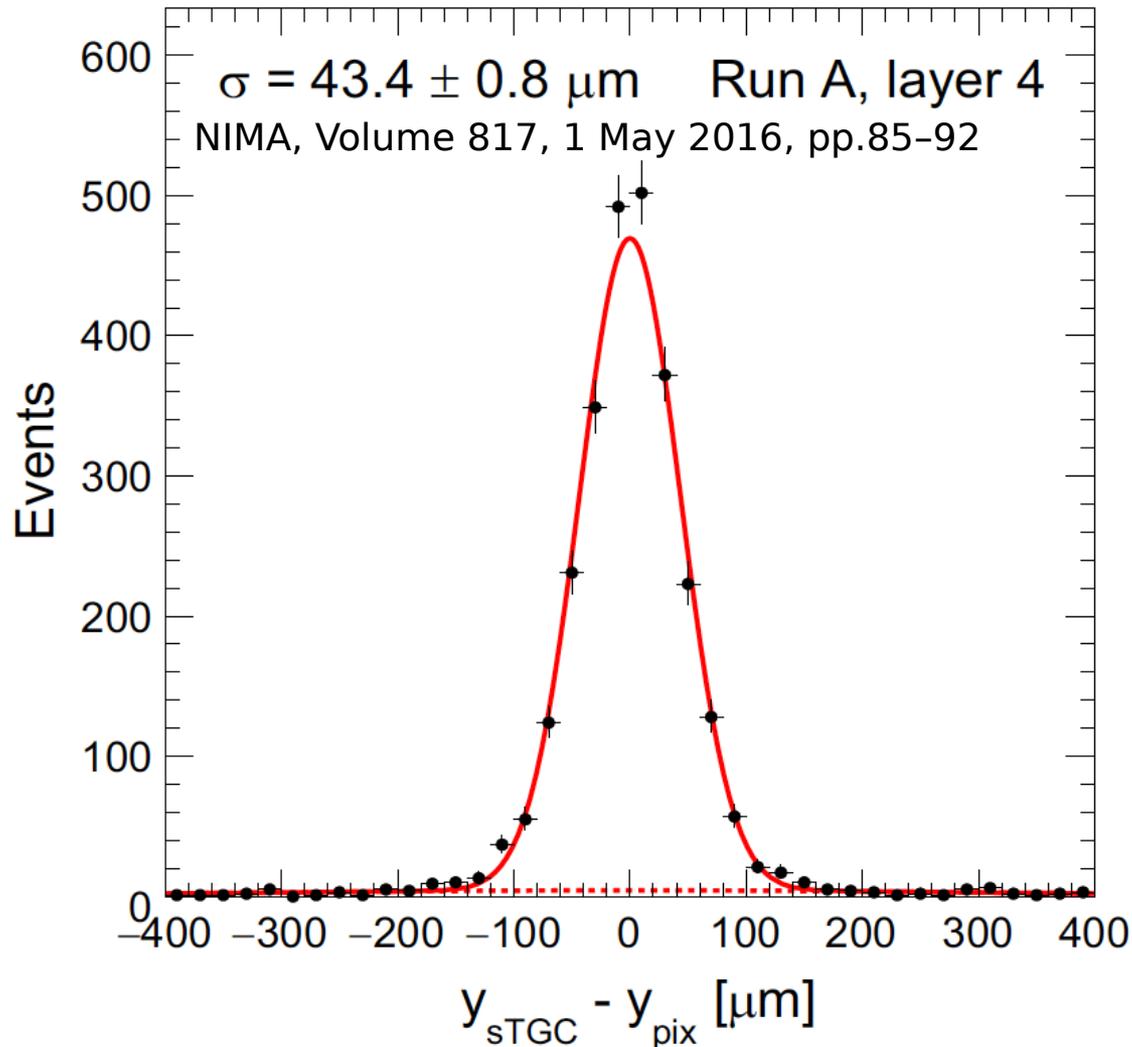
Pads: for **triggering** and to determine
areas of interest for strip readout

Strips: for **tracking** in the precision
coordinate (η)

Single-hit strip spatial resolution

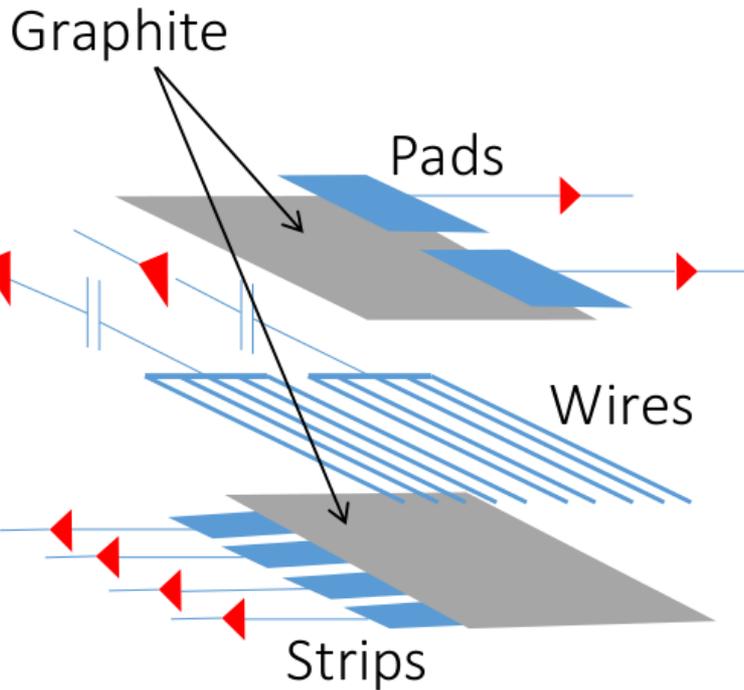


$\sigma = 45 \pm 8 \mu\text{m}$ All runs - All layers



Resolution determined with respect to precise [pixel telescope](#) measurements (y_{pix})

Simulation Geometry Validation



Important to have **accurate geometry** for digitization results to be correct

We took the approach of simulating a **hit** on every **pad** of every **layer**

—► Ensure that the simulation returns the correct **pad** every time

Geometry is defined by the **NSW xml**:
`MuonSpectrometer/MuonG4/NSW_Sim/trunk/data/stations.v1.73.xml`

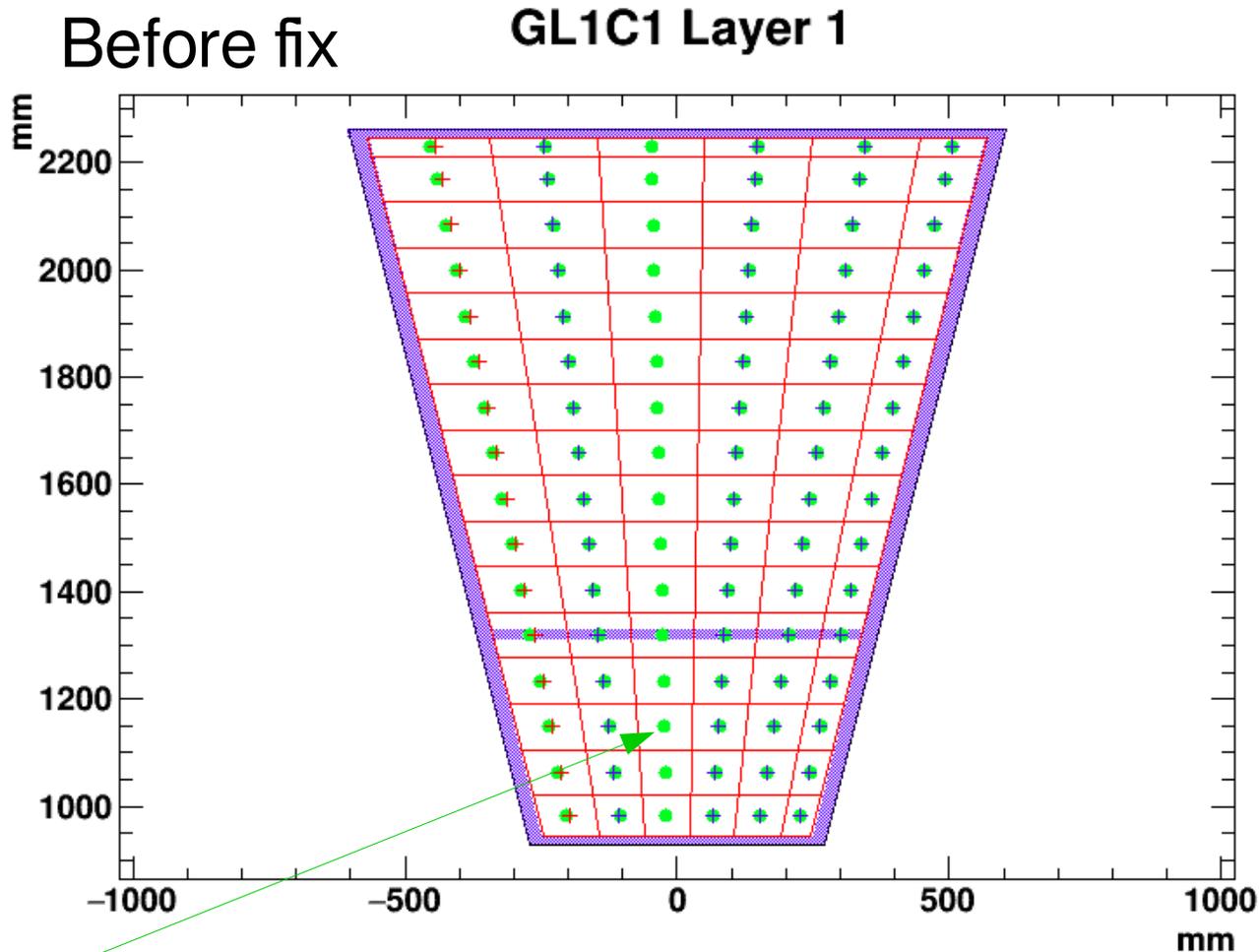
And by the package:

`MuonReadoutGeometry-03-03-03`

Simulation Geometry Validation



Visualization of pad geometry was implemented to *understand, categorize* and **fix** geometry problems



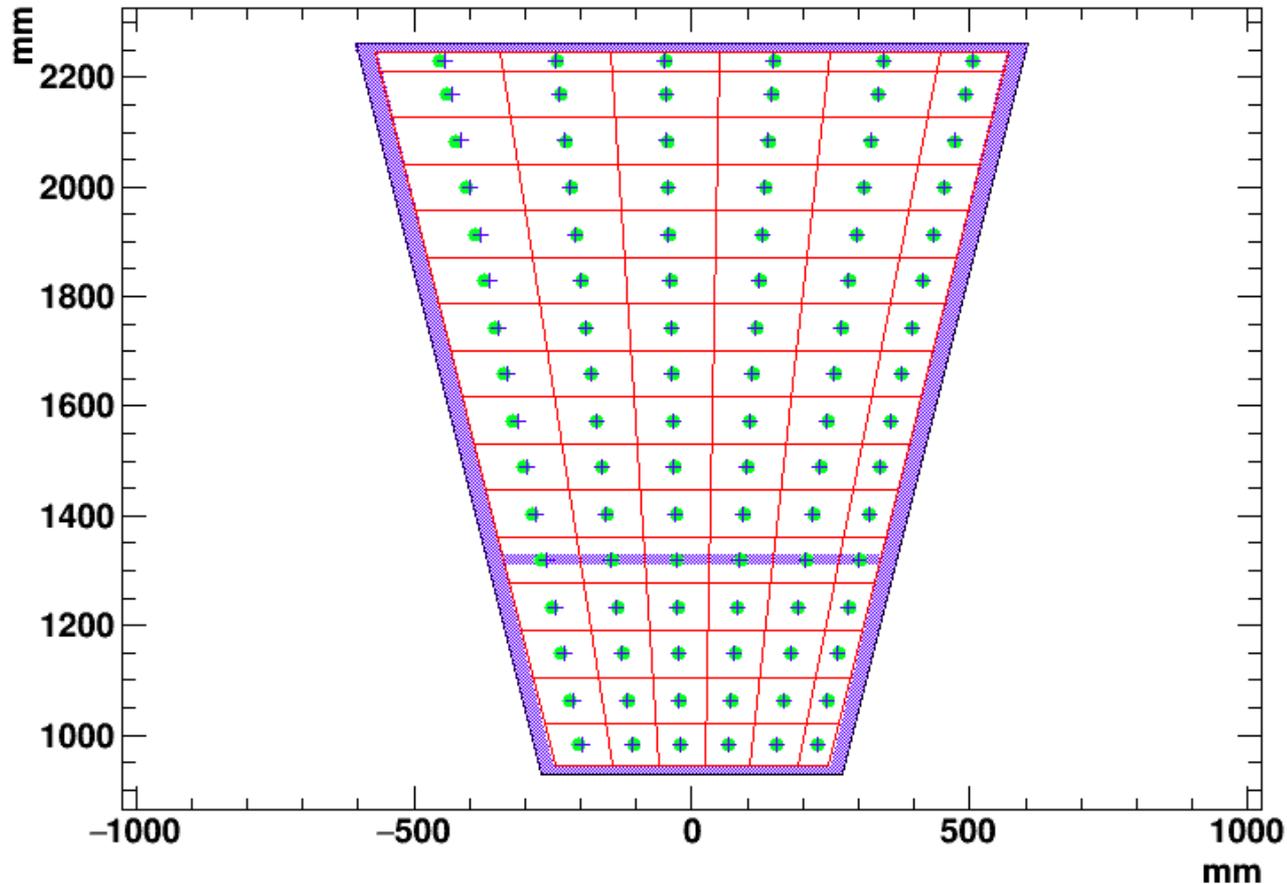
Green circles are input **hit positions**, Blue crosses are the **digitized position**, Red crosses are positions returned **more than once** (**Wrong pad!**)

Simulation Geometry Validation



Half of the **layers** were *inverted* in the geometry -> **hits created on the wrong pad**

After fix GL1C1 Layer 1



Green circles are input **hit positions**, Blue crosses are the **digitized position**

sTGC signal simulation



Raw induced
signal

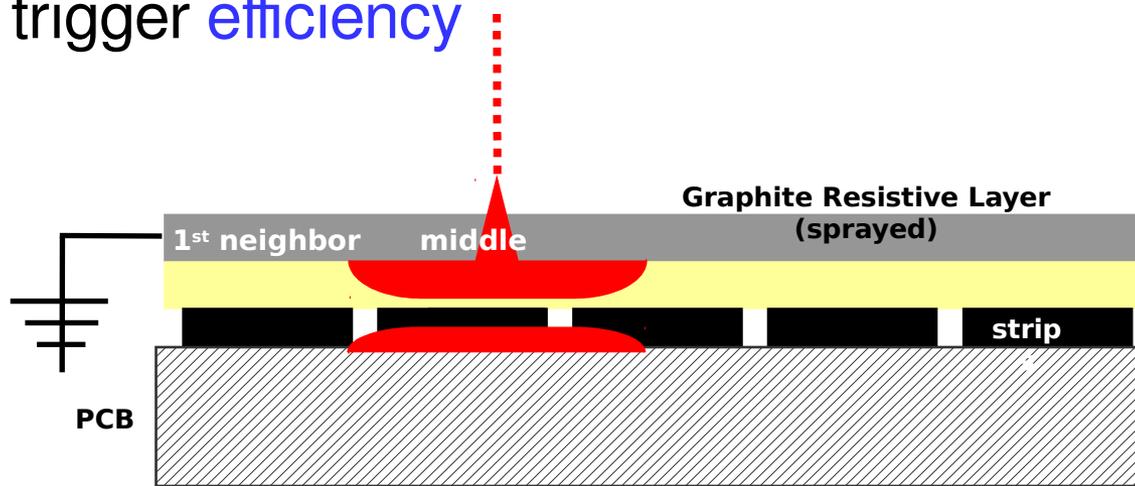


Resistive
layer



Electronics
response

- Simulate **full waveform** of signal on strips after the **VMM readout chip**
- Study of time delay associated with the **resistive layer** (carbon coating)
- Allows for **detailed trigger simulation**
- Investigate pad trigger **efficiency**

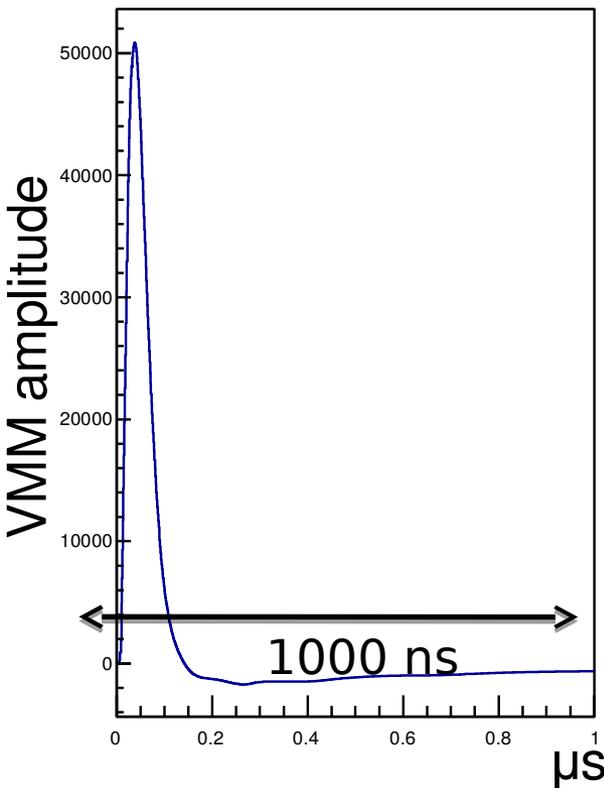


sTGC signal simulation

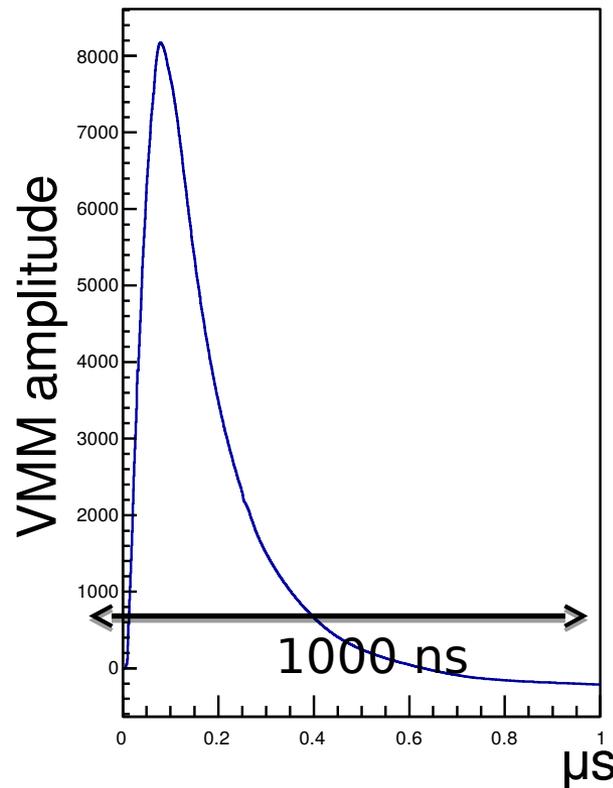


Shaped and amplified sTGC electronic signal versus time

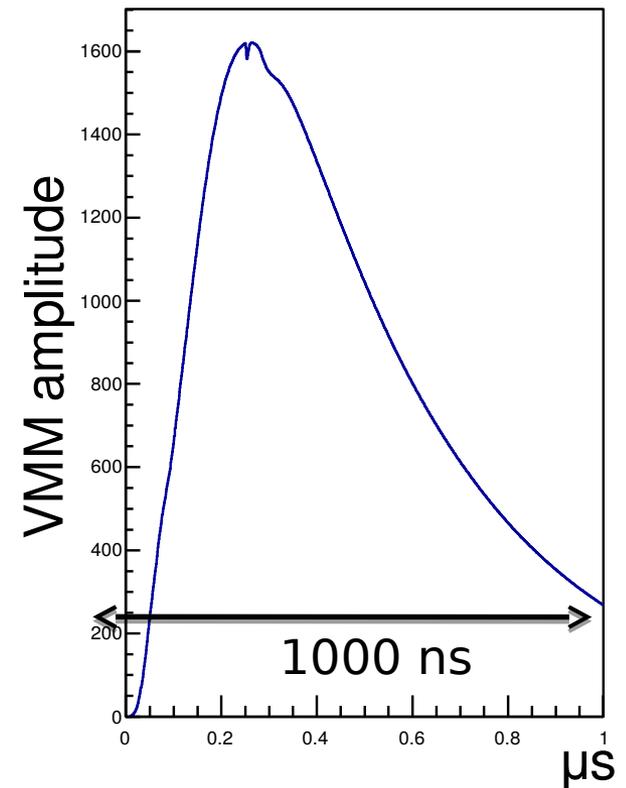
Strip main (middle)



Strip (1st neighbor)



Strip (2nd neighbor)



The charge signal time profile is **different on each strip**
This will be reflected in the simulation

sTGC timing simulation



Need to assign BCID: detector electronics will determine which **bunch crossing (BC)** a digitized hit corresponds to

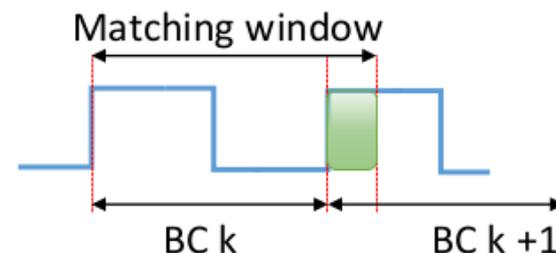
Start with a **global hit time** for Geant4 and account for several **Physical timing effects:**

- Time of flight (**ToF**) = (global hit position)/(speed of light)
- Detector Jitter (**J_d**): *statistical* fluctuation from **charge drift time**
- Electronic Jitter (**J_e**): *statistical* fluctuation of **readout electronics**
- Strip propagation time (**SPT**): time for signal to **propagate to the readout** down a strip

$$\text{Digit time} = \text{global hit time} - \text{ToF} + J_d + J_e + \text{SPT}$$

Then BCID is determined:

- 25 ns < (Digit time) < 5 ns → **Previous BC**
- 0 ns < (Digit time) < 30 ns → **Current BC**
- 25 ns < (Digit time) < 55 ns → **Next BC**



sTGC Deadtime Simulation

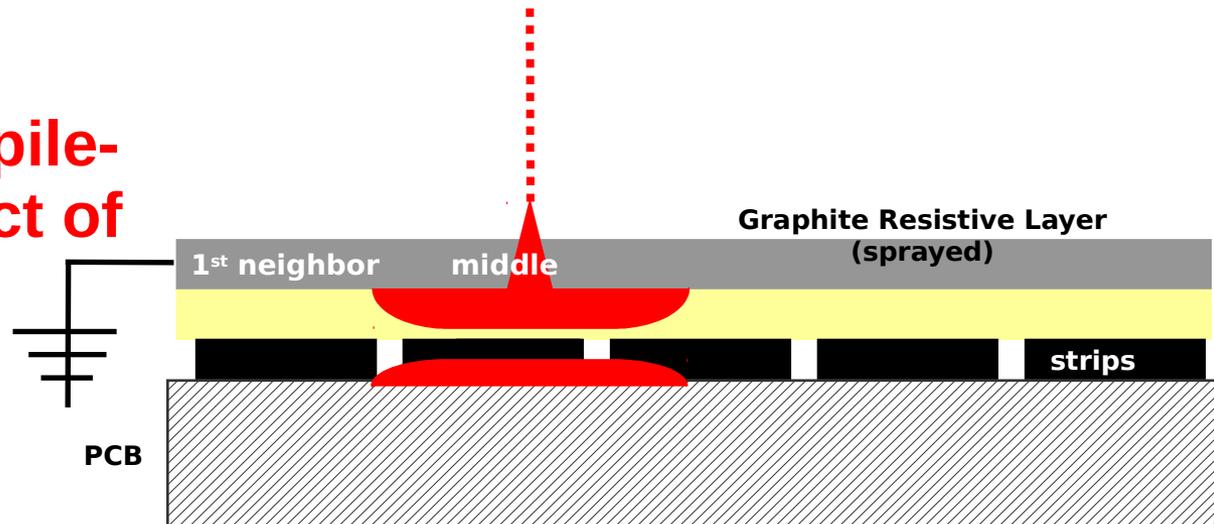


Hit deposited on sTGC channel

Charge is converted by ADC in **VMM readout chip**
Takes **~250 ns** for strip channel (precise 10 bit ADC)
~140 ns for pad channel (6 bit ADC)

2nd hit arrives within *digitization time window* -> **channel is dead**

Must simulate with pile-up to study the effect of this deadtime!



Pile-up Digitization



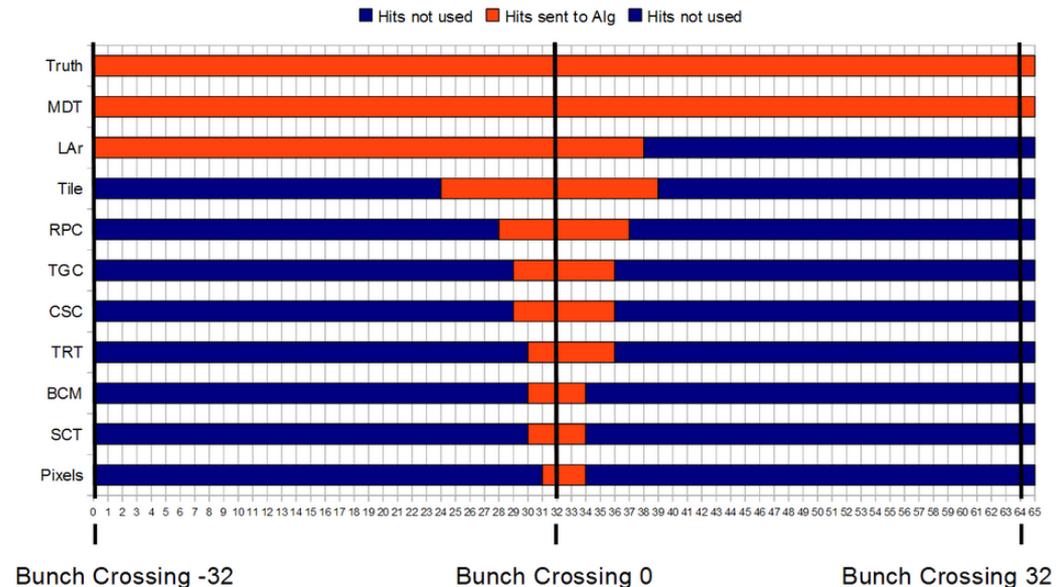
Pile-up events are sourced from separate input samples
2 types of pile-up events: **low pT** (abundant) and **high pT** (rare)

Pile-up events are included from a set number of **BC** before and after the **current BC**

For **sTGC** the electronics deadtime of the **strip** digitization is **~250 ns**
-> Need to consider pile-up from at least 10 BC (225 ns)

Bunch structure will affect **deadtime**

More time between filled bunches
-> **less deadtime due to pile-up**



Code for pile-up deadtime is *in place and functional*; need to **determine parameters** and **validate**



- LHC upgrades provide the opportunity to **really improve** our knowledge of the Higgs boson, the Standard Model and the search for new physics
- However, in its current state **ATLAS** would be unable to take **full advantage** of these opportunities
- The first full scale **sTGC** module meets the specification with single-hit spatial resolution ($\sigma = 45 \pm 8 \mu\text{m}$)
- **sTGC** digitization simulation is underway to test whether pile-up induced electronics **deadtime** will be acceptable

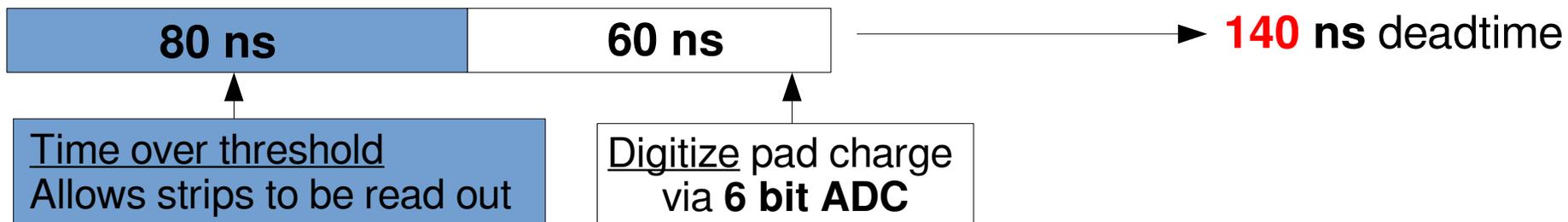


Backup

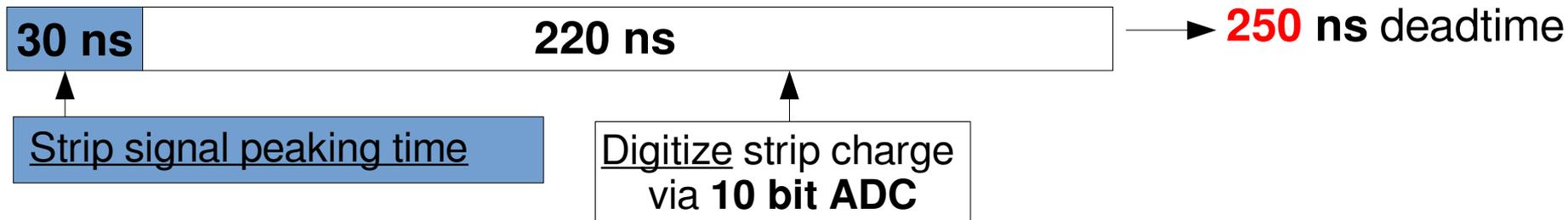
sTGC deadtime simulation



Pad deadtime structure



Strip deadtime structure



Neighbor on mode will add another strip on each end of the cluster
Strips activated by **neighbor on mode** will be dead for ~**250 ns** as well

Neighboring strip channels **will be delayed**, time for the charge to diffuse in the resistive layer —> **longer deadtime**

Pile-up event rate in HL-LHC



Rough estimation:

Inelastic cross section assumed: 70 mb

HL-LHC luminosity assumed: 7.0×10^{34} Hz/cm²

Event rate = Luminosity * Cross section.

$$\longrightarrow (70 \times 10^{-27} \text{ cm}^2) \times (7.0 \times 10^{34} \text{ Hz/cm}^2) = 4900 \text{ MHz}$$

Head-on meetings between bunches at every collision point occur every 25 ns \longrightarrow 40 MHz

But, the entire ring is not filled with bunches

$$\langle \text{crossing rate} \rangle = \text{number of bunches} \times \text{revolution frequency} = 2808 \times (3 \times 10^8 \text{ m/s}) / (26.73 \times 10^3 \text{ m}) = 31.5 \text{ MHz} = 1/(31.7 \text{ ns})$$

Thus, the average bunch spacing in the LHC in real life is ~32 ns
(4900 MHz/31.5 MHz) \approx **160 events per bunch crossing**