Electronics Development for the ATLAS Liquid Argon Calorimeter - Trigger and Readout for Future LHC Running -

Steffen Stärz

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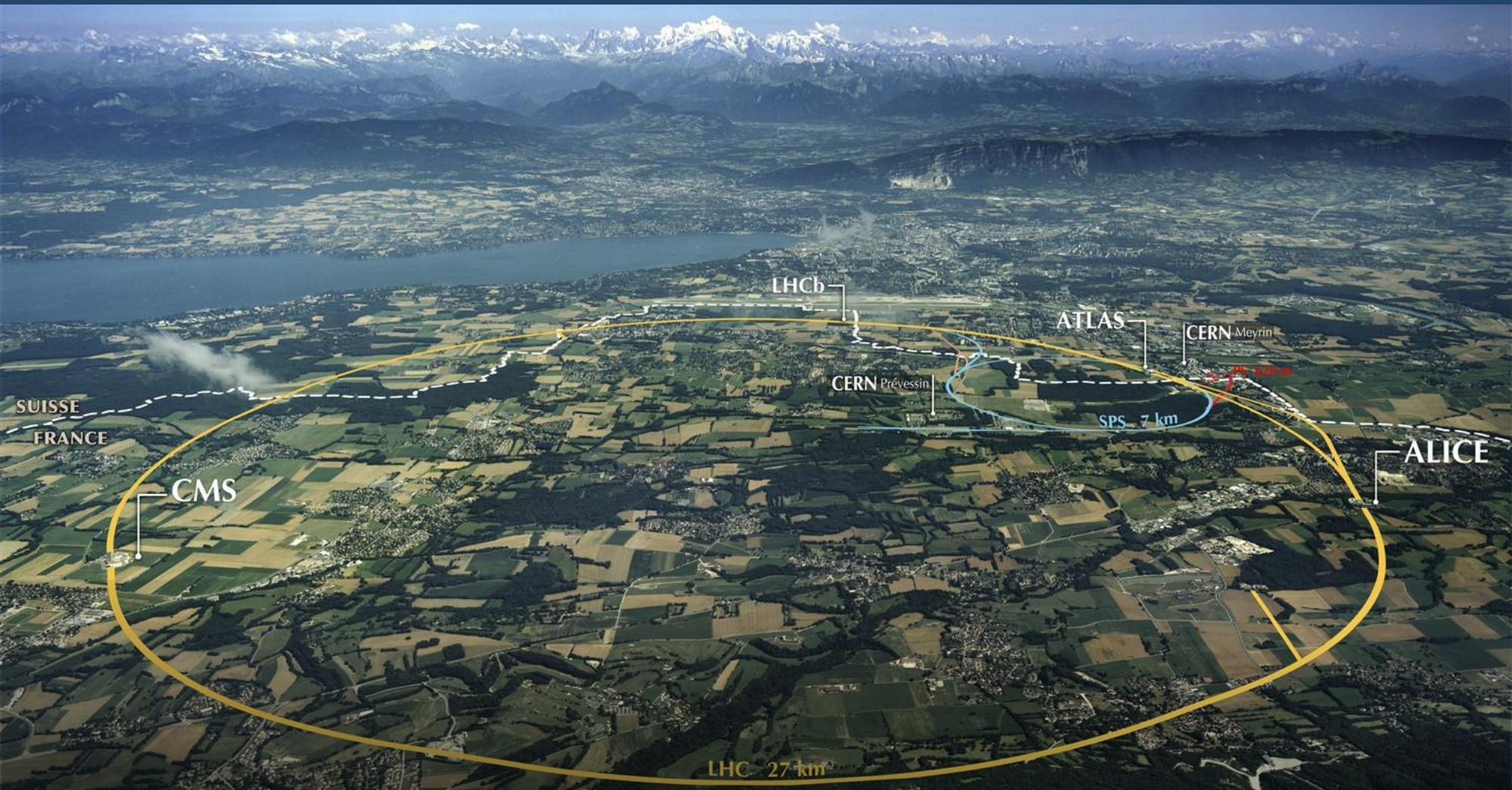
18 May 2016
Daegu, Republic of Korea

Outline

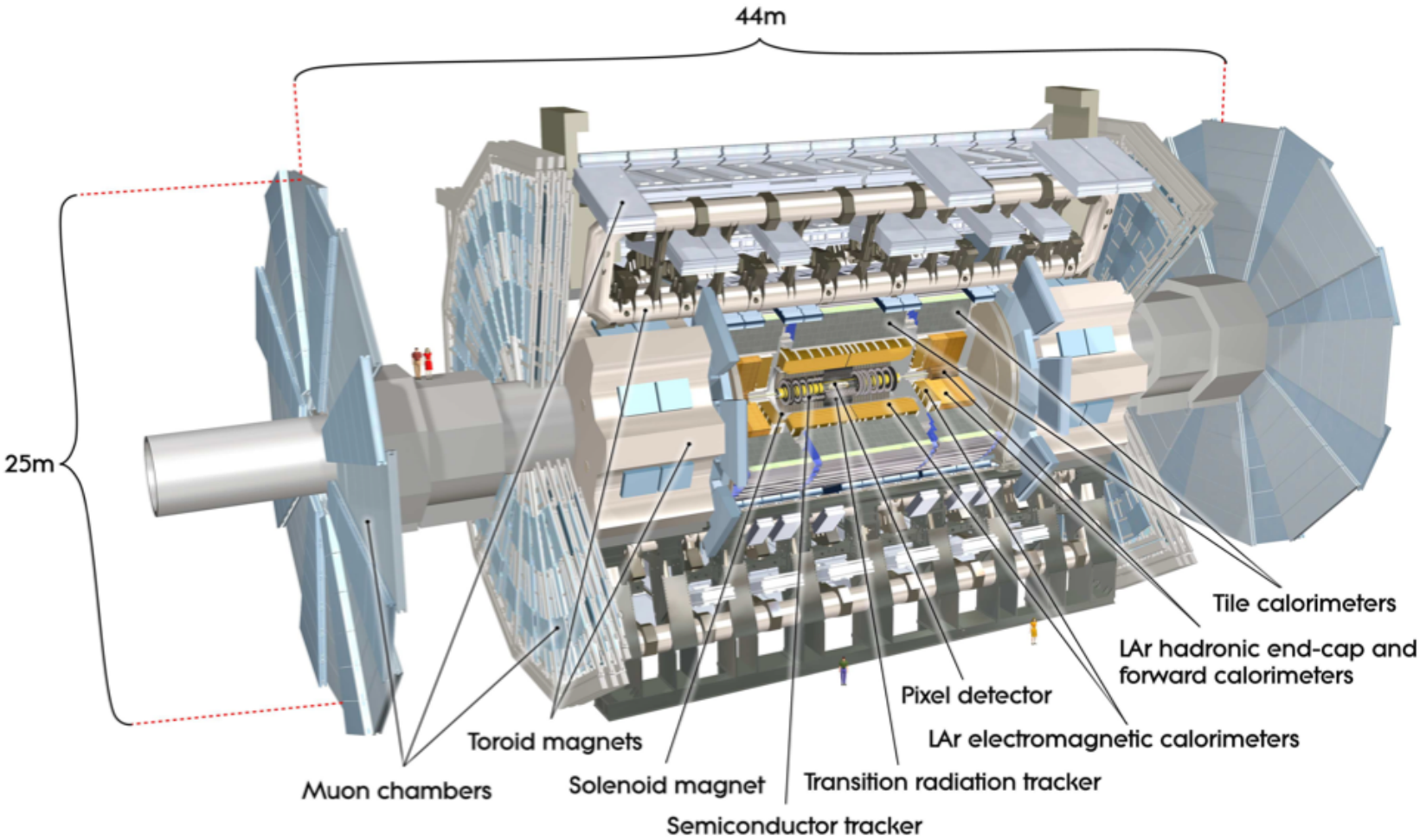
The Large Hadron Collider (LHC) design values



Center of mass energy: $\sqrt{s} = 14\ \mathrm{TeV}$ Collision rate: $f_{\mathrm{LHC}} = 40\ \mathrm{MHz}$

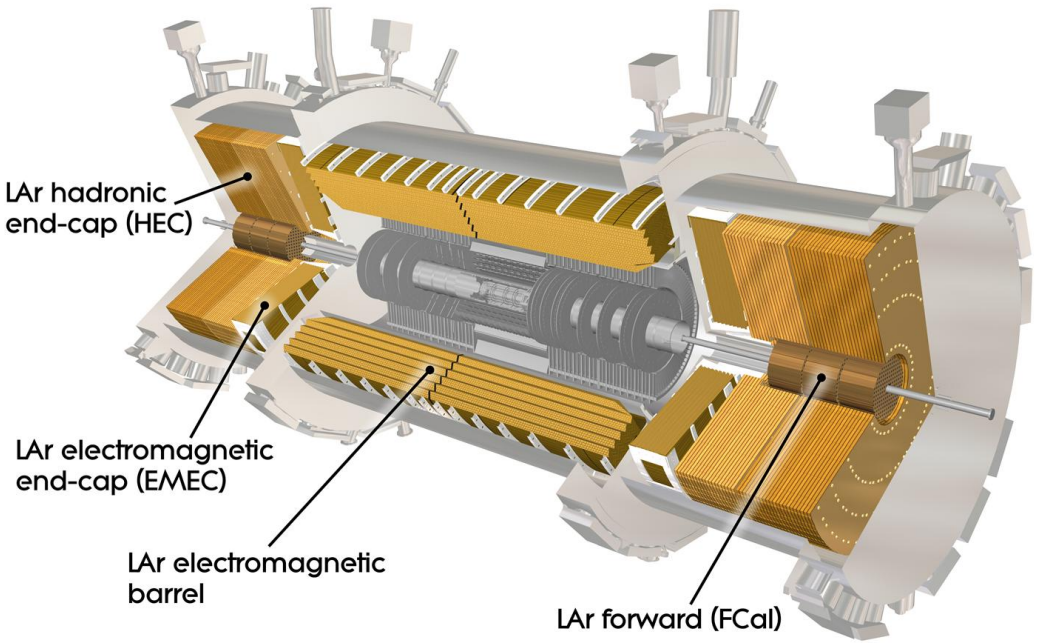
Luminosity: $\mathcal{L} = 10^{34}\ \mathrm{cm}^{-2}\mathrm{s}^{-1}$ Protons per bunch: $\approx 115 \times 10^{9}$

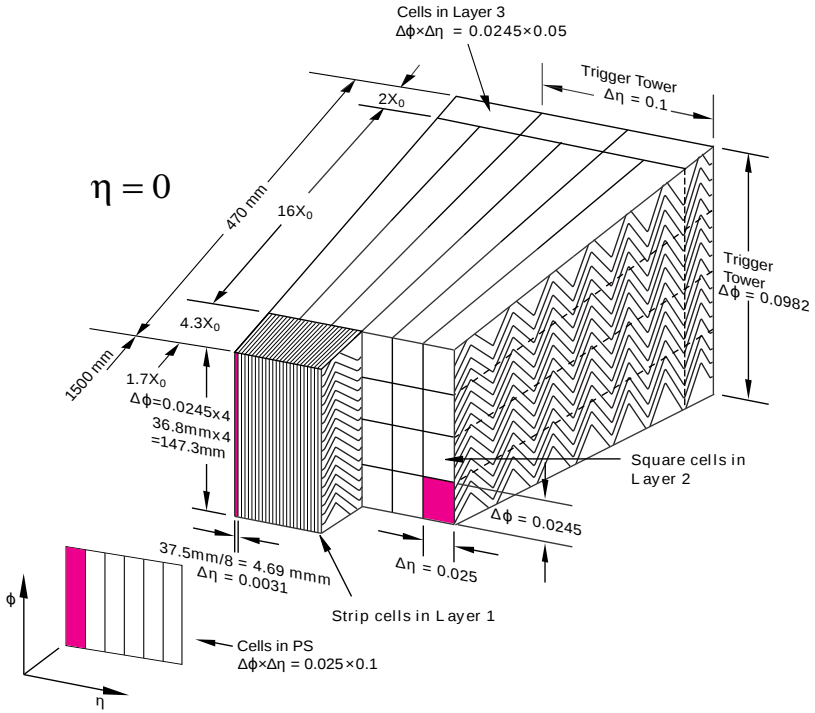
The ATLAS Detector



trigger-based multi purpose detector, ca. 88 M readout channels
(Pixel: 80.4; SCT: 6.3; LAr: 0.2; Muon: 1 [millions])

The ATLAS Liquid Argon Calorimeter

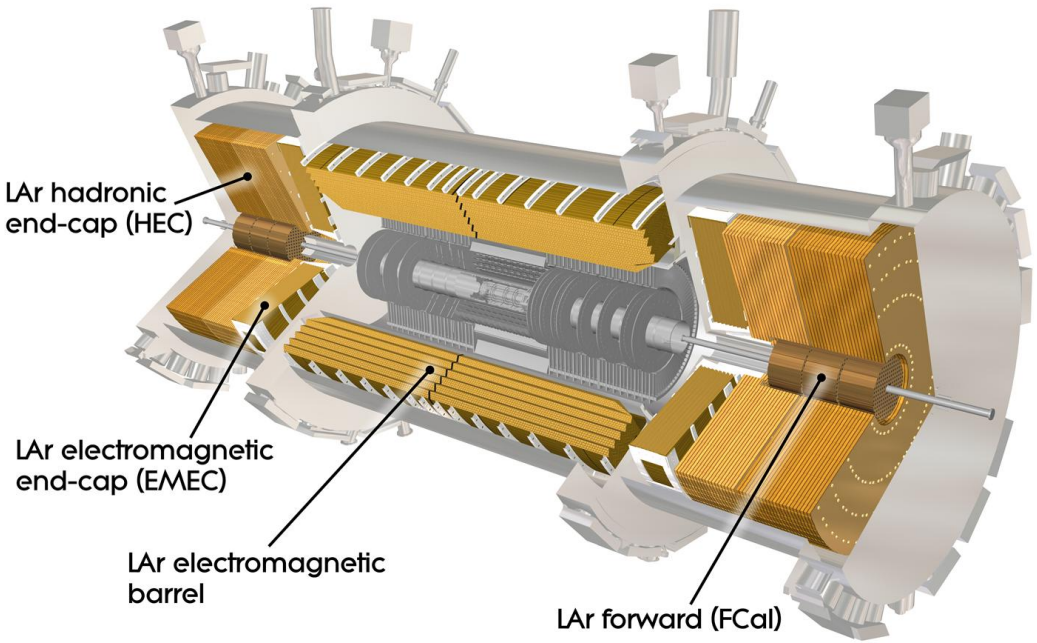


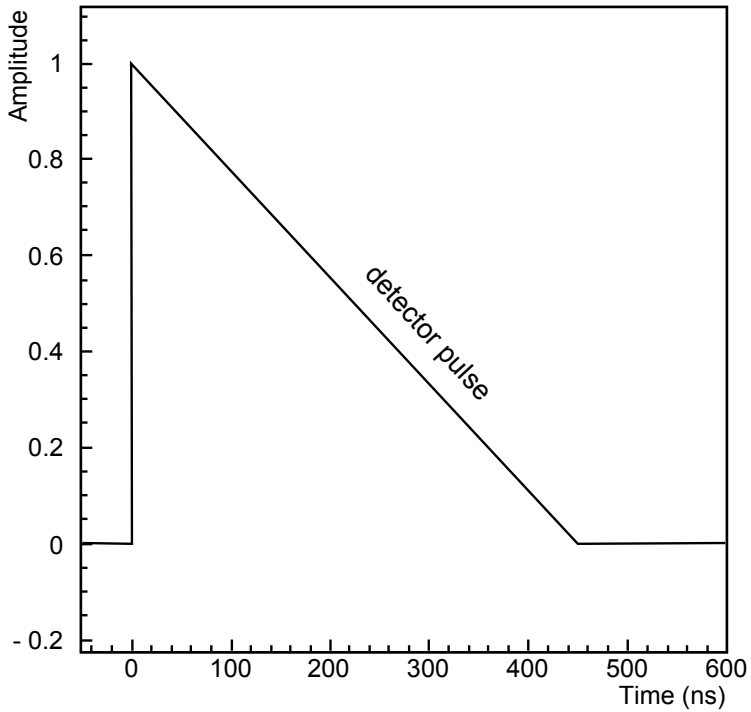


- Sampling calorimeter
- 182468 single detector cells

- Absorber: Pb; Active: Liquid Ar
- Total radiation length: 22 X_0
- 4 layers, different spacial resolution

The ATLAS Liquid Argon Calorimeter

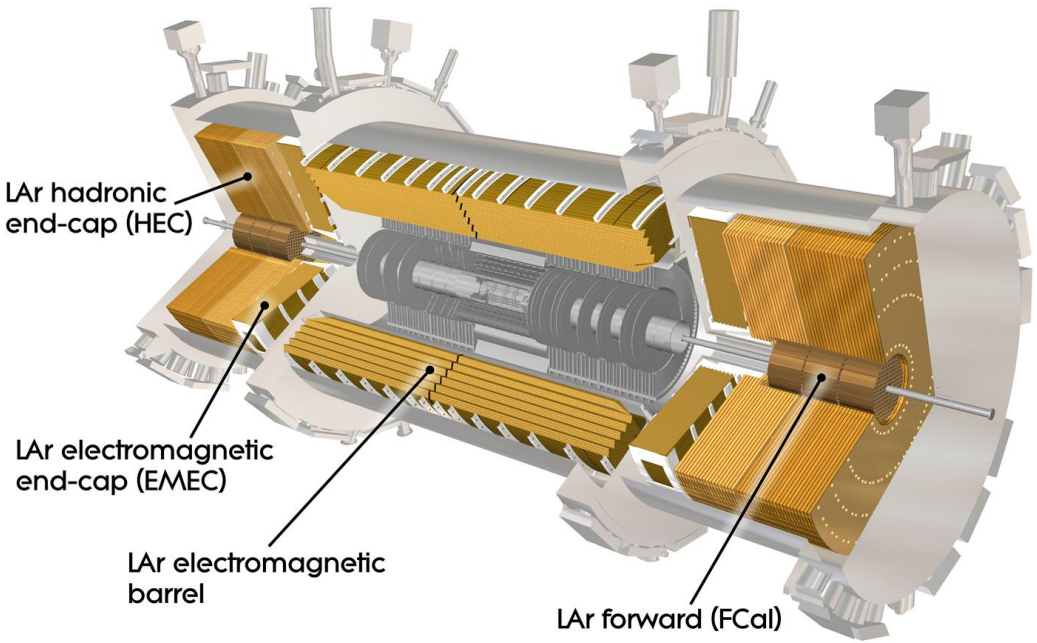


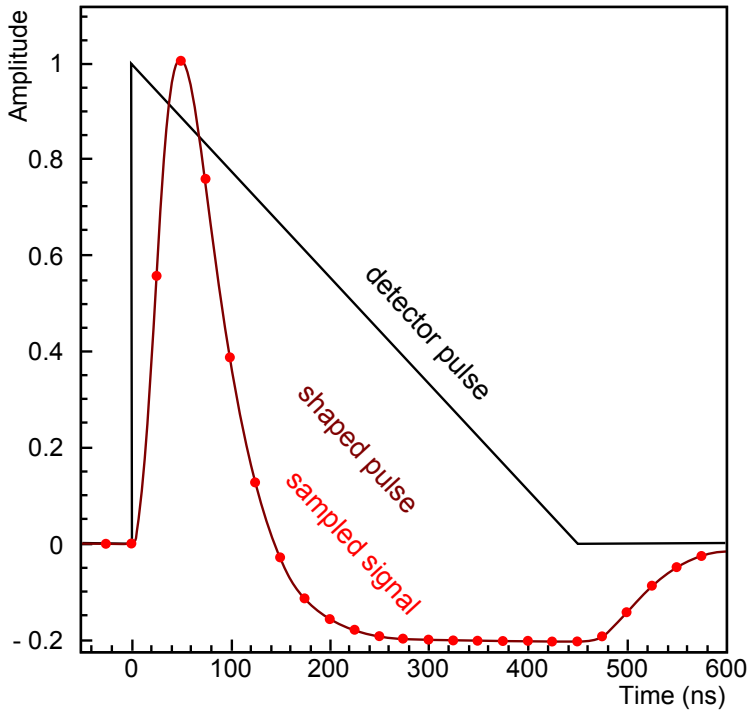


- Sampling calorimeter
- 182468 single detector cells

- Absorber: Pb; Active: Liquid Ar
- Total radiation length: 22 X_0
- 4 layers, different spacial resolution
- Feeds the Level-1 Trigger system

The ATLAS Liquid Argon Calorimeter

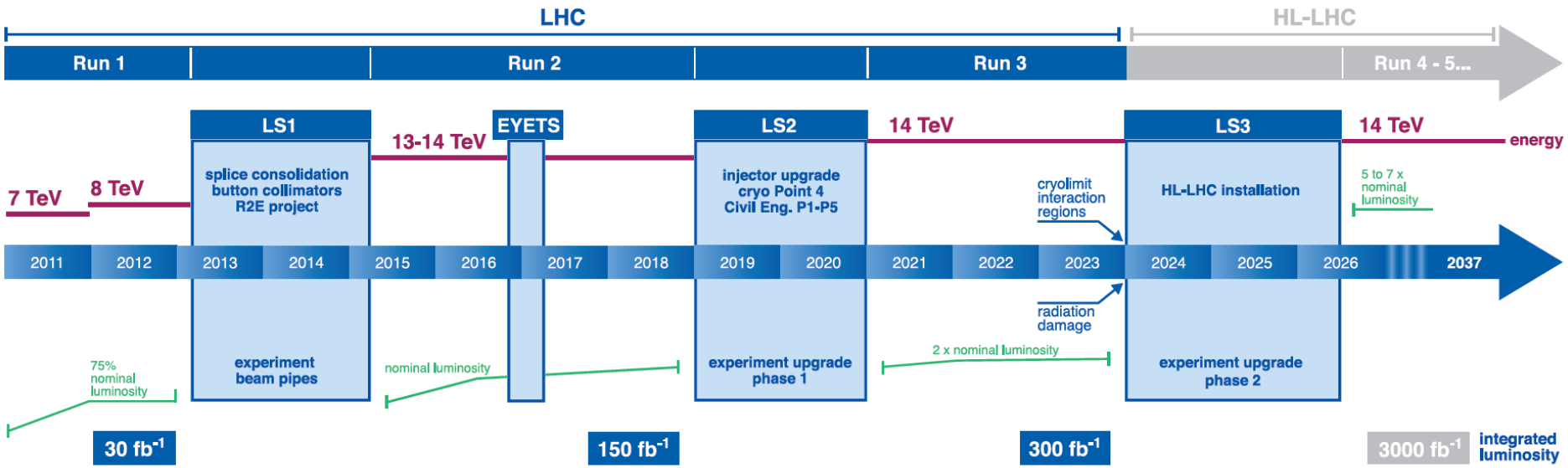




- Sampling calorimeter
- 182468 single detector cells
- energy reconstruction by pulse shaping and sampling

- Absorber: Pb; Active: Liquid Ar
- Total radiation length: 22 X_0
- 4 layers, different spacial resolution
- Feeds the Level-1 Trigger system
- readout of samples each 25 ns

Forseen schedule: From LHC to HL-LHC



LS2: Phase-I Upgrade goals

- $\mathcal{L} \cong 3 \times 10^{34}\ \mathrm{cm}^{-2}\mathrm{s}^{-1}$
- $\langle \mu \rangle \cong 80$
- Keep trigger (max) 100 kHz; latency $\leq 3\ \mu\mathrm{s}$

Upgrade of LAr trigger readout

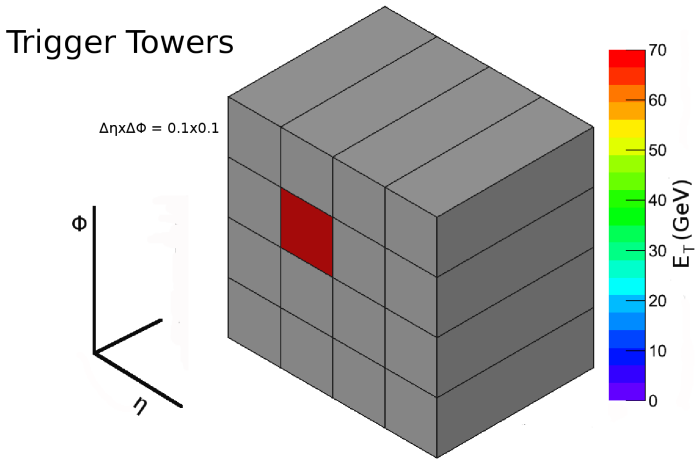
LS3: Phase-II Upgrade goals

- $\mathcal{L} \cong 7.5 \times 10^{34}\ \mathrm{cm}^{-2}\mathrm{s}^{-1}$
- $\langle \mu \rangle \cong 200$
- Upgrade trigger to 1 MHz; latency $\leq 10\ \mu\mathrm{s}$

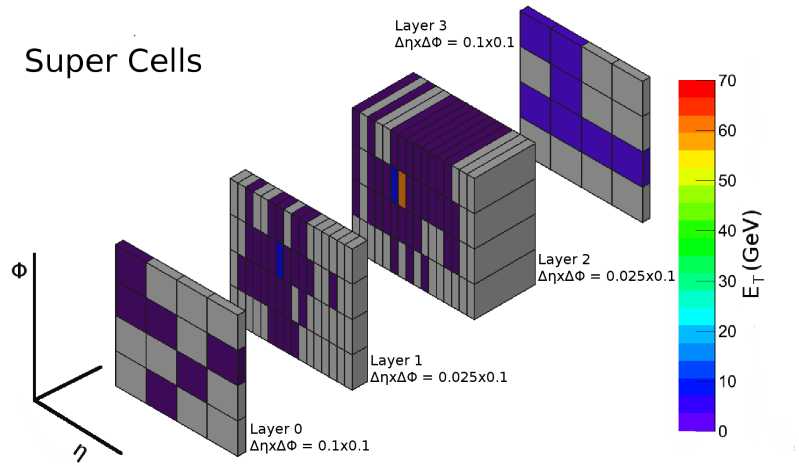
Upgrade of LAr main readout*

* and possible replacement of LAr forward calorimeter and addition of a high granularity timing detector

Phase-I: From Trigger Towers to Super Cells



(a) Current: 1 TT in $\eta \times \phi = 0.1 \times 0.1$



(b) Upgraded: 10 SCs in 0.1×0.1

Figure: e^- at $E_T = 70$ GeV: Granularity increase in barrel for Level-1 trigger electronics from current to upgraded scenario to maintain (or improve) trigger performance in high luminosity and high pile-up conditions

- Apply offline reconstruction algorithms already at Level 1
- Improves: jet rejection capability, isolation, electron reconstruction
- Ensure forward compatibility with HL-LHC and Phase-II upgrade

LAr Phase-I Upgrade Plan

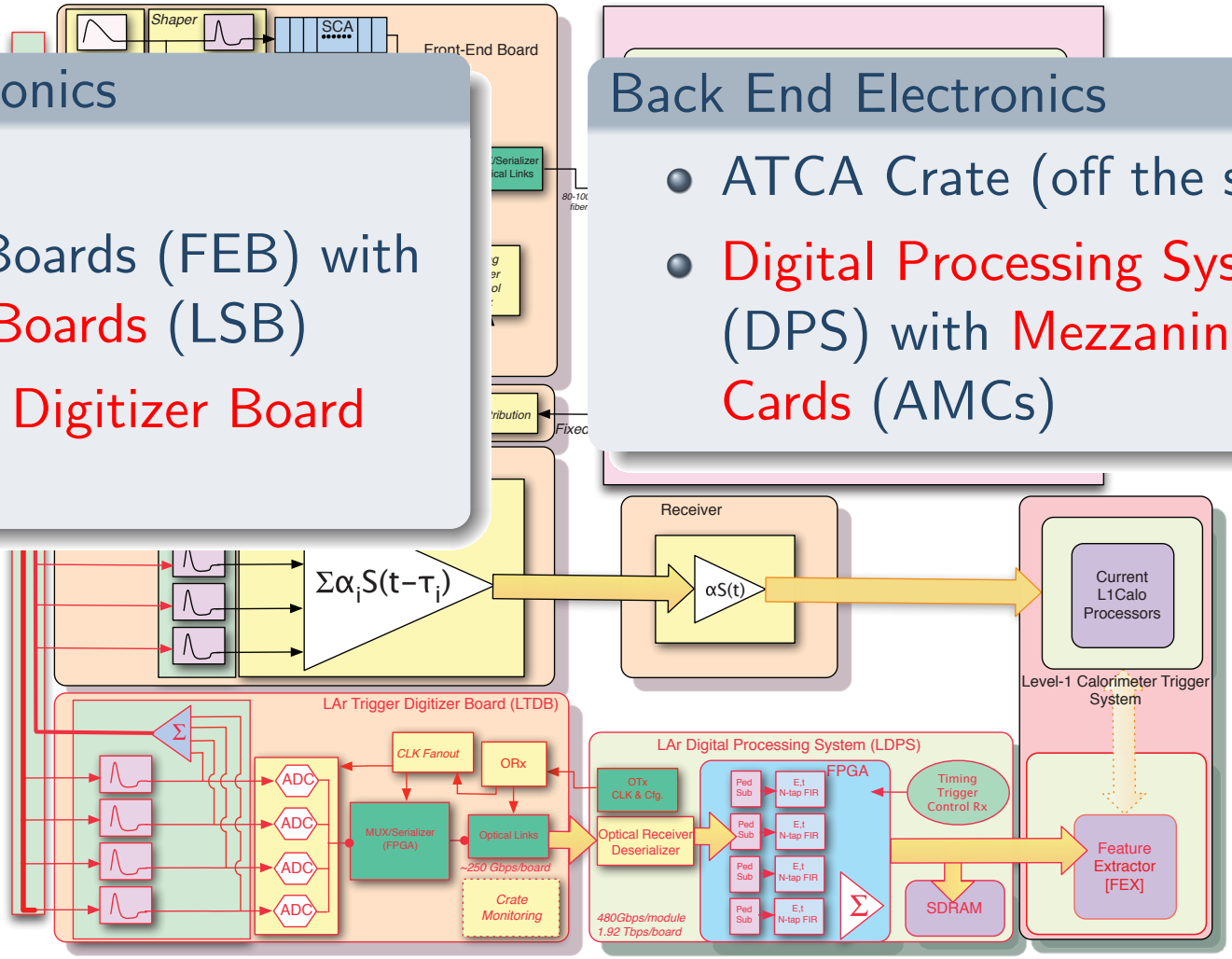
New readout electronics to feed digitized data to L1 trigger

Front End Electronics

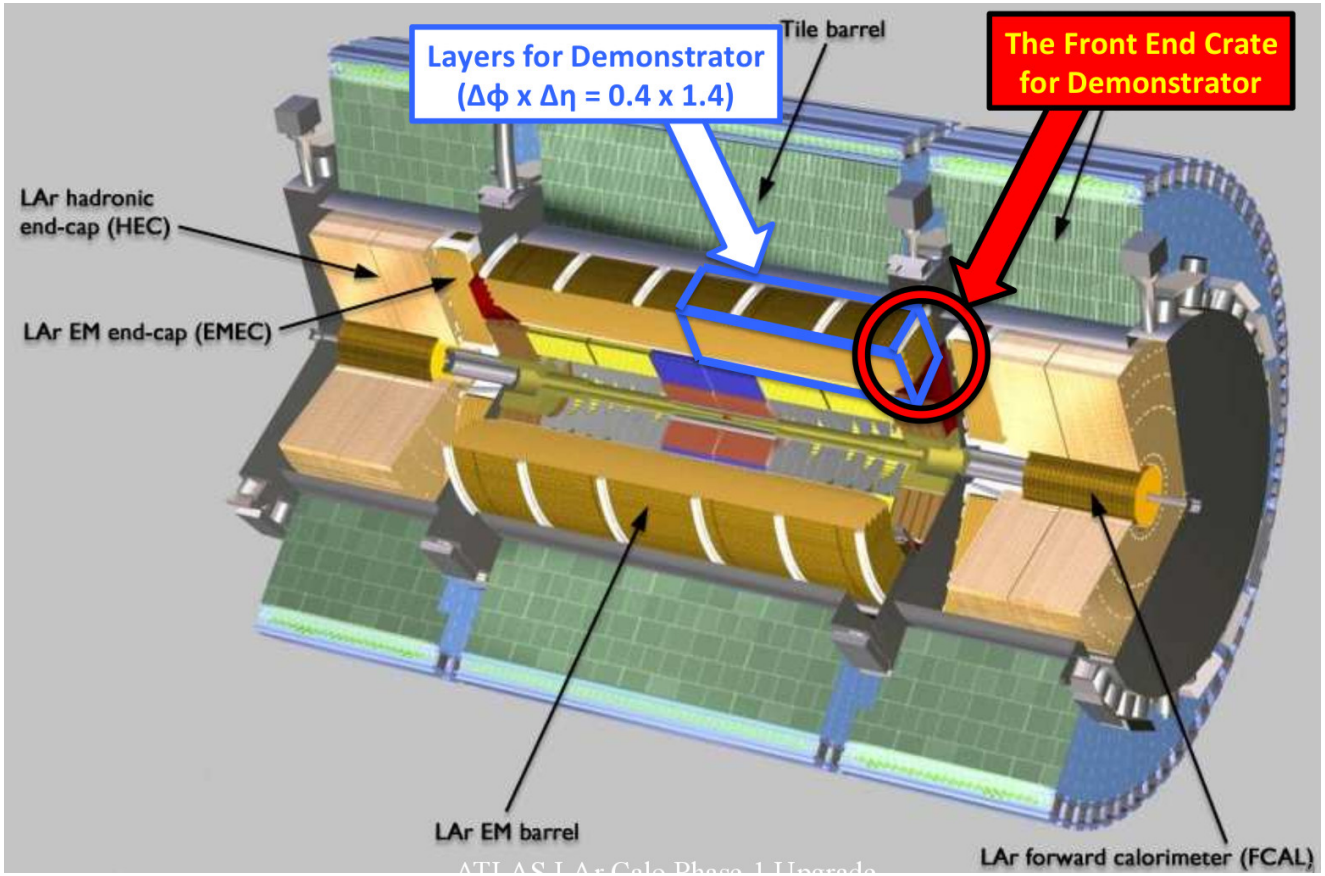
- Baseplane
- Front End Boards (FEB) with Layer Sum Boards (LSB)
- LAr Trigger Digitizer Board (LTDB)

Back End Electronics

- ATCA Crate (off the shelf)
- Digital Processing System (DPS) with Mezzanine Cards (AMCs)



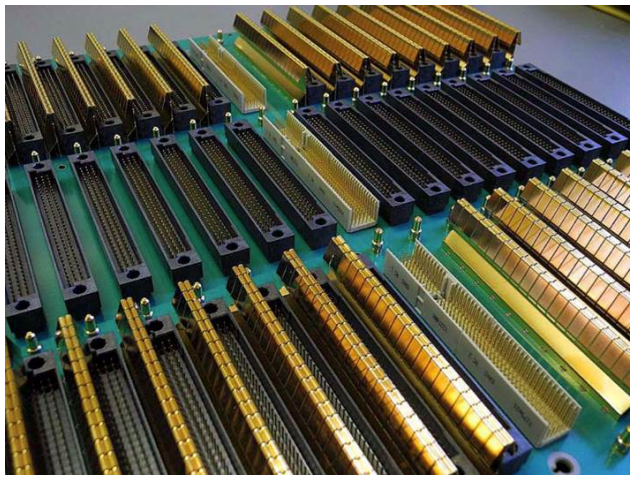
LAr Demonstrator - Where is it?

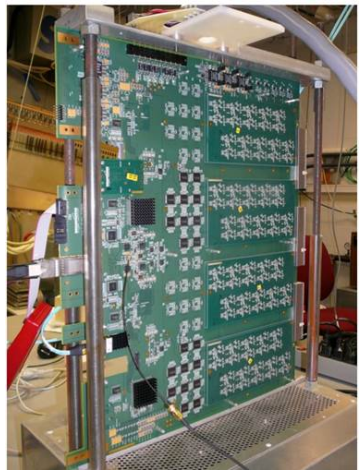


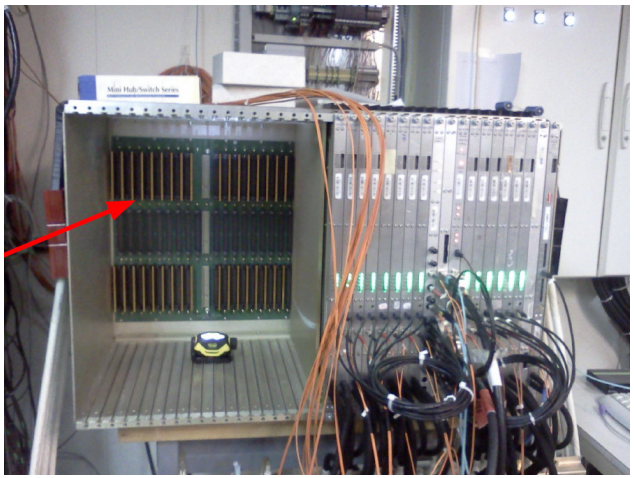
- ATLAS review and approval in May 2014
- Installation of Demonstrator in summer 2014

LAr Demonstrator Front End electronics

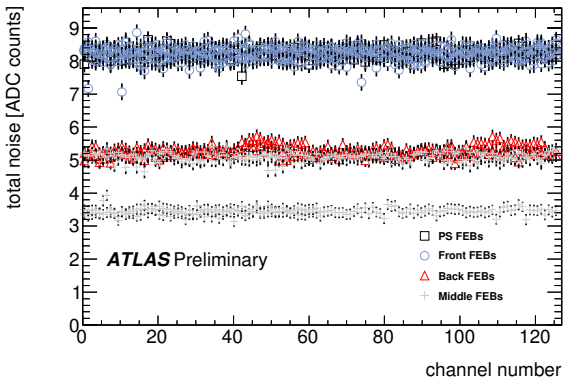
New Baseplane tested at CERN, populated with FEBs and LTDB





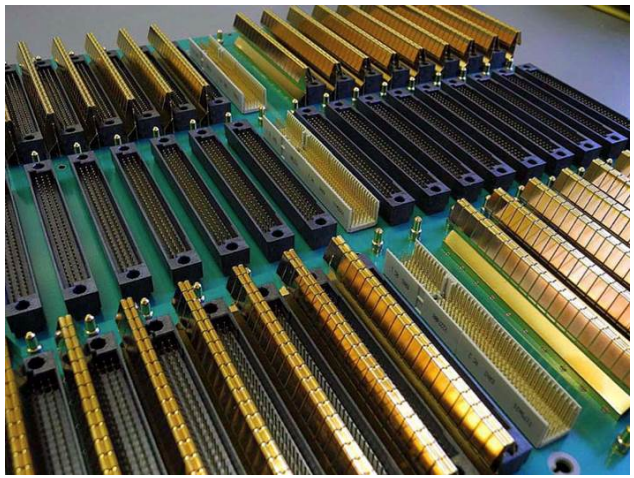


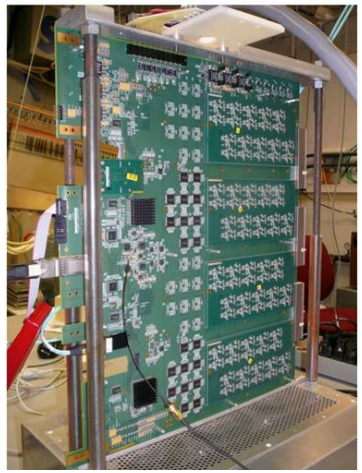
- ✓ Processing properly and operational
- ✓ Same total noise levels for trigger (150 . . . 250 MeV)
- ✓ Same cross-talk across trigger towers
- ✓ Linearity satisfies ATLAS requirements

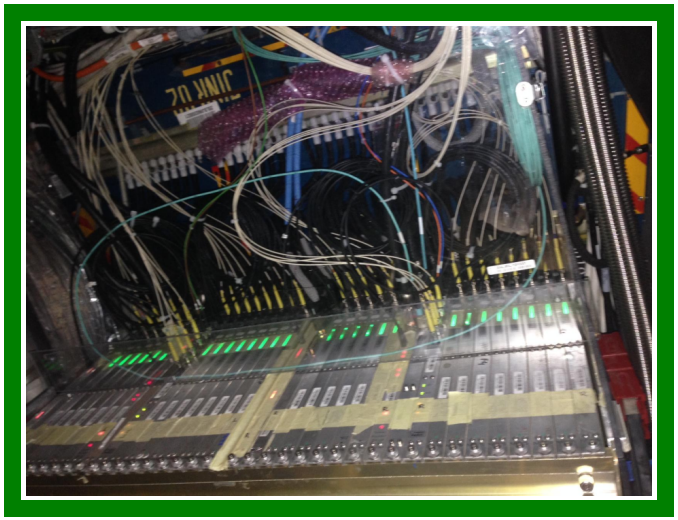


LAr Demonstrator Front End electronics

New Baseplane tested at CERN, populated with FEBs and LTDB







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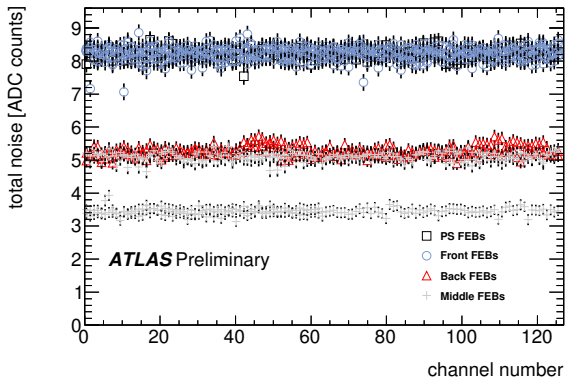
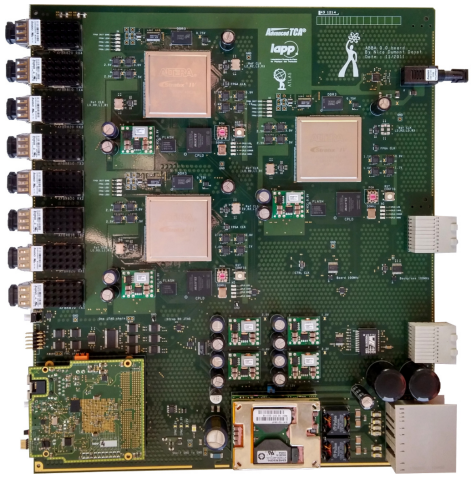
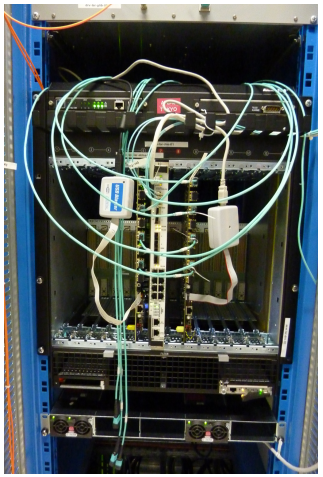


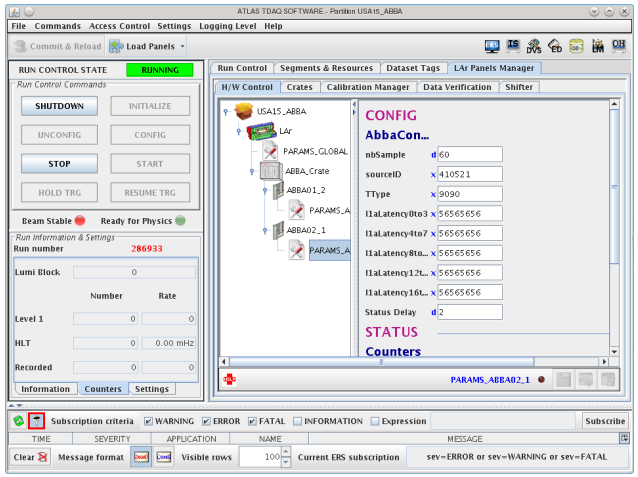
⇒ No impact on analog trigger and standard readout ⇒ 2014: Deployed in pit

LAr Demonstrator Back End electronics

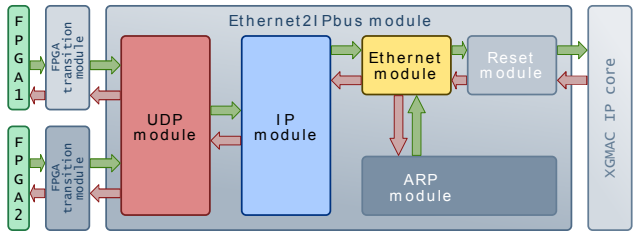
ABBA (prototype DPS) in ATCA crate, populated: 3 Stratix IV FPGAs







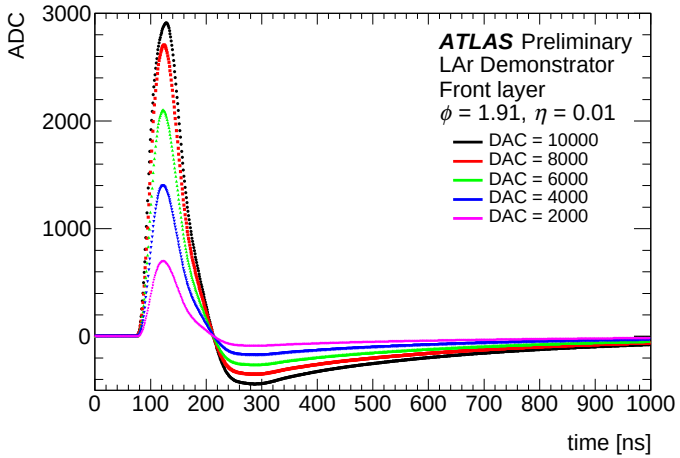
- ✓ 40 fibers receive data of 320 Super Cells: 40×5.12 Gbps $= 208.4$ Gbps
- ✓ ATCA crate with commercial 10 GbE switch
- ✓ Readout by ATLAS LAr TDAQ software via interface to ABBA using IPBUS protocol over UDP on 10 GbE network



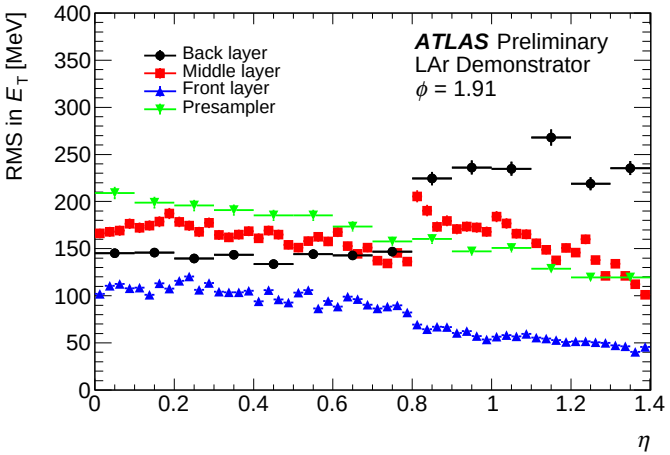
⇒ Concurrent readout of demonstrator region in parallel to ATLAS default readout since October 2015 thanks to dedicated "L1Topo" trigger item

First results from the LAr demonstrator

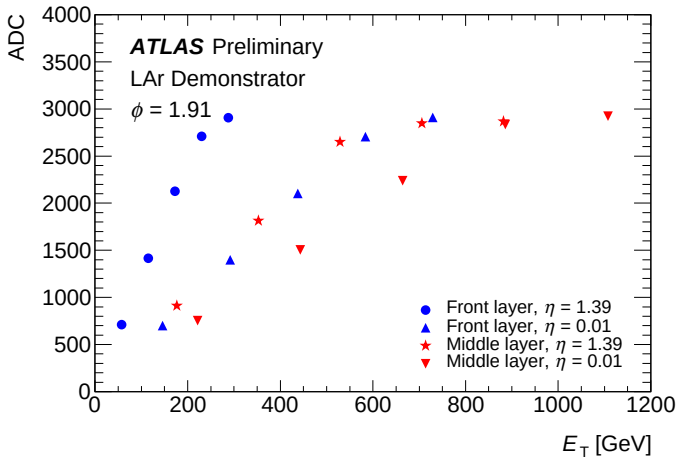
Calibration pulse shape



Noise levels of SCs



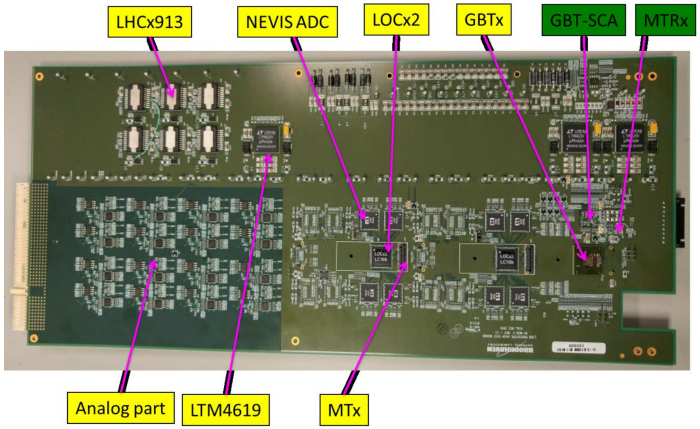
Pulse maximum vs. transverse energy



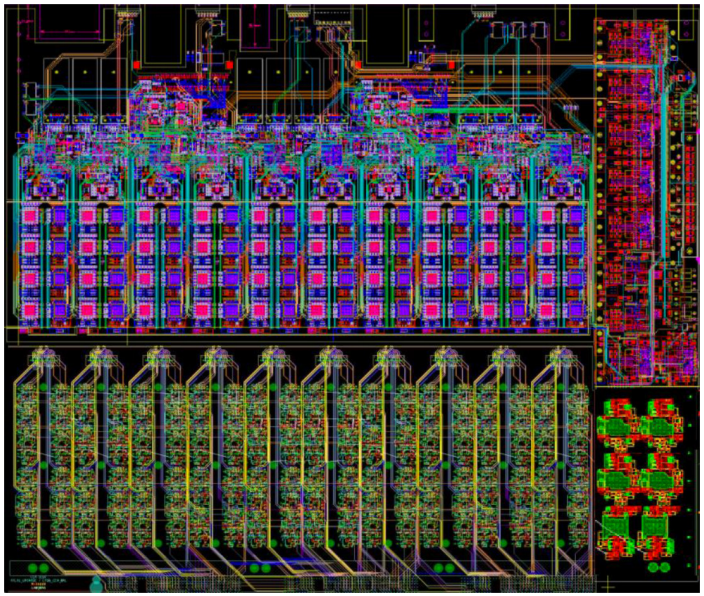
✓ Successful data taking in 2015 pp and HI runs

Phase-I Front End Electronics

64-ch LTDB prototype (back side)

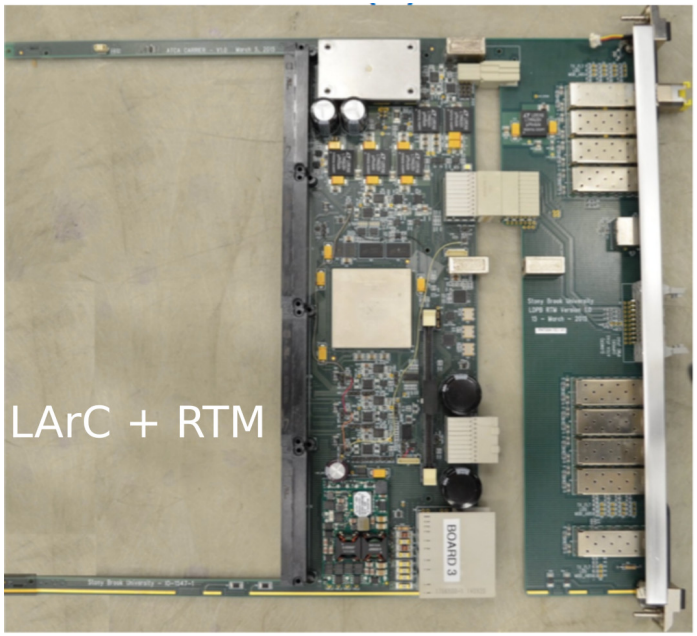


320-ch LTDB prototype

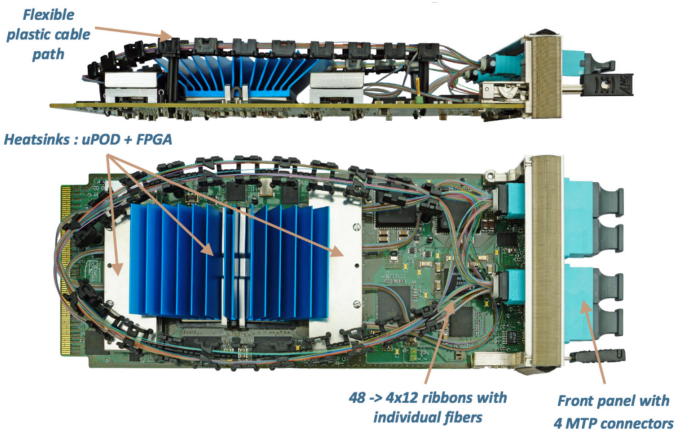


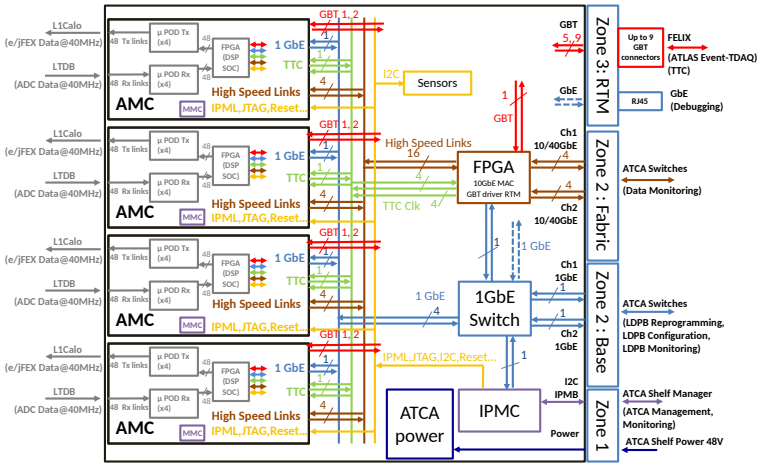
- ✓ Baseplane and LSBs: Prototypes produced and being tested
- ✓ ADC: Final prototypes produced and being tested on 64-ch LTDB
- ✓ Serializer LOCx2: iteration with SoS foundry, final production ongoing and fallback ASIC (130 nm CMOS) under design
- ✓ 64-ch LTDB prototype: operational, used to test ASIC components
- ✓ 320-ch LTDB prototype: integration of digital and analog part is manufactured
- Final 320-ch LTDB: Compound of 5 × 64-ch prototype, expected 09/2016

Phase-I Back End Electronics

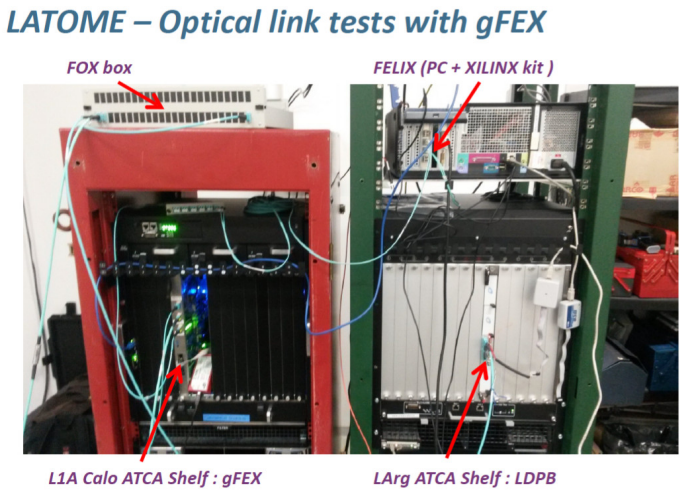


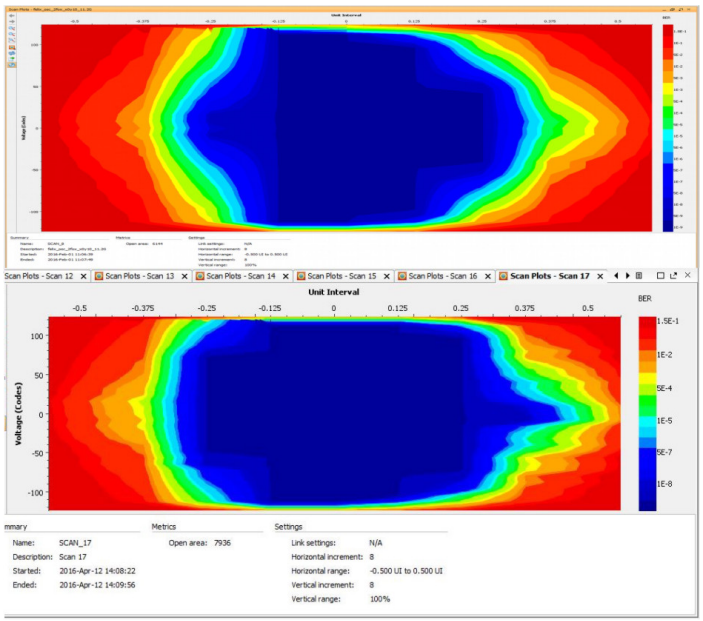
- LArCarrier: ATCA custom board
  - ✓ Integration tests with LATOME OK
  - ✓ Carrier v2 tested and working well
- LAr Trigger prOcessing MEzzanine
  - First prototype with ARRIA-10 FPGA
  - 3 pre-prototypes have been produced
  - ✓ Fully tested and working as expected
  - Various optical link speeds available: 6.4, 9.6, 11.2, 12.5 and 12.8 Gbps
  - Firmware development well progressing





Phase-I Back End Electronics

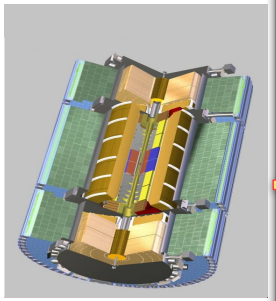


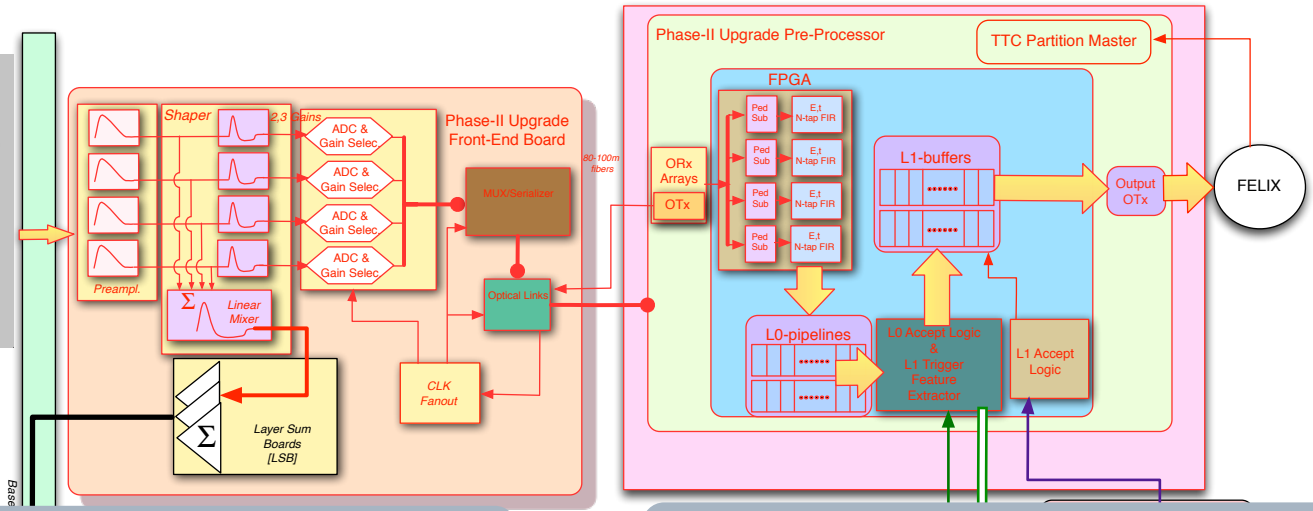


- Link Speed and integration test
  - Between calorimeter (LAr: sender) and trigger (L1Calo: receiver)
  - ATCA test setup at CERN
  - Goal: test 48 optical links from LATOME to e/gFEX
  - Exercise different clock architectures and setups of optical (fiber) spliters
  - ✓ Good eye opening and BER ($\leq 10^{-14}$), baseline speed adopted to 11.2 Gbps after both link speed tests

LAr Phase-II Upgrade Plan

New readout electronics for fully digitized data to trigger and DAQ





Front End Electronics

Front End Boards 2 (FEB2s) with Layer Sum Boards (LSBs)

Back End Electronics

LAr Pre-PRocessor Boards (LPPR) feeding trigger system

Motivation

FEB analog pipeline restricts Level-I latency to 3 μs

Level-1 accept rate limited to 100 kHz

Radiation hardness requirements for Phase-II: factor 3 above original design

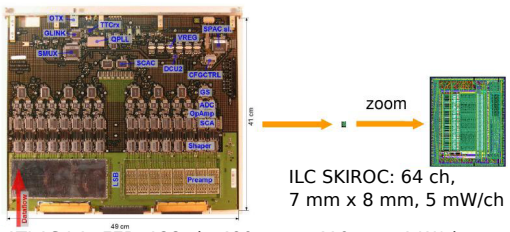
Phase-II Front-End Electronics Plans

New Front End Boards - Challenges

- 1524 FEBs (each up to 128 channels) to be replaced
- Amplification, shaping and digitization with 40 or 80 MHz
- Require at least 9 Gbps per fibre: serialisation and data transmission
- Allow higher latencies
  - up to 10 $\mu\mathrm{s}$ (L0 at 1 MHz) vs. up to 60 $\mu\mathrm{s}$ (L1 at 400 kHz)
- Choices under study
  - Bi-polar vs. uni-polar shaping (with option of moving shaping to digital domain)
  - 2 vs. 3 gain ranges (16 bit dynamic range)
  - 10 to 14 bit ADCs
  - Noise, Linearity
  - Digital filtering ("Optimal" Filtering, "Extended Optimal" Filtering, ...)
- Electronics Specifications Group formed in 2015

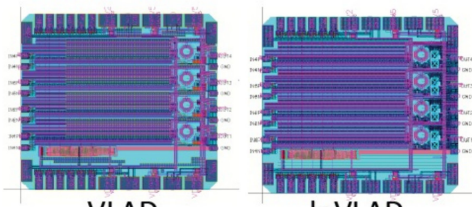
  $\Rightarrow$ Planning to converge on a baseline until second half of 2017

Phase-II First Prototypes



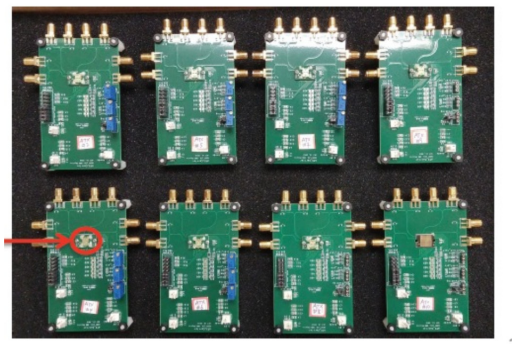
ILC SKIROC: 64 ch,
7 mm x 8 mm, 5 mW/ch

ATLAS LAr FEB: 128 ch, 490 mm x 410 mm, 1 W/ch



VLAD lpVLAD

Taped out on Feb. 7, 2016



Several produced and tested

- CMOS Front-End System On a Chip (FESOC)
  - ASIC of amplifier, shaper, ADC, serializer
  - Starting with development of components
- ADCs
  - 12 bit prototypes available
  - 14 bit developments started
  - TID radiation tests up to 10 kGy
- Optical Link and Serializer
  - Allow 2×14 bit per channel at 40 MHz
  - VCSEL Array Driver (VLAD) and low power VLAD in 65 nm TSMC CMOS technology
- New Back End Board (LPPR)
  - Phase-I LDPB as prototype: 4 high end FPGAs
  - Implementation of digital shaping and filtering (pile-up suppression)
  - Simulation software AREUS for filter studies being adapted for Phase-II

Summary

- HL-LHC tackled by Phase-I and Phase-II Upgrade
  - $\Rightarrow$ New LAr trigger and readout electronics
- "Phase-0": LAr demonstrator
  - Successful data taking in 2015 pp and HI runs
  - Ready for 2016 ATLAS data taking
- Phase-I
  - Final prototypes are being produced and tested
  - Fallback solutions available
  - On track for start of installation in 2019
- Phase-II
  - LAr Phase-II Upgrade activity gained momentum in recent years
  - Re-optimization of the readout and signal processing for high pile-up
  - Profiting from overlap with Phase-I Upgrade

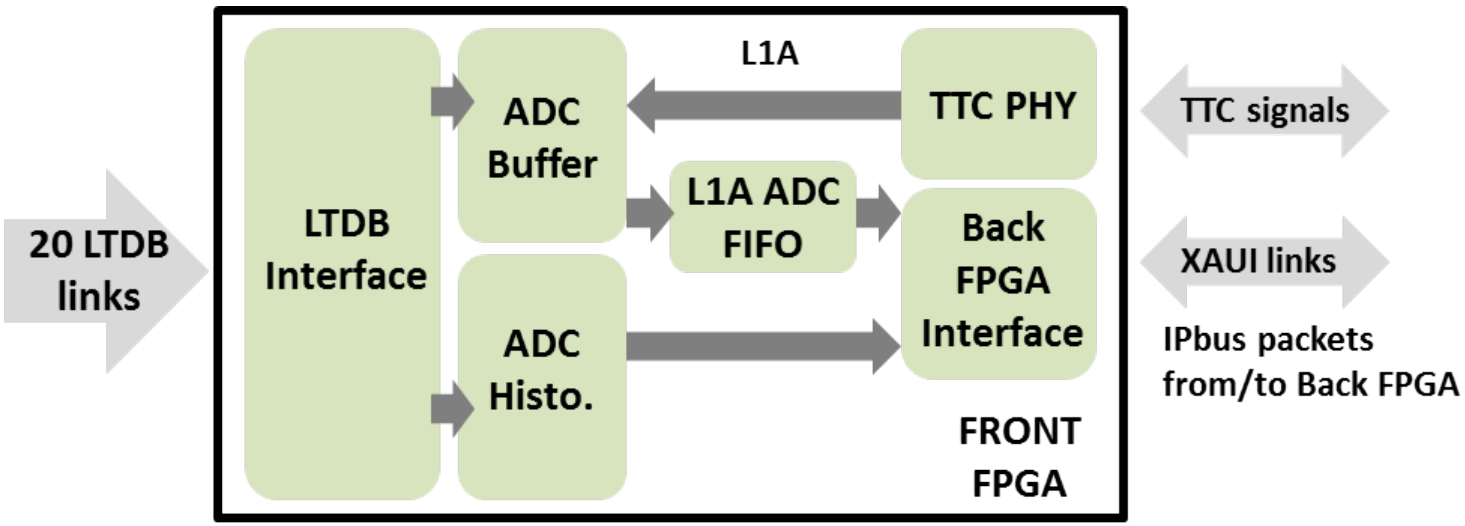
The last slide

Thanks for your attention!

Questions?

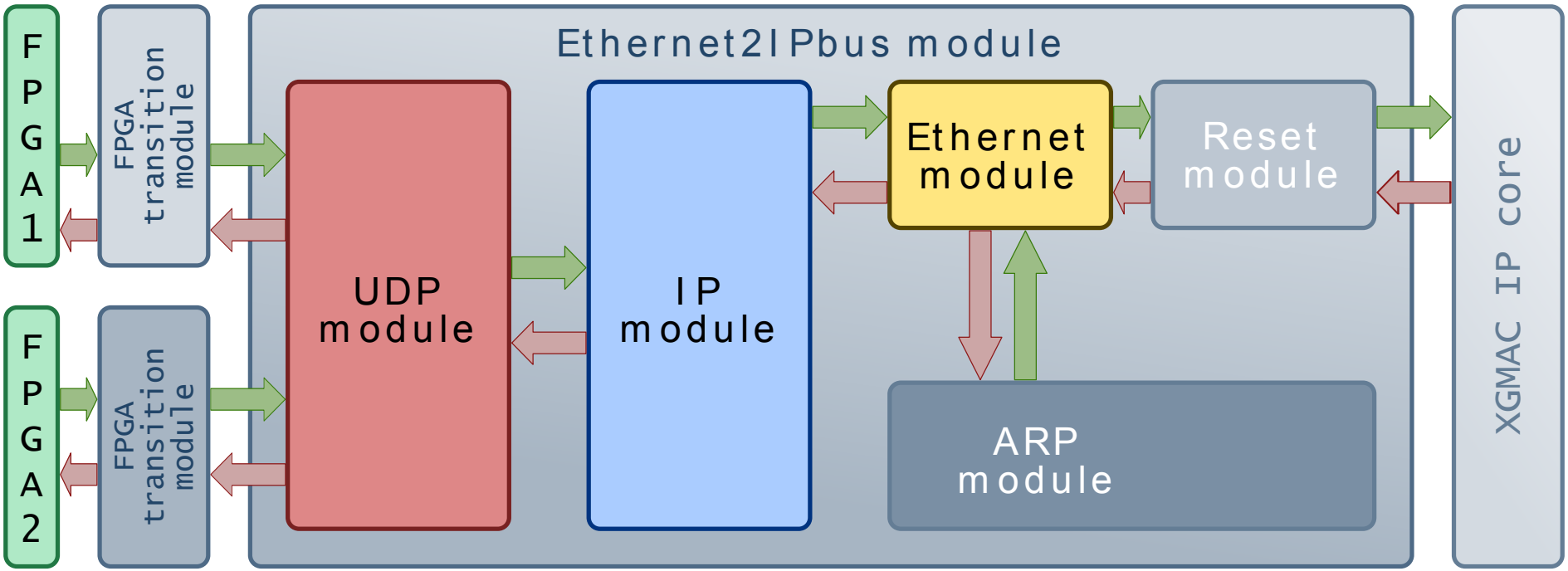
- Backup slides -

DPS Front FPGA firmware (for Demonstrator)

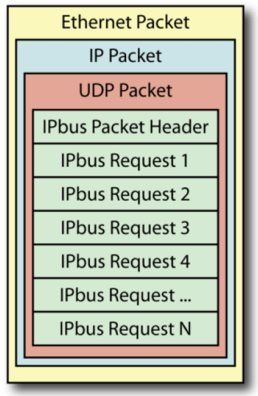


- Receive and decode ADC frames from LTDB
- Circular buffer to await L1A
- ADC data histograms for monitoring
- Back FPGA interface using IPbus via XAUI

DPS Back FPGA firmware (for Demonstrator)



- Fully streaming based functional 10 GbE design
- Individual modules for different protocol layers
- Where possible, different modules use same core logic
- Includes ARP and ICMP (ping)



Trigger-Type (TType)

Definition and distribution of TType

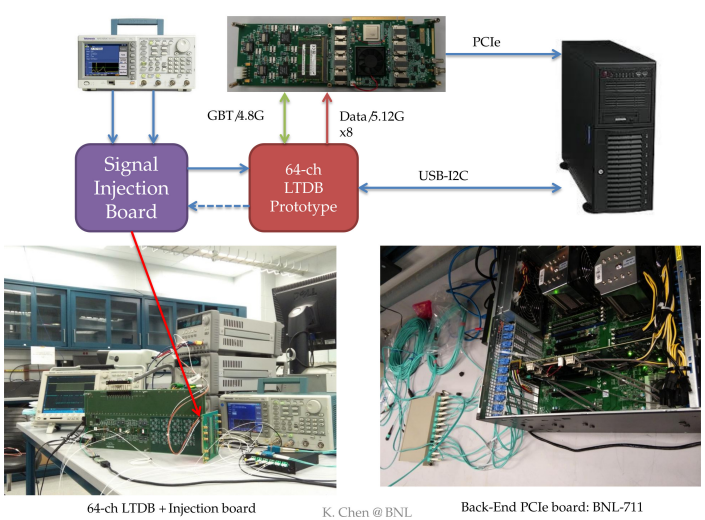
- 8 bits to indicate which $\approx$ subdetector issued trigger
- E.g.: bit 7: Physics; bit 4: LAr Demonstrator; bit 0: Random
- Encoded in (serialised) TTC signal, issued with some delay after L1A

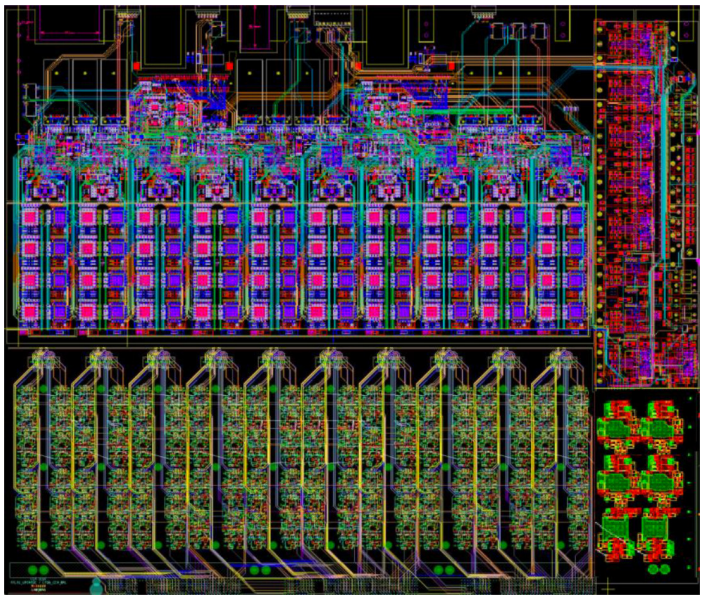
Realisation in ABBA

Implementation of Trigger-Type based readout only started in early October 2015 ...

1. Use actual value and mask for TType decoding (0x90)
2. Store data buffer address when L1A is seen in FIFO
3. Read data buffer address from FIFO when TType is decoded
   - Discard address if TType does not match requirement
   - Read data from buffer address if TType matches requirement
4. Read up to 60 samples per event $\rightarrow$ full pulse shape

Phase-I Front End Electronics





- 64-ch LTDB prototype is tested
  - ✓ Many prototype components (including Nevis ADC, LOCx2, GBTx, GBT-SCA, MTx, MTRx) have been tested
  - ✓ Nevis ADC-to-LOCx2 interface verified
  - Few issues identified and followed up
- LTDB pre-prototype (320-ch)
  - Using all final baseline components
  - Under production
  - Pre-selection irradiation testing for analog COTS components done
  - Tests in the coming months, final design review foreseen end of this year

Phase-I Front End Electronics

Baseplane and LSBs

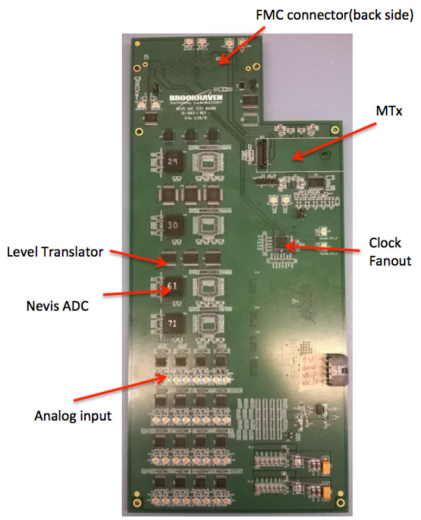
- Specific baseplane prototypes: EMB (2nd prototype), EMEC: design finished; HEC, FCAL: assembled
- ✓ EM LSBs OK: irradiation tests for COTS components concluded
- FCAL LSBs: design finished, prototype produced, under test

LTDB ASIC ADC

- June 2014: PDR* recommend Nevis ADC ASIC (power and latency gain)
- Nevis14 produced "bad codes" at ≈ 10 Hz

$\Rightarrow$ March 2016: Nevis15: Tests show no bad code

$\Rightarrow$ 16 ADCs to be assembled on new 64-ch LTDB at BNL



32-ch test board

* PDR = Preliminary Design Review

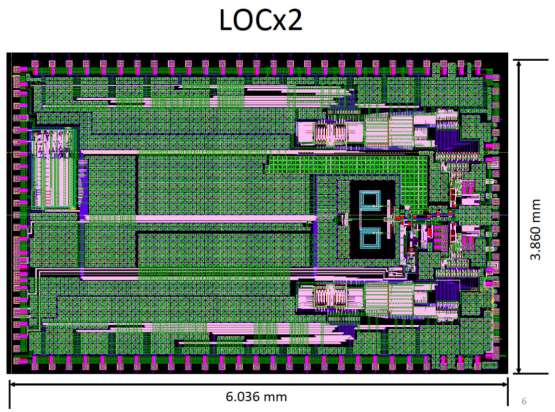
Phase-I Front End Electronics

LTDB ASIC LOCx2 serialiser chip

- Oct 2014: PDR of LOCx2 in 0.25 μm SOS
- Good chips from some lots
  - Measured to design specs
  - SEU test with 800 MeV neutron: no SEU observed
- But also failures in other lots from foundry

$\Rightarrow$ production shows uncertainty with the process

  - New submission (minor design corrections) sent to foundry in April '16
- Solid back-up plan has been developed



Phase-I ASIC backup

LTDB ASICs Backup Plans

- Nevis ADC backup: COTS ADC (TI ADS5272)
- LOCx2 serialiser backup 1: LOCTDS (130 nm RF-CMOS)
- LOCx2 backup 2: existing operational ASICs: GBTx + MUX chip

$\Rightarrow$ Carry two options until one succeeds