Contribution ID: **61** Type: **not specified**

Electronics Development for the ATLAS Liquid Argon Calorimeter Trigger and Readout for Future LHC Running

Wednesday, 18 May 2016 11:00 (20 minutes)

The upgrade of the LHC will provide up to 7.5 times greater instantaneous and total luminosities than assumed in the original design of the ATLAS Liquid Argon (LAr) Calorimeters. Radiation tolerance criteria and an improved trigger system with higher acceptance rate and longer latency require an upgrade of the LAr readout electronics. In the first upgrade phase in 2019-2020, a trigger-readout with up to 10 times higher granularity will be implemented. This allows an improved reconstruction of electromagnetic and hadronic showers and will reduce the background for electron, photon and energy-flow signals at the first trigger level. The analog and digital signal processing components are currently in their final design stages and a fully functional demonstrator system is operated and tested on the LAr Calorimeters. In a second upgrade stage in 2024-2026, the readout of all 183,000 LAr Calorimeter cells will be performed without trigger selection at 40 MHz sampling rate and 16 bit dynamic range. Calibrated energies of all cells will be available at the second trigger level operating at 1 MHz, in order to further mitigate pile-up effects in energy reconstruction. Radiation tolerant, low-power front-end electronics optimized for high pile-up conditions is currently being developed, including pre-amplifier, ADC and serializer components in 65-180 nm technology. This talk will give an overview of the future LAr readout electronics and present research results from the two upgrade programs.

Summary

The LHC luminosity upgrades in 2019-2020 and 2024-2026 require the associated detectors to operate at luminosities of up to $7x10^{34}cm^{-2}s^{-1}$, with the goal of accumulating a total integrated luminosity of $3000fb^{-1}$. To be able to retain interesting physics events even at rather low transverse energy scales, ET ≈ 20 GeV, for single objects, increased trigger rates are foreseen for the ATLAS detector. At the Level-0 and Level-1 selection stage acceptance rates of 1 MHz and 400 kHz are planned, combined with longer latencies in order to read out the necessary data from all detector channels. Under these conditions, the current readout of the ATLAS Liquid Argon (LAr) Calorimeters does not provide sufficient buffering and bandwidth capabilities. Furthermore, the expected total on-detector radiation doses of $10^{13}n_{eq}/cm^2$ (NIEL) and 0.3 kGy (TID) are beyond the qualification range of the current front-end electronics. For these reasons, an upgrade of the ATLAS LAr Calorimeter readout electronics is foreseen in two stages.

In 2019-2020, a new trigger readout will be installed to process 35,000 so-called Super-Cells which improves the longitudinal and lateral granularity for shower reconstruction by a factor of up to 10 compared to the current calorimeter trigger towers. This will allow the usage of more detailed shower shape variables in the reconstruction of electron, photon and energy flow trigger signals, and thus a further suppression of the background rate. The new readout components consist of 124 LAr trigger driver boards equipped with custom developed, radiation tolerant 12-bit SAR ADCs which sample the Super-Cell pulses at 40 MHz. Digital data are transferred on custom optical links at 5.44 Gb/s to the back-end system. 32 LAr digital processing board equipped with 4 Altera Arria-10 FPGAs each receive the data and apply a refined energy calibration already at trigger level. Digital filtering techniques are explored to mitigate the expected pile-up effects from 80-200 proton-proton collisions per LHC bunch crossing. Prototype versions of the front-end and back-end boards have been tested successfully. A demonstrator set-up is installed on the LAr Calorimeter system, which covers about 10% of the detector area. First measurements of calibration and collision data are performed with this setup in order to gain experience with the developed hardware components and to optimize the final system design.

The second upgrade phase is planned for 2024-2026. The Super-Cell readout will remain and will feed the future Level-0 trigger of ATLAS. In parallel, the full LAr Calorimeter will be read out at 40 MHz in order to provide the best possible information to the Level-1 trigger running at 1 MHz input rate. For this reason and for radiation tolerance requirements, the current front-end and back-end readout system for the 183,000 calorimeter cells will be fully replaced. The corresponding readout components are mainly an evolution of the Super-Cell readout, however exceeding the performance requirements in several aspects: 10 times higher bandwidth, 2 times faster optical links, improved ADC precision, low noise and low power.

The new electronics must be able to capture the triangular detector pulses of about 400-600 ns length with signal currents per channel of up to 10 mA and a dynamic range of 16-17 bit. The noise should be kept below 100 nA and the ADC power per front-end channel should not exceed 50 mW. With the available ASIC technologies different concepts of the readout design will be possible.

In 180 nm SiGe technology (IBM 7WL) and chosing unipolar shaping, two gain stages can cover the desired dynamic range. An ADC which matches the pre-amplifier and shaper will need to provide 14 bit digitization range. Such a design is shown to meet the noise requirements and achieve an integral non-linearity below 0.1%. Moreover, in simulations of the complete readout chain using the unipolar shaping approach signal pile-up is introducing a controllable baseline shift, and an additional digital CR shaping stage does not introduce a degradation of the energy resolution.

A recent approach in 65 nm technology is targeting a combination of pre-amplifier, shaper, ADC and serialiser in s single Front-End System-On-Chip (FESOC). In this context, the development of a pre-amplifier and shaper as well as SAR ADCs is performed in 65 nm CMOS technology. Due to the lower voltage range, 2-gain and 4-gain readout modes are studied. The analog part is designed with programmable peaking time to optimize the noise level in presence of signal pile-up. The 65 nm ADC is laid out in SAR architecture and is completed with an active SEE detection mechanism by feeding the signals into two ADCs in parallel and comparing their output. In this way, the signal-to-noise ratio can be further improved in presence of radiation. Results for a 80 MHz 12-bit prototype design show ENOB values above 10.8 bits after 10 kGy irradiation, and similar performance is reached for a 14-bit layout.

In this contribution, results from the development and design of the two upgrade stages of the LAr Calorimeter readout will be presented, including experience from prototype boards and the demonstrator system of the Super-Cell readout as well as design studies and first tests of prototype ASIC components for the second upgrade phase.

References:

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Session Classification: High Luminosity LHC