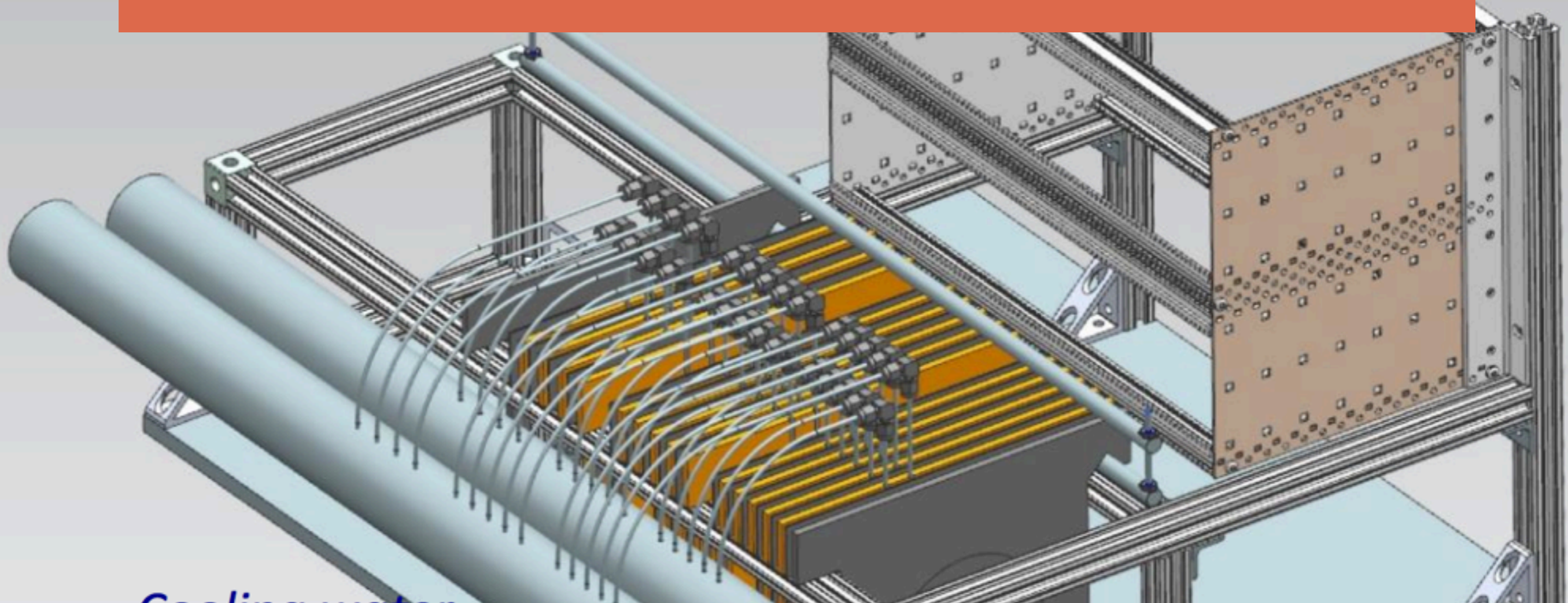


Construction and First Beam-tests of a Prototype Silicon-Tungsten High Granularity Calorimeter for CMS at HL-LHC



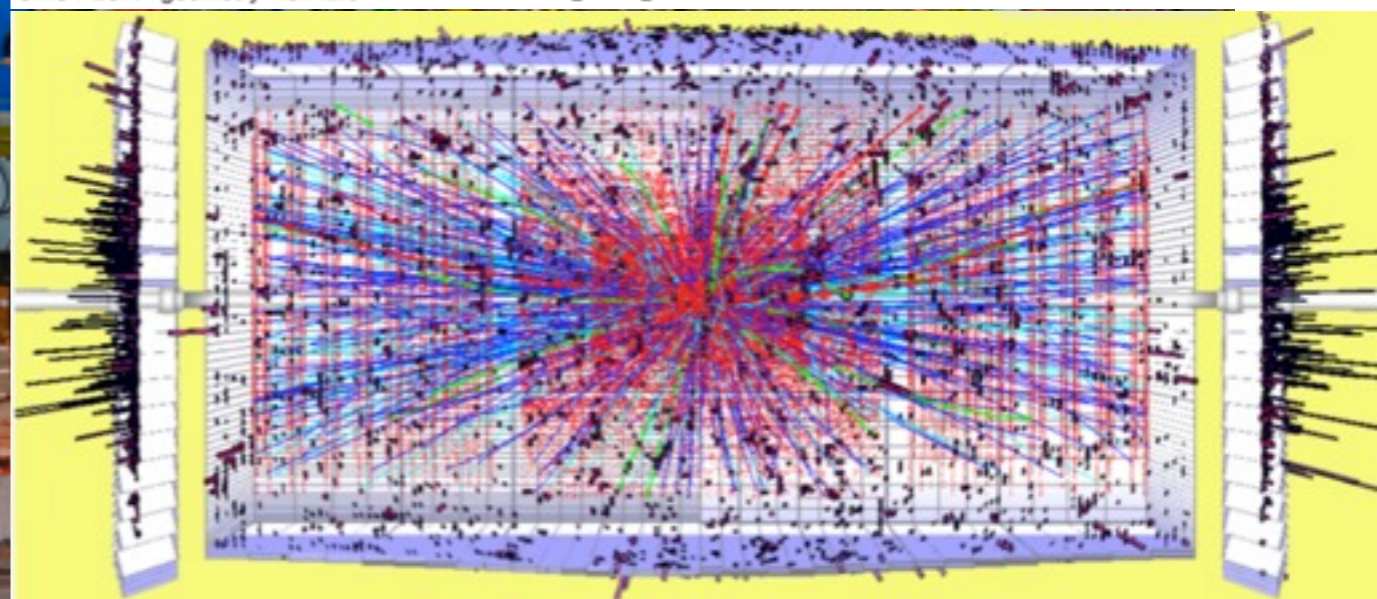
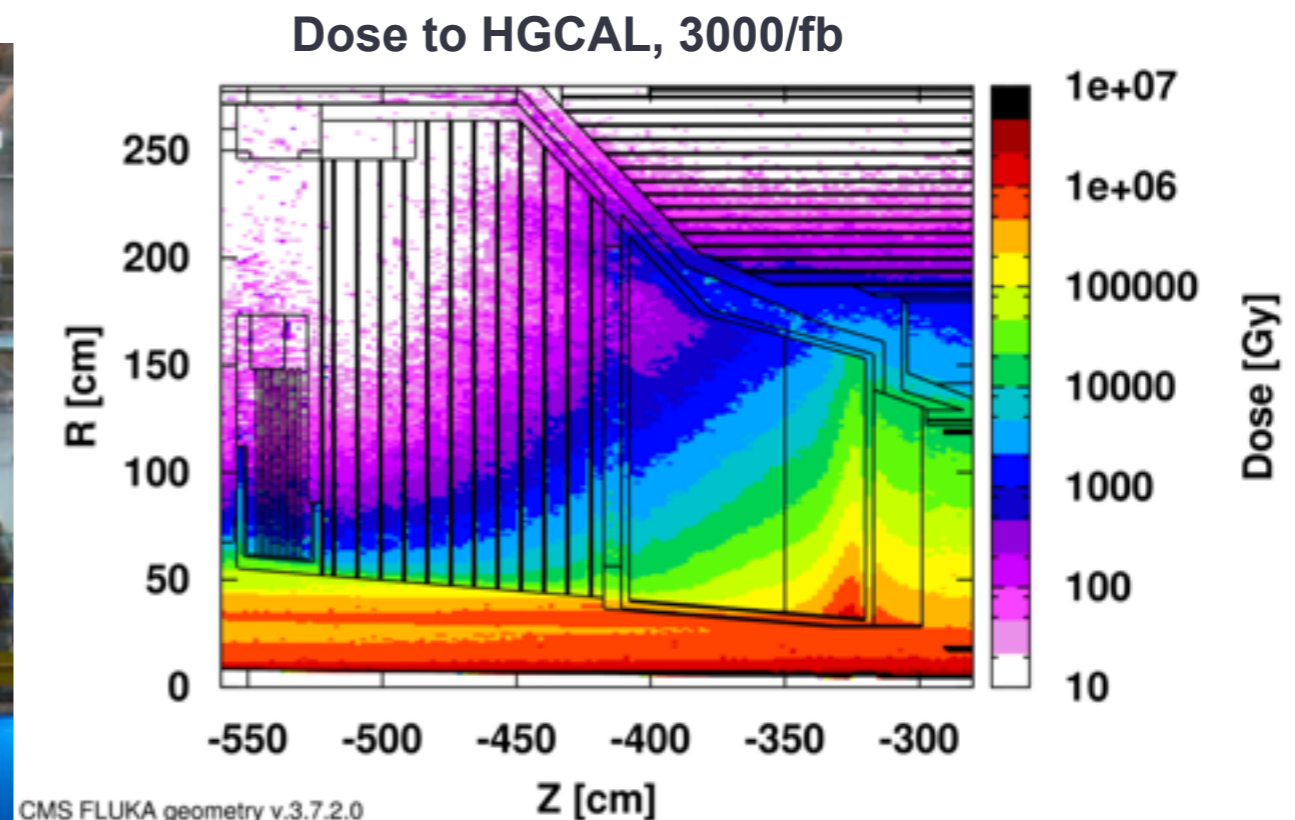
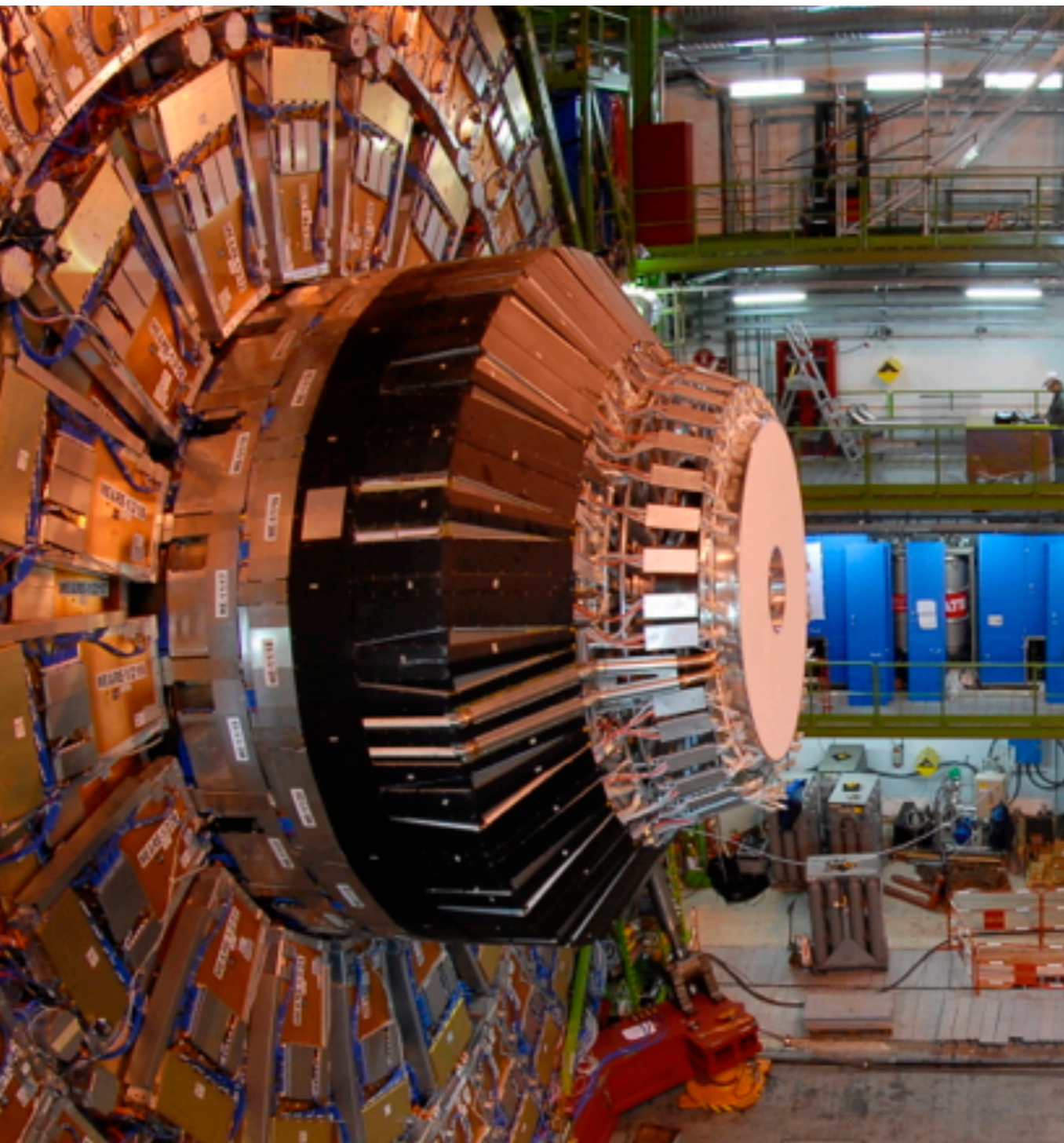
Zoltan Gecse



May 18, CALOR 2016, Daegu

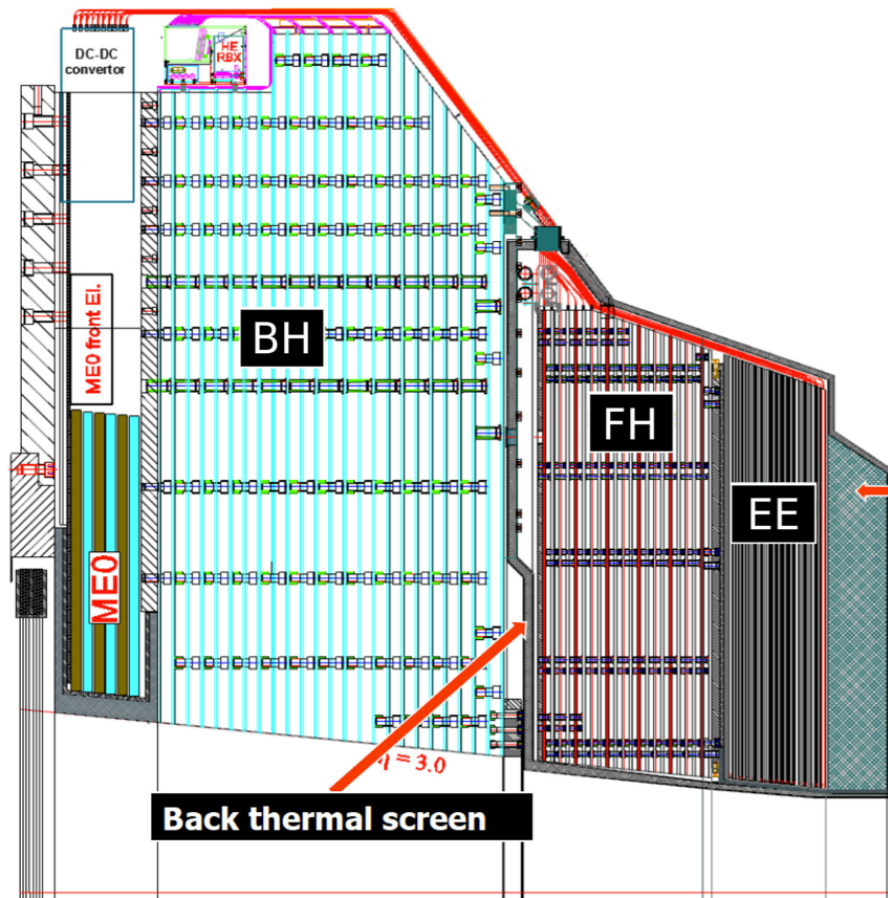
CMS Calorimeter Endcap

- **Calorimeter endcap needs replacement for HL-LHC (3000/fb)**
 - High radiation dose (150Mrad, 10^{16} n/cm²) and high pile-up conditions (200 PU)



cds.cern.ch/record/2020886/files/LHCC-P-008.pdf

The CMS HGC Design



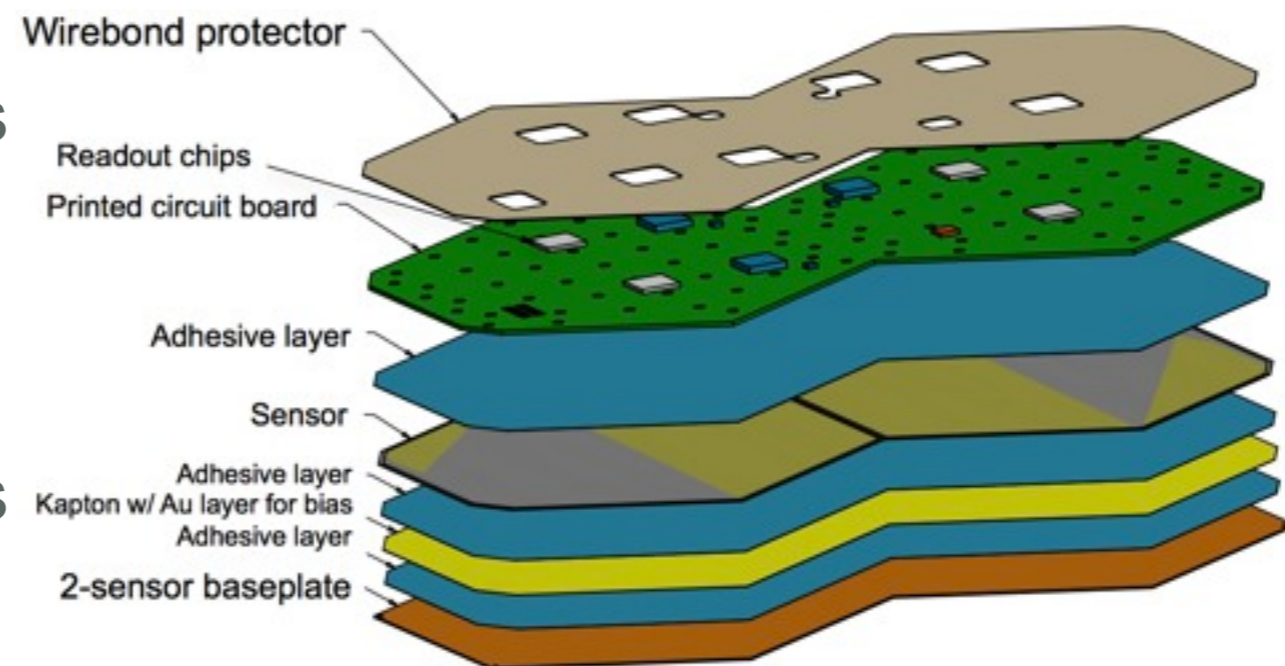
- **System divided into three parts:**

- EE – Silicon with tungsten absorber
28 sampling layers – $25 X_0 + \sim 1.3 \lambda$
- FH – Silicon with brass or steel absorber
12 sampling layers – 3.5λ
- BH – Scintillator with brass or steel absorber
11 layers – 5.5λ

- **EE and FH are maintained at -30C ,
BH is at room temperature**

- **Construction:**

- Hexagonal Si-sensors built into modules
- Modules with a W/Cu base plate and PCB readout board.
- Modules mounted on copper cooling plates to make wedge-shaped cassettes
- Cassettes inserted into absorber structures at integration site (CERN)

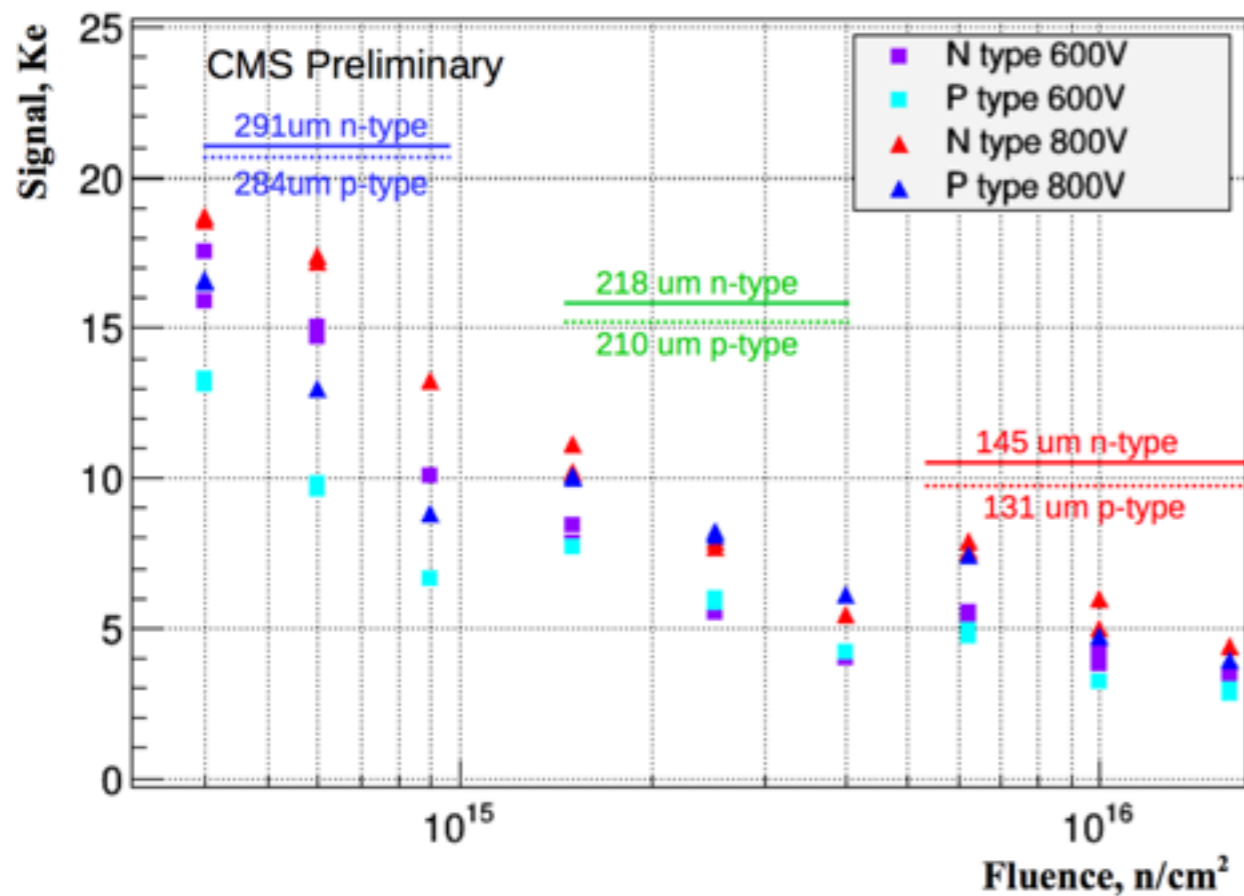


Dual 6" or single 8" modules

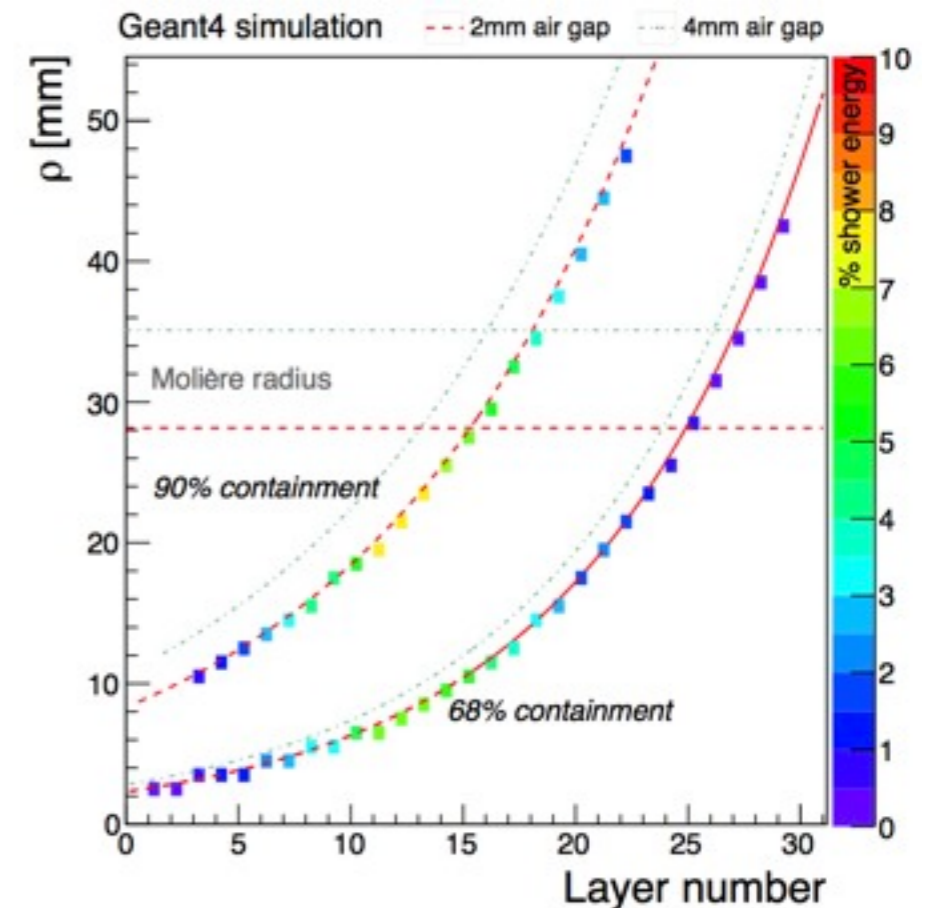
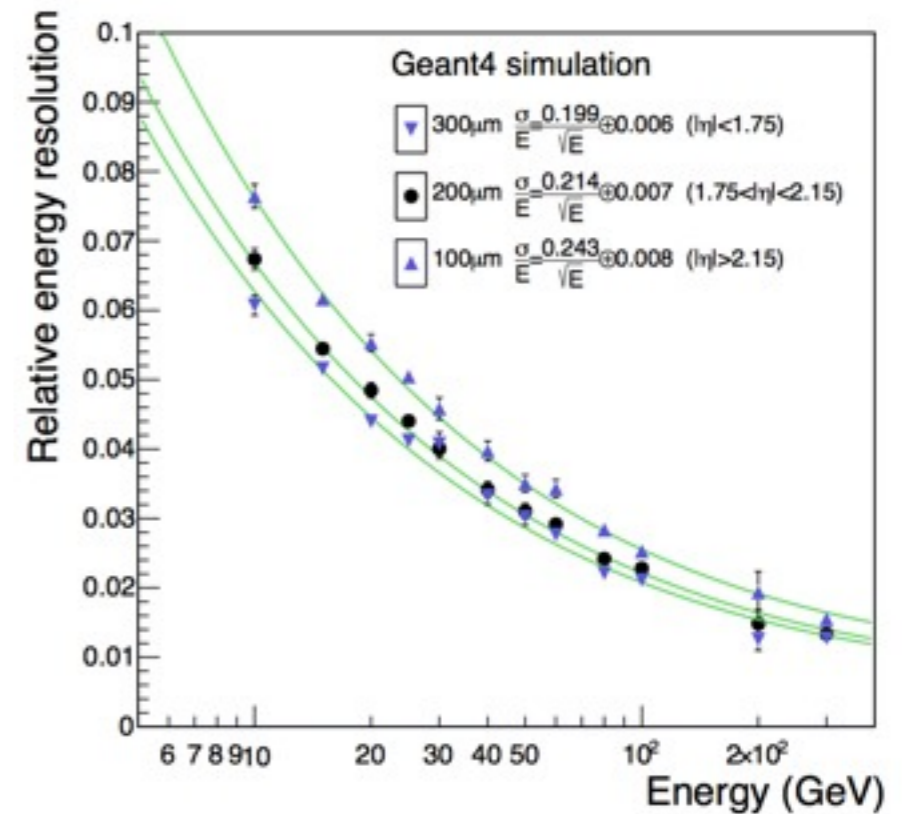
Key Parameters and Performance

- **Key parameters:**

- 593 m² of silicon
- 6M ch, 0.5 or 1 cm² cell-size
- 21,660 modules (8" or 2x6" sensors)
- 92,000 front-end ASICS.
- Power at end of life 115 kW



cds.cern.ch/record/2020886/files/LHCC-P-008.pdf



Test Beam Plans and Goals

Fermilab	Single layer with $6X_0$ absorber	March 25 - April 5	Complete Construction and results shown today
Fermilab	up to 28 layers with $25X_0$ absorber	May 18 - 31	
CERN (SPS)	28 layers with $25X_0$ absorber	Aug 31 - Sep 7	
CERN (SPS)	28-layer ECAL + up to 12-layer HCAL	Nov 9 - 14	

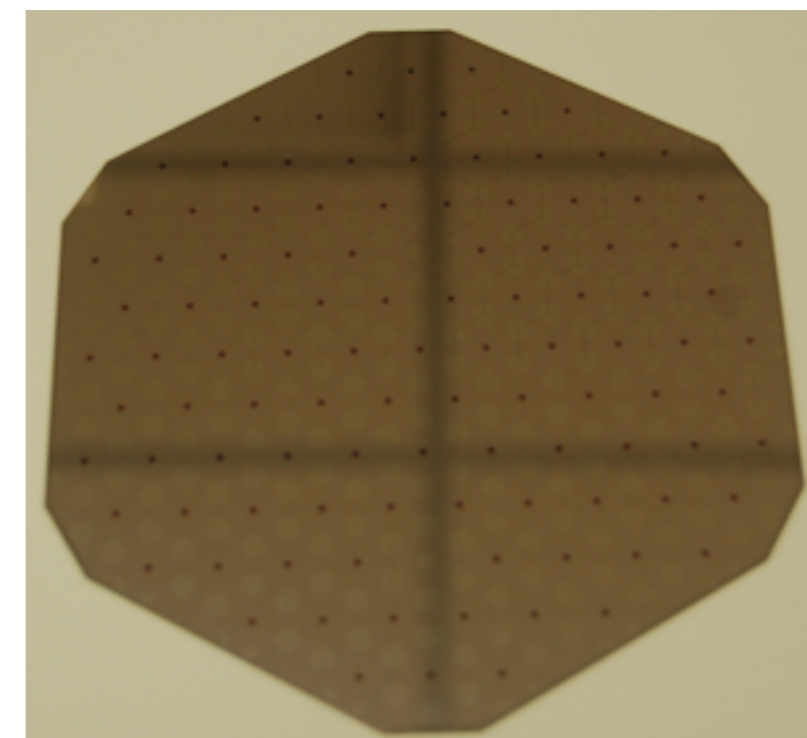
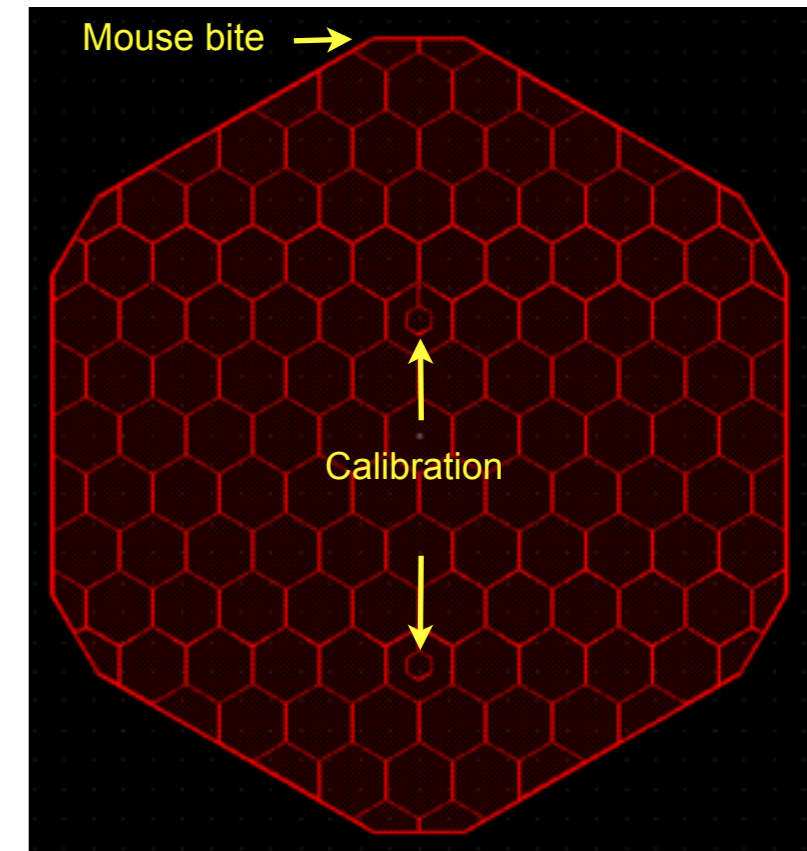
- **Goals:**

- Measure energy response
- Measure time and position resolutions
- Compare to simulation
- Test the proposed design of compact module with deep wire-bonding

Silicon Sensors

• Prototype sensors from Hamamatsu

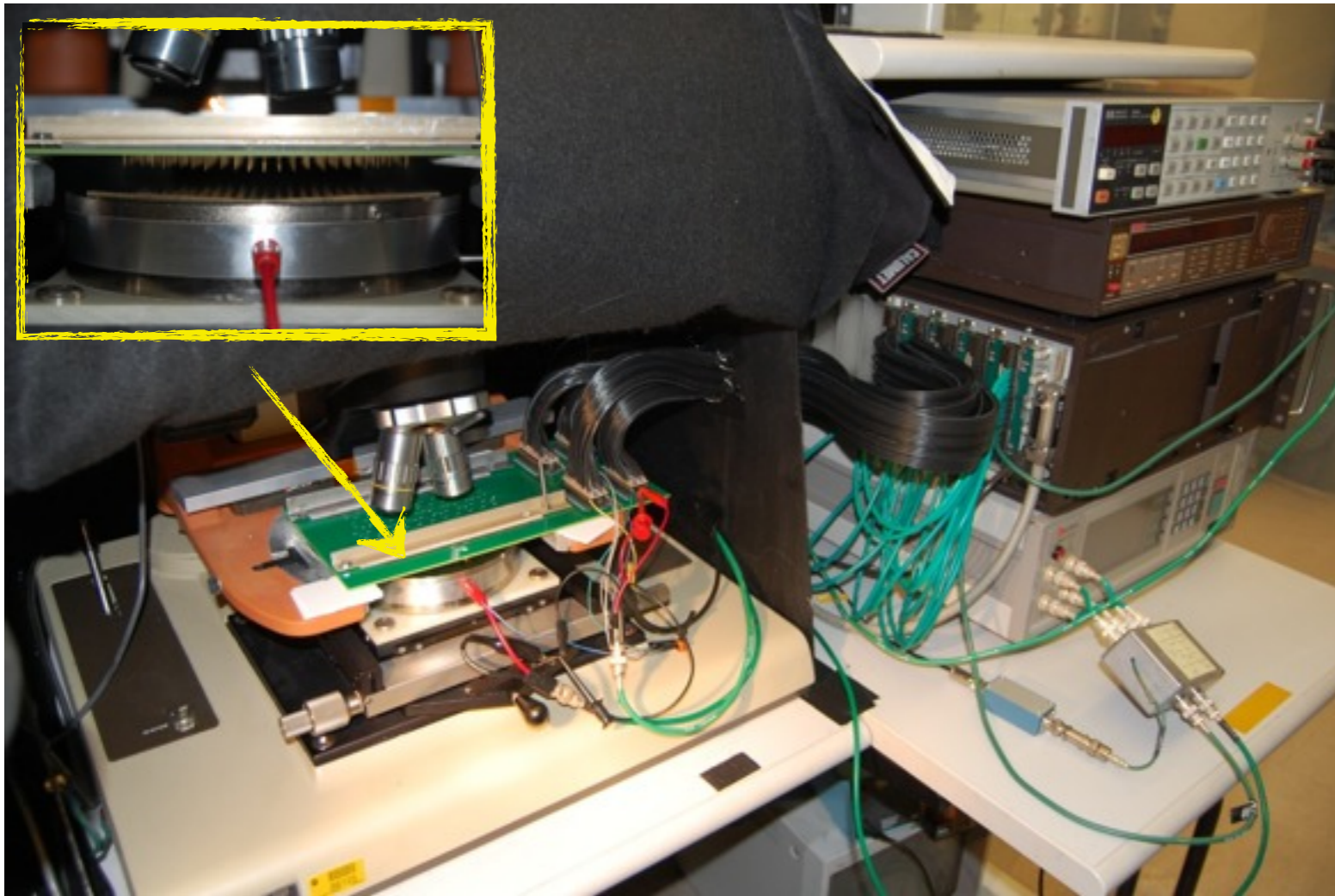
- 6" wafers, 200 μm active thickness (100 μm and 300 μm will be used later)
- physical thickness 320 μm
- 128 channels of 1.1 cm^2 area



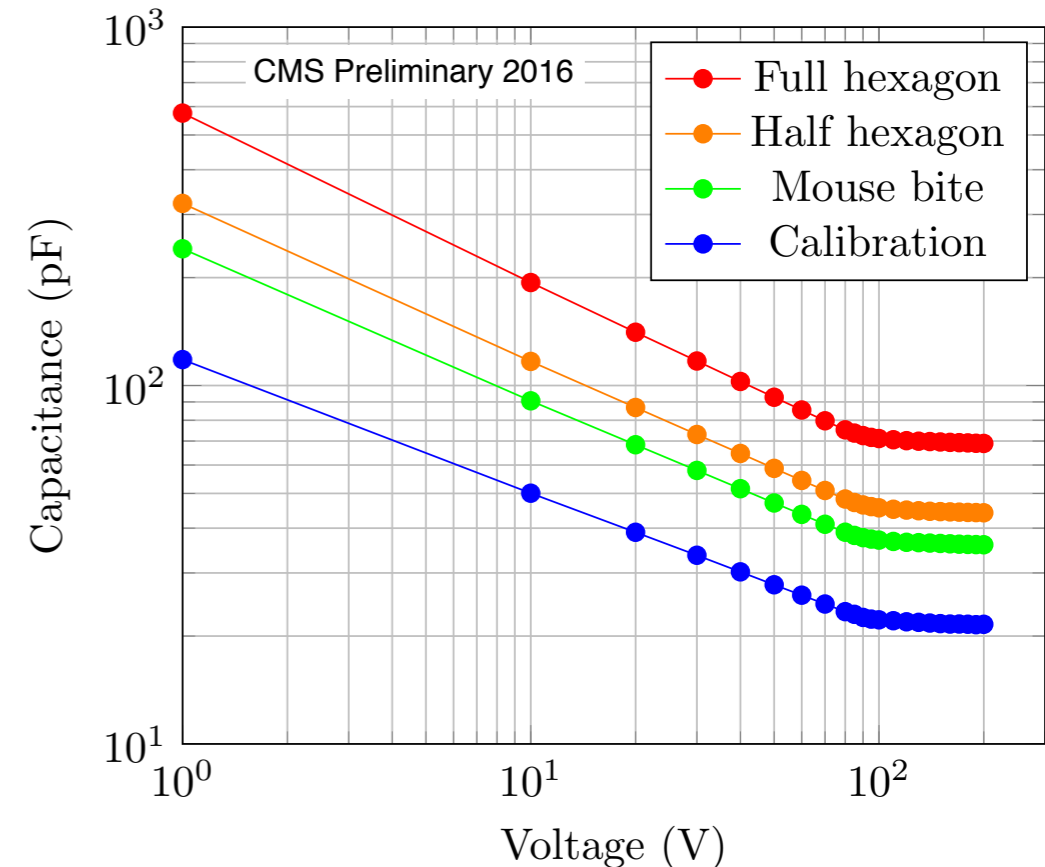
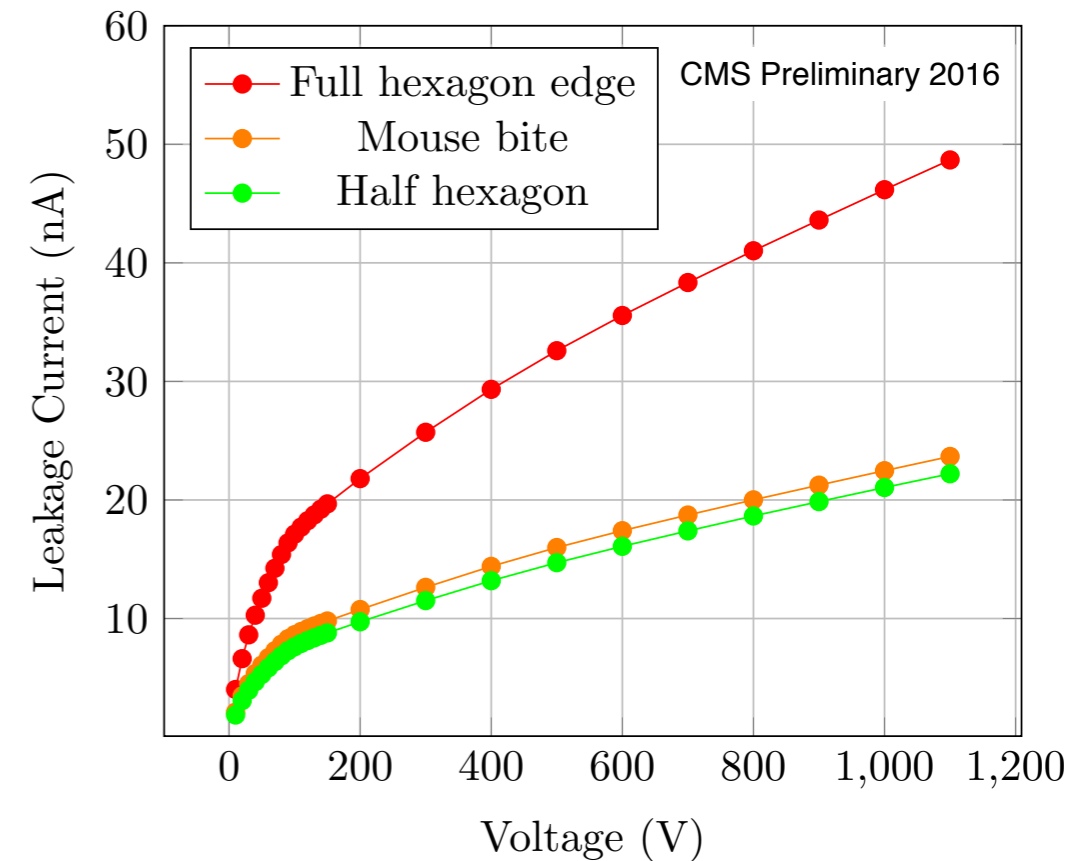
Thickness	300 μm	200 μm	100 μm
Maximum dose (Mrad)	3	20	100
Maximum n fluence (cm^{-2})	6×10^{14}	2.5×10^{15}	1×10^{16}
EE region	$R > 120 \text{ cm}$	$120 > R > 75 \text{ cm}$	$R < 75 \text{ cm}$
FH region	$R > 100 \text{ cm}$	$100 > R > 60 \text{ cm}$	$R < 60 \text{ cm}$
Si wafer area (m^2)	290	203	96
Cell size (cm^2)	1.05	1.05	0.53
Cell capacitance (pF)	40	60	60
Initial S/N for MIP	13.7	7.0	3.5
S/N after 3000 fb^{-1}	6.5	2.7	1.7

cds.cern.ch/record/2020886/files/LHCC-P-008.pdf

Sensor Testing

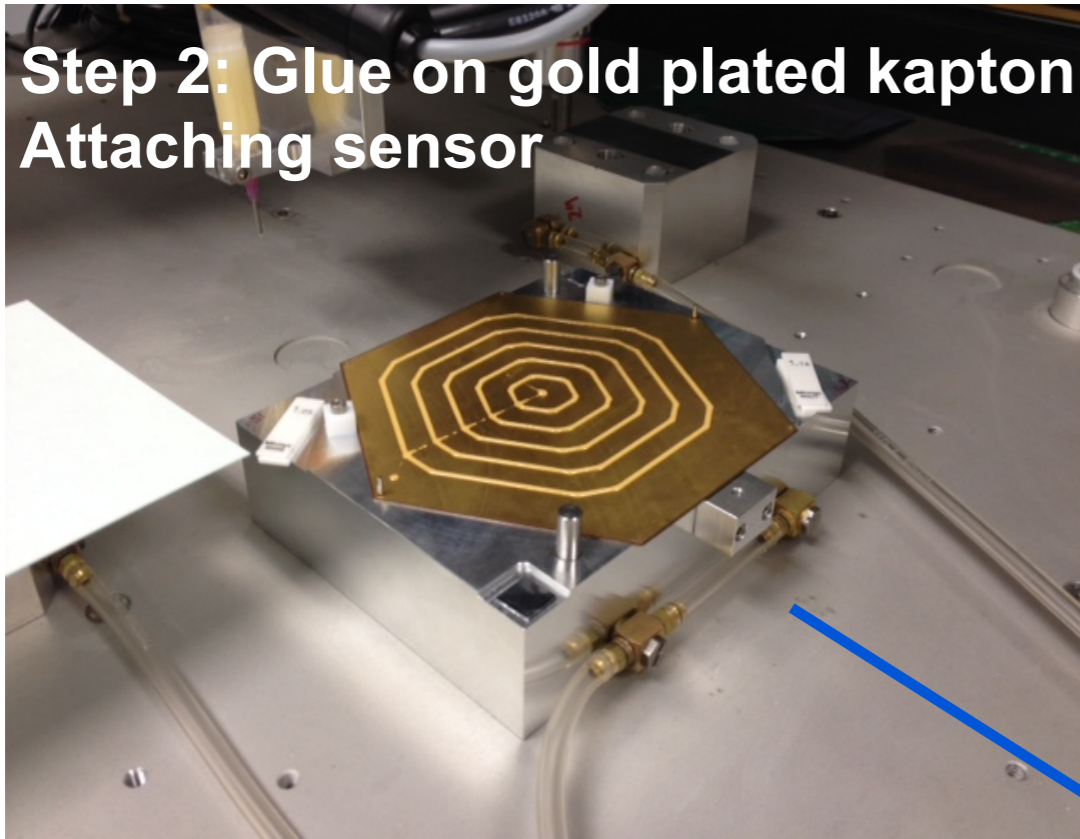


- Break down voltage $> 900\text{V}$
- Leakage currents 10-100 nA per channel
- Depletion voltage 90 V
- Measured capacitance of full hexagons is 70 pF, which includes $\sim 10\text{pF}$ of strain capacitance of test stand

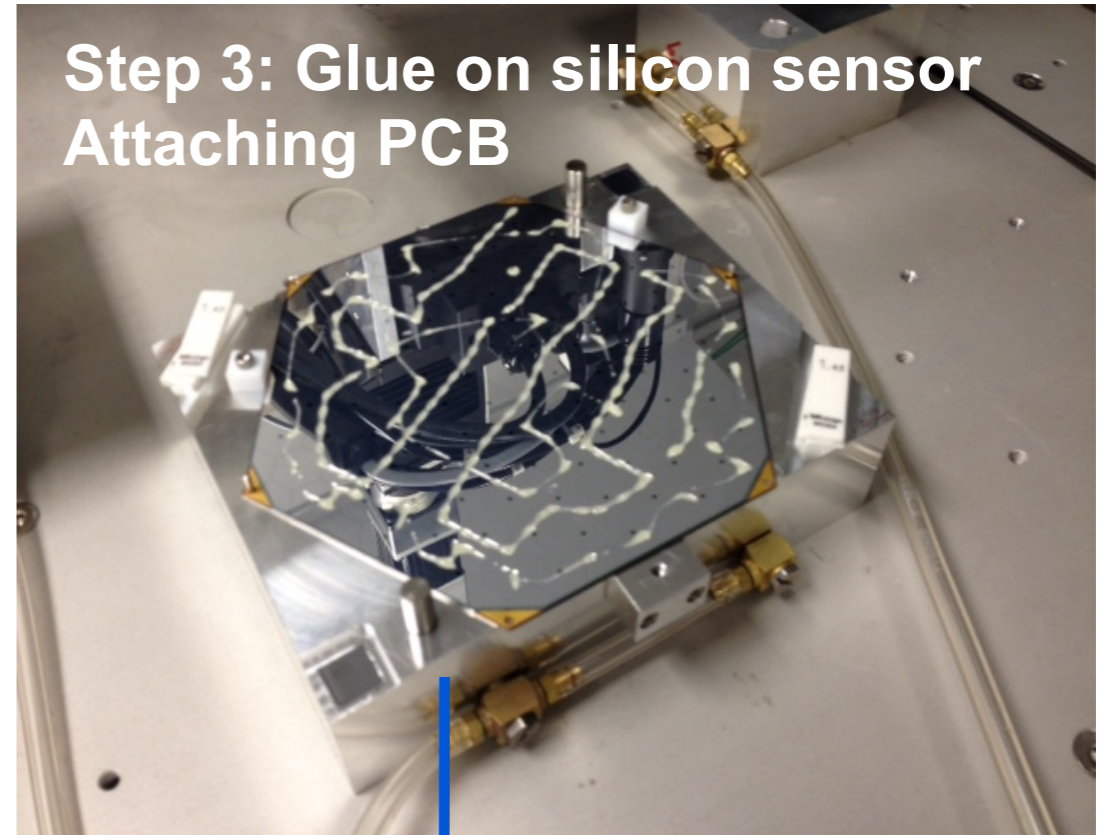


Module Assembly

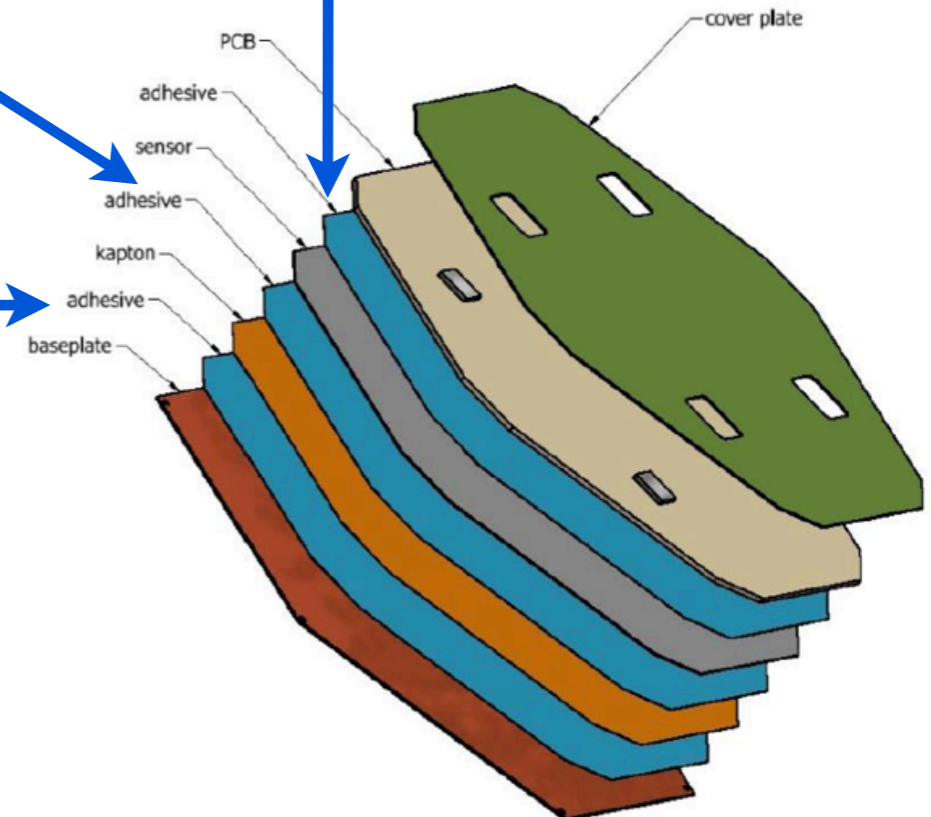
**Step 2: Glue on gold plated kapton
Attaching sensor**



**Step 3: Glue on silicon sensor
Attaching PCB**

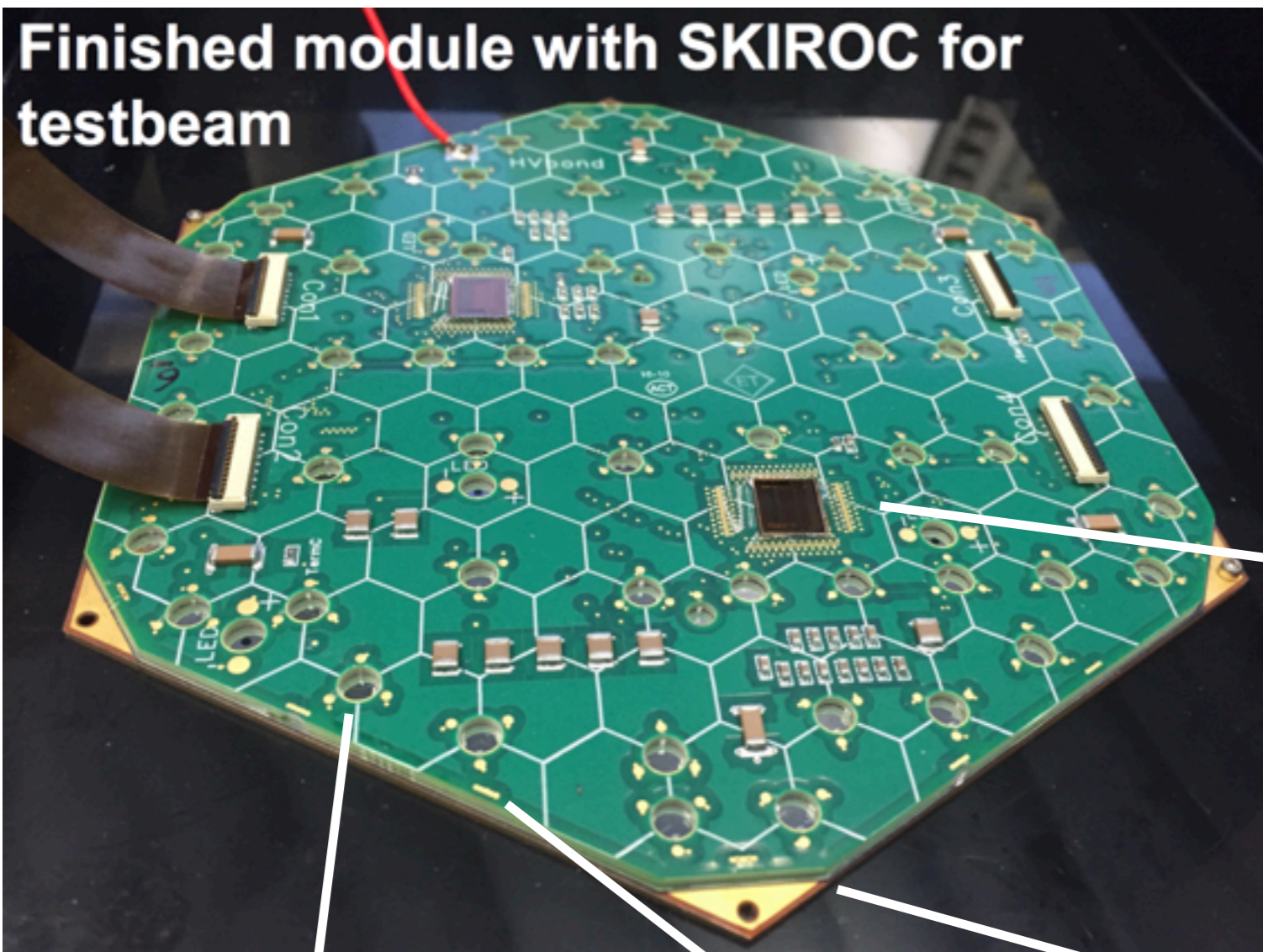


**Step 1: Glue on W/Cu baseplate
Attaching kapton**

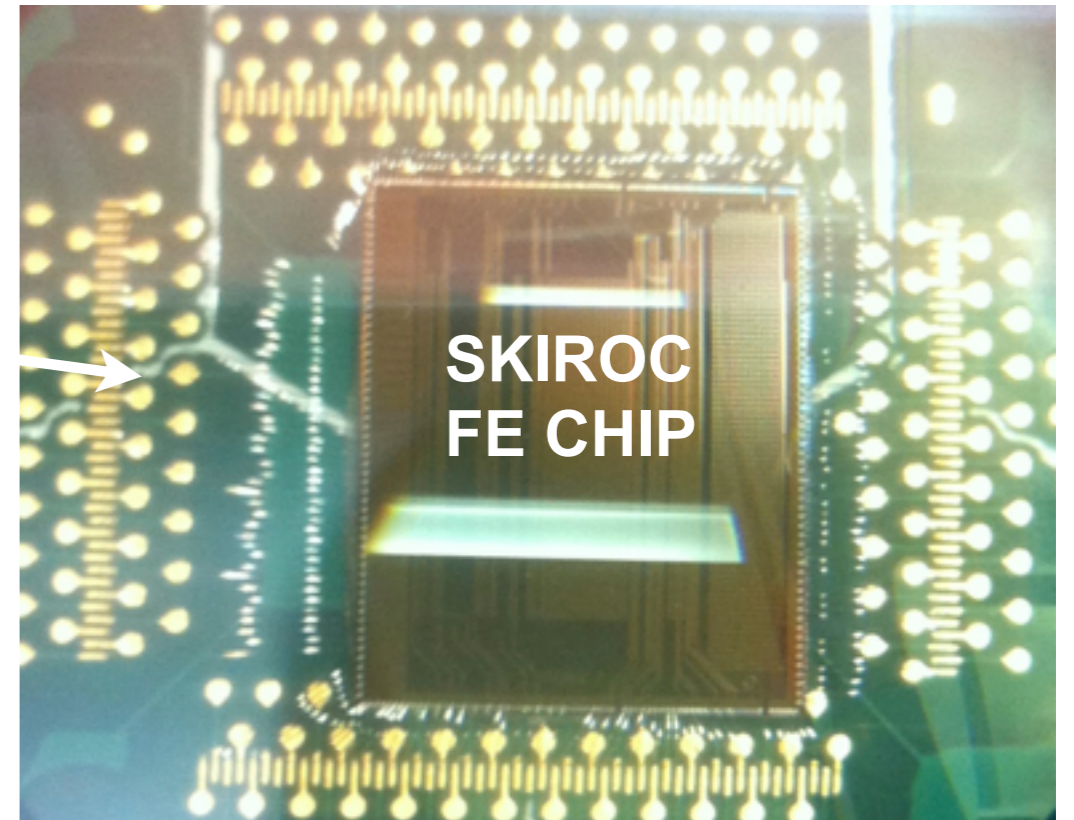


Wire Bonding

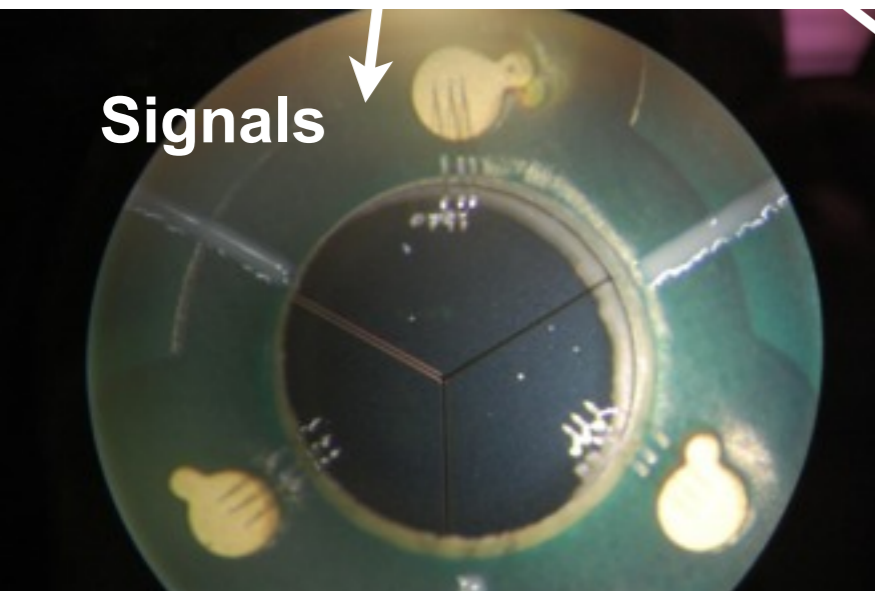
Finished module with SKIROC for testbeam



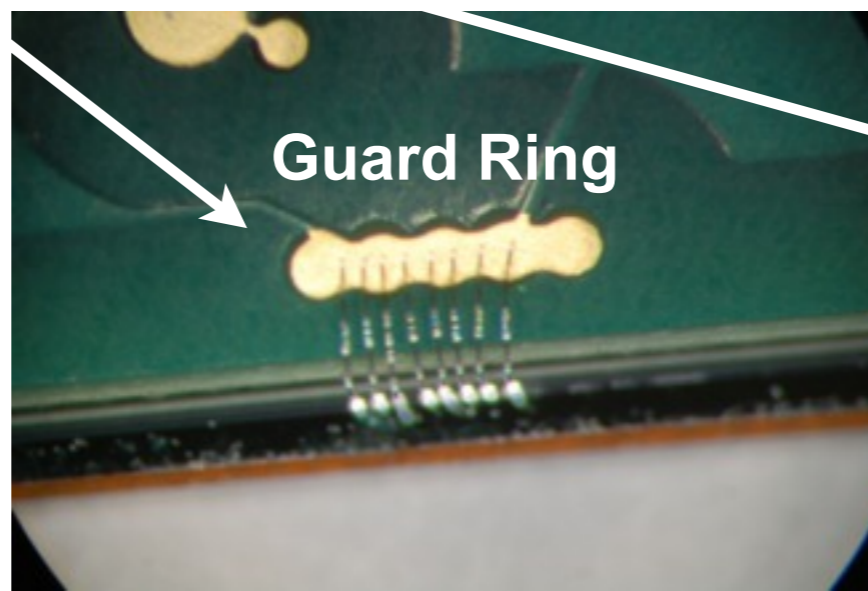
- **~ 700 wire bonds on a single module!**



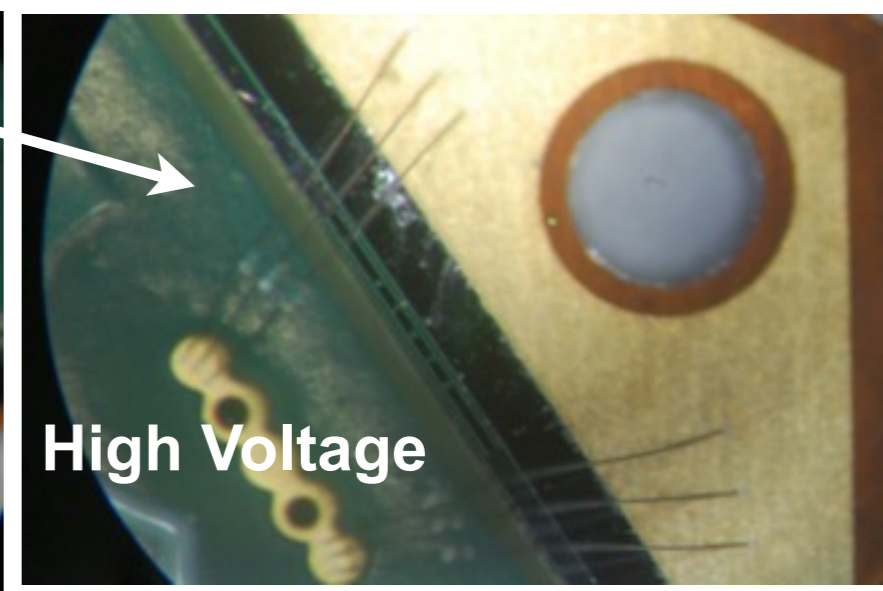
Signals



Guard Ring

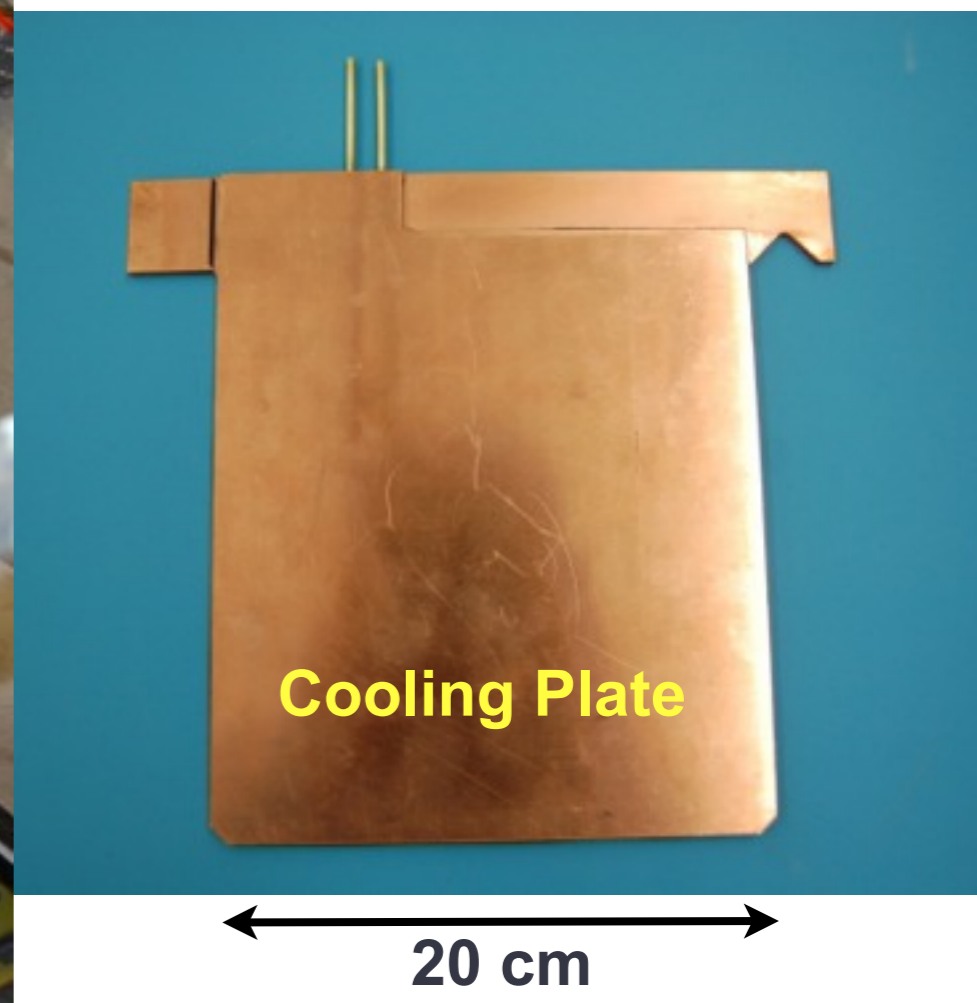
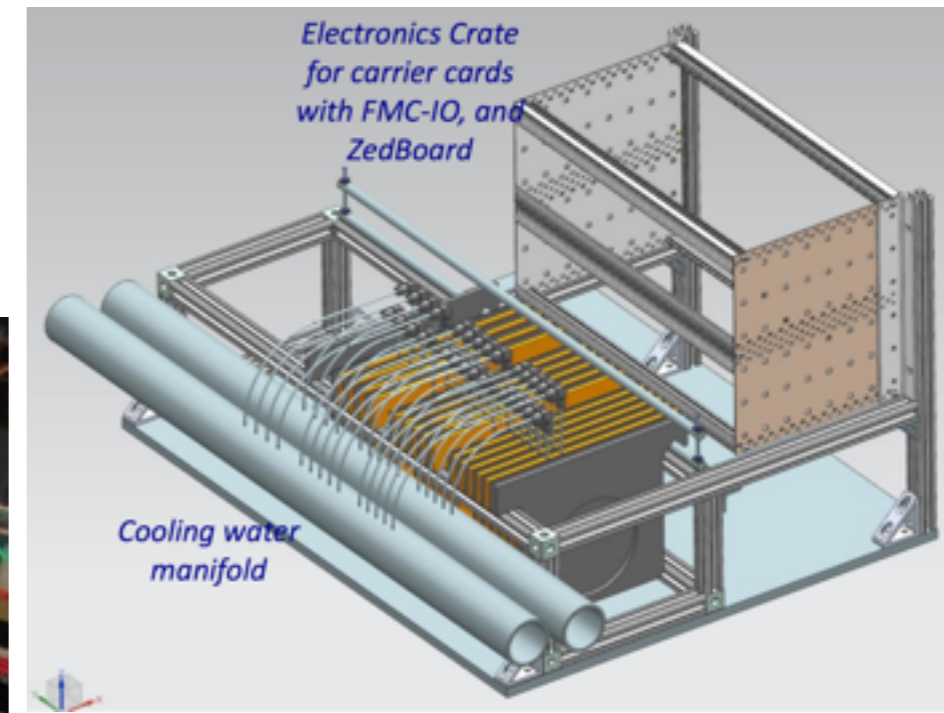
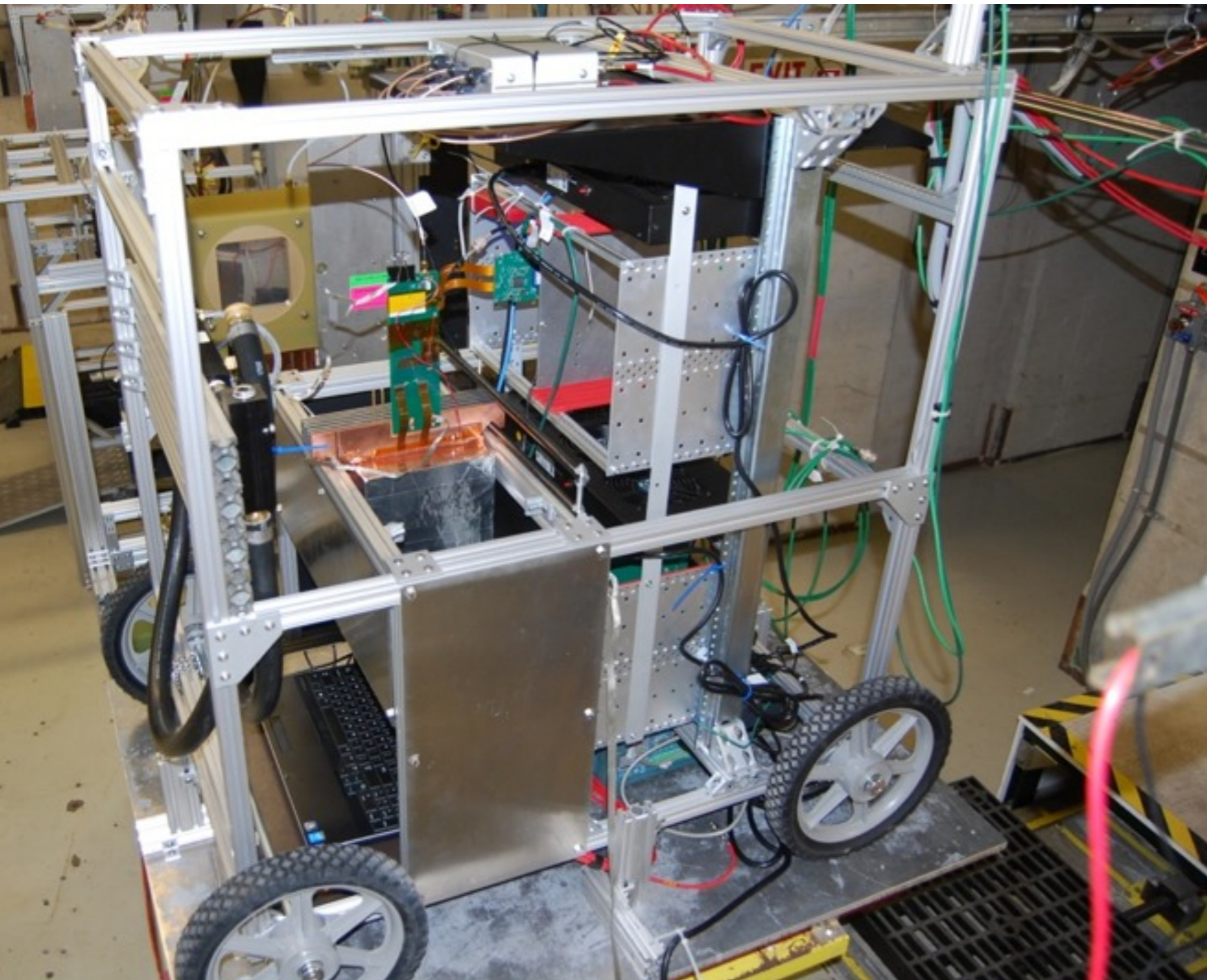


High Voltage

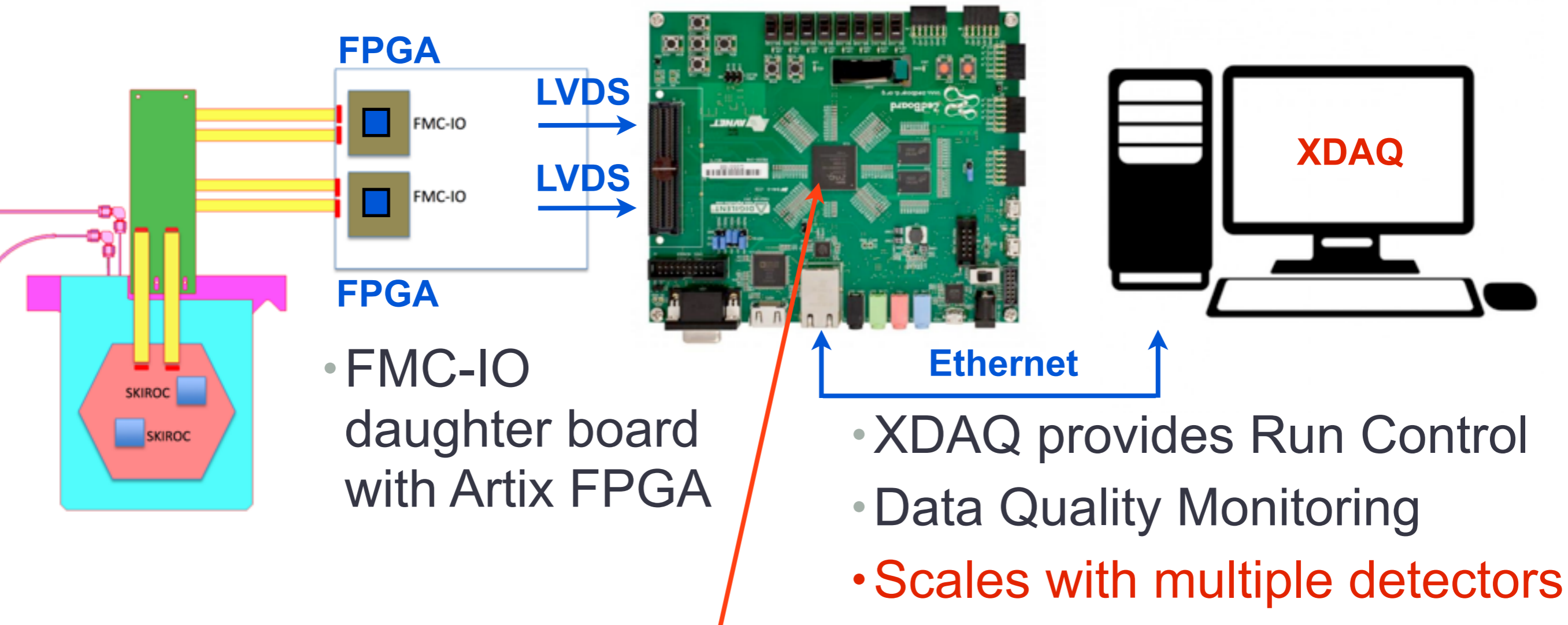


Mechanics and Cooling

- **Hanging file design for flexible insertion of absorbers and modules on cooling plates**



DAQ



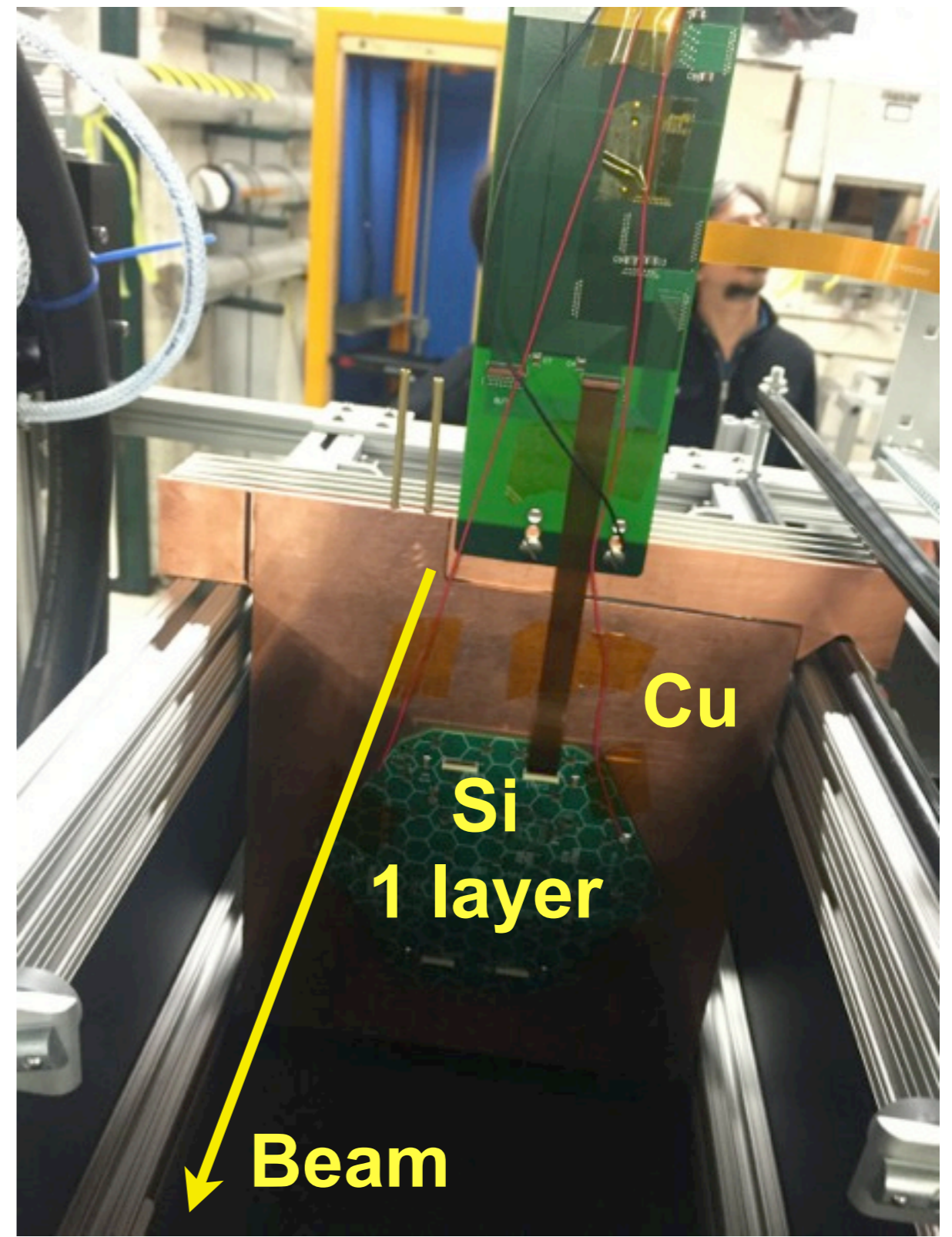
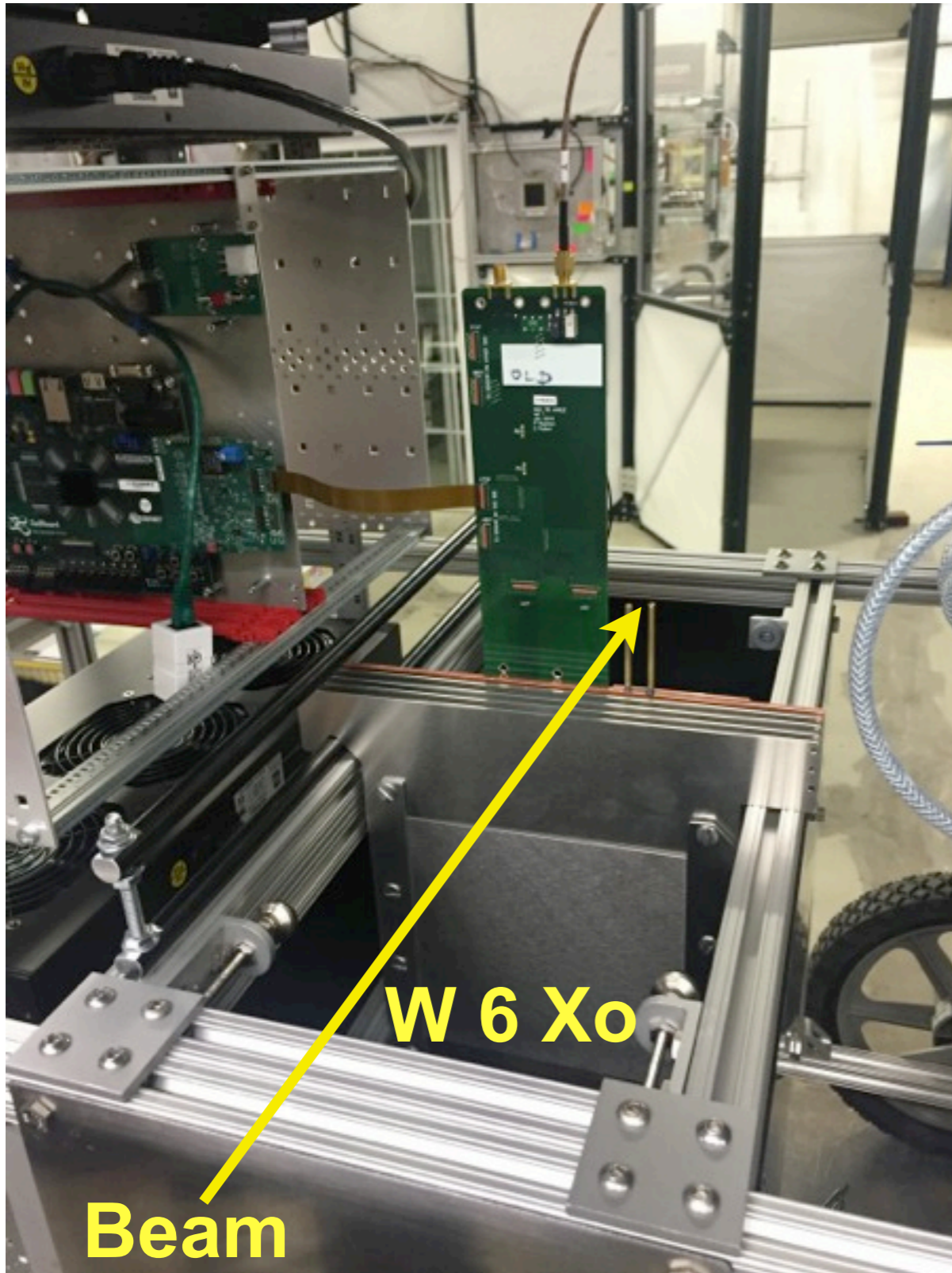
- FMC-IO daughter board with Artix FPGA

- XDAQ provides Run Control
- Data Quality Monitoring
- Scales with multiple detectors

- SKIROC ASIC FE chips, designed for ILC and used as starting point
- 200 ns signal rise time
- 12 bit ADC

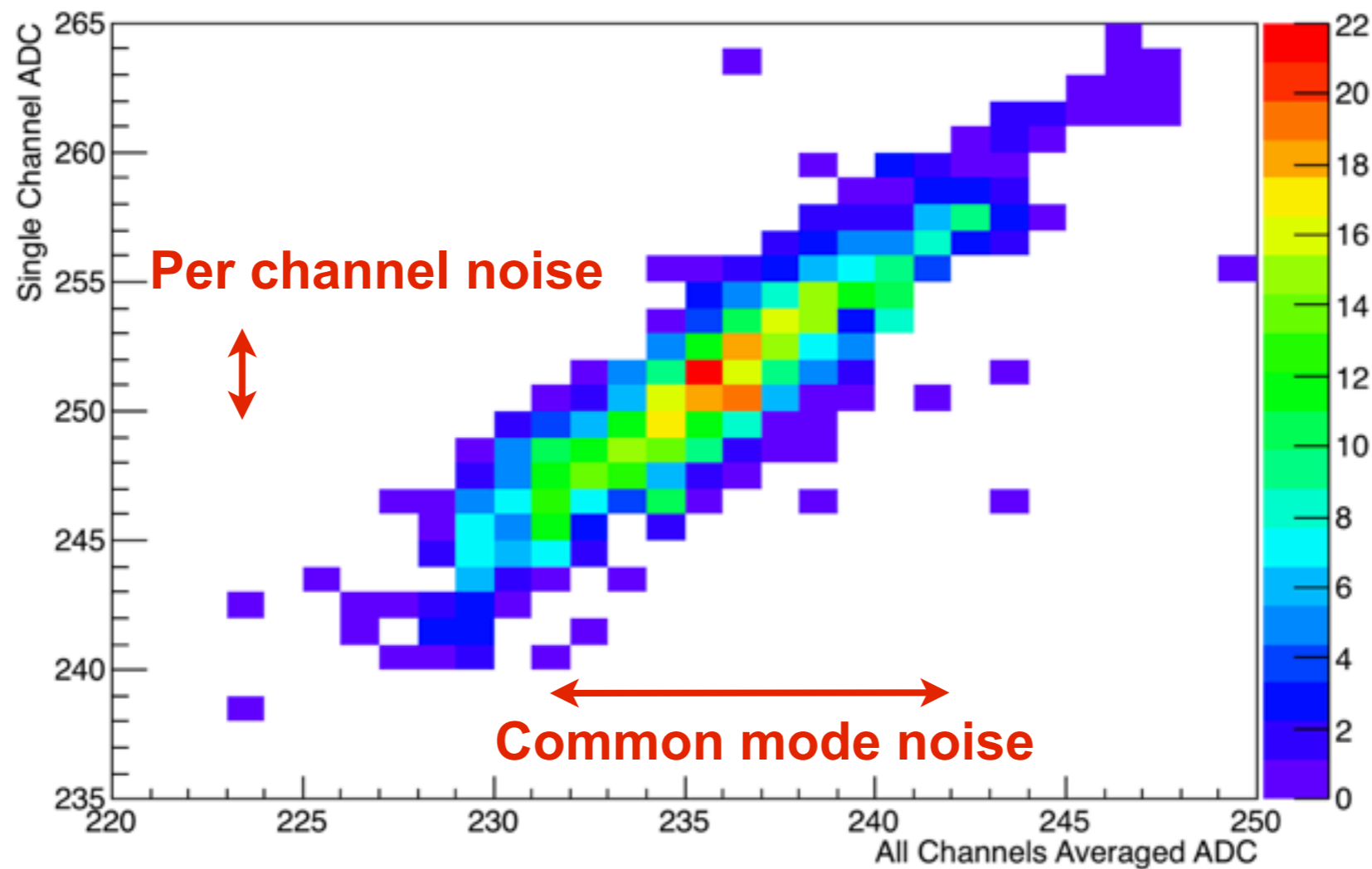
- Commercial ZedBoard: FPGA and CPU running Linux in a single CHIP
- Allows easy transfer of data from FPGAs to Computers
- Scales from 1 to 28 FMC-IO boards

Installed HGC Prototype, FNAL March 23



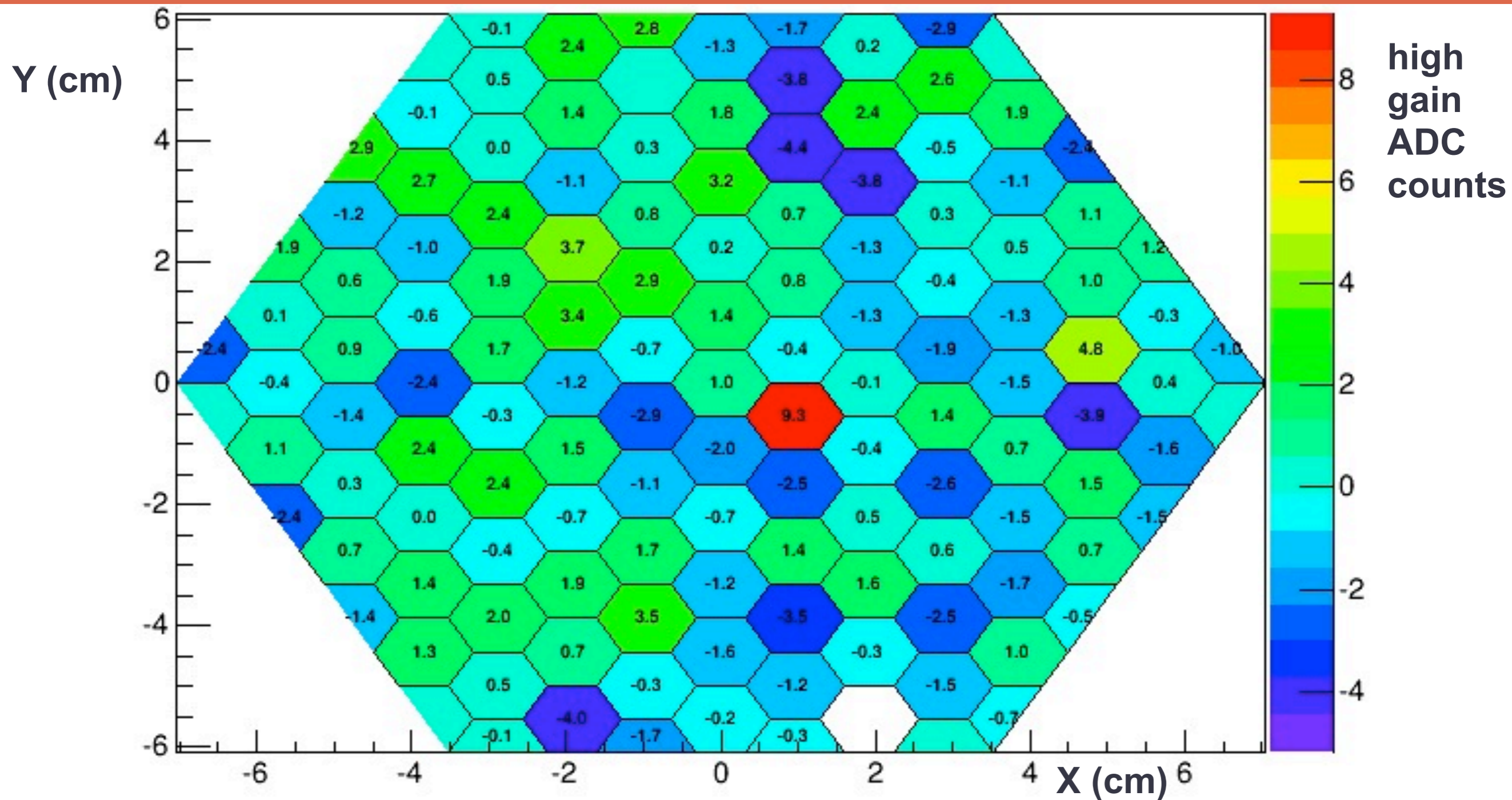
Pedestal Subtraction

- Pedestal runs (no beam) are used to estimate the per channel pedestals
- Observed common mode noise in addition to per channel noise



- Fit pedestal subtracted distribution of ADC counts per event to determine common mode noise and subtract it

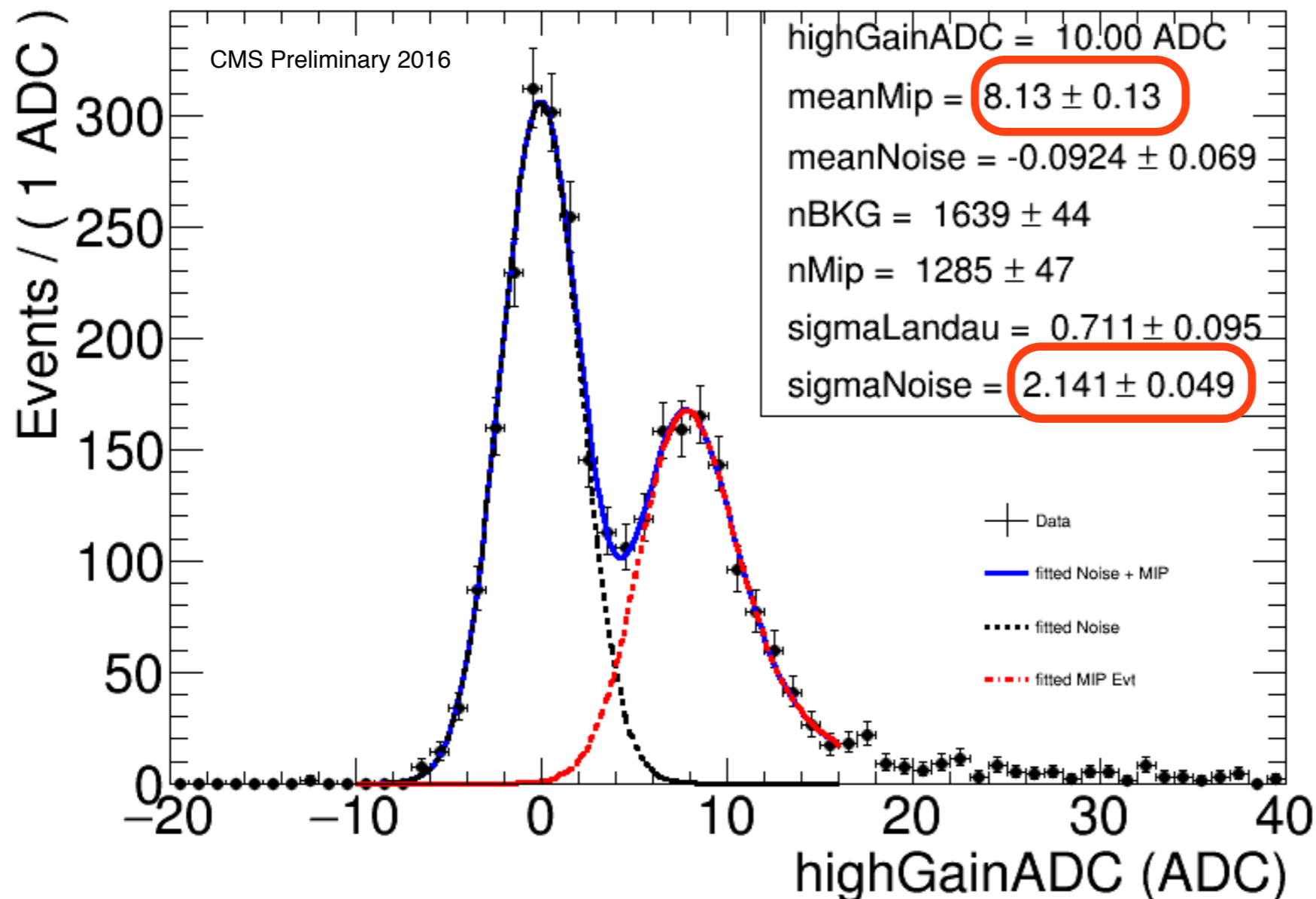
120 GeV Proton, Event Display



- **ADC count is proportional to energy deposited in Si**
 - Shown values are after pedestal subtraction
- **Most 120 GeV protons appear as MIP, only 0.3λ of absorber**

120 GeV Protons as Proxy to MIP

- **120 GeV protons is the primary beam at Fermilab Test Beam**
 - Muons are available as small fraction of secondary beam, less collimated and requires selection
- **Using 120 GeV protons as a proxy to MIP and calibration**



- Plot shows distribution of ADC counts for the cell in the beam line
- Run contains background triggers (blue peak) and proton triggers (read peak)
- Fit Gaussian + Landau convoluted with Gaussian of same width
- **Define 1 MIP = 8.13 ADC**

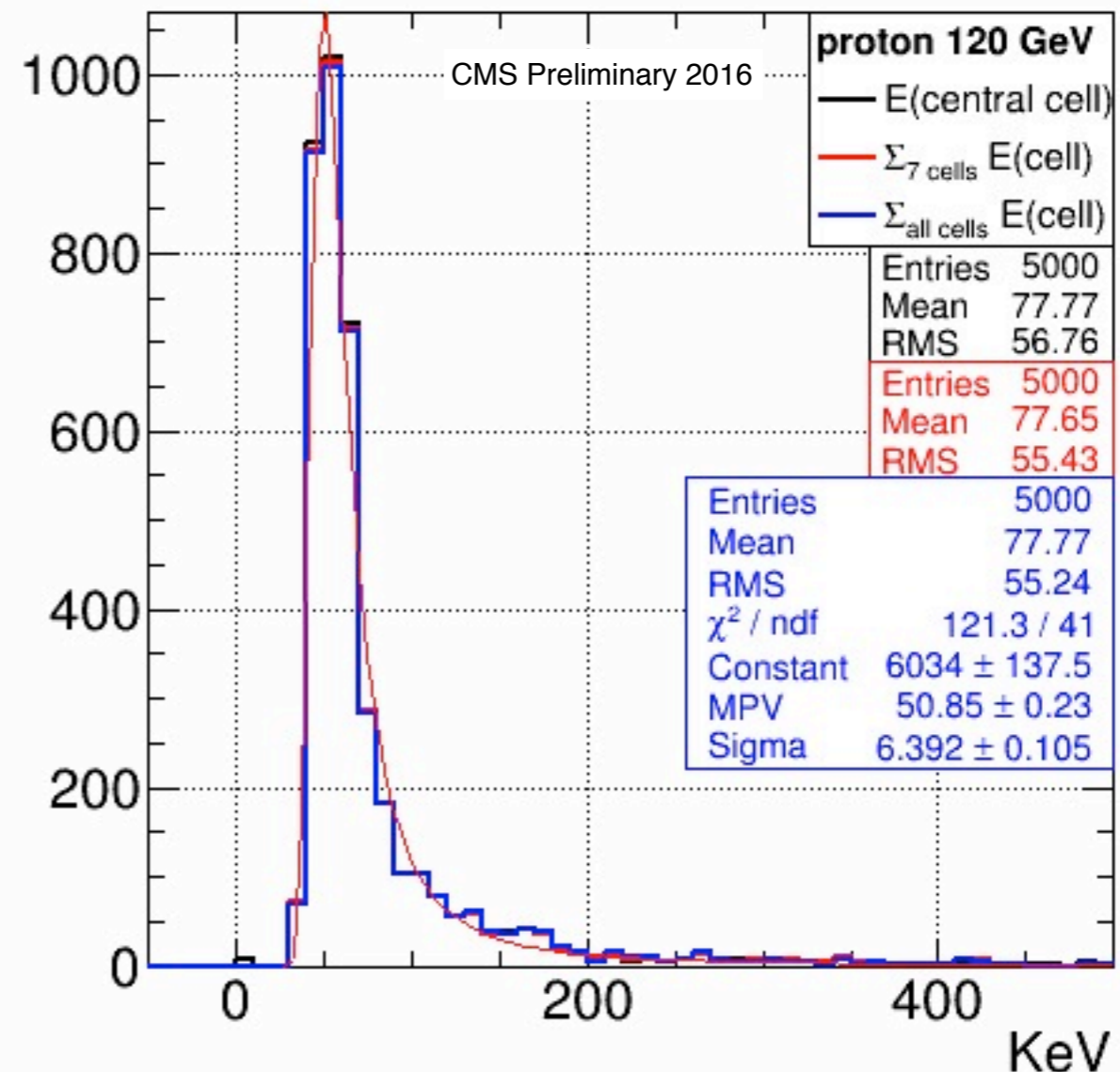
Simulation of 120 GeV Protons

Thickness (mm)	Material	Notes
Front (beam side) of		
4.2	"W"	
6.0	"Air"	
4.2	"W"	
6.0	"Air"	
4.2	"W"	
6.0	"Air"	
2.1	"W"	
6.0	"Air"	
2.1	"W"	
6.0	"Air"	
2.1	"W"	
3.0	"Air"	
6.0	"Cu"	
1.2	"WCu"	
0.01	"Air"	kapton
0.12	"Si"	
0.1	"Si"	depletion zone
0.1	"Si"	depletion zone

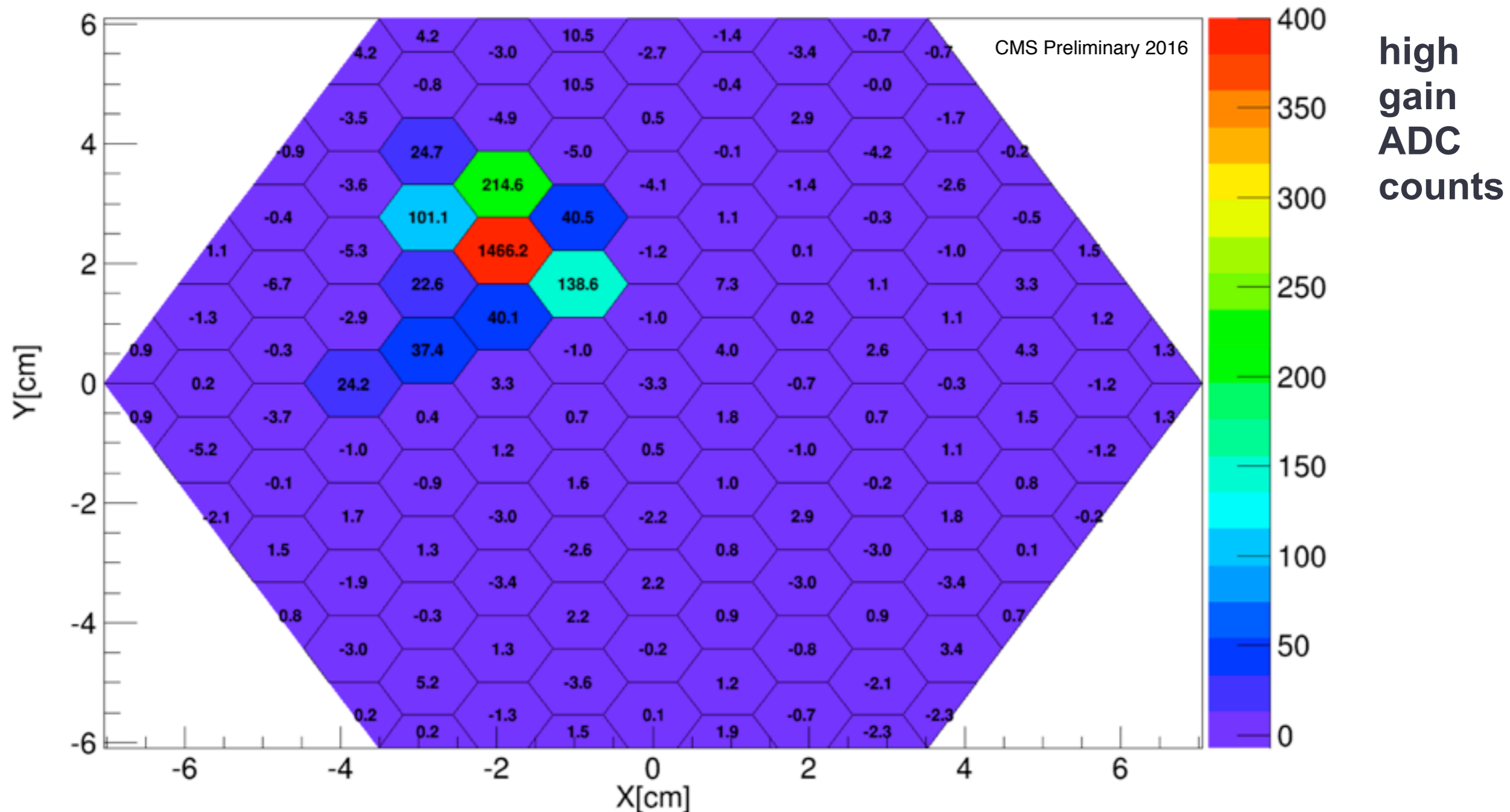
- **Standalone Geant 4 simulation**

- 120 GeV proton gun shooting at the material budget of the prototype

- **MPV of Landau fit: 50.9 keV, defines 1 MIP as in test beam data**



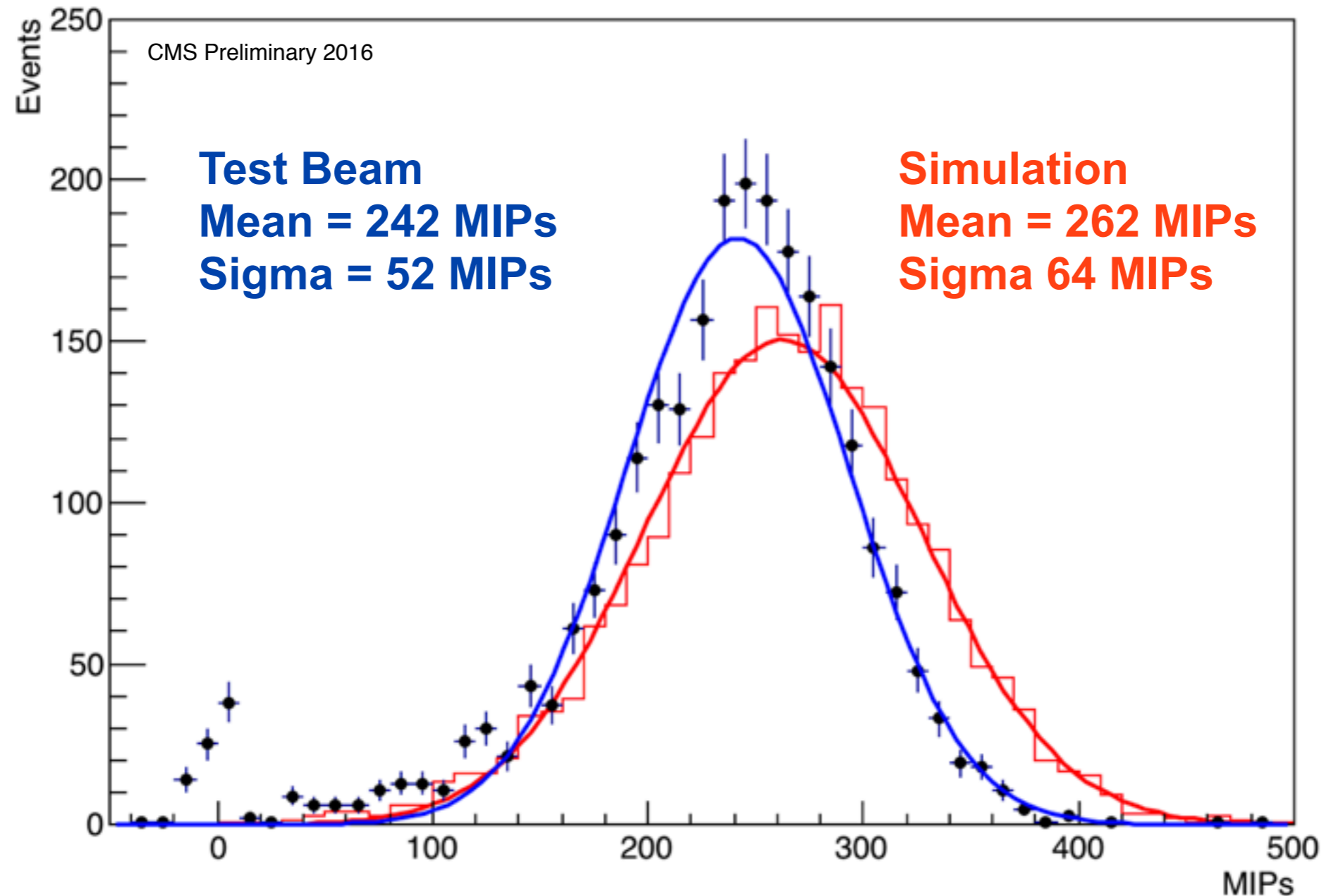
32 GeV e^- Event Display



- **Event display of an electron candidate**
- **The pedestals have been subtracted**
- **Size of cluster ~ 2 cm radius**

Response to 32GeV e^- at $6 X_0$

- After pedestal subtraction, all cells summed up in the event



- Preliminary results show 8% agreement between test beam measurements and simulation

Conclusions and Next Steps

- **Successfully constructed and operated the first HGC module in the Fermilab Test Beam**
 - Assembled the module stack according to the technical proposal
 - Verified wire bonding capability of PCB to sensor with deep access wire bonder
- **Results are within 8% of simulations**
- **Next, building a prototype with up to 28 Si layers for the Fermilab May beam test**
 - **Collect Test Beam data, analyze and compare performance to simulations**
- **CERN Test Beams are planning large-scale tests**
- **28 ECAL + 12 HCAL prototype is especially challenging due to large number of modules (112) / channels (14000)**
 - Will use faster SKIROC-CMS ASIC
 - Explore constant term
 - Perform timing studies

