Upgrade of Tile Calorimeter of the ATLAS detector for the High Luminosity LHC.

"CALOR 2016" conference, Daegu, South Korea, May 15 - May 20, 2016.)

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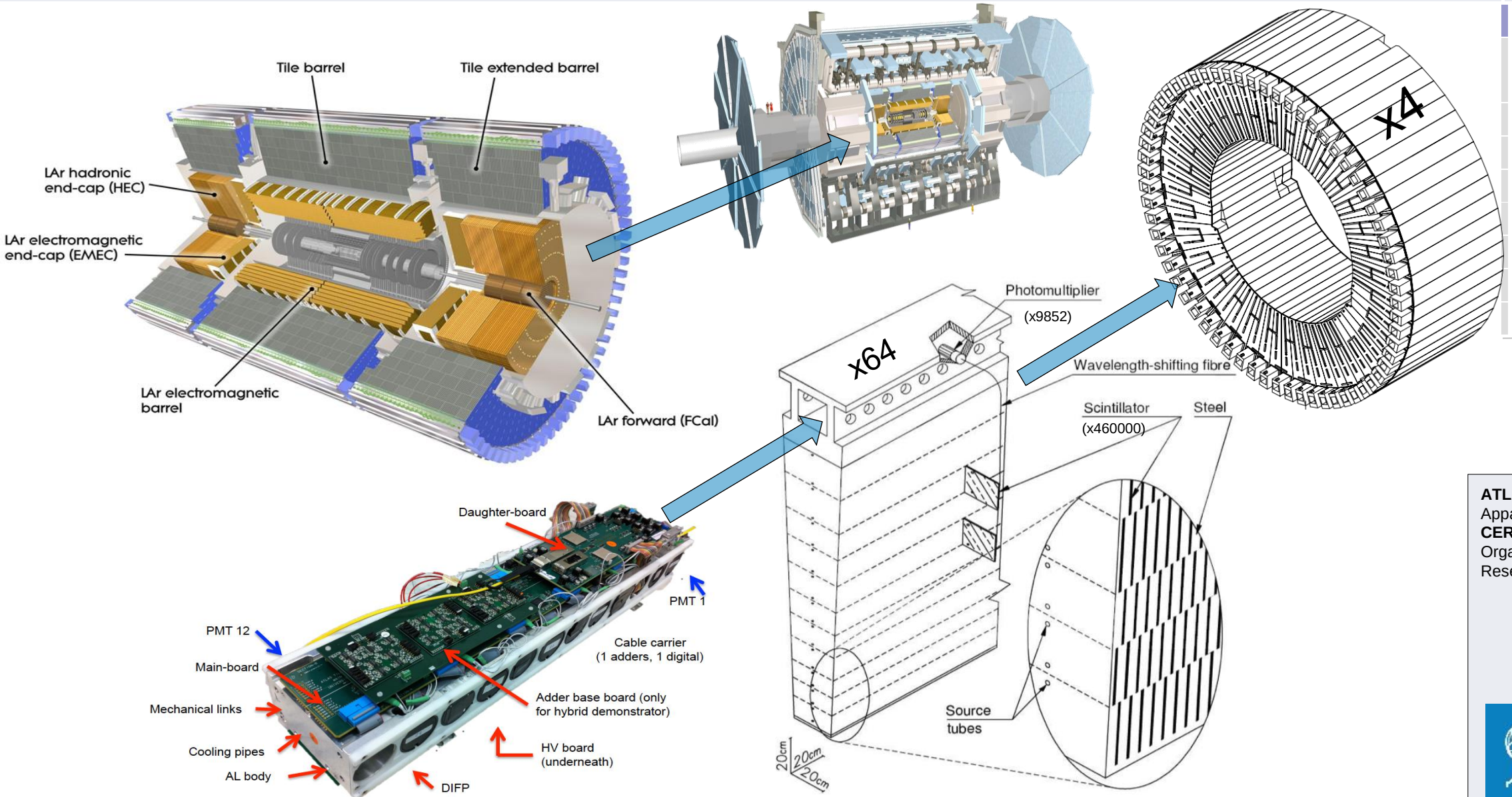
Introduction…

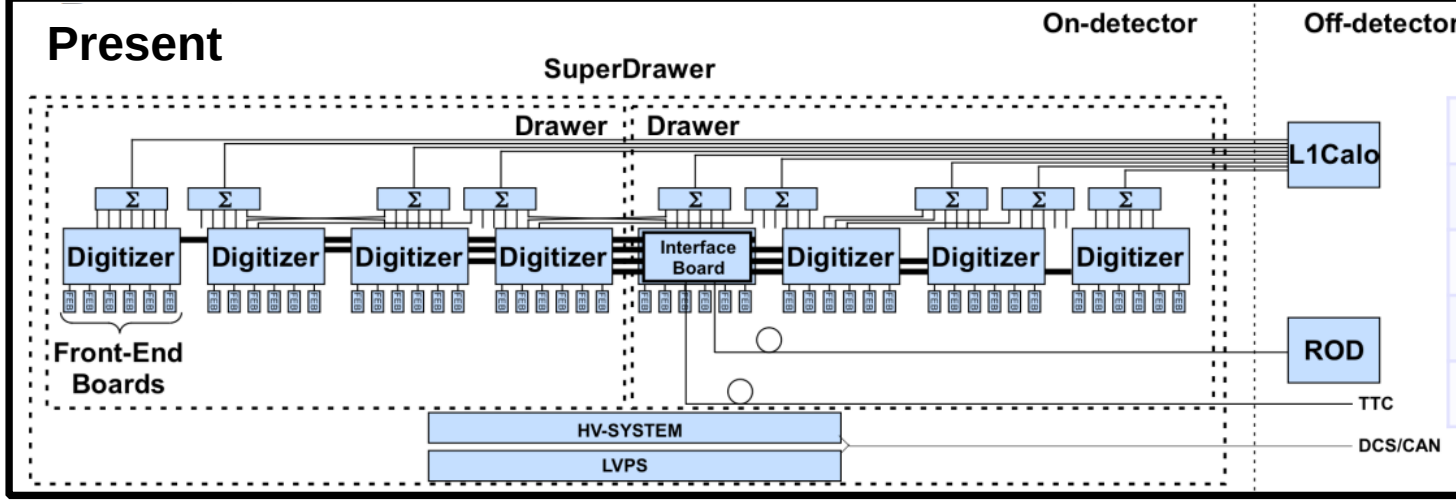


ATLAS: A ToroidaL ApparatuS.
CERN: European Organization for Nuclear Research.

Eduardo Valdes S... PhD

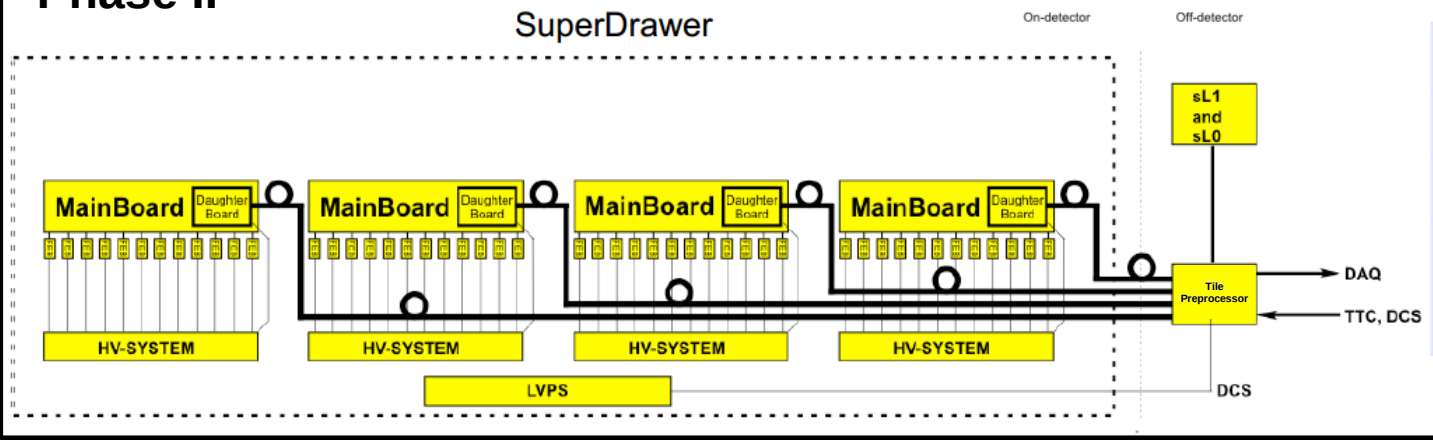
From present to phase II…

Present



Total data rate	~165 Gb/s
Number of links	256
Data rate per link	640 Mb/s
Links per super-drawer	1 (+1)
Data rate per super-drawer	640 Mb/s

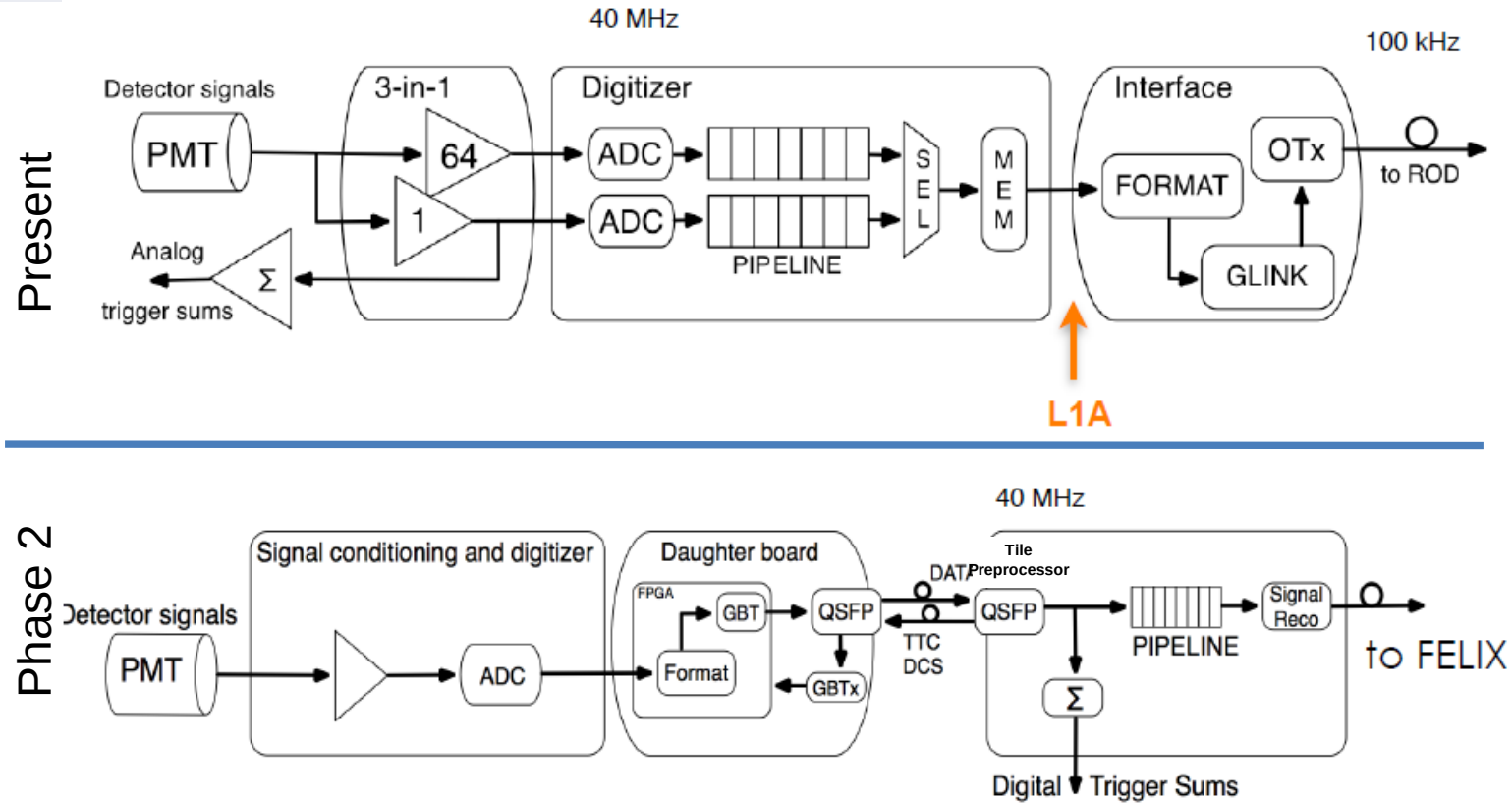
Phase II



Total data rate	~80 Tb/s
Number of links	8192
Data rate per link	10 Gb/s
Links per super-drawer	4x4 (+4x4)
Data rate per super-drawer	160 Gb/s

ROD: Read Out Driver
TTC: Trigger Timing and Control
LVPS: Low Voltage Power Supply
DCS: Detector Control System
L1Calo: Level 1 Calorimeter trigger
sLX: super Level X calorimeter trigger
HV: High Voltage
CAN: Controlled Area Network.
∑: Summation Cards
FELIX: Front-End LInk eXchange

From present to phase II…



Up Link only	Present	Upgrade
Total BW	***~ 165 Gbps***	***~80 Tbps***
Nb fibers	256	8192
Fiber BW	***640 Mbps***	***10 Gbps***
Nb RODs	32	32?
ROD Crates	***4***	***4***
In BW/ROD	5 Gbps	2 Tbps
Out BW/ROD DAQ	***2,56 Gbps***	***~ 20 Gbps***
Out BW/ROD L1	Analog FE	< 80 Gbps

- Complete replacement of on-detector and off-detector electronics
- New readout strategy to provide digital trigger information at low latency for L0/L1
- Pipelines, derandomizers, DCS&TTC interface moved off-detector
- Improve reliability: reducing interconnections and stack of boards, implementing redundancy
- Minimize impact of failures with smaller DAQ elements: 1 super drawer is split in 4 independent mini-drawers with full redundant data path and powering.

Timeline ($^{4}/_{21}$)

ROD: Read Out Driver
TTC: Trigger Timing and Control
LVPS: Low Voltage Power Supply
DCS: Detector Control System
L1Calo: Level 1 Calorimeter trigger
L1A: Level 1 Acceptance (from the ATLAS level 1 Central Trigger).
sLX: super Level X calorimeter trigger
HV: High Voltage
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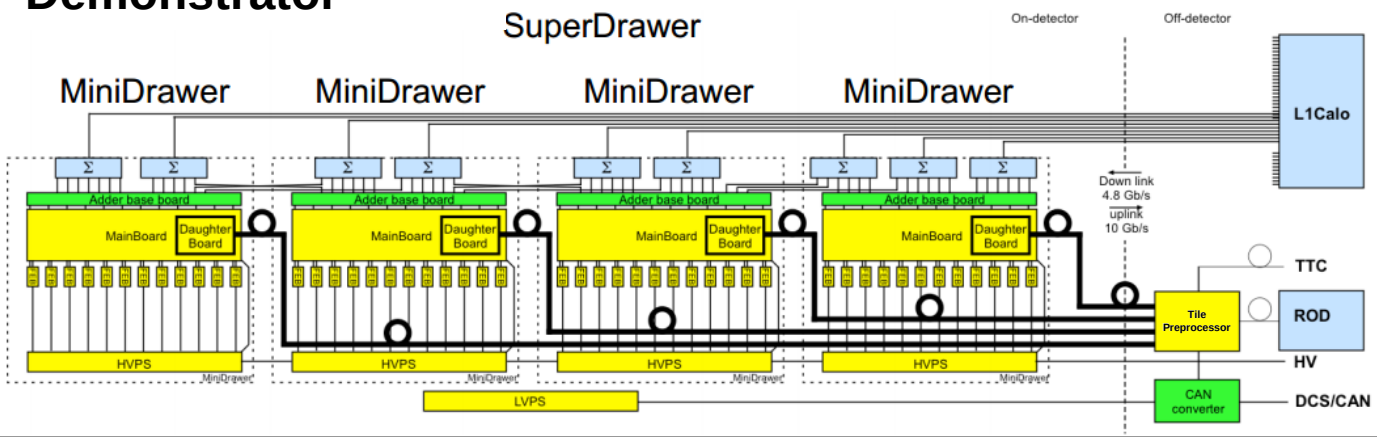
Hybrid drawer for the insertion in the current ATLAS detector…

Demonstrator



Total data rate	~80 Tb/s
Number of links	8192
Data rate per link	10 Gb/s
Links per super-drawer	4x4 (+4x4)
Data rate per super-drawer	160 Gb/s

- Compatibility of on detector and off-detector electronics with the current system (Hybrid drawer).
- Possibility of insertion in ATLAS for testing the performance of the upgrade system without compromising the present data taking.

ROD: Read Out Driver
TTC: Trigger Timing and Control
LVPS: Low Voltage Power Supply
DCS: Detector Control System
L1Calo: Level 1 Calorimeter trigger
sLX: super Level X calorimeter trigger
HV: High Voltage
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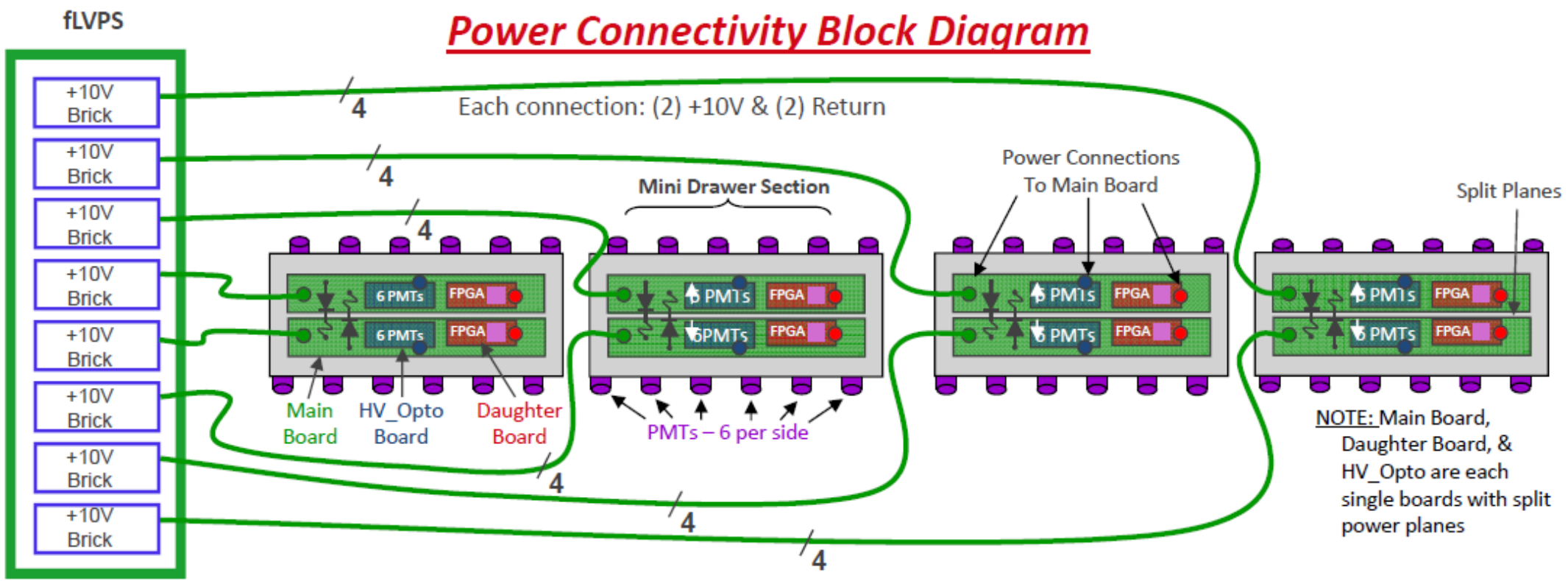
Demonstrator…

- New LVPS
- 2 different HVPS are proposed
- 3 different front end solutions are proposed
  - Modified 3 in 1 cards + mainboard
  - QIE + mainboard
  - FATALIC + mainboard
- A common control “daughterboard” compatible with the 3 front end solutions.
- One off detector tile preprocessor that will communicate with the on detector electronics and make the system compatible with the current tilecal electronics.

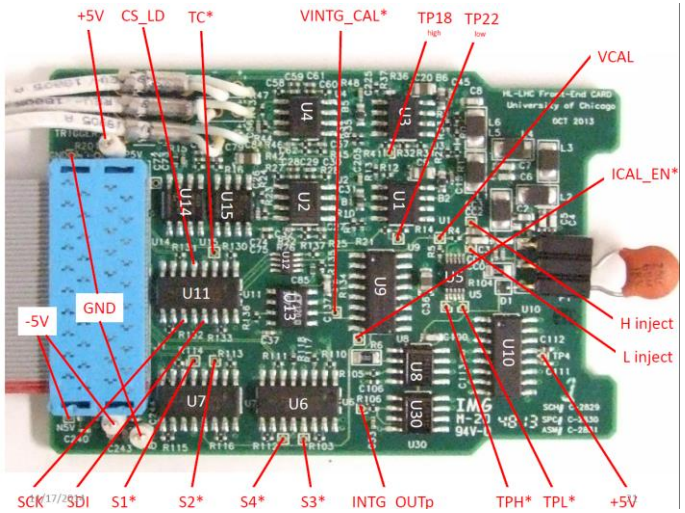
Low Voltage Power Supply and HV OPTO briefly…



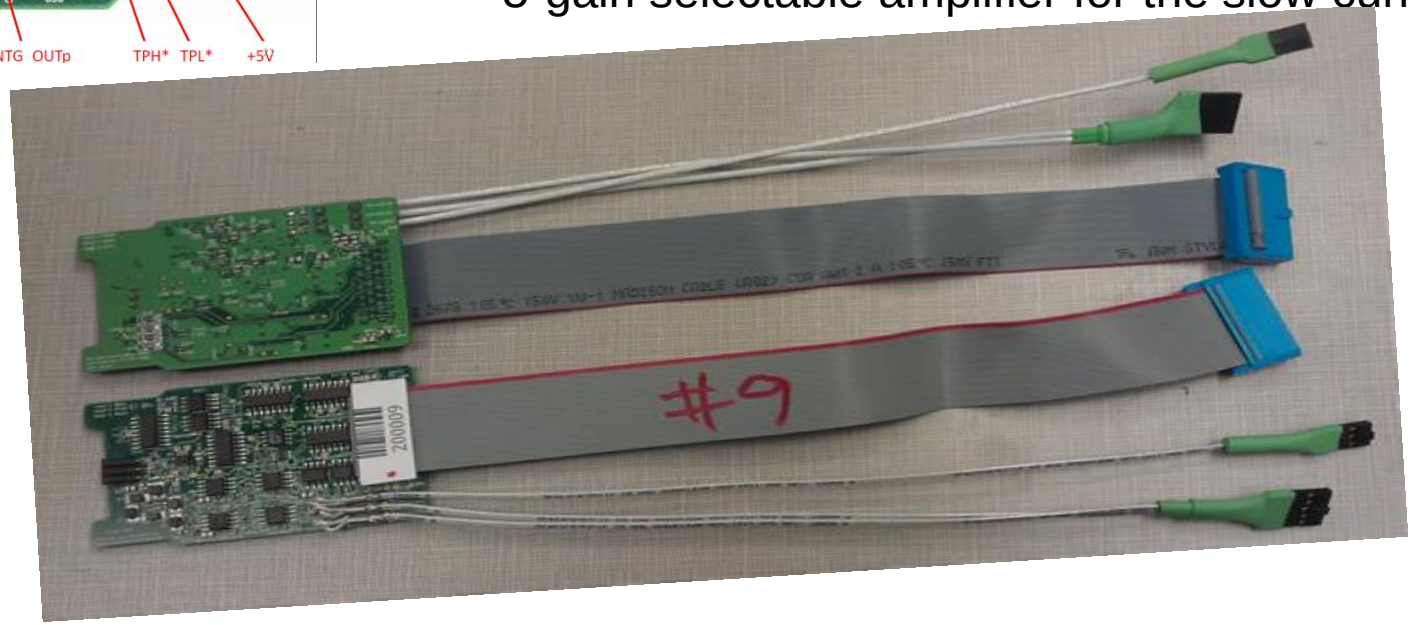
- New LVPS and HVPS with double redundant design.
- Two High Voltage solutions are proposed with local or remote source.

PMT: Photomultiplier
FPGA: Filed Programmable Gate Array.

3 in 1 Front end cards + Mainboard…

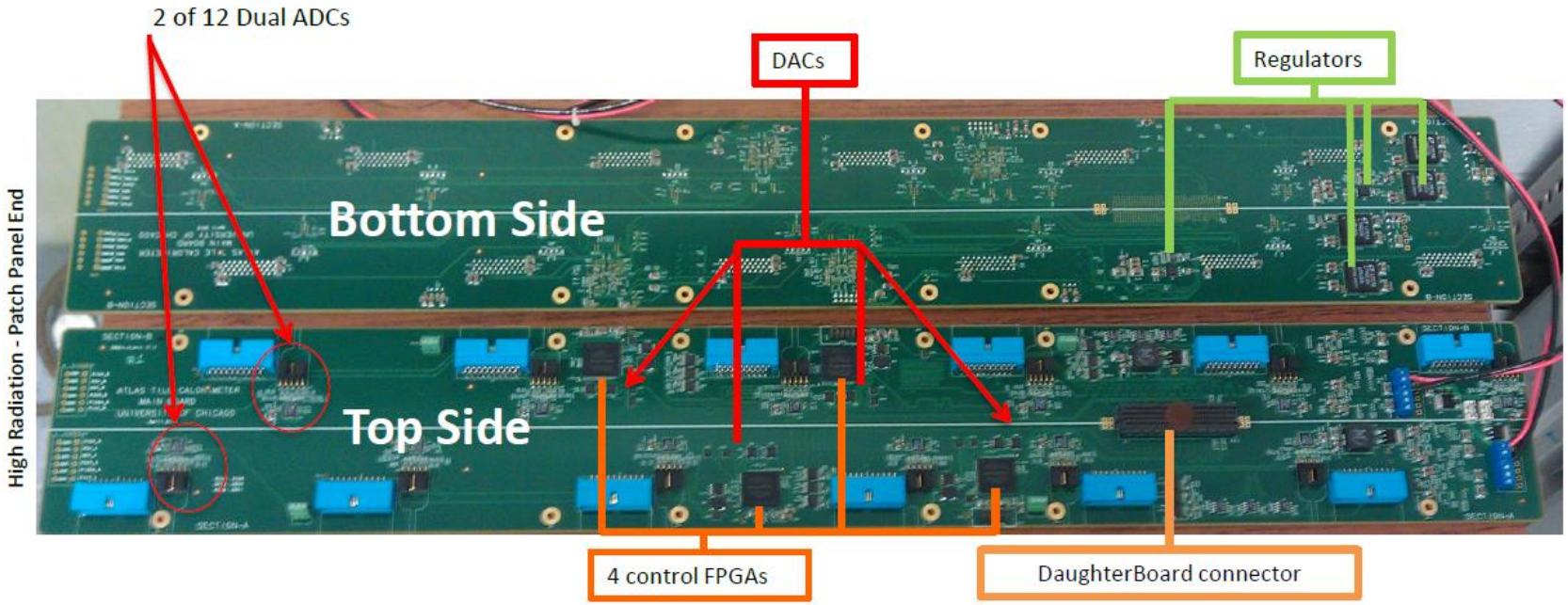


- Current design with modern components and improved performance
- Better linearity.
- Successful radiation tests.
- shape the PMT signal to a stable pulse with 27 ns width.
- bi-gain system with gain ratio 32.
- 17 bit dynamic range.
- injects calibration pulses
- 5-gain selectable amplifier for the slow current integrator



3 in 1:
- High and low gain analog outputs
- Charge injection calibration
- Integrator to read out Cs calibration data

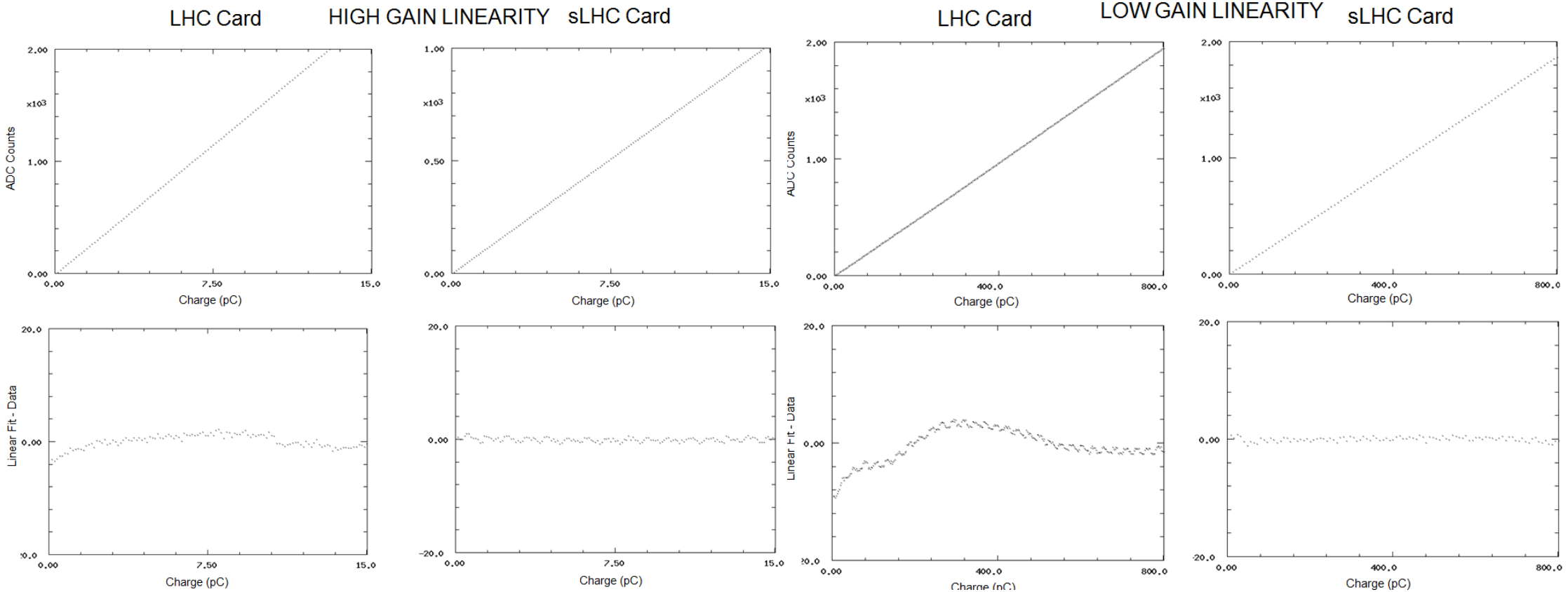
3 in 1 Front end cards + Mainboard…



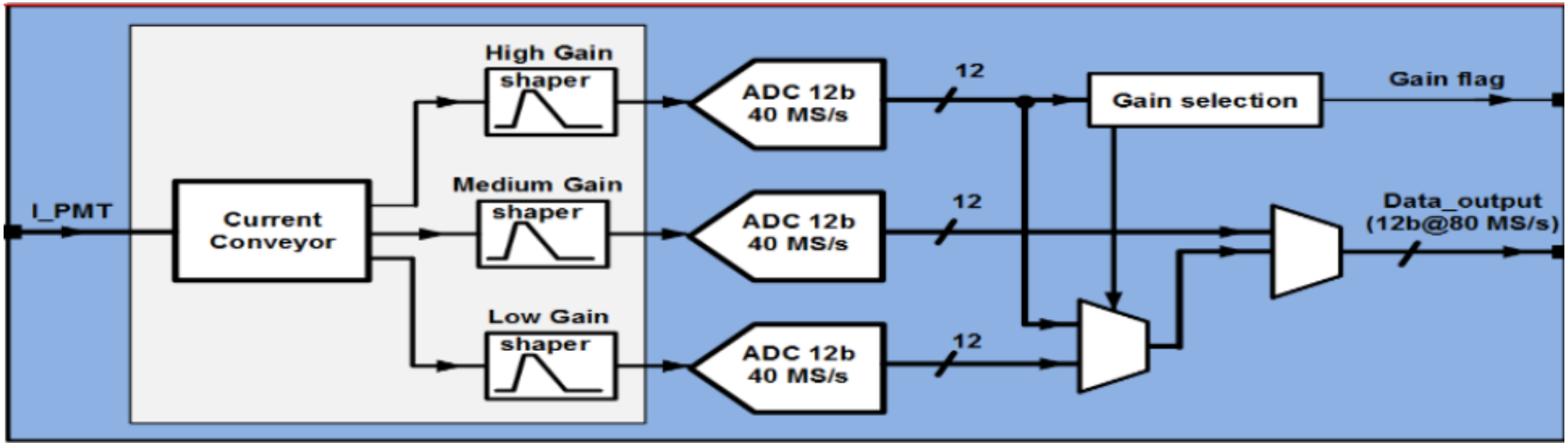
- interfaces the front end cards to the Daughter Board.
- two independent symmetric parts.
- each part reading out all cells.
- Supply low voltage levels to frontend cards and Daughter Board.
- Digitize fast and slow signals, and send parallel streams to the Daughter Board.
- Set gains on 3-in-1 frontend cards.
- Control DAC for charge injection calibration.

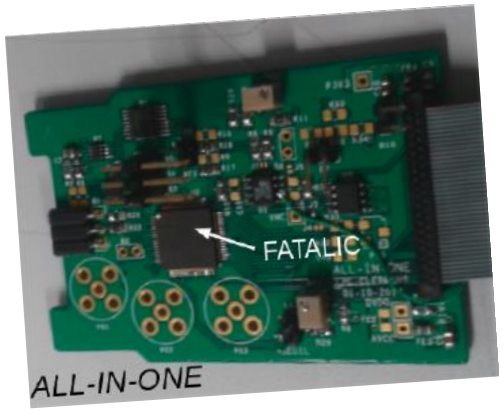
Timeline ($^{9}/_{21}$)

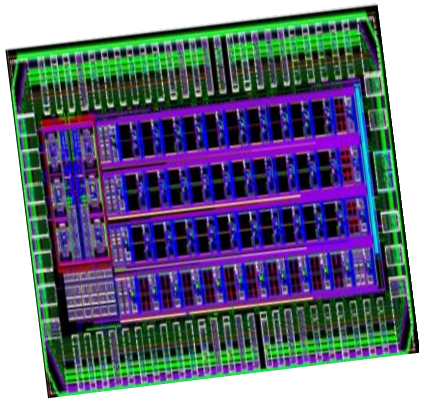
3 in 1 Front end cards + Mainboard… Better performance than current electronics…



Front-end ATlAs tiLe Integrated Circuit (FATALIC)

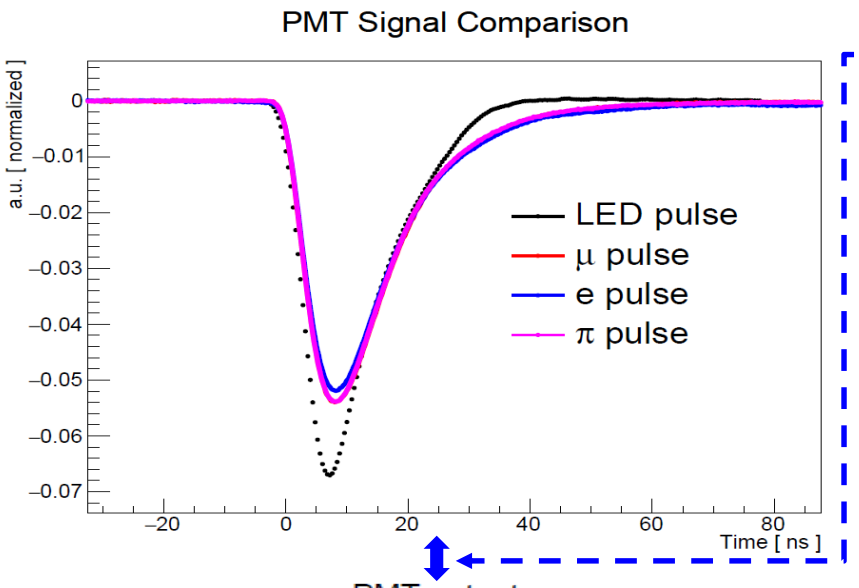


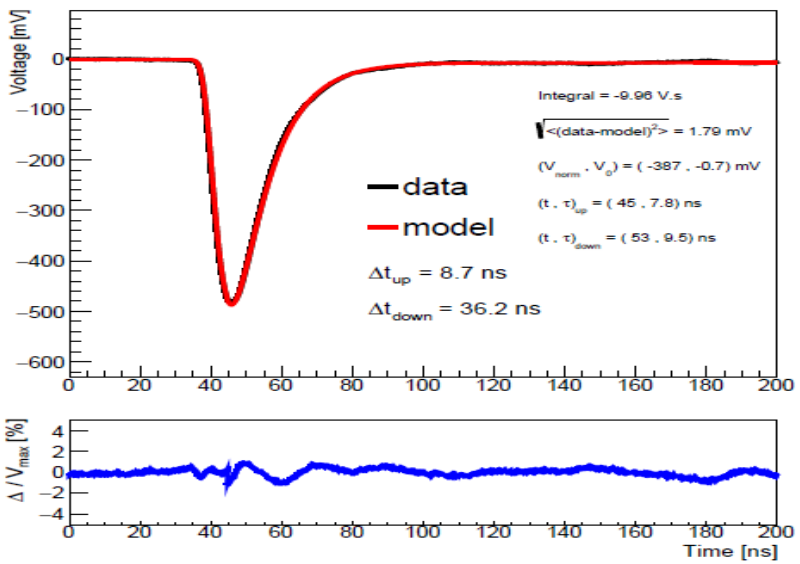


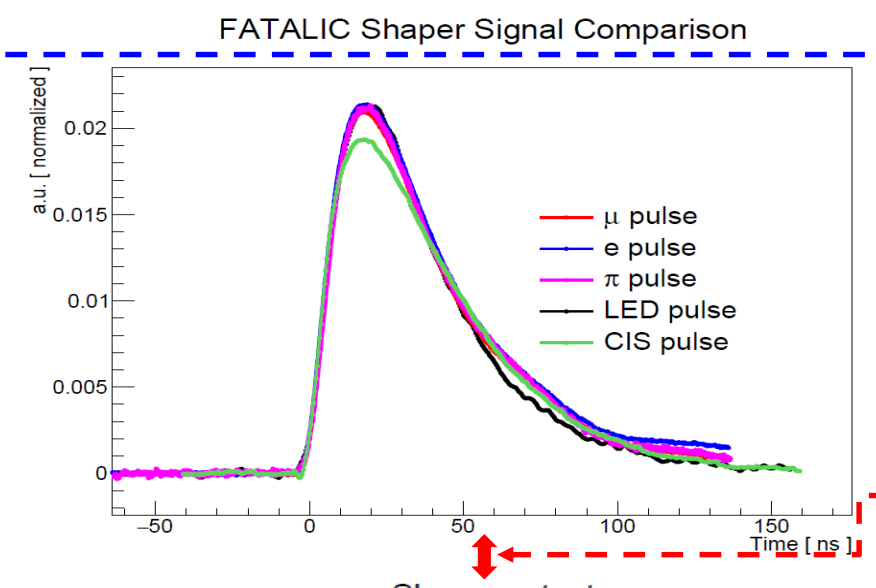


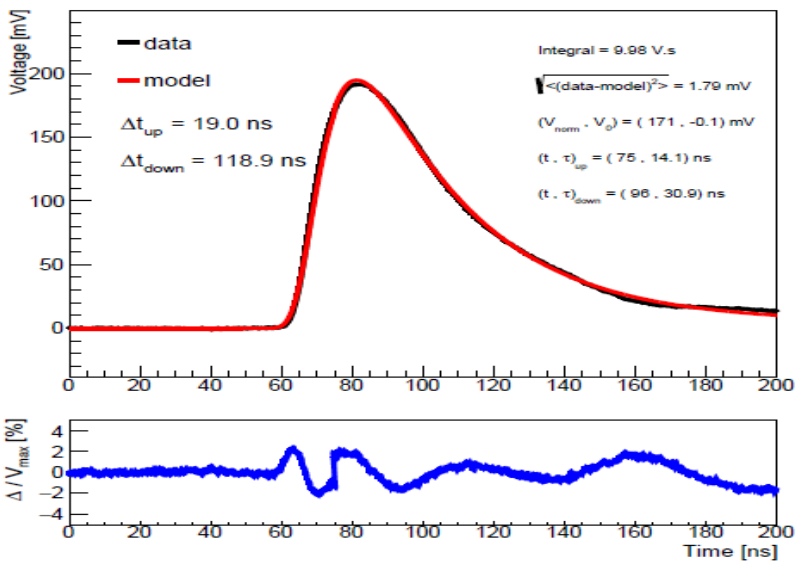
- Potentially low noise chip.
- Most functionality in ASIC.
- 3 signal paths for analog processing.
- 3 embedded 12-bits ADCs
- Auto Gain Selection (Medium + (High or Low))
- 2 x12 bits data output (2 gains)

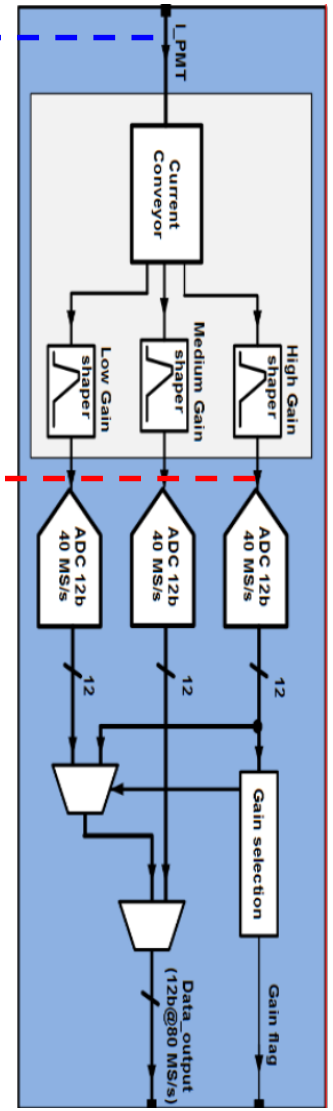
Calibration tests… Pulse Analysis…





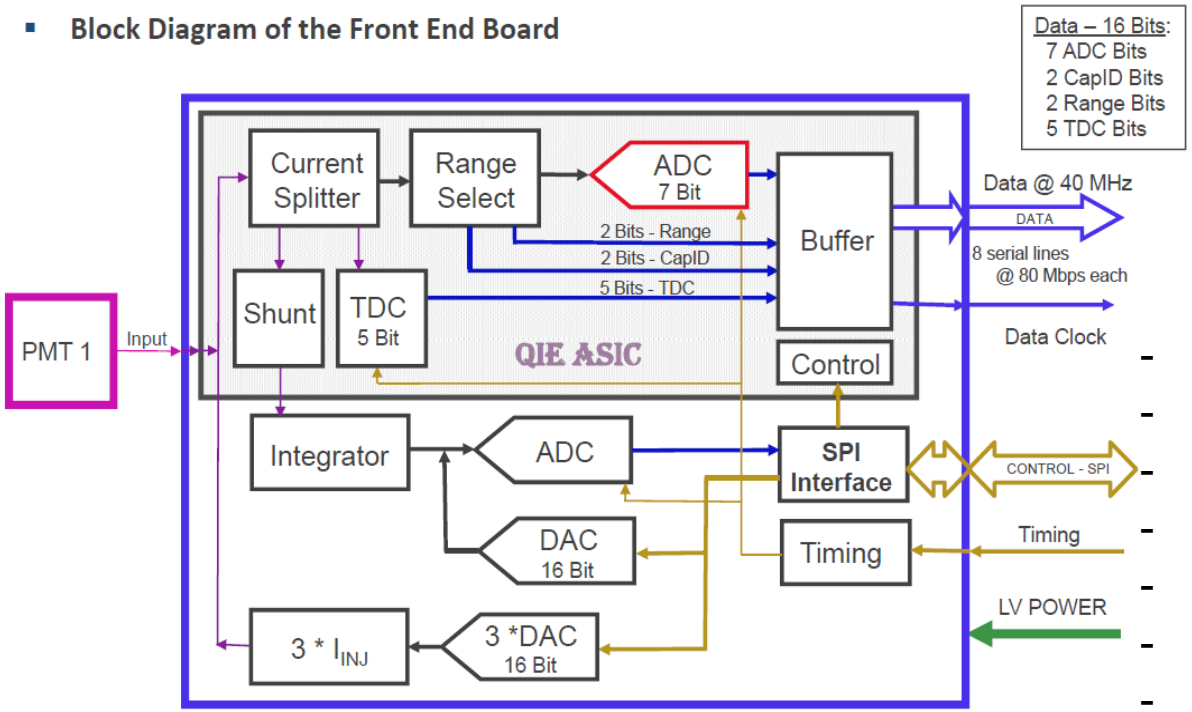




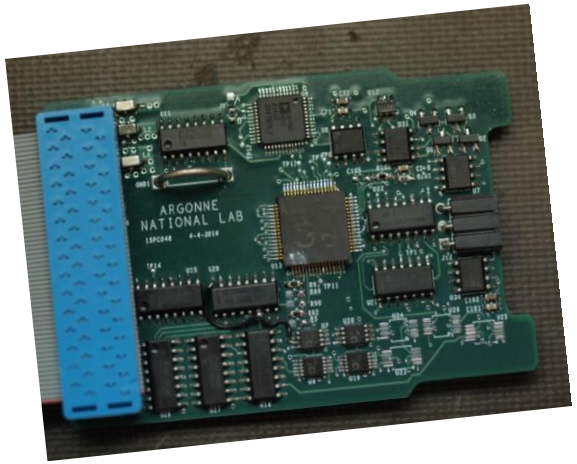


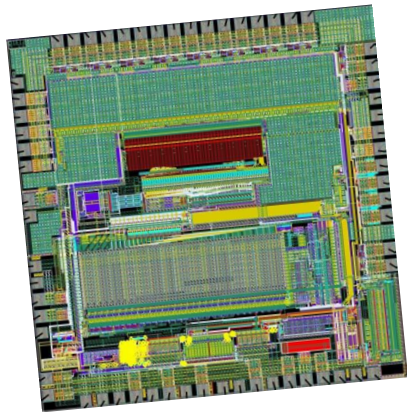
QIE Front End Board

- **Block Diagram of the Front End Board**



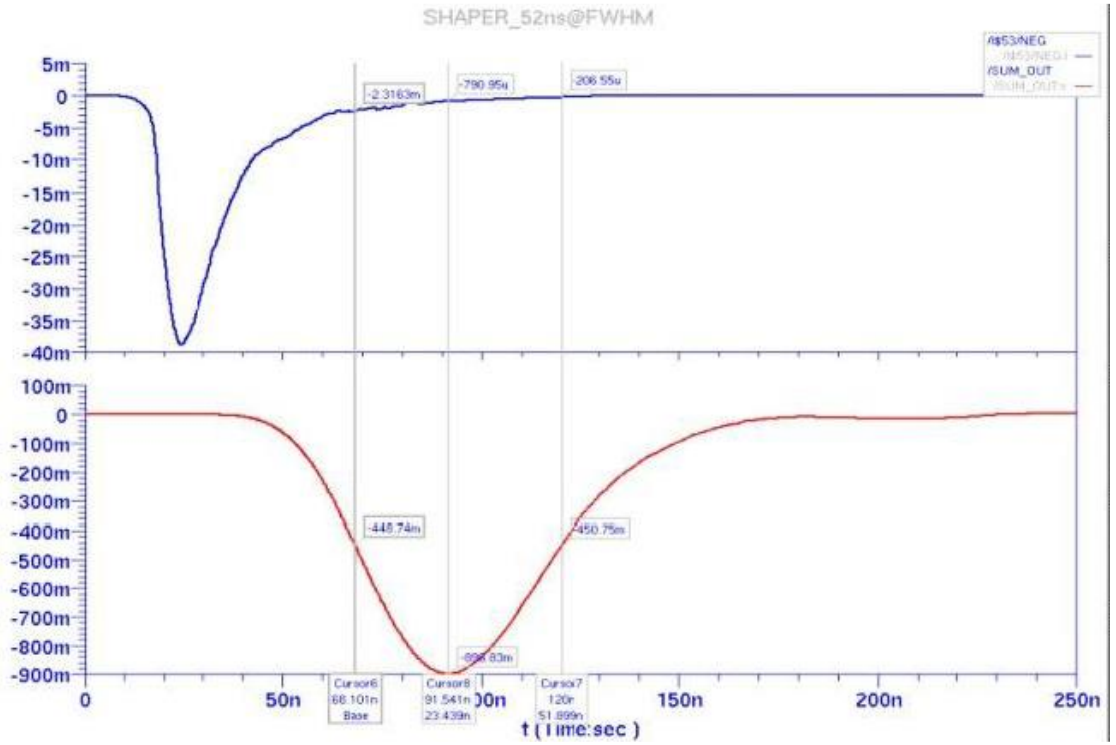
- "Current Splitter" with gated integrator
- 4-range Charge Integrator
- 17 bits of dynamic range
- 5 bits Internal TDC -> 1 ns resolution
- (4) 16-bit DACs for calibration
- No Pulse Shaping
- Dead-timeless Digitization at 40 MHz
- Pipelined operation
- Radiation tolerant (SiGe for TID; SEU-tolerant design)

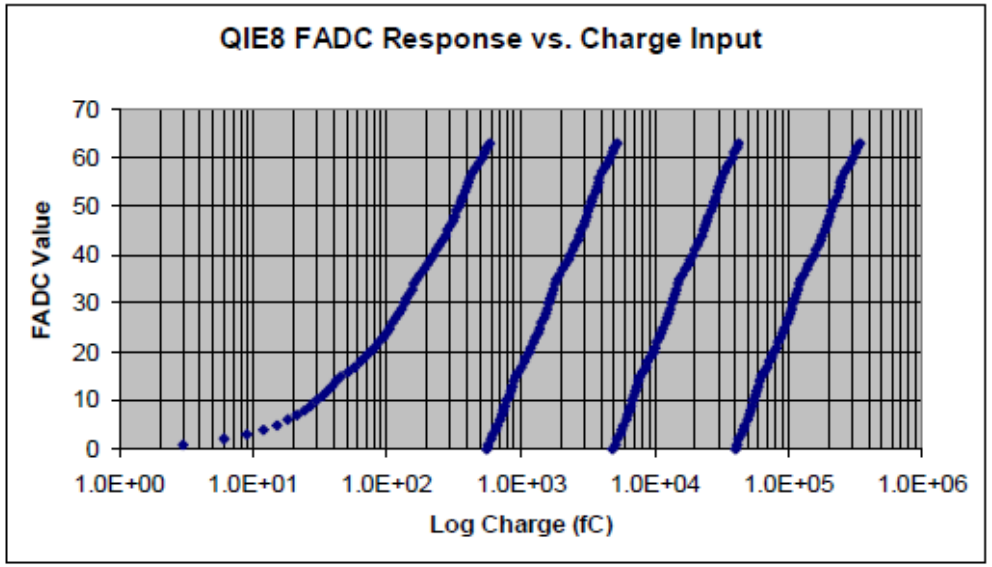


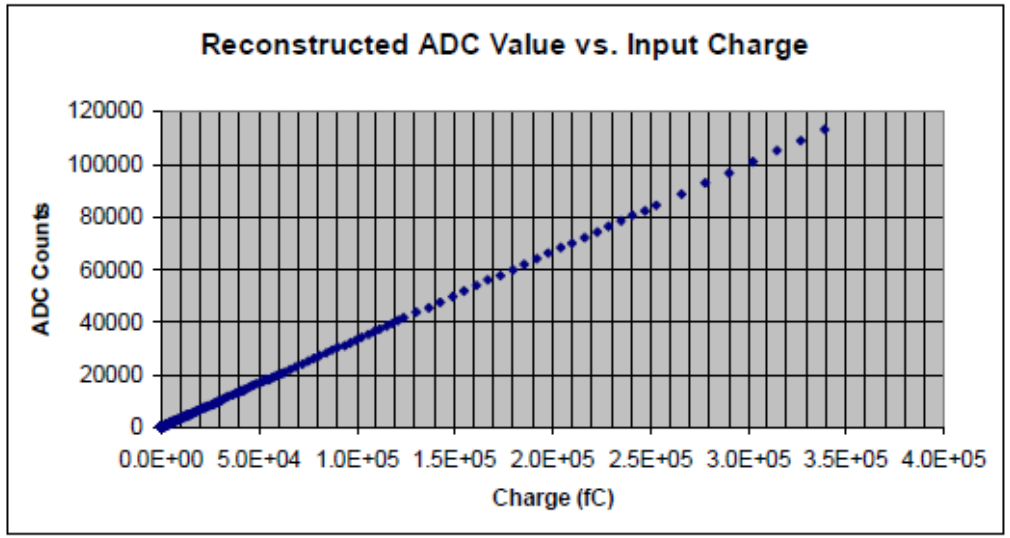


SiGe: Silicon-Germanium
TID: Total Ionizing Dose
SEU: Single Event Upsets
TDC: Time to Digital Converter

Tests and calibration…

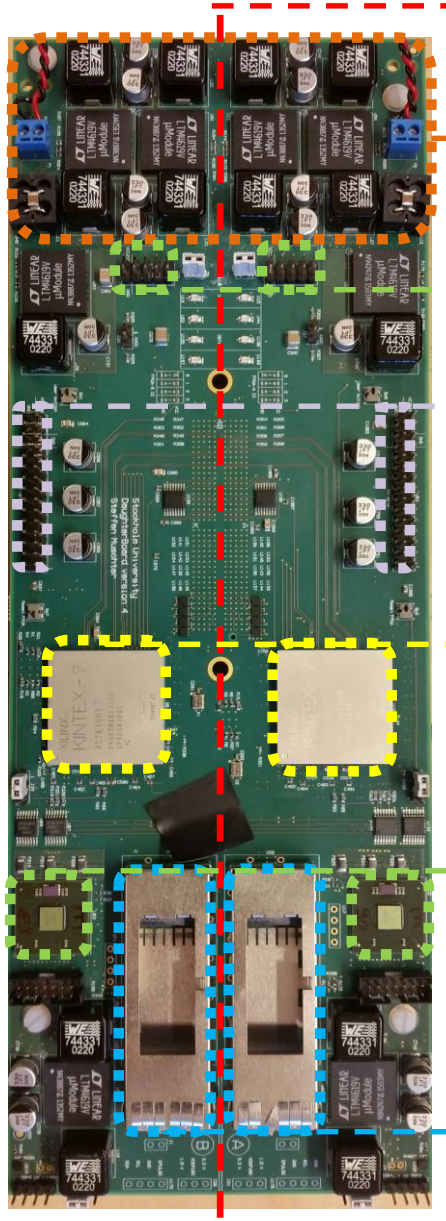






Timeline ($^{14}/_{21}$)

Daughterboard (r4)…



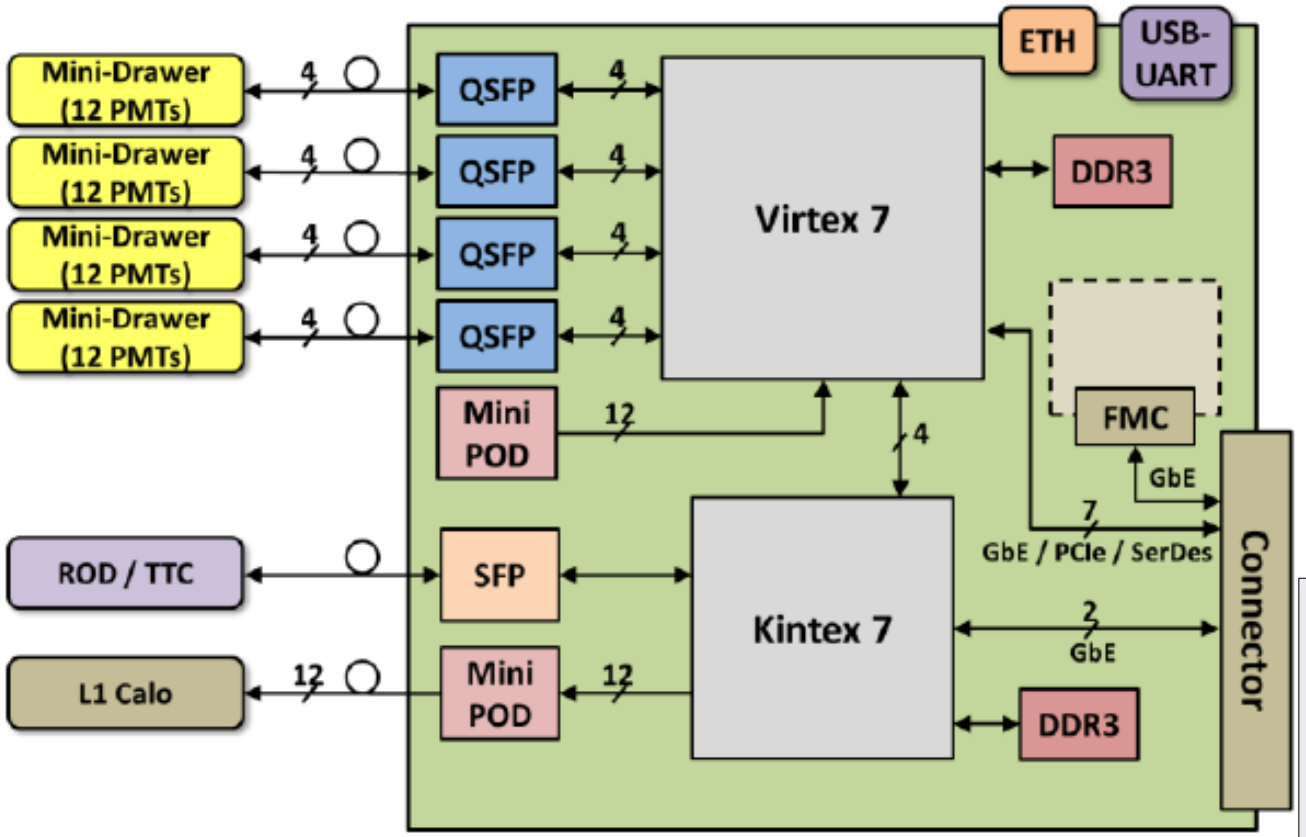
- Control and communication of the front end with back end.
  - Mainboards
  - HV Opto
  - Cesium Calibration System

- Common front end and read out interface for all the alternatives.
- System Clock recovery and distribution to the front end.
- Daughterboard current and temperature monitoring.
- High Speed communication: uplink (4x 9.6Gbps) and downlink (4x 4.8Gbps) with back end via one of the two QSFP (including additional 2 fold redundancy).

FPGA: Field Programmable Array
TTC: Trigger Timing and Control
QSFP: Quad Small Form-factor Pluggable
HV: High Voltage
GBTx: radiation tolerant chip with 3.2-4.48 Gbps communication via bidirectional optic links for High Energy Physics.

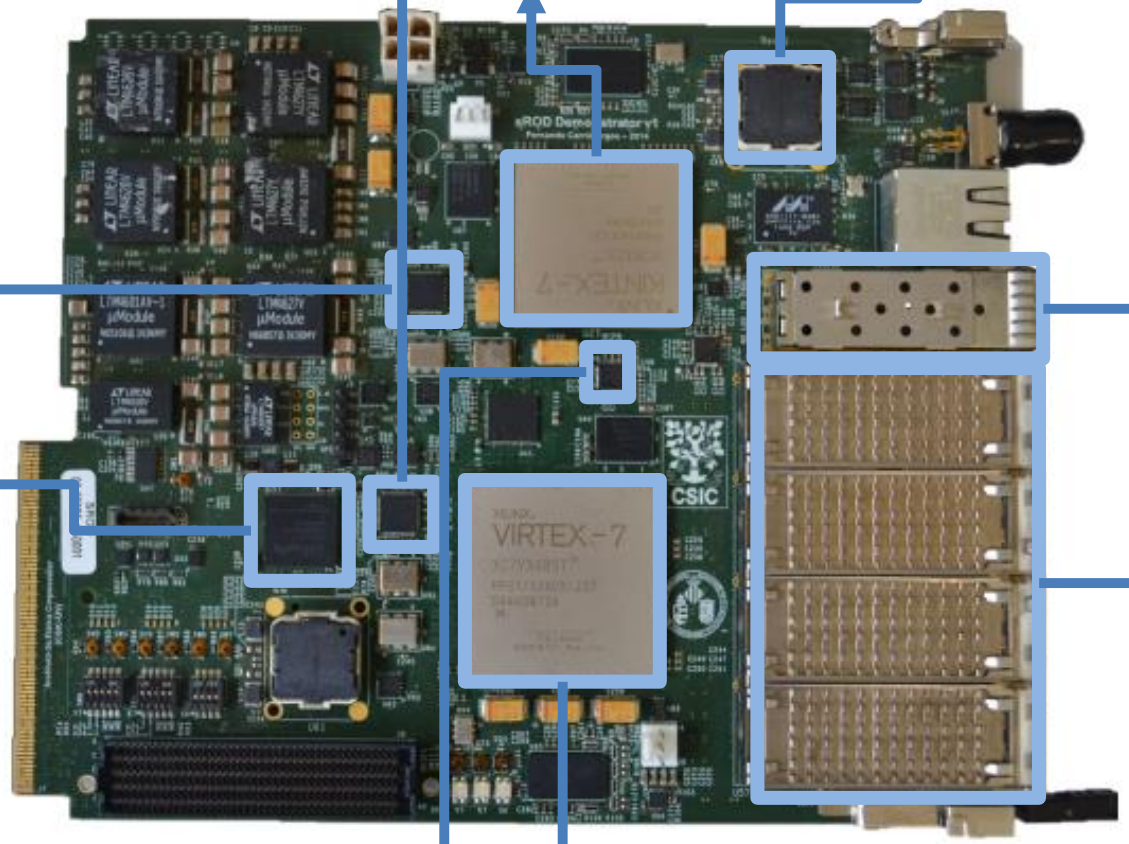
Tile Preprocessor Prototype (Off Detector)…

- Readout data coming from the detector
  - 4 Mini-Drawers
  - Up to 48 PMTs
- TTC distribution to the front-end electronics
  - Clock distribution for sync
- Communication with the Detector Control System (DCS)
  - Front-end electronics monitoring and configuration commands
- Keeps backward compatibility with the present DAQ system
  - G-Link to Legacy System
  - TTC decoding and clock recovery
- Real time data processing
  - Reconstruction algorithms: energy, time and quality factor
- Communication with the L0/L1 trigger system
  - Sending preprocessed data for L0/L1 trigger decision



ROD: Read Out Driver
TTC: Trigger Timing and Control
DCS: Detector Control System
L1Calo: Level 1 Calorimeter trigger.
LX: Level X trigger
QSFP: Quad Small Form-factor Pluggable
PMT: Photomultiplier Tube
FMC: FPGA Mezzanine Card.
SerDes: Serializer / Deserializer.

Tile Preprocessor Prototype (Off Detector)…



Jitter cleaners
- TI CDCE62005
- Low jitter (< 1ps)
- Clean recovery clocks for GTX
- Unify clock domains

Xilinx Kintex 7 FPGA
- XC7K420T
- 28 GTX transceiver @ 10 Gbps

MiniPOD TX
- 12 x 10 Gbps
- L0/L1 trigger comm.

SFP module
- TTC reception
- Communication with current DAQ system

4 x QSFP modules
- FE communication
- Each module at 40 Gbps
- Total max. BW: 160 Gbps

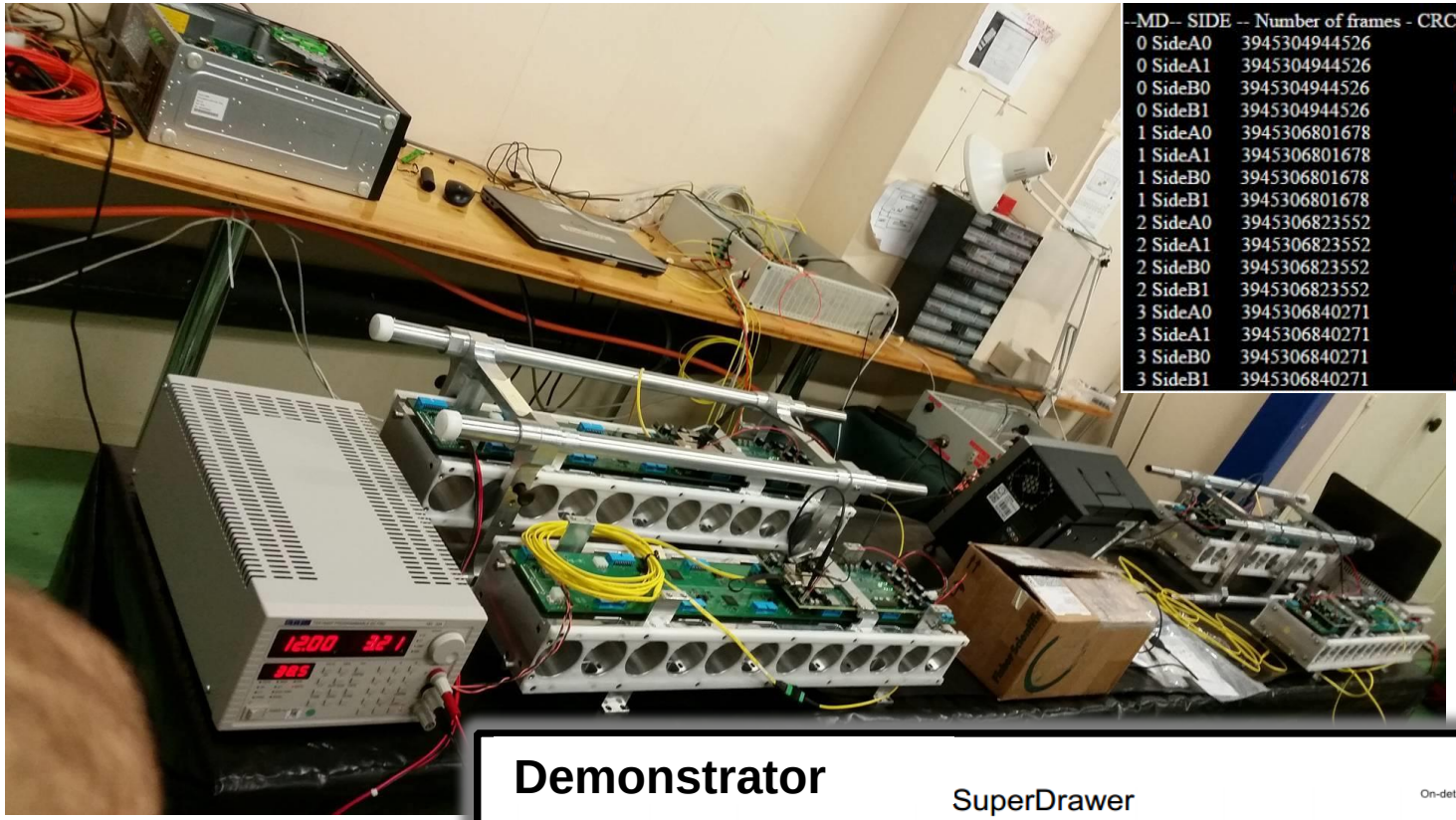
Xilinx Spartan 6
- Slow control
- Clock managment
- Read module status
- Read temp. sensors

Xilinx Virtex 7 FPGA
- XC7VX485T
- 48 GTX transceiver @ 10 Gbps

ADN2814
- Clock/data recovery from TTC

FPGA: Field Programmable Array.
TTC: Trigger Timing and Control
LX: Level X trigger
QSFP: Quad Small Form-factor Pluggable
SFP: Small Form-factor Pluggable
PMT: Photomultiplier Tube
FMC: FPGA Mezzanine Card.
GTX: Gb Transceivers

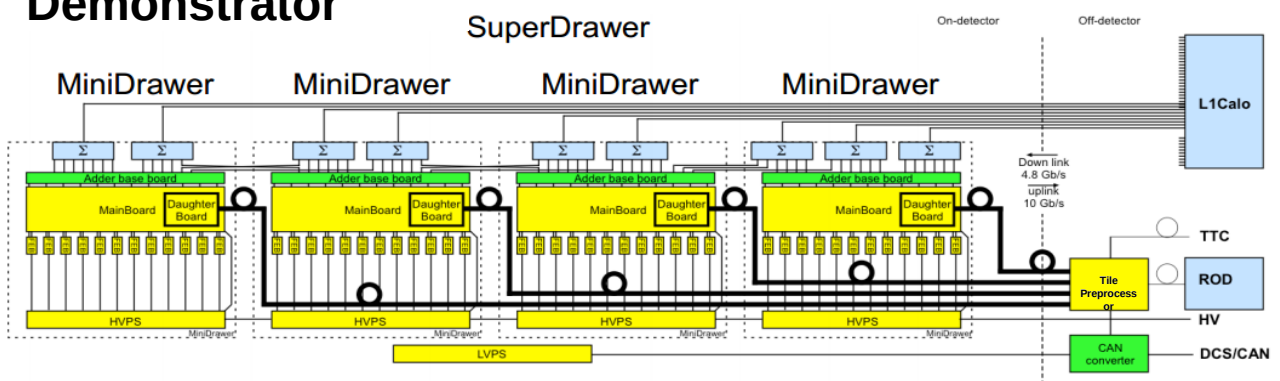
Latest configuration in action…Reliability…



--MD--	SIDE	-- Number of frames -	CRC Frame Errors -	Fraction per million -	Bit Error Rate -	Effective Errors
0	SideA0	3945304944526	0	0	0.000000e+00	0
0	SideA1	3945304944526	0	0	0.000000e+00	0
0	SideB0	3945304944526	0	0	0.000000e+00	0
0	SideB1	3945304944526	0	0	0.000000e+00	0
1	SideA0	3945306801678	0	0	0.000000e+00	0
1	SideA1	3945306801678	0	0	0.000000e+00	0
1	SideB0	3945306801678	0	0	0.000000e+00	0
1	SideB1	3945306801678	0	0	0.000000e+00	0
2	SideA0	3945306823552	0	0	0.000000e+00	0
2	SideA1	3945306823552	0	0	0.000000e+00	0
2	SideB0	3945306823552	0	0	0.000000e+00	0
2	SideB1	3945306823552	0	0	0.000000e+00	0
3	SideA0	3945306840271	0	0	0.000000e+00	0
3	SideA1	3945306840271	0	0	0.000000e+00	0
3	SideB0	3945306840271	2	0	4.224429e-15	0
3	SideB1	3945306840271	0	0	0.000000e+00	0

- 48 Hours continuous test including CRC checking and communication stability with no effective errors.

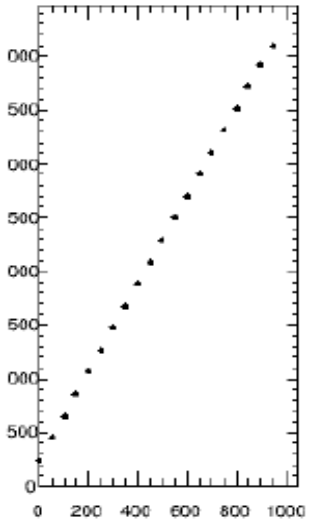
Demonstrator



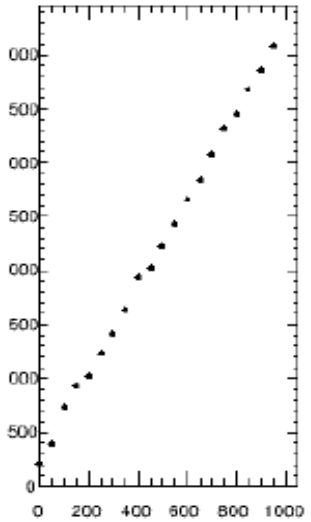
Total data rate	**~80 Tb/s**
Number of links	4096
Data rate per link	10 Gb/s
Links per super-drawer	4x4 (+4x4)
Data rate per super-drawer	160 Gb/s

Linearity tests…

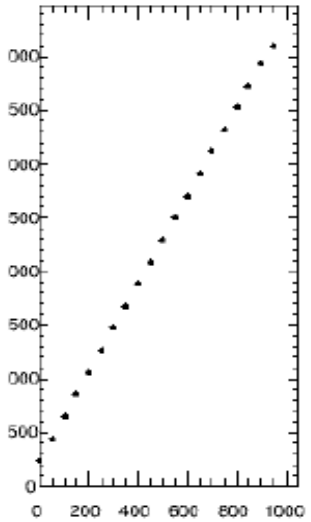
Channel 0



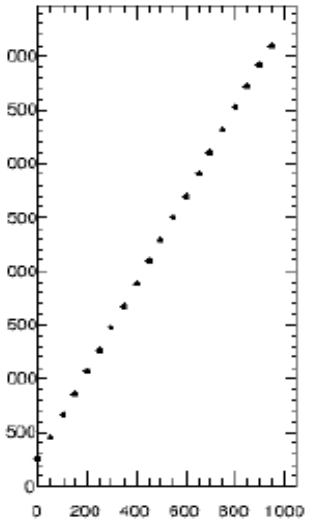
Channel 1



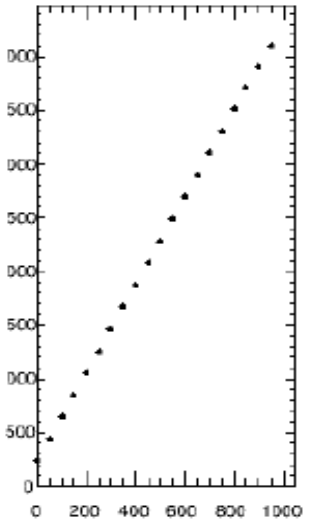
Channel 2



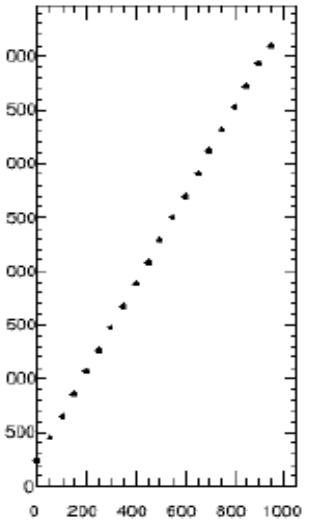
Channel 3



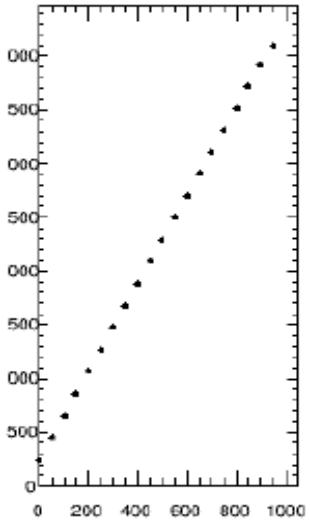
Channel 4



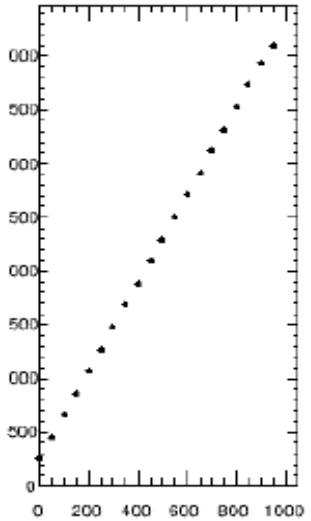
Channel 5



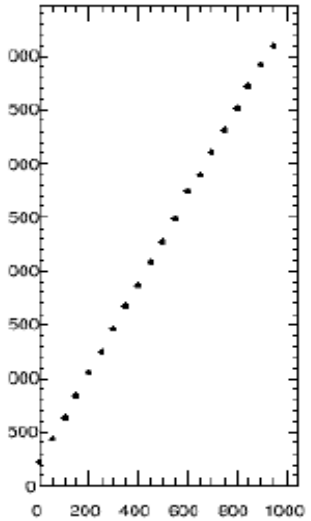
Channel 7



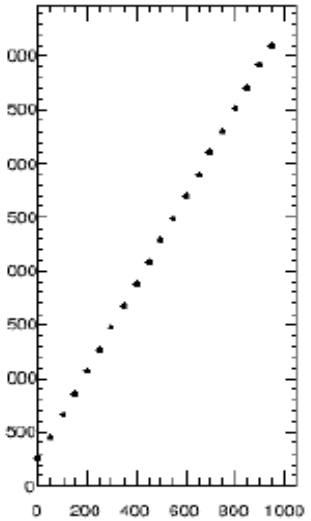
Channel 8



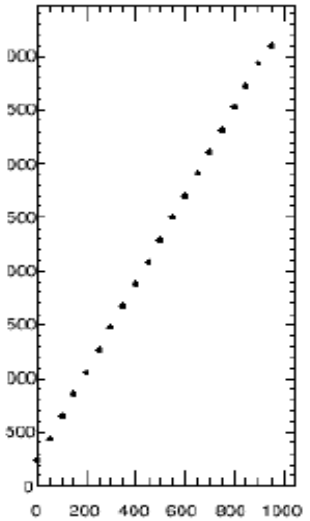
Channel 9



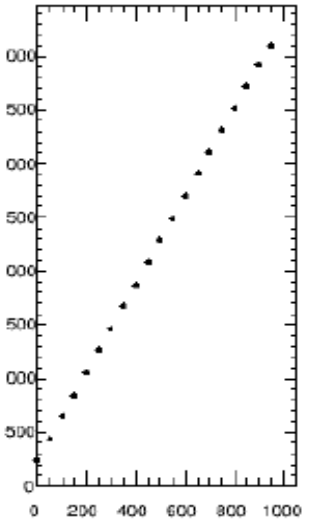
Channel 10



Channel 11



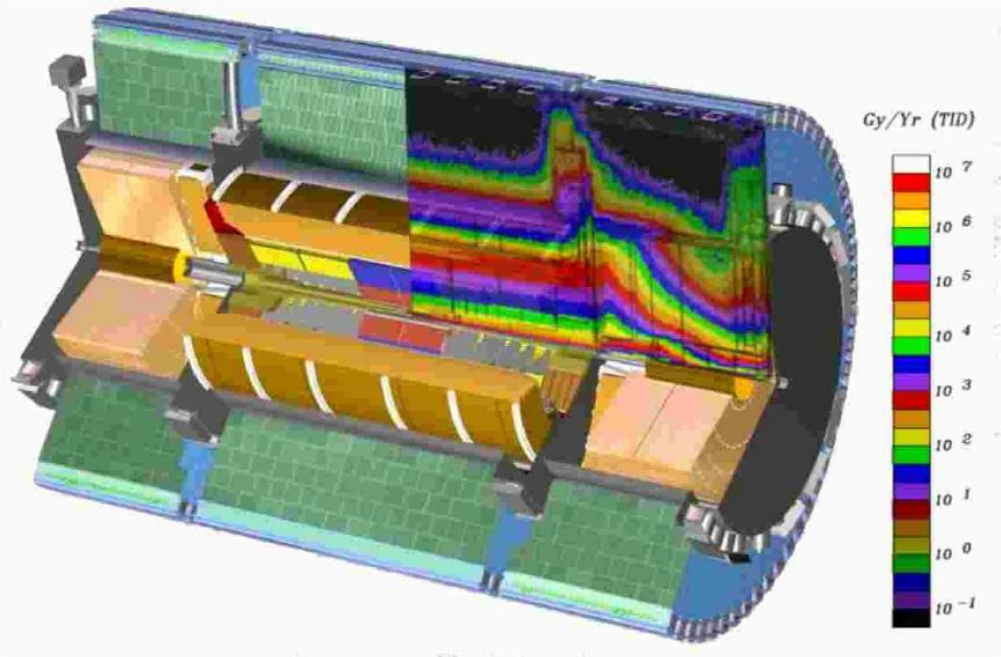
Channel 12



Timeline ($^{19}/_{21}$)

- Introduction…
- Upgrade…
- LVPS + HV OPTO...
- [1]3 in 1 + MB…
- [2]FATALIC…
- [3]QIE…
- Daughterboard…
- Tile Preprocessor…
- Radiation Tolerance...
- Conclusions…

Some words about Radiation Tolerance…



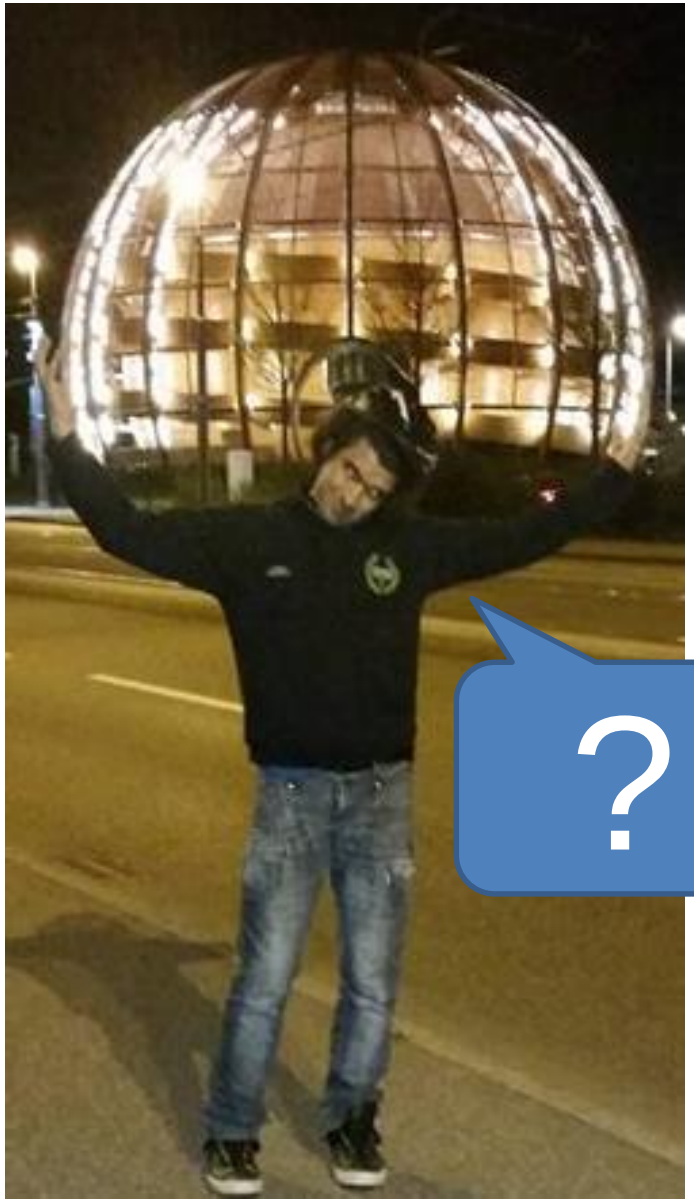
	TID	NIEL	SEE	
COTS regulators	Done - OK	Not done	Not done	Need different -5V
3-in-1	Preliminary	Pending	Preliminary	More testing needed
Main board	Not done	Pending	Not Done	Size limitations
Daughter board	Not done	Pending	Done – OK	More testing needed
Modulator	Done – OK	Pending	Done – OK	Good to go
HV_Opto	Done – OK	Done – OK	Done – OK	Good to go
LVPS	Done (v7.5)	Done (v7.5)	Done (v7.5)	Needs full testing
Adders	Not needed	Not needed	Not needed	Testing not needed
Active bases	Done	Done	Not needed	Good to go
FATALIC	Not done	Not done	Not done	Not started
QIE	Not done	Not done	Not done	Not started
Scintillators	Preliminary			More tests needed

- Perform radiation tests to the system parts.
- Double Redundancy in the electronic design.
- Use of Radiation Tolerant components.
- Use of triple redundancy mode (TMR) in the FPGAs.
- Link Redundancy.
- Upstream Data Protection: CRC.
- Downstream Data Protection: GBT with FEC.

Timeline ($^{20}/_{21}$)

TID: Total Ionizing Dose
SEE: Single Event Effects
NIEL: Non ionizing energy loss.
TMR: Triple Mode redundancy
CRC: Cyclic Redundancy Check
GBT: GigaBit Transceiver data transmission protocol.
FEC: Forward Error Correction.
LVPS: Low Voltage Power Supply.

Conclusions and Questions…



–Better reliability have been achieved with the current version of the demonstrator comparing it to the previous prototypes.

– Validation of front ends alternatives will take place soon in the coming test beams.

– Radiation tests are needed to validate the radiation tolerance of the different parts of the Demonstrator

– A hybrid demonstrator drawer will be ready soon!