ALICE INDIA Collaboration Meeting
6th February 2016

Common Readout Unit (CRU)

Design And Integration

BY

JUBIN MITRA

Outlook

Motivation of CRU Design

CRU connectivity and Location

Interface Links - Reason of Choice

CRU Application in ALICE Electronics

CRU Functionality

CRU as Trigger Distribution Unit

CRU Requirements

PCIe40 – A candidate board for CRU firmware

Snapshots of Test setups

Motivation Of CRU Design

New Inner Tracking System (ITS)
- Improved pointing precision
- Less material -> thinnest tracker at the LHC
- **25x10^9 channels**

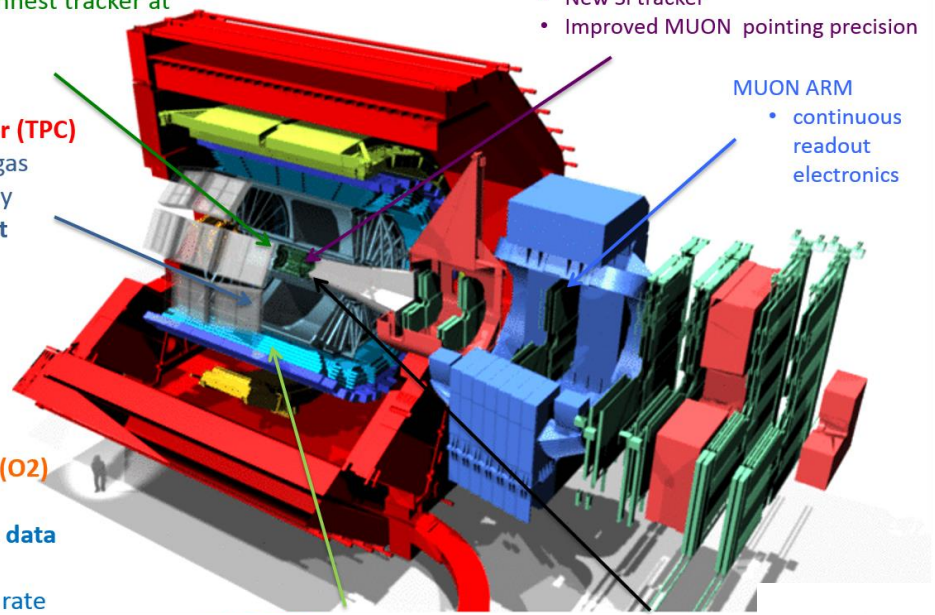
Time Projection Chamber (TPC)
- New Micropattern gas detector technology
- **Continuous readout**

New Central Trigger Processor (CTP)

Online Offline Systems (O2)
- New architecture
- **On line tracking & data compression**
- 50kHz PbPb event rate

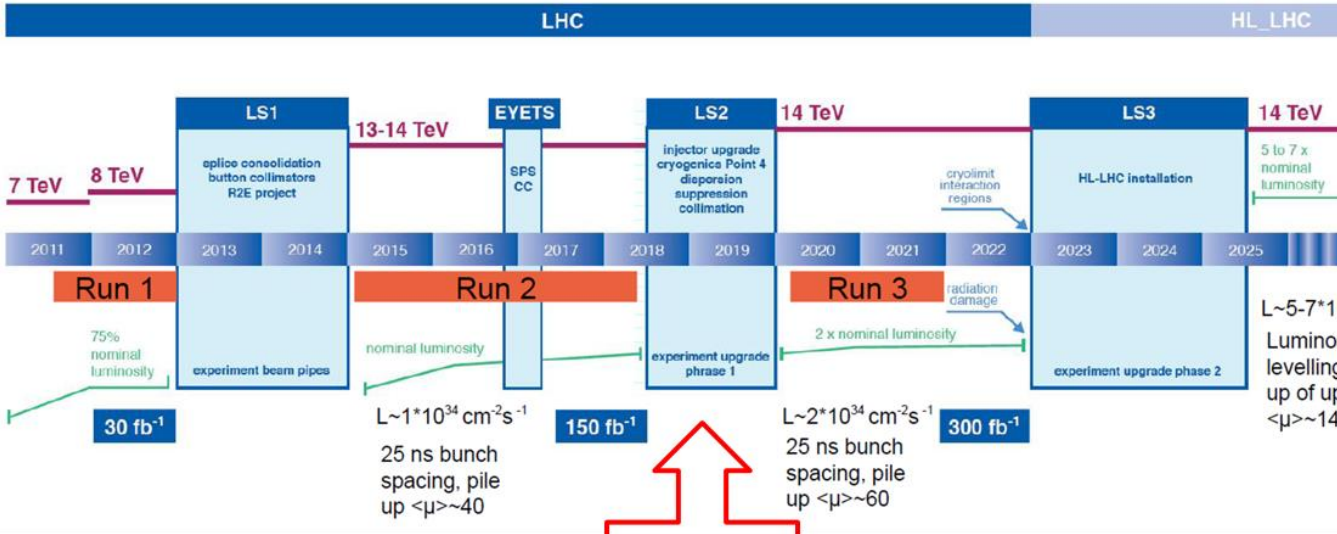
Muon Forward Tracker (MFT)
- New Si tracker
- Improved MUON pointing precision

MUON ARM
- continuous readout electronics

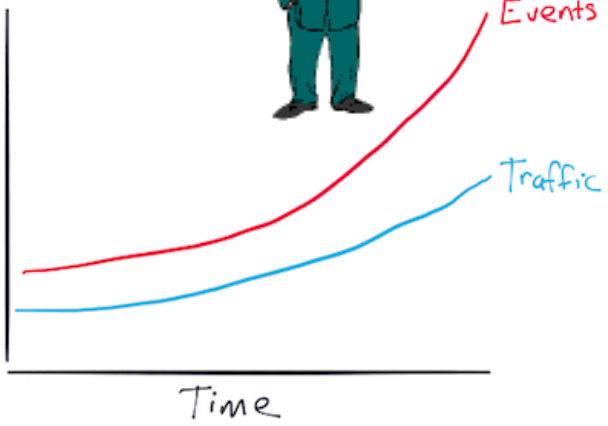


TOF, TRD
- **Faster readout**

New Trigger Detectors (FIT)



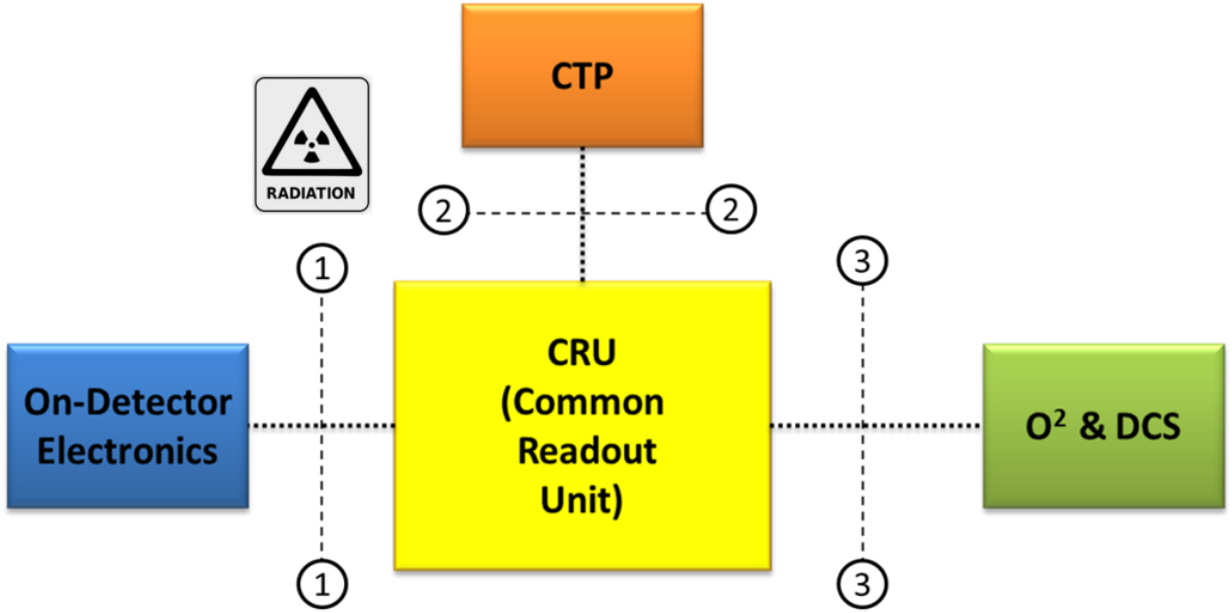
Major Upgrade in ALICE



$$N_{event} = L_{int} \times \sigma_p$$

COMMON READOUT UNIT (CRU)

GENERAL CONNECTIVITY



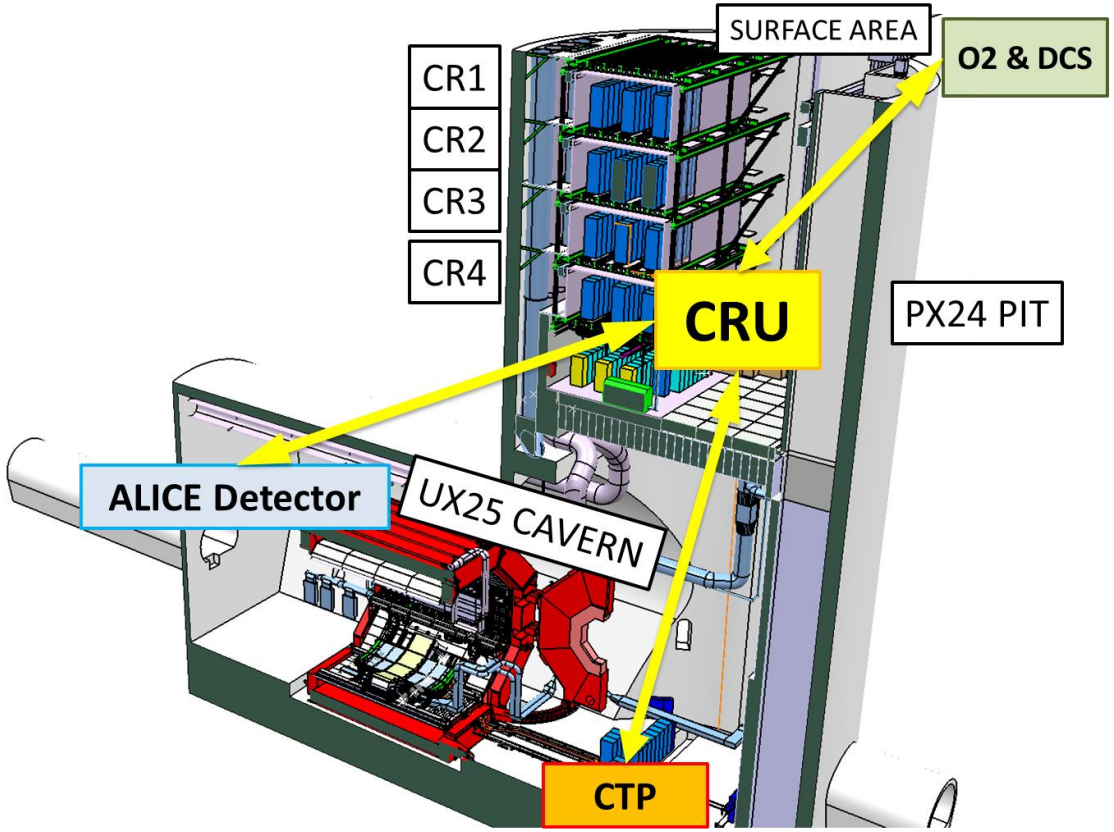
CRU has three interfaces:

1 – GBT Link (Radiation Tolerant High Speed Optical Link)

2 – TTC PON (2015 Standard)

3 – PCIe Gen 3 x16

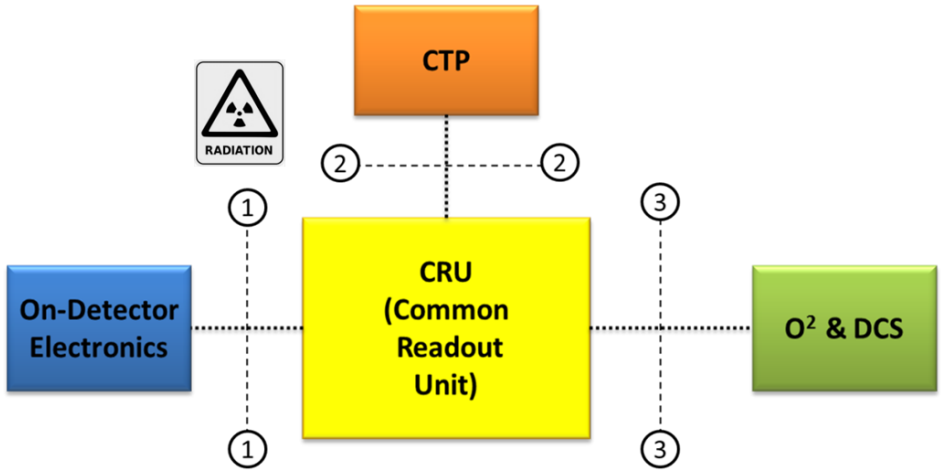
LOCATION



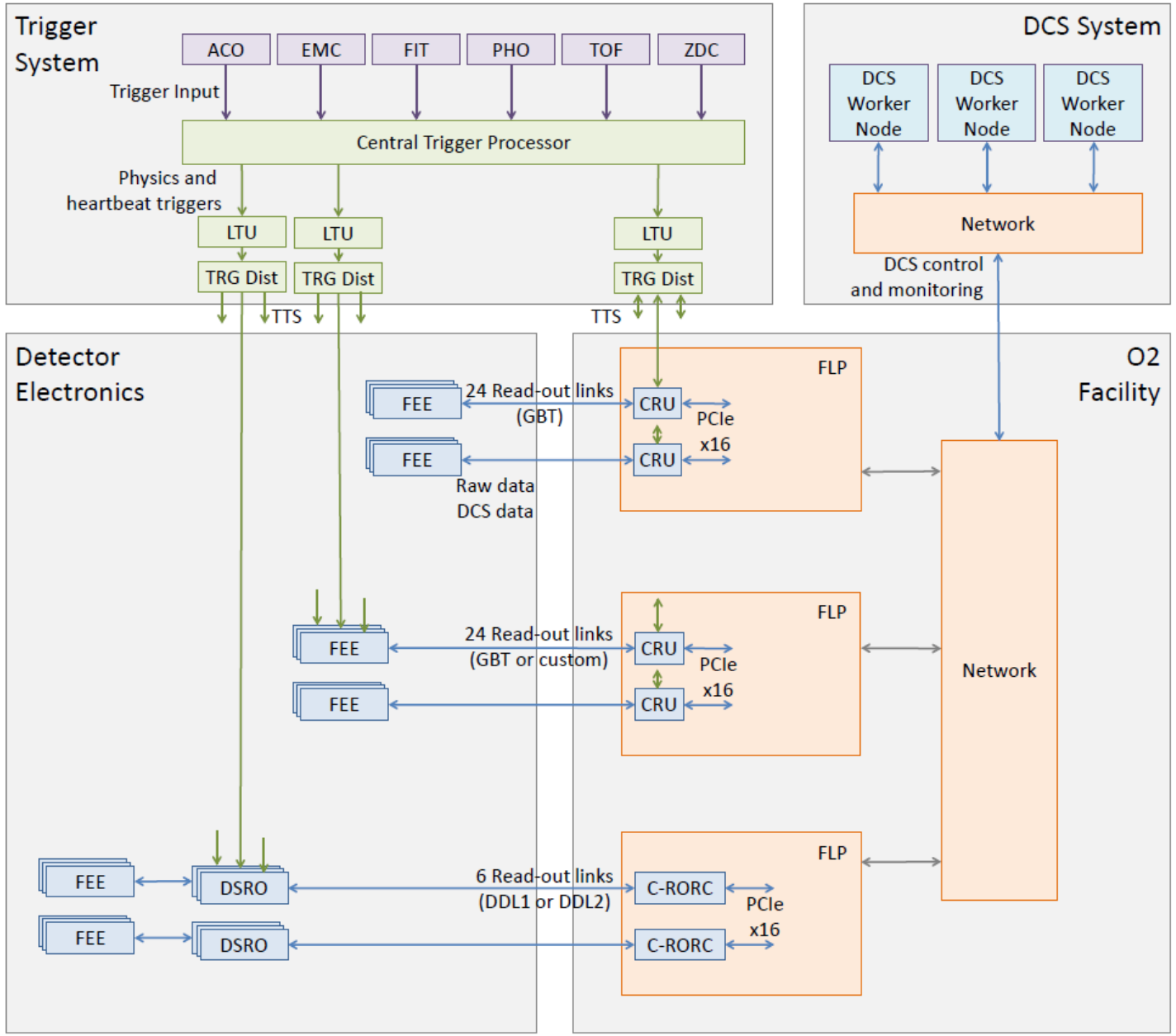
INTERFACE LINKS

Reason of Choice

	①	②	③
Parameters	**GBT**	**TTC-PON**	**PCIe® Gen3**
Technology Specification	Custom	XGPON1 with modifications	PCI Express® Base Specification Revision 3.1
Designer Group	CERN	ITU-T with CERN modifications	PCI-SIG
Line Rate	4.8 Gbps	Downstream: 9.6 Gbps Upstream: 2.4 Gbps	8 Gbps per lane
Payload Rate	3.2 Gbps	Downstream: ~7.68 Gbps Upstream: 640 Mbps	985 MB/s per lane
Payload Size	120 bits@40 MHz	Downstream: 192 bits@40 MHz Upstream: ~16 bits@40 MHz	256 bits@250 MHz for 8 lanes
Wavelength	850 nm (Multi-mode Tx) 1310 nm (Single-mode Tx)	Downstream: 1577 nm Upstream: 1270 nm	Not Applicable
Network Topology	Point-to-Point	Point-to-Multipoint	Point-to-Point
Encoding	RS Encoding with Block Interleaver	8b/10b	128b/130b
Synchronous Trigger Support	Yes	Yes	No
Trigger Latency	Optical loop-back Round-trip: 150 ns	Downstream: ~100 ns Upstream: 1.6 μs	Not Applicable
Commercially Available	No	No	Yes

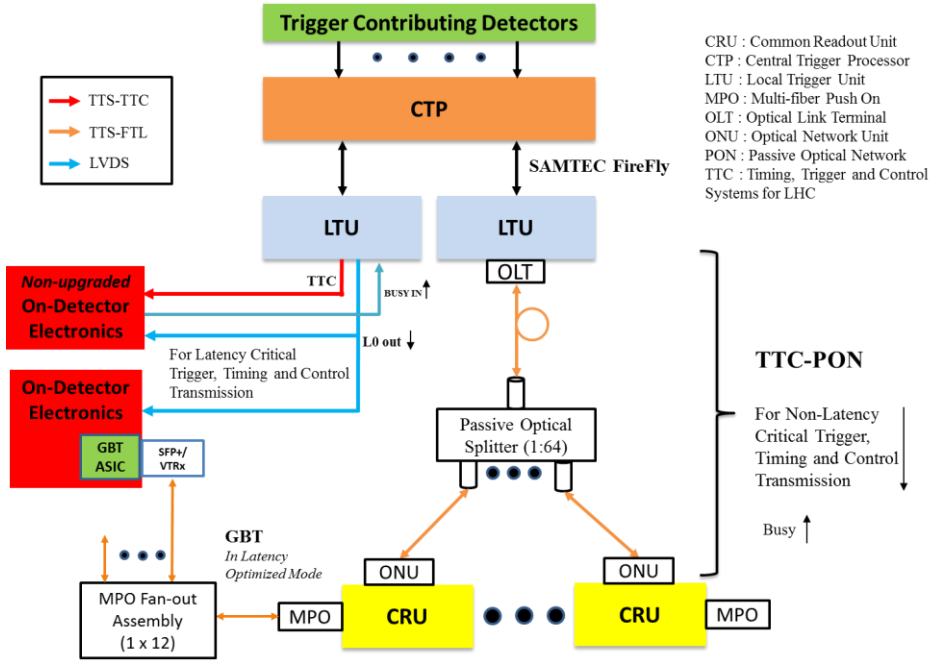


CRU Application in ALICE Electronic Architecture

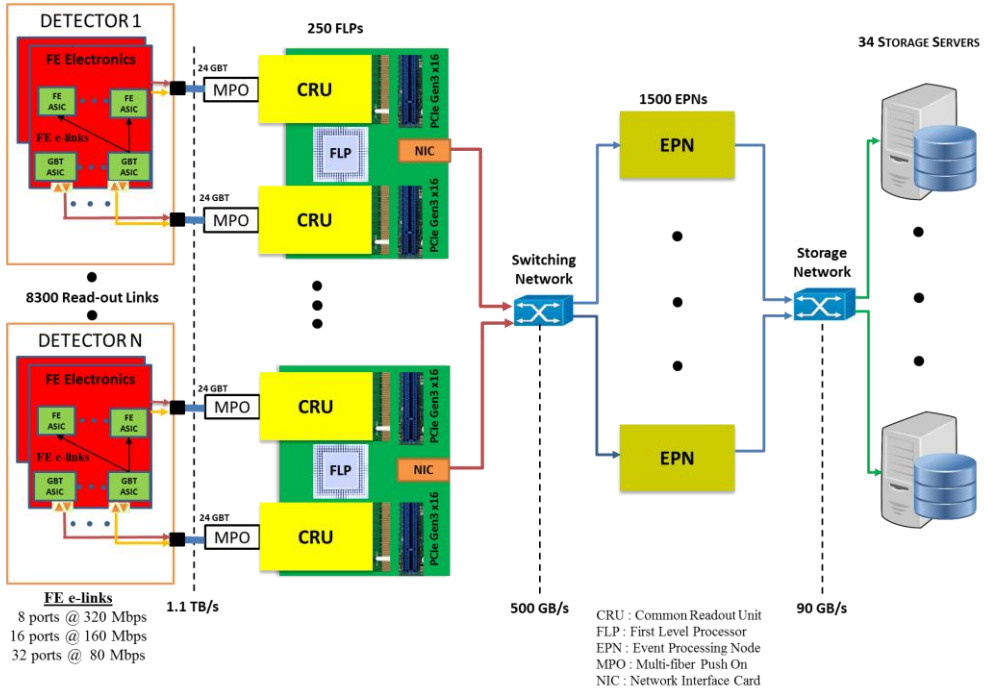


Taken from O2 TDR

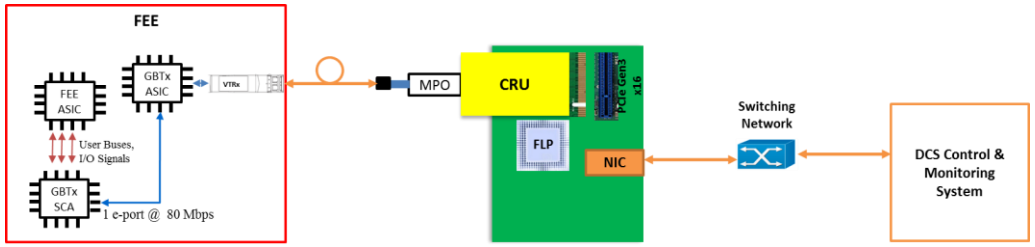
CRU FUNCTIONALITY



Trigger Distribution Unit

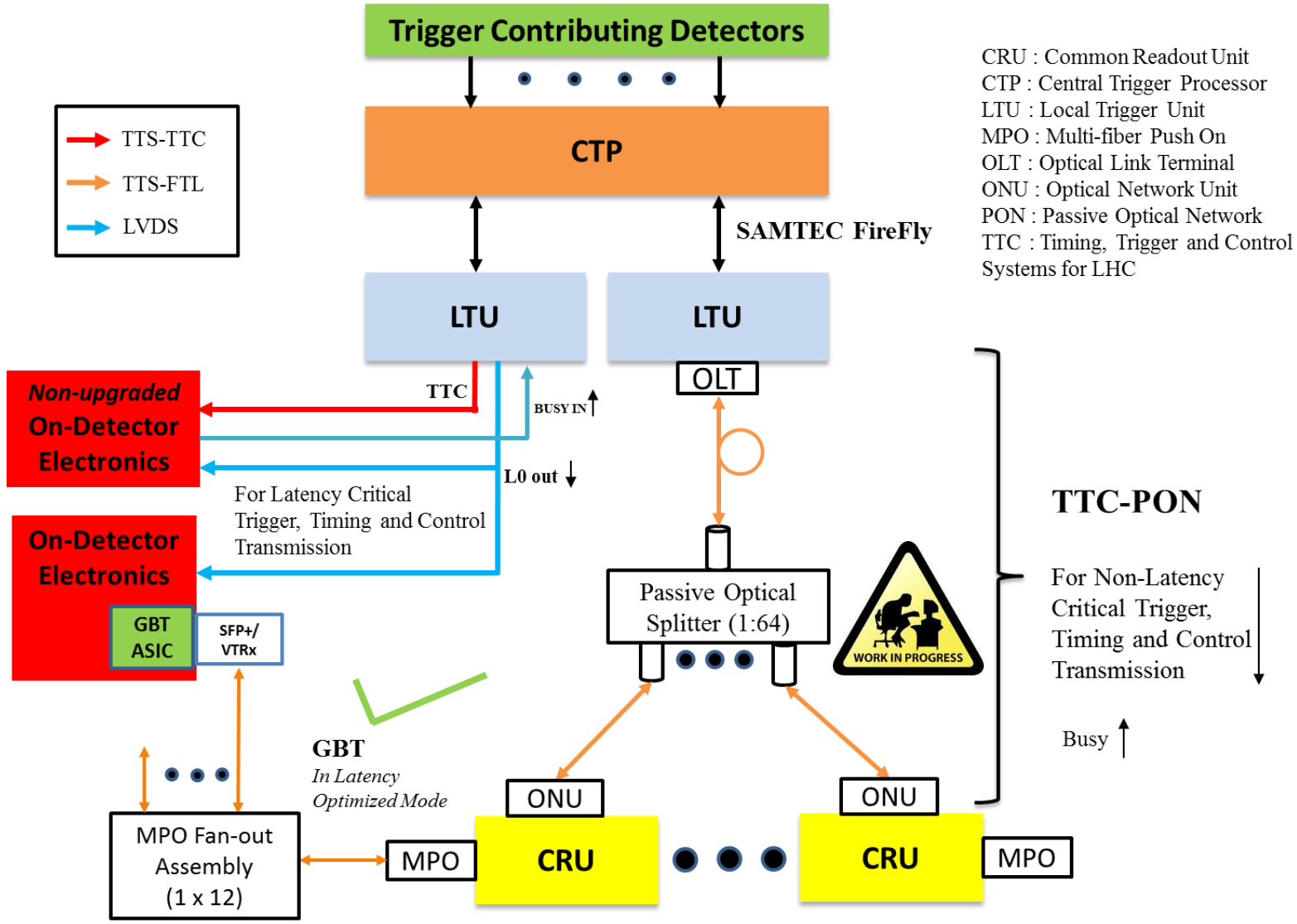


Data Aggregation Unit



Detector Control Moderation

CRU Trigger Distribution

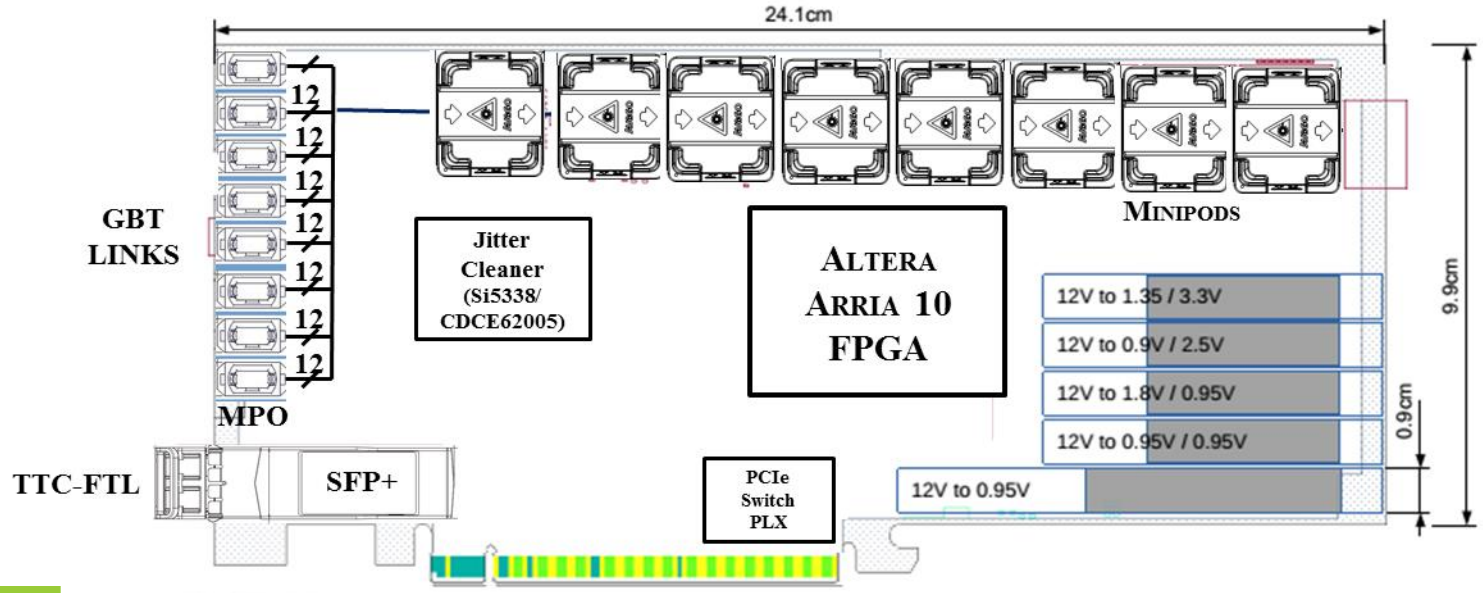


CRU Requirements

User Groups	FEE / Readout Boards	No. of Channels	Maximum Readout Rate (kHz)	Data Rate for Pb-Pb (GB/s)	Readout Mode	Link Type	No. of Links	No. of CRU boards
CTP (Central Trigger Processor)	FPGA (Kintex 7)	–	200	0.02	Triggered / Continuous	GBT & 10G PON	14	1
ITS (Inner Tracking System)	FPGA (Kintex 7)	25×10^9	100	40	Triggered	GBT	495	23
MCH (Muon Chamber)	ASIC (SAMPA)	10^6	100	2.2	Triggered / Continuous	GBT	550	25
MFT (Muon Forward Tracker)	FPGA (Kintex 7)	500×10^6	100	10	Triggered	GBT	304	14
MID (Muon Identifier)	FPGA (8x Max10, 2x Cyclone V)	21×10^3	100	0.3	Triggered	GBT	32	2
TOF (Time Of Flight)	FPGA (IGLOO2)	1.6×10^5	100	2.5	Triggered	GBT	72	3
TPC (Time Projection Chamber)	ASIC (SAMPA)	5×10^5	50	1012	Triggered / Continuous	GBT	5832	324
TRD (Transition Radiation Detector)	FPGA	1.2×10^6	200	20	Triggered	Custom	1044	54
ZDC (Zero Degree Calorimeter)	FPGA (Vertex 5,6)	22	100	0.06	Triggered	GBT	1	1
Total				1087			8344	447

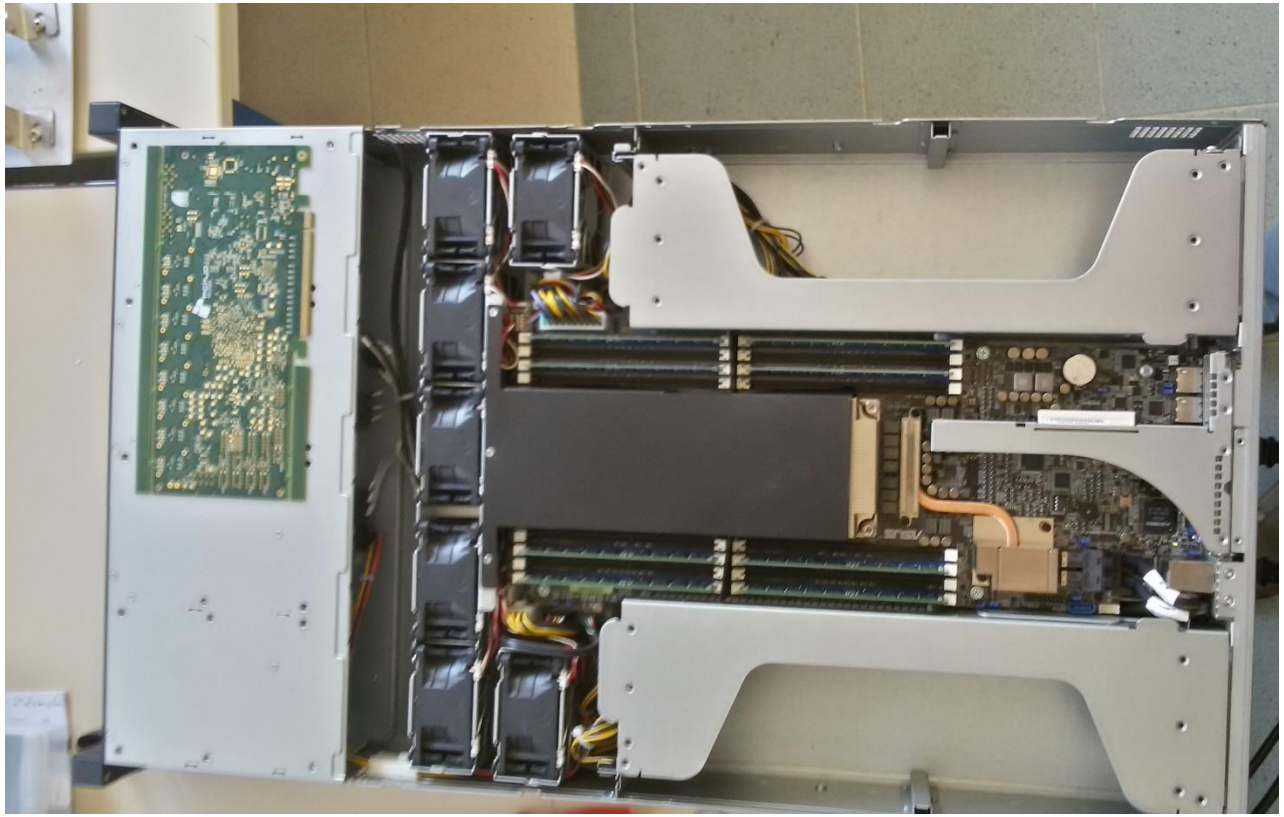
Largest User Group →

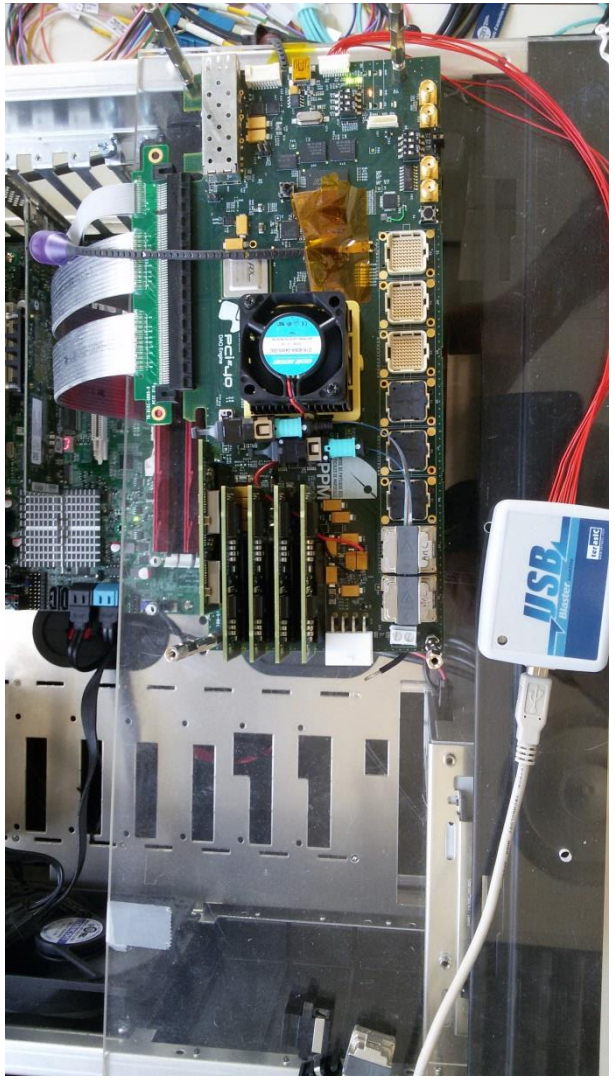
WHICH FPGA BOARD CRU FIRMWARE WILL USE?



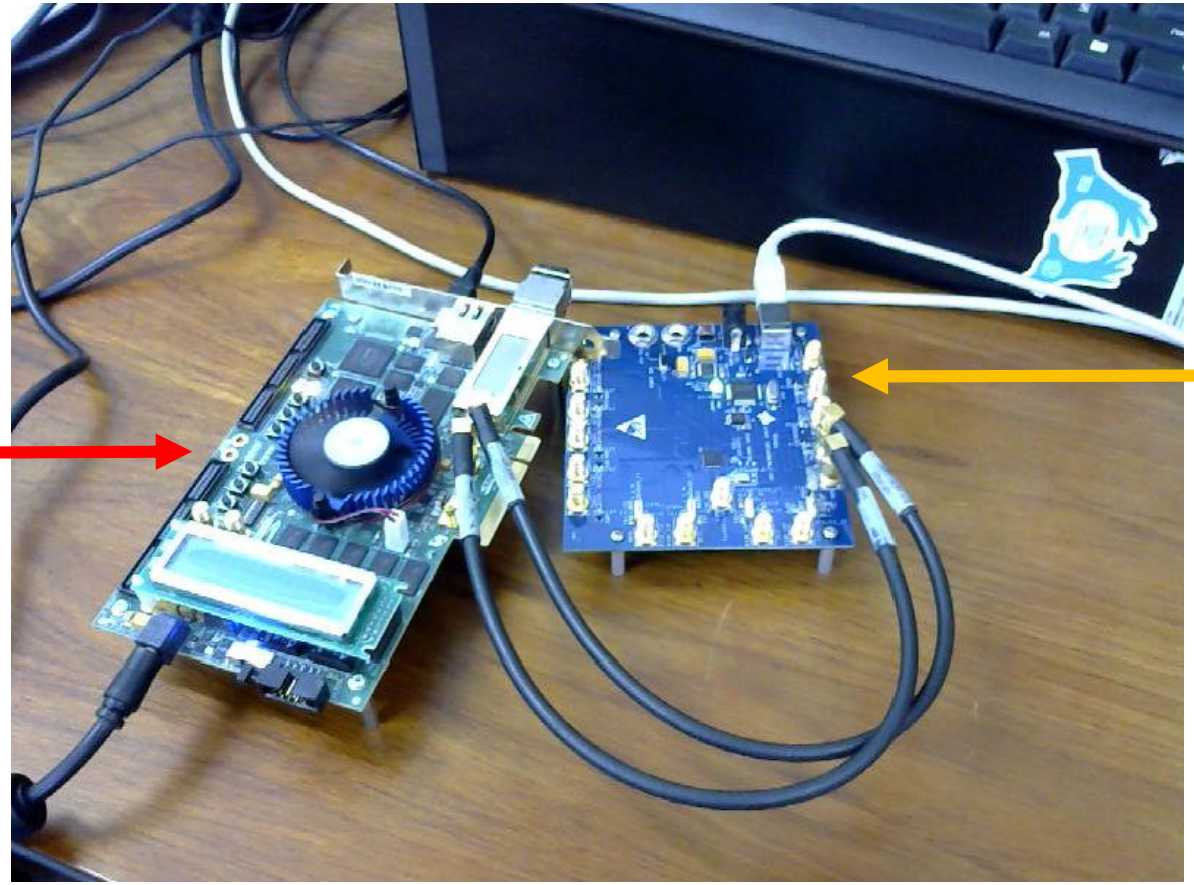
Developed By:
CPPM Marseille

WHERE CRU WILL BE FITTED ?

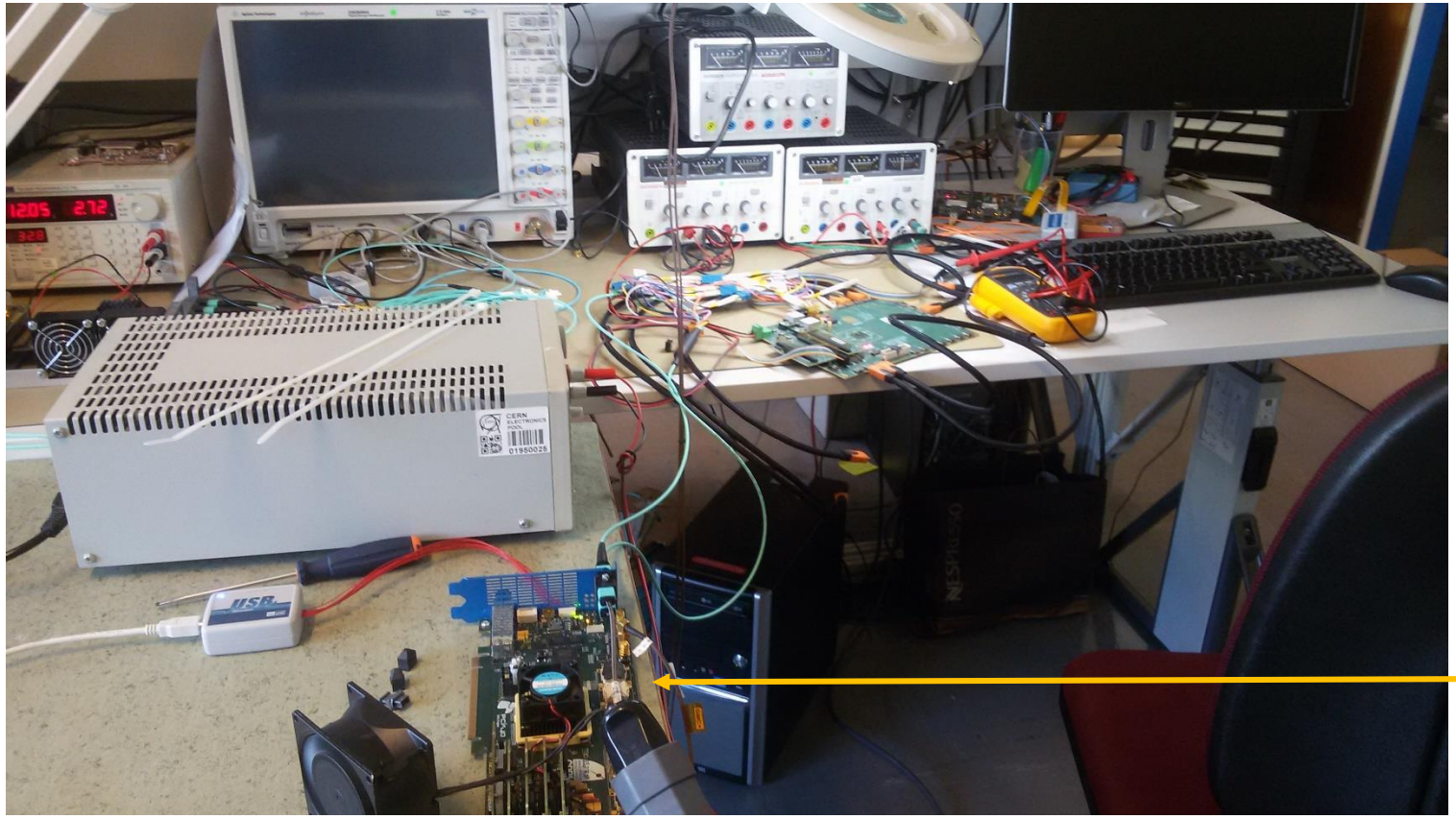




A Glimpse Of GBT Test Setup At VECC On Stratix V FPGA Board



PCIe40 Under Test During GBT Protocol Evaluation at CERN




Thank You!

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BACKUP SLIDES

Periphery Logic resource usage estimation for TPC requirement

TABLE V: Aggregated Links without inter-connect glue logic for TPC sub-detector resource estimation (40 GBT link in combination 2 + x16 PCIe Gen 3 + 1 Transceiver Toolkit design (Apprx. 10G PON))

Resource Type	**Total Available**	**Resource Usage**	
Logic utilization (in ALMs)	427,200	87,664	(20.52 %)
Total registers	1,708,800	139,613	(8.17 %)
Total block memory bits	55,562,240	1,530,852	(2.75 %)
Total RAM Blocks (M20K)	2,713	292	(10.76 %)
Total DSP Blocks	1,518	0	(0.00 %)
IOPLL	16	8	(50.00 %)
FPLL	32	2	(6.25 %)
HSSI ATX PLL	32	10	(31.25 %)
Total HSSI RX channels	72	57	(79.17 %)
Total HSSI TX channels	72	57	(79.17 %)
PCIe Hard IPs	4	2	(50.00 %)

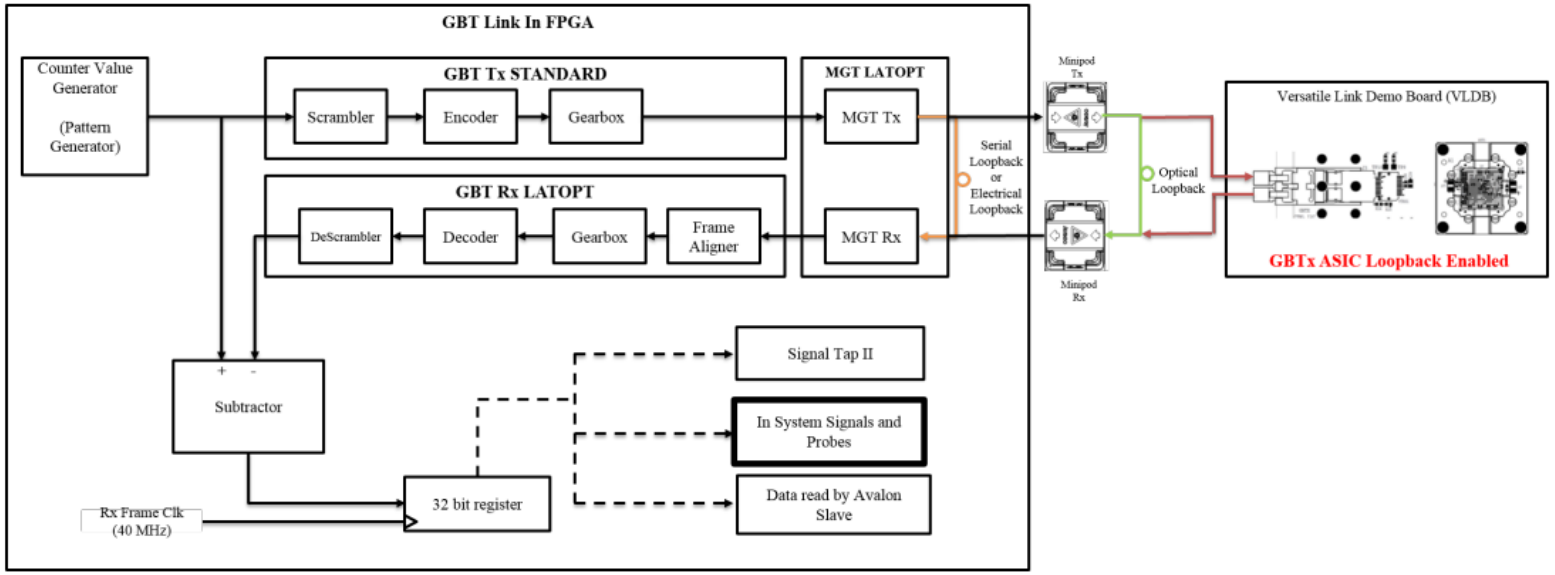

Figure 21: Test Setup for 3 types of round trip measurement, each loopback arrangement are marked by different colours

Table 19: Round Trip delay measurement for multi-level loopback of GBT firmware

GBT Protocol		**ROUND TRIP DELAY** (In terms of LHC bunch crossing Rate= 25ns)		
Transmission Side	**Receiver Side**	**Serial or Electrical Loopback**	**Optical Loopback**	**GBT ASIC Loopback**
Latency Optimized	*Latency Optimized*	6	7	11
Latency Optimized	*Standard*	13	14	18
Standard	*Latency Optimized*	8	9	13
Standard	*Standard*	18	18	22