COMMON READOUT UNIT (CRU)

Present Status

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VECC

ALICE INDIA Collaboration Meeting
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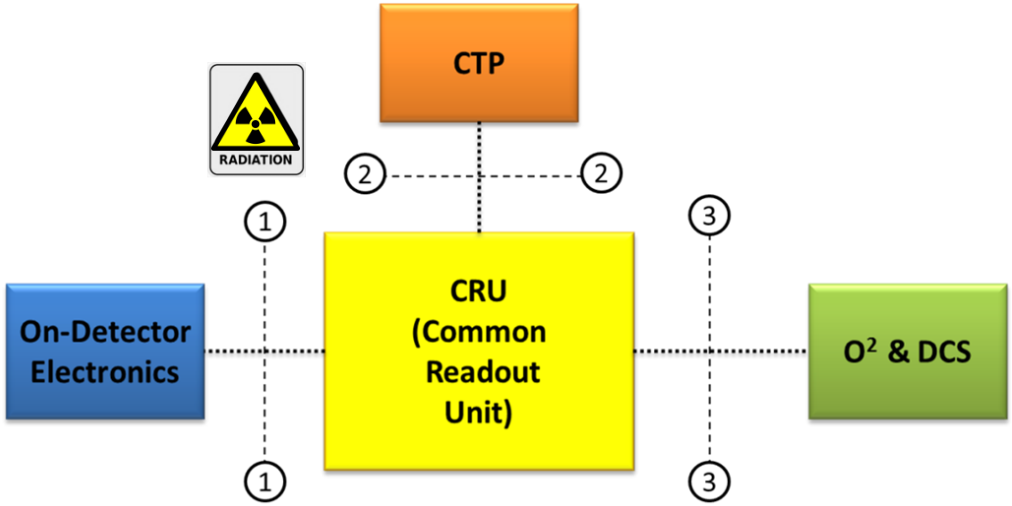


1. GBT Link Interface
2. PON (Passive Optical Networks) for Trigger Interface
3. PCIe Interface
4. Cluster Finding
5. DCS Development
6. Development of CRU Hardware

Cluster Finder

•Previously in Run-1, 1 data stream link was operated at 133 MHz and in Run-2 it was operated at 320 MHz. In Run-3, GBT have roughly the same data throughput of DDL2 link used in Run-2.

• Here instead of 1 link, N number of links (approximately N=40) will be used. It is impossible to handle N times increased data speed in FPGA platform. It may be proposed that M number of Cluster Fragments (CFs) can handle data from N number of links where one CF can process data from more than one GBT link using internal round robin distribution.

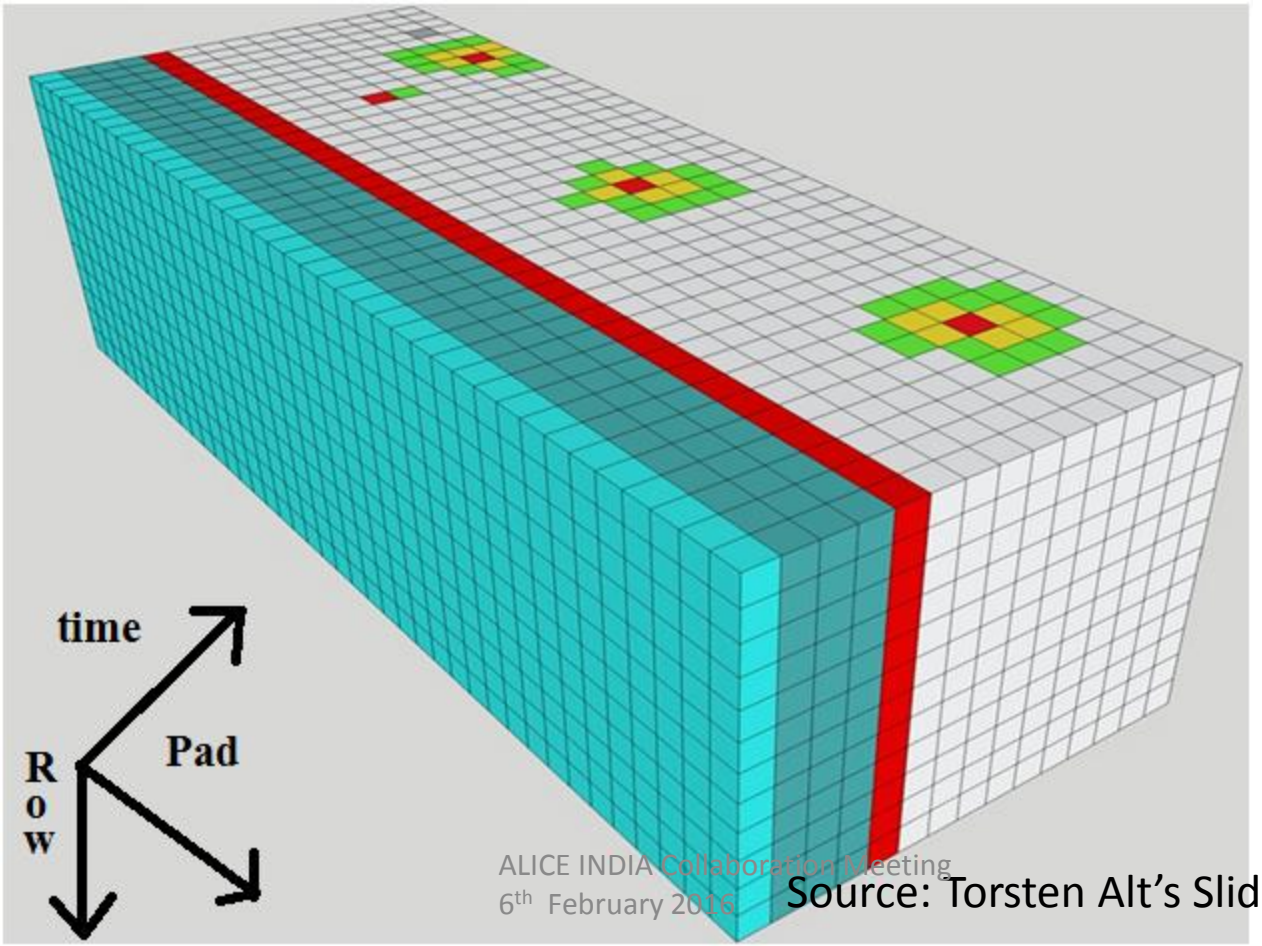
•For Run 2 Cluster Algorithm in one time instant one charge value comes from one pad, where as for Run 3, 2D cluster will accept charge values from all pads mounted in a row.

• The hardware architectures of Charge Peak Finding unit, Merging process, Time comparator unit etc of Cluster algorithm core required to be changed.

• Presently 2 things will be tried

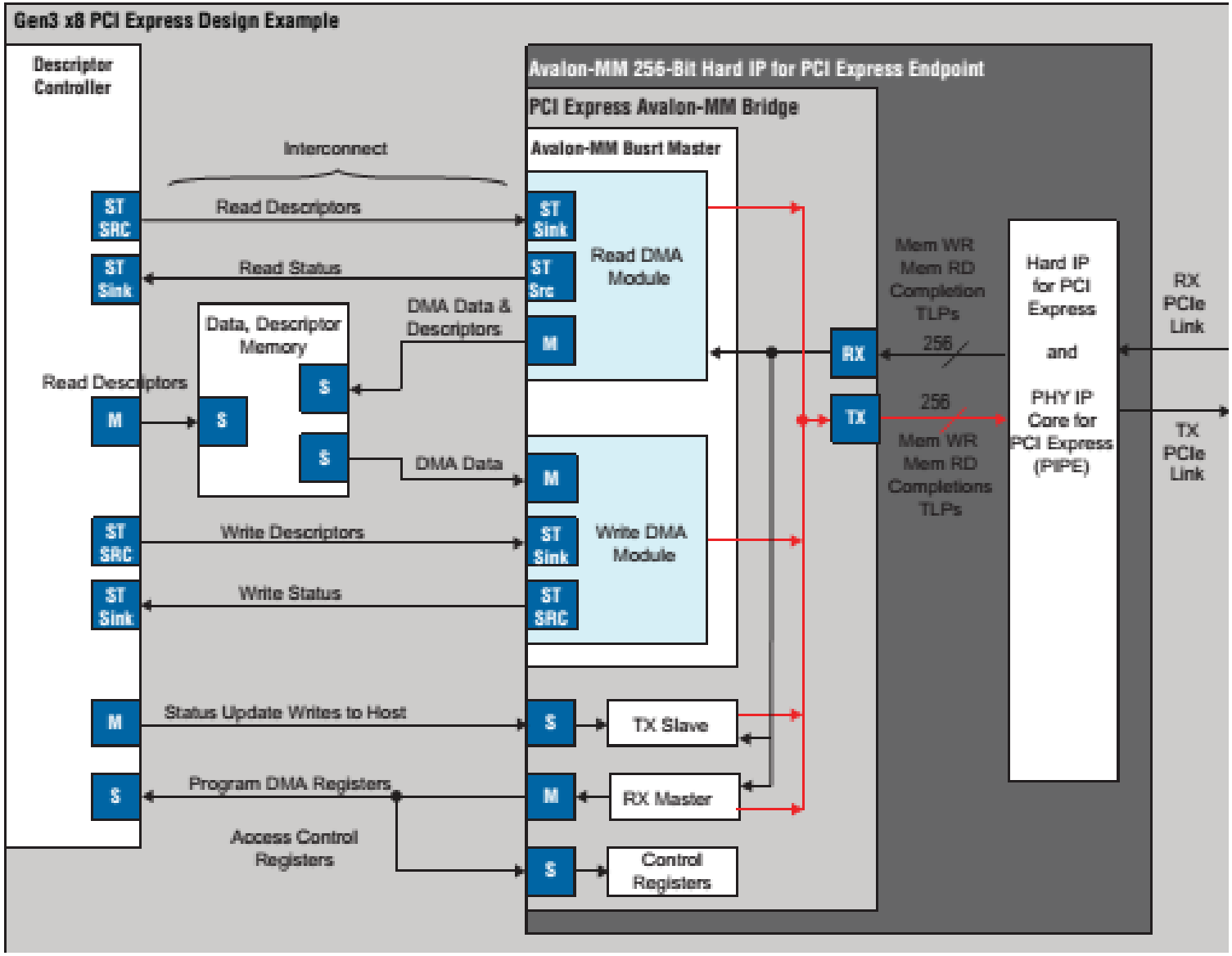
- •Shifting whole Cluster Core from Virtex 4 to Aria 10 FPGA .
- •Exploring for the suitable architectures of Peak Finding, Merging process , Time comparator unit etc

•Sort the incoming data from the GBTs into a Pad-Row Matrix (light green, first stage of the CUBE)
•Perform Common-Mode correction based on N pads (>100) (dark green, second stage of the CUBE)
•(Optional) Buffer the data in small memories (ALTERA, MLAB - 32x20bit) (bright red, third stage of the CUBE)
•Perform 2D ClusterFinding in one Row (grey, third stage of the CUBE)

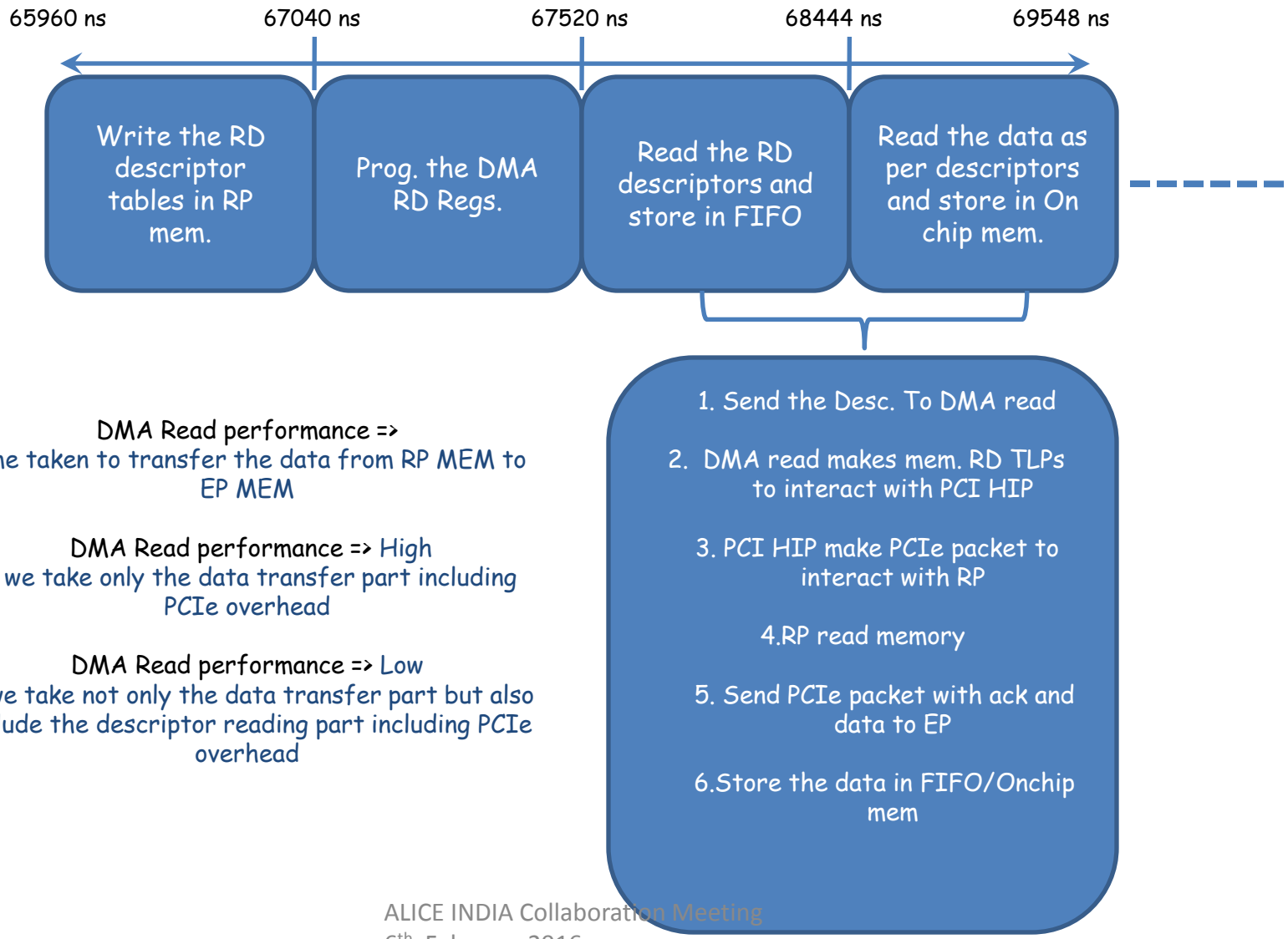


Source: Torsten Alt's Slide

PCIe Design Under Test



DMA Read Stages(RP MEM->EP MEM)

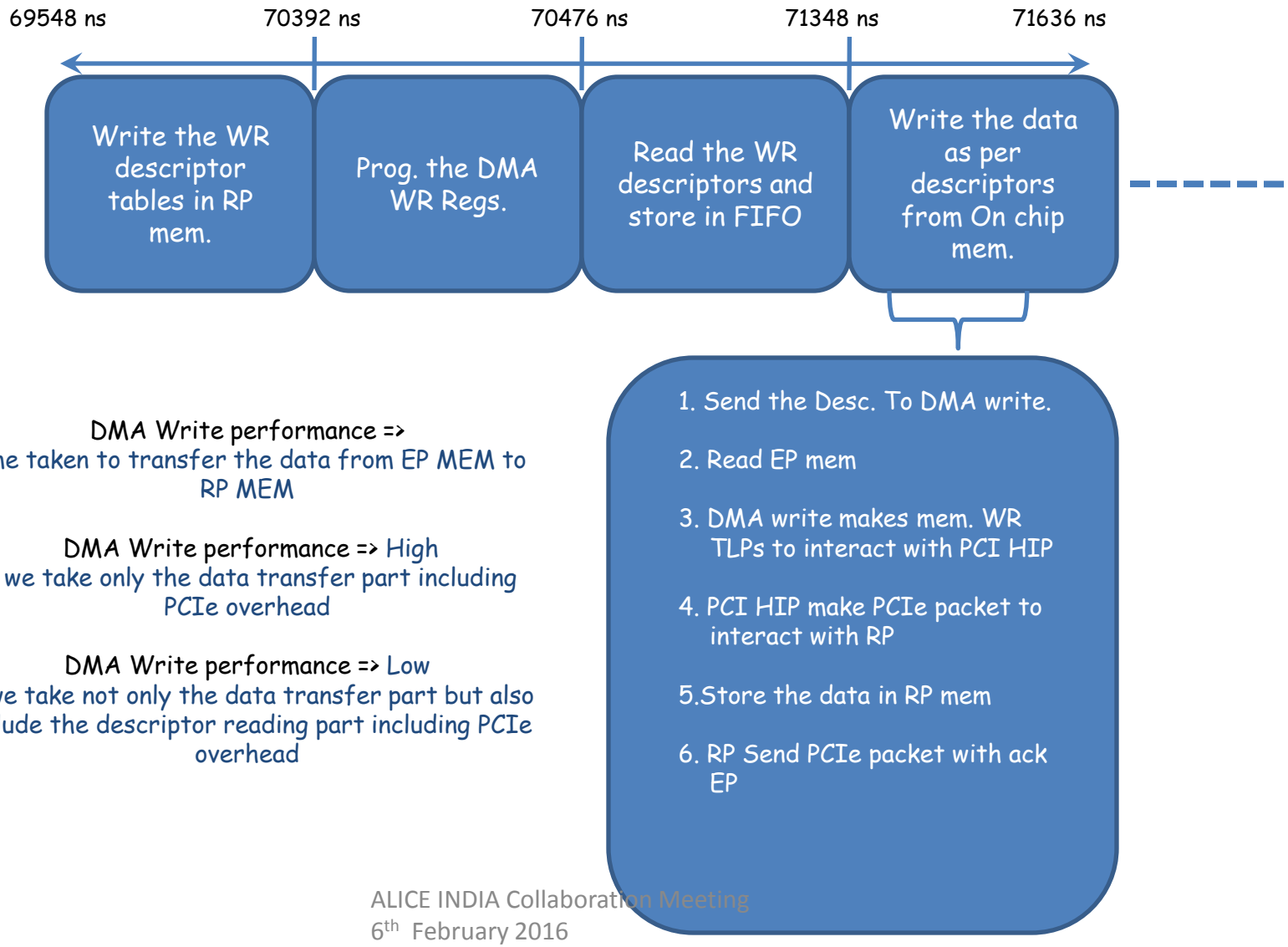


DMA Read performance =>
time taken to transfer the data from RP MEM to EP MEM

DMA Read performance => High
if we take only the data transfer part including PCIe overhead

DMA Read performance => Low
if we take not only the data transfer part but also include the descriptor reading part including PCIe overhead

DMA Write Stages (EP MEM->RP MEM)



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CRU PCIe DMA

Hardware result of PCIe DMA

1. Prog. DMA Read/Write regs. in real time

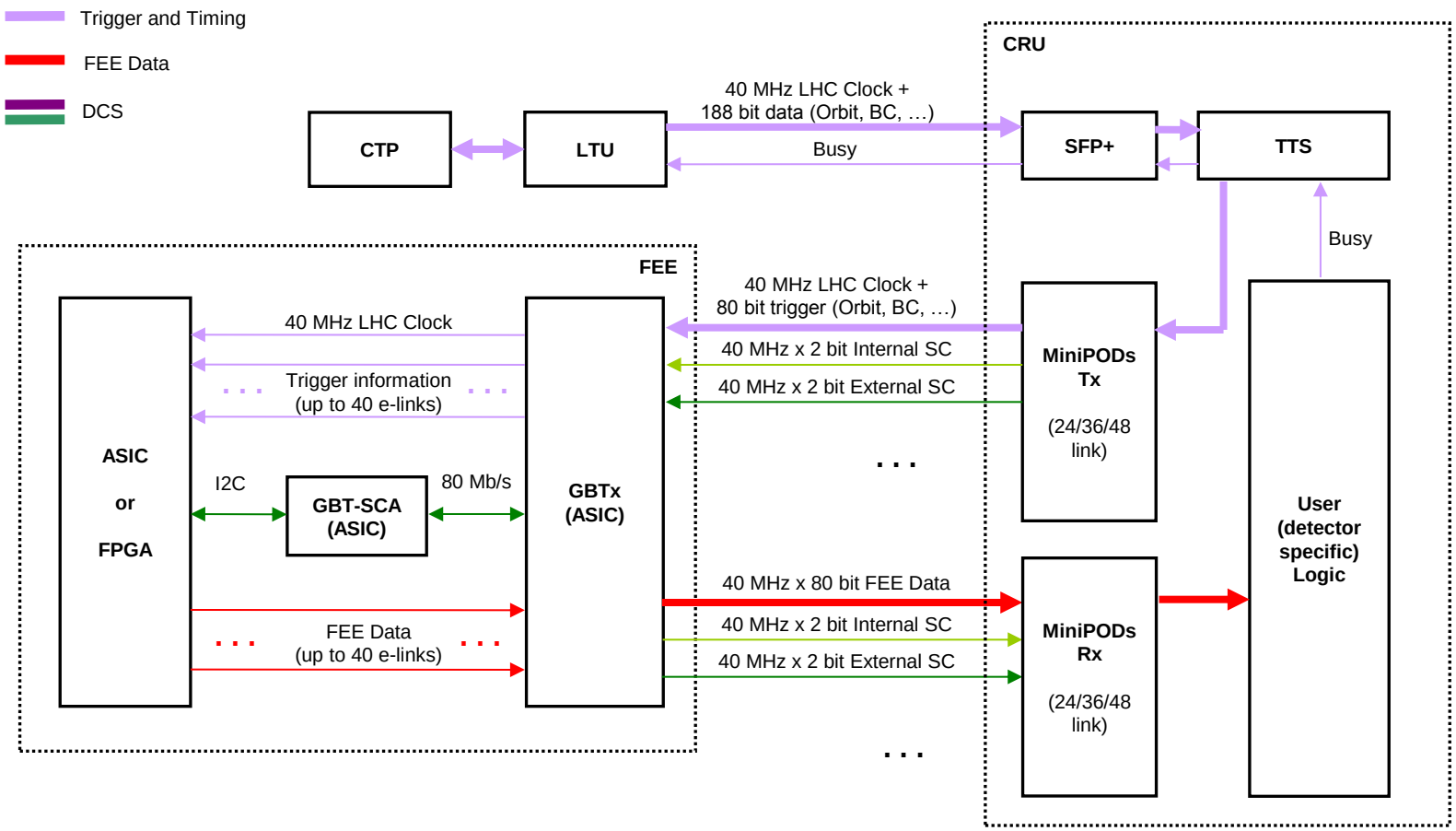
2. Measured DMA performance in real time: 73% of PCIe G3 X1 lane BW

3. Difference in performance may be due to less amount of descriptors

DMA performance may improve if we push multiple address with high DMA length in pipelined manner.

Tested the Arria 10 PCIe HIP with Altera Arria 10 ES2 board available at CERN. It is programmed in G3 mode but

DCS Interface



- Development of CRU Hardware
- First Arria10 Commercial Development Board at VECC Around March end