CLICpix2 and C3PD Bump Pads

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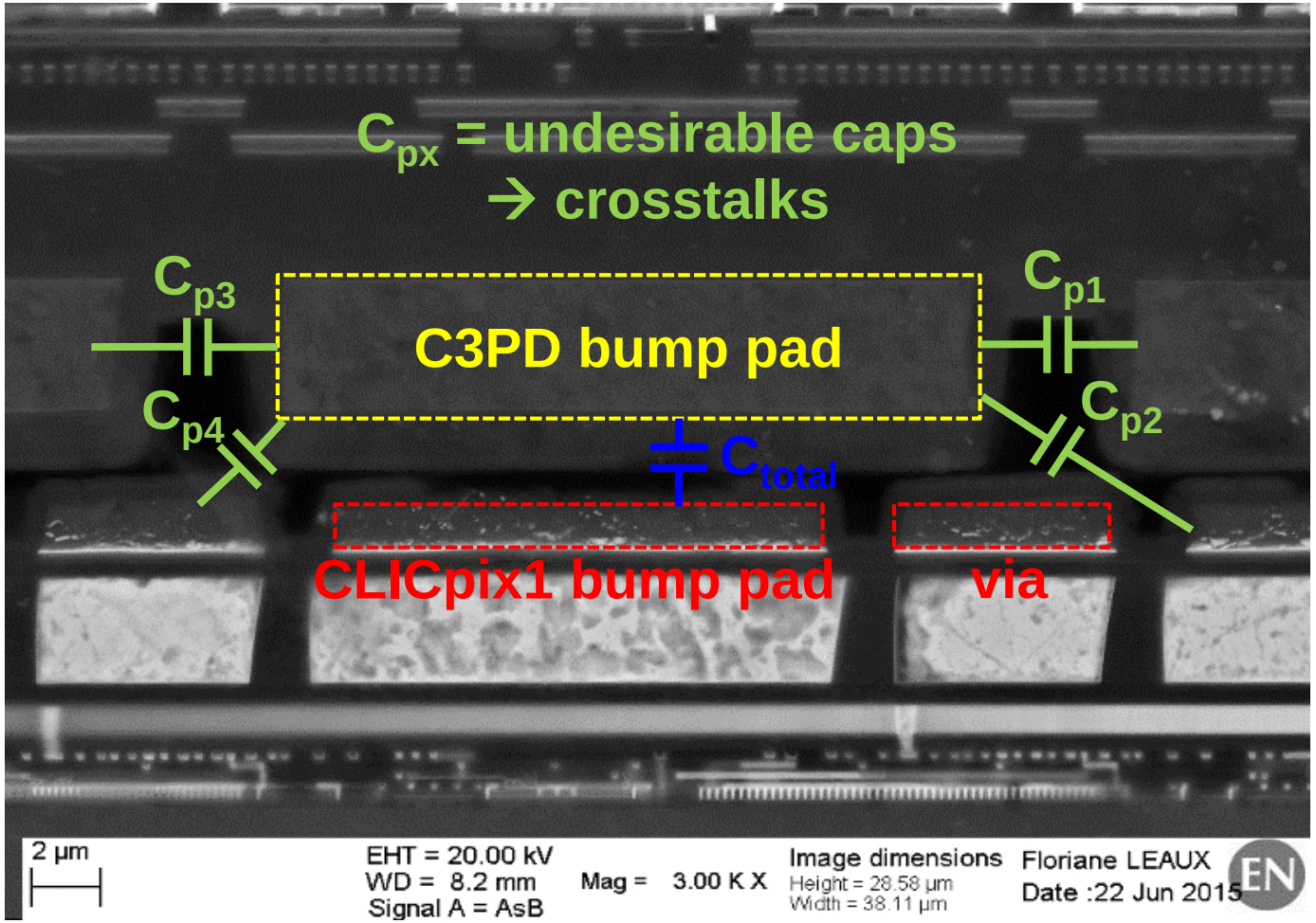
Motivation

- Define the bump pads layout for the C3PD chip (based on the CLICpix2 bump pads)
- Summarize (and get feedback of, if any) the final bump pads layouts for both chips: CLICpix2 & C3PD

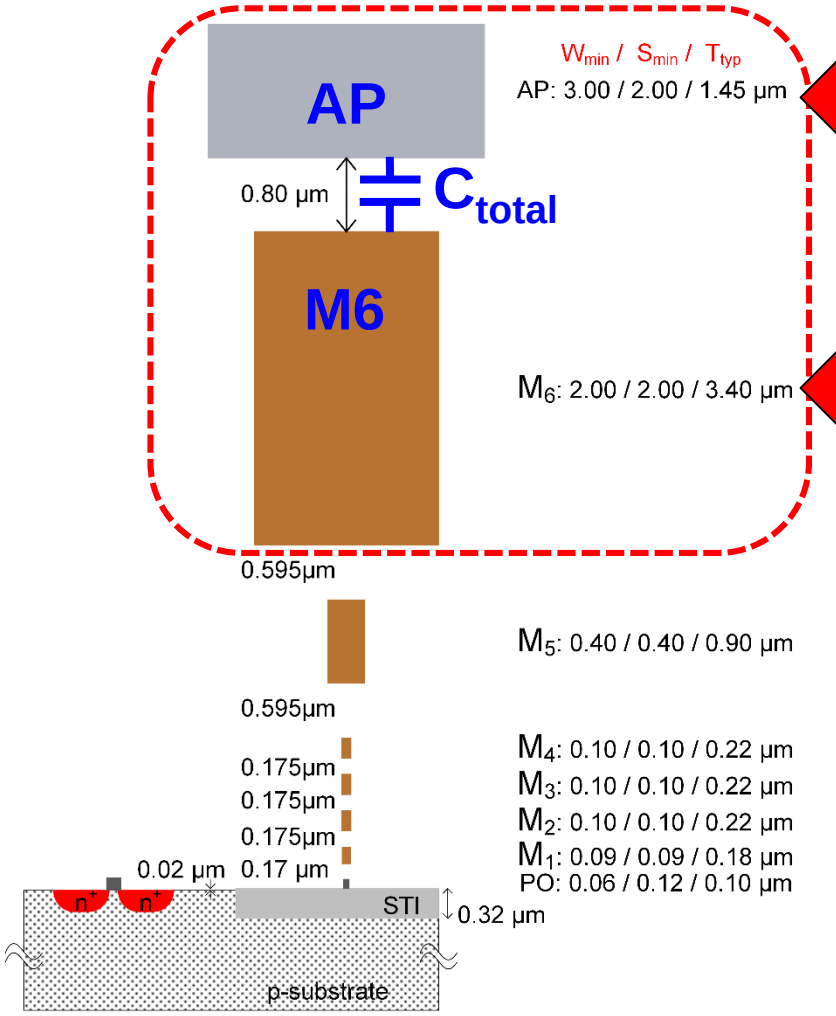
Topological cross-section of 1st prototype



- Aim: Maximize C_{total} and minimize C_{px}

An approximate study…

TSMC 65nm cross-section



ASSUMPTIONS

AP layer of TSMC 65nm as the CLICpix2 bump pad

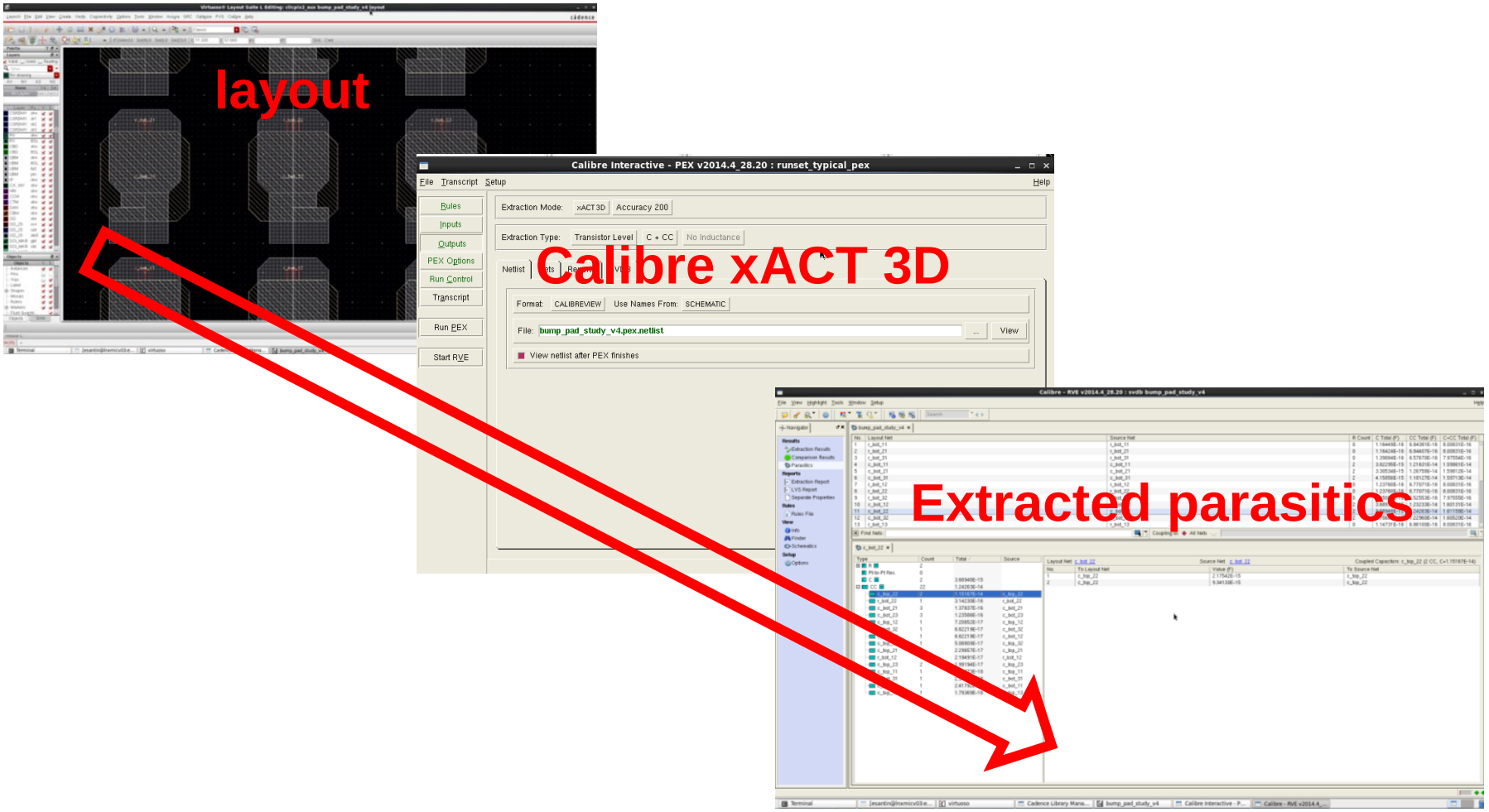
Assume M6 of TSMC 65nm as the C3PD bump pad

→ some limitations wrt the actual scenario:

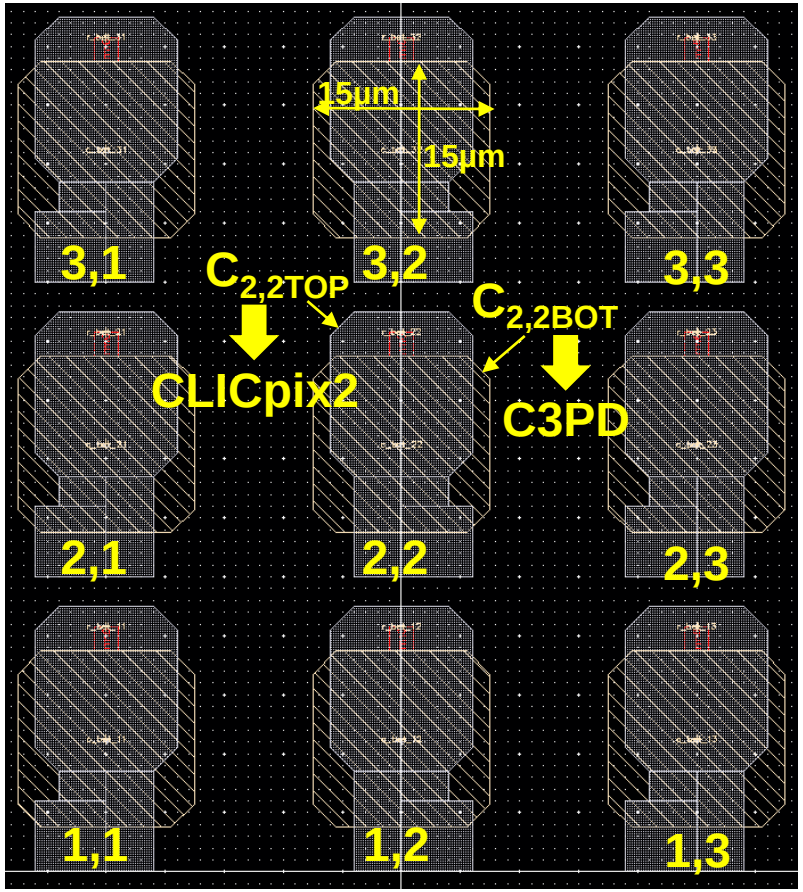
- Different dielectric height
- Different dielectric material
- Different (M6-approximated) C3PD pad thickness

→ "absolute" values shown next do not match the reality

Accurate 3D field solver



Coupling capacitances without GRs



$C_{2,2BOTtoTOP}$ =11.5 fF

$C_{2,2BOTto2,1BOT}$ = 0.14 fF

$C_{2,2BOTto2,3BOT}$ = 0.12 fF

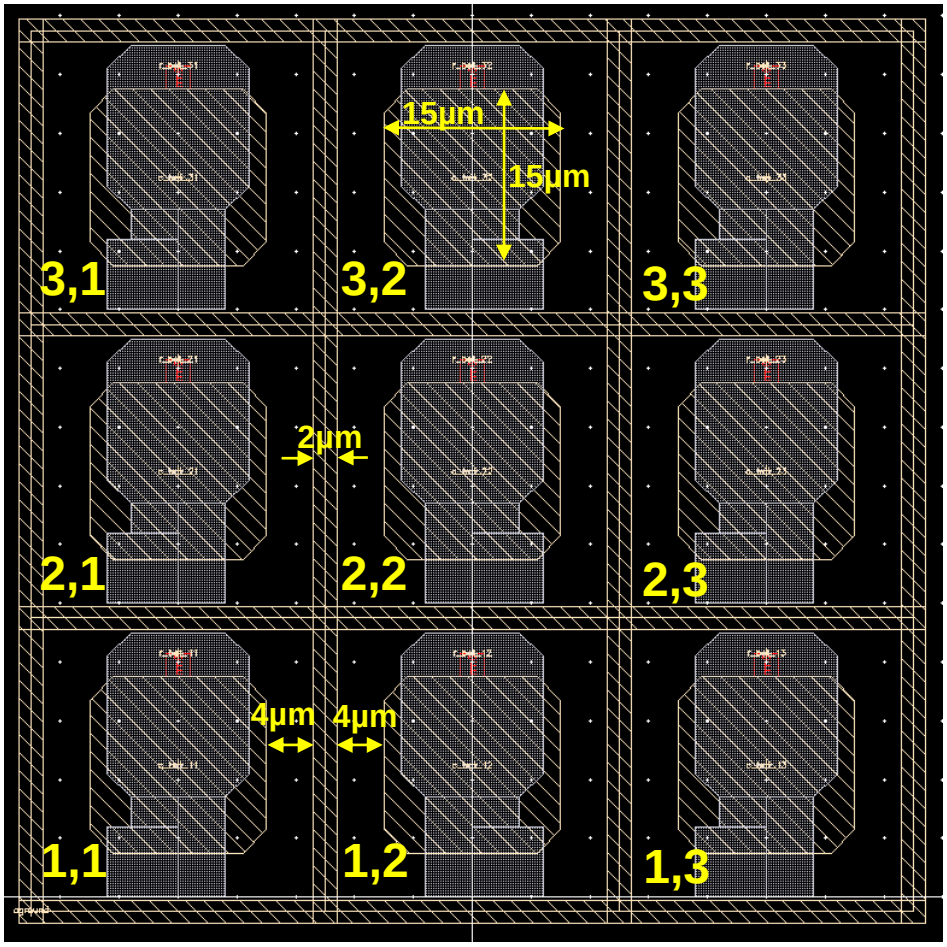
$C_{2,2BOTtoOTHERS}$ < 0.07 fF

create signal crosstalks

we want to minimize this phenomenon

- Without guard rings (GRs), there are capacitive couplings from $C_{2,2BOT}$ (i.e. C3PD bump pad) to all other bump pads (i.e. adjacent C3PD and CLICpix2 pads). The couplings to the CLICpix2 pads are, however, very small.

Coupling capacitances with GRs



$C_{2,2BOTtoTOP}$ =11.2 fF

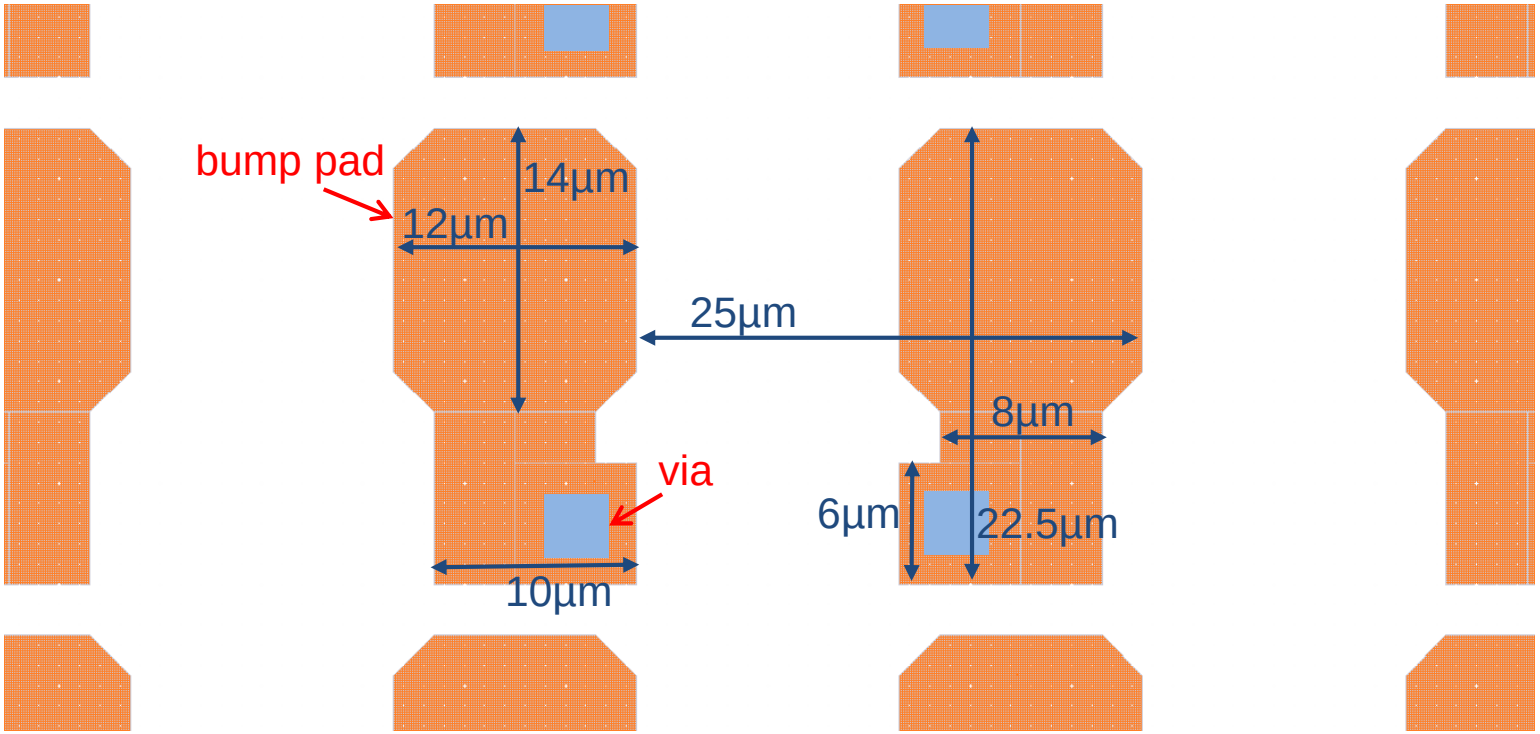
$C_{2,2BOTtoVSSA}$ = 2.5 fF

not a problem

Guard rings are a good solution to minimize undesirable crosstalks!

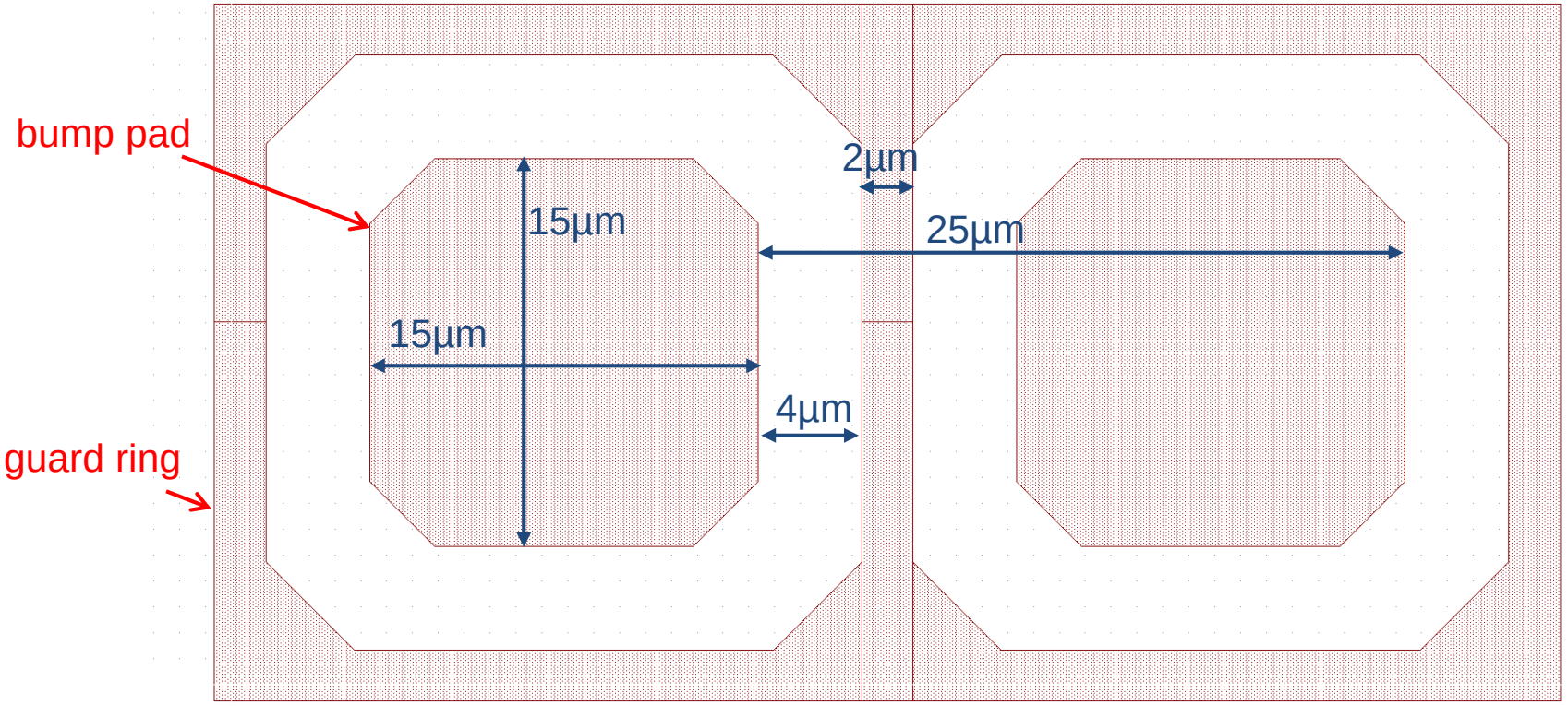
- With guard rings (GRs) around the C3PD bump pads, the capacitive coupling from $C_{2,2BOT}$ to other adjacent bump pads are negligible. On the other hand, there is a fixed capacitance between the pads and the analog ground, V_{ssa}, which is not a problem.

Final CLICpix2 bump pads layout



- Bump pad size is 240 µm^2
- Vias adjacent to the bump pad openings to comply with foundry DRC rules

Final C3PD bump pads layout

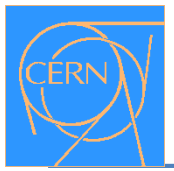


- Bump pad size is about 15 x 15 μm^2
- Guard rings around the bump pads are connected to the same low-noise, low-impedance voltage (i.e. V_{ssa}) and they minimize inter-pad (capacitive) coupling

Conclusion

- CLICpix2 bump pad final size is imposed by the power distribution grid and technology constraints (i.e. via)
- C3PD bump pad final size is imposed by the “shielding” guard rings (to minimize crosstalks)

- Open question: Is it possible to avoid the passivation layer on the C3PD chip to increase C_{total} (i.e. the intended coupling capacitance between C3PD and CLICpix2 bump pads)?

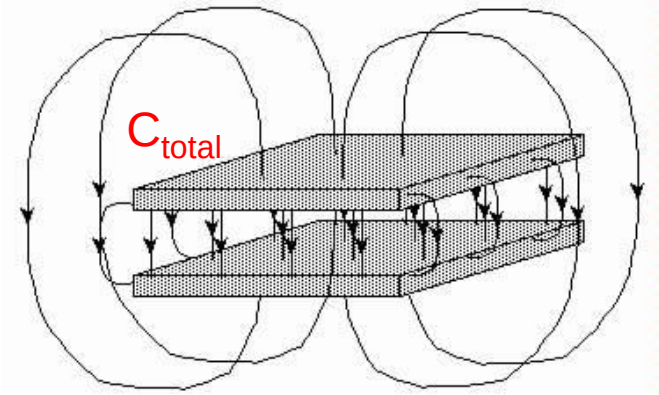


Thank you for your attention!

Backup slides

Capacitance between two plates

$$C_{total} = C_{area} + C_{fringe}$$

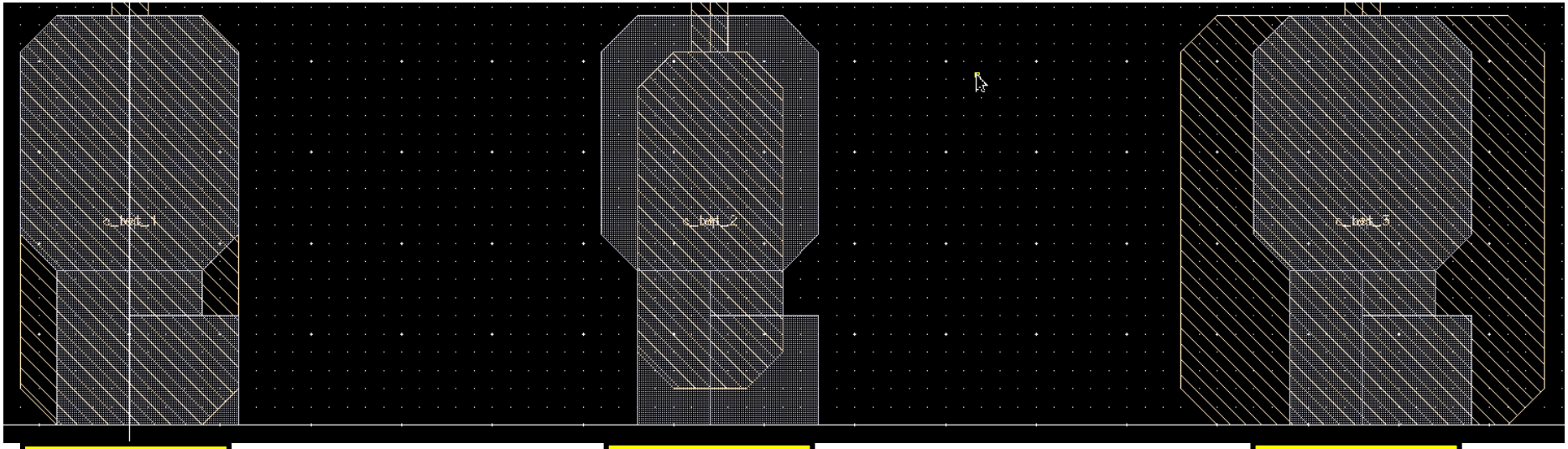


http://maxwell.ucdavis.edu/~electro/dc_circuits/images/cap_fields.jpg

- Total capacitance is a result of two components: area capacitance, C_{area}, and fringe capacitance, C_{fringe}
- Question: Which one of the two dominates in the CLICpix2 and C3PD bump pads arrangement?

Extracted coupling capacitances (using TSMC 65nm back-end layers as an approximation)

CLICpix2 bump pad vs three C3PD bump pad layouts



Case 1 | Case 2 | Case 3

C_{total}=15.1 fF **C_{total}=10.7 fF (-29%)** **C_{total}=16.3 fF (+8%)**

- Case 2 should favor the fringe capacitance component, but since the C_{total} is smaller than the other two cases it tells us that the area capacitance component dominates in these three scenarios
  - But, do not ignore the analysis limitations mentioned on slide 4