Update on the C3PD chip submission

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CLICdp Vertex Meeting – February 29th 2016

Chip Submission

- CLICpix Capacitively Coupled Pixel Detector (C3PD) chip was submitted on 22-02-2016

- Design Rules Checks (DRC) for antenna process violations were revised after receiving feedback from the foundry

- Re-submitted on 25-02-2016

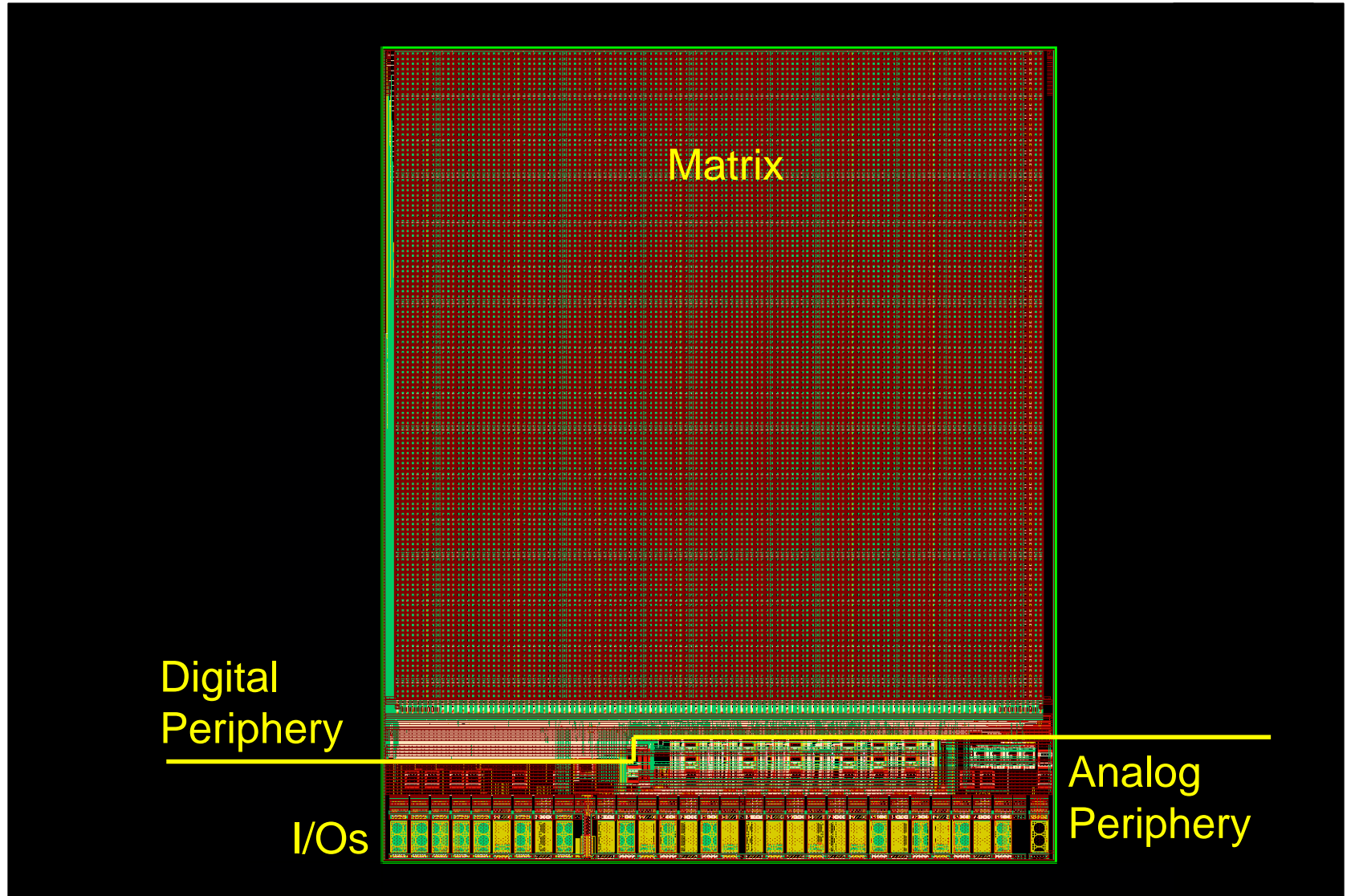- Chips are expected to be received ~3 months after submission
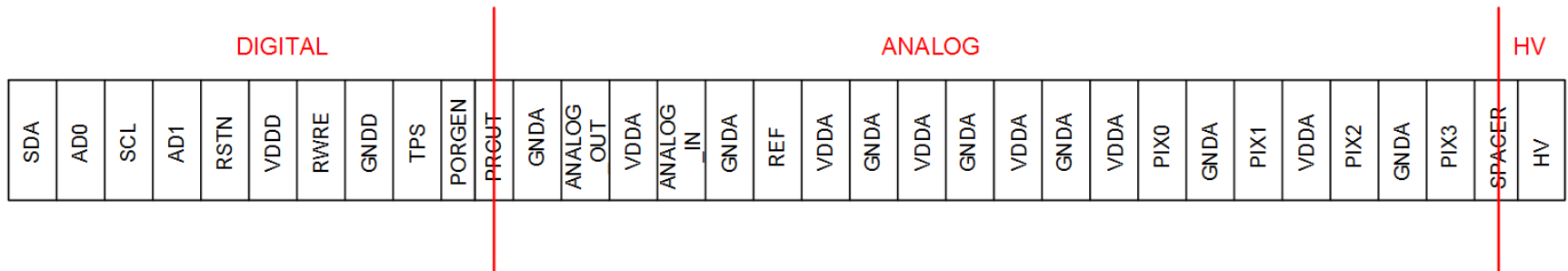
Chip Layout

Chip Layout

Matrix

Digital
Periphery

Analog
Periphery
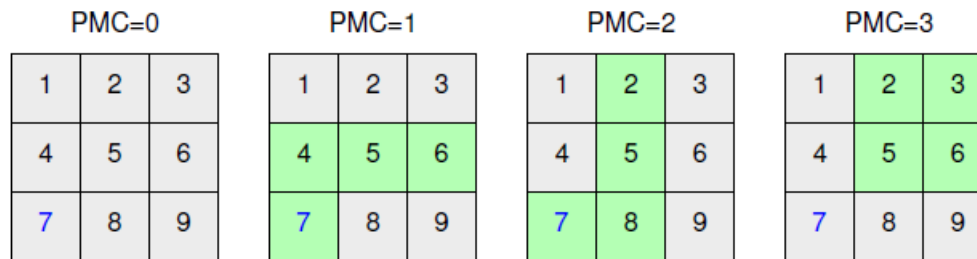
I/Os
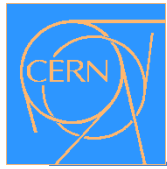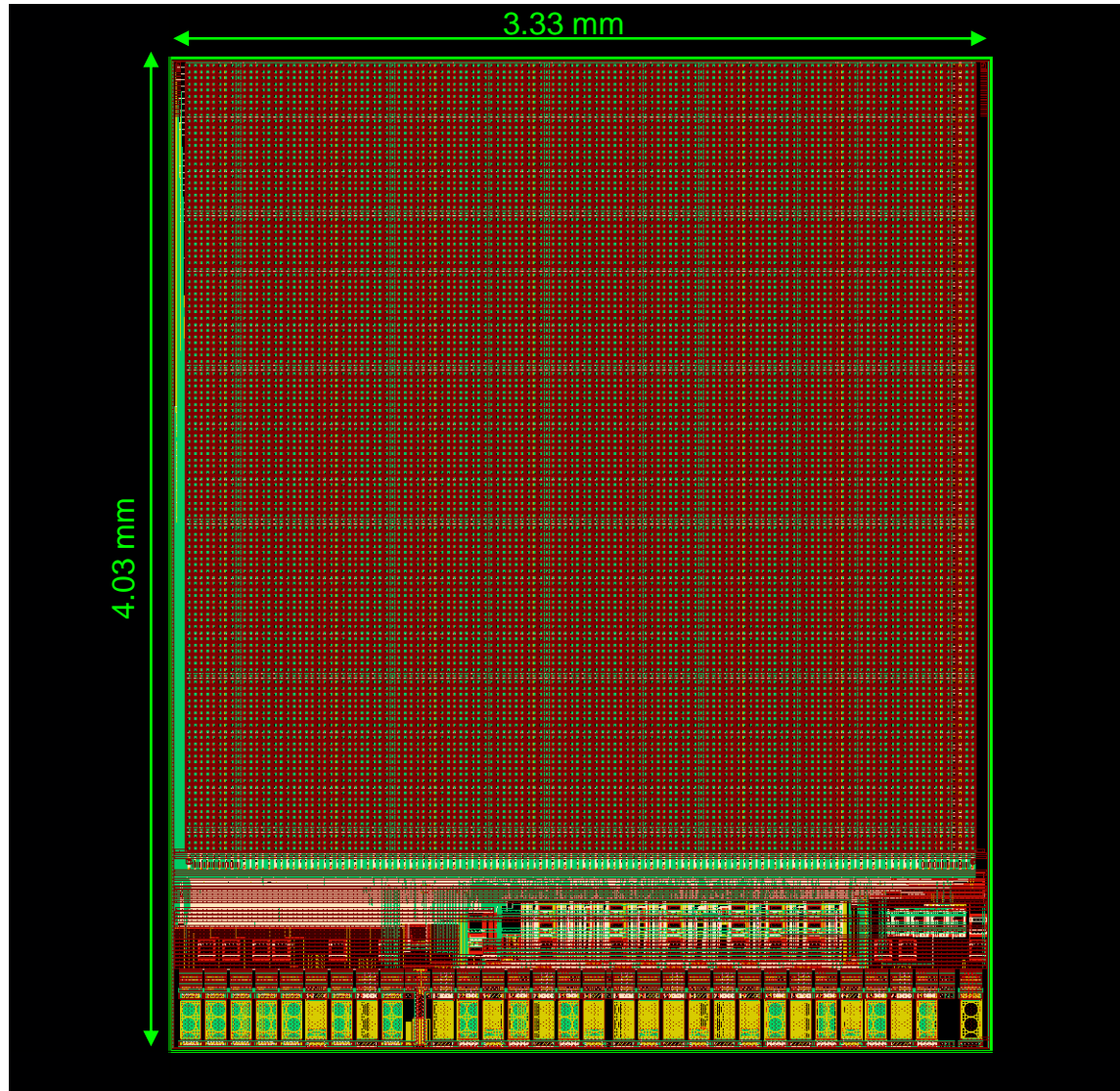
C3PD Chip Design

- Digital Part (*A. Fiergolski, S. Kulis*):
    - I^2C standard interface
    - Improved programmability
    - Power pulsing feature
    - Test pulse injection in individual pixels
    - Power On Reset

- Pixel (*R. Ballabriga*):
    - Reduced current consumption (2.5uA instead of 14.3uA)
    - Faster peaking time
    - Improved gain matching between pixels

- Matrix:
    - Full-size matrix: 128x128 pixels
    - 3 different flavours of pixels:
        - 62 double columns with regular pixel (CMOS coupling, original sensor bias)
        - 1 double column with modified biasing for the sensor (single PMOS transistor)
        - 1 double column with modified coupling capacitance (Metal-to-metal coupling)
    - Cluster of pixels buffered directly to the IOs
    - Alignment marks for precise alignment with CLICpix2

- Top-level chip integration
    - Use of programmable IOs
    - Analog periphery
        - Multiplexers
        - DACs
        - Unity gain buffers
        - Decoupling capacitors

Chip Interface

- 30 IO pins:

SDA	AD0	SCL	AD1	RSTN	VDDD	RWRE	GNDD	TPS	PORGEN	PRGUT	GNDA	ANALOG_OUT	VDDA	ANALOG_IN	GNDA	REF	VDDA	GNDA	VDDA	GNDA	VDDA	GNDA	VDDA	PIX0	GNDA	PIX1	VDDA	PIX2	GNDA	PIX3	SPACER	HV

- 3x3 pixel cluster used to monitor different combinations of pixel outputs:

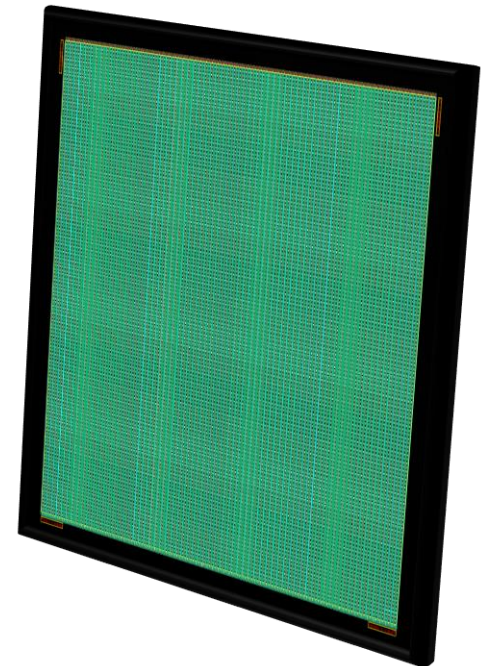*) Pixel 7 is used to monitor actual test pulse amplitude

S. Kulis

Summary – Next steps

- Full matrix HV-CMOS sensor chip to match CLICpix2 read-out chip
  - 128x128 pixels
  - 25 µm pitch

- Pixel and basic building blocks have been (re)designed
  - Current consumption per pixel reduced by factor of 5
  - Faster rise time
  - Test pulse injection
  - Power pulsing

- Next steps:
  - PCB design
  - Test preparation

Thank you!