Status of the Caribou readout

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Original requirements for multi-chip μASIC 2.0 (CLIC workshop)

- FMC mezzanine
  - 400 pins vs legacy 68-pin VHDCI
- PCIe×16 receptacle for the chipboard
  - 164 pins vs legacy 98-pin or 80-pin SEAM connector
  - ×8 compatible with ×16
  - simple adapters, ex. PCIe edge to VHDCI (CERN Timepix3)
- 8 × general purpose power supplies with monitoring capabilities
  - Maximum current: 4 A
  - Voltage range: 0 — 4 V
- 8 × voltage outputs (0 — 4 V)
- 4 × current outputs (0 — 100 μA)
- 4 × voltage inputs (0 — 4 V)
- ADC (8 channels, 80 MSPS/12-bit)
- FEASTMP support
- high voltage input
- 8× full-duplex GTX links
- 16 × general CMOS signals (I/O) with adjustable voltage levels
- differential pairs (I/O) — CML converters only on the specific chipboards
- clock and trigger/shutter input (RJ45 compatible with TLU)
- I2C bus

Current version of the CaR V1.0 (under design)

- FMC mezzanine

  The ZC706 development board is equipped with two FMC connectors: high (HPC) and low (LPC) pin-count.

  The connectors of the board implement only subset of the standard connectivity:

  - 34 differential signals
  - 8 (HPC) / 1 (LPC) GTX transceivers
  - 2 (HPC) / 1 (LPC) GTX clock
  - 4 (HPC) / 2 (LPC) differential clocks
  - power domains: 12V, 3.3V, 2.5V (V_{adj})

  All signals from CaR board are differential (up to 1m FMC cable).

Current version of the CaR V1.0 (under design)

- FMC mezzanine
- ~~PCIe×16~~ SAMTEC SEAF 40 × 8 receptacle for the chipboard
  - higher pin-count
  - Caribou group has positive experience with it
  - no backward compatibility the with legacy CLICpix chipboard without an additional adapter

Current version of the CaR V1.0 (under design)

- FMC mezzanine
- SAMTEC SEAF 40 × 8 receptacle for the chipboard
- 8 × general purpose power supplies with monitoring capabilities — TPS74401
  - Maximum current: ~~4 A~~ 3 A
  - Voltage range: ~~0 — 4 V~~ 0.8 — 3.6 V

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  Copy from the μASIC design.

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- ~~4~~ 8 $\times$ voltage inputs (0 — 4 V) — ADS7828
  To monitor slow voltage changes.

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- ADC ~~(8 channels, 80 MSPS/12-bit)~~ (16 channels, 65MSPS/14bit) — AD9249
  To observe faster signals.

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- ~~FEASTMP support~~

  Dual 4A DC/DC regulator — LTM4619
  - smaller
  - neither radiation nor magnetic field tolerant

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Two flavours of the connection from the ZC706

- through standard FMC lines (single ended)
- through differential pairs

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- high voltage input
- 8× full-duplex GTX links
- 22 × general CMOS (14 outputs/8 inputs) signals with adjustable voltage levels
- 17 differential pairs (I/O) — CML converters only on the specific chipboards
- clock and trigger/shutter input (RJ45 compatible with TLU)
- I2C bus
- clock generator / jitter cleaner — SI5345
  - 3 inputs (FMC, UMCC, TLU)
  - 5 outputs (GTX, FMC, ADC, 2 × SEAF)
  - 0-delay mode

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- high voltage input
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- 22 × general CMOS (14 outputs/8 inputs) signals with adjustable voltage levels
- 17 differential pairs (I/O) — CML converters only on the specific chipboards
- clock and trigger/shutter input (RJ45 compatible with TLU)
- I2C bus
- clock generator / jitter cleaner — SI5345
- 4 × pulse injection circuits
  - adjustable pulse height (0 — 4 V)
  - controlled duty cycle

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- 32 × voltage outputs (0 — 4 V) — DAC7678
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- 8 × voltage inputs (0 — 4 V) — ADS7828
- ADC (16 channels, 65MSPS/14bit) — AD9249
- high voltage input
- 8× full-duplex GTX links
- 22 × general CMOS (14 outputs/8 inputs) signals with adjustable voltage levels
- 17 differential pairs (I/O) — CML converters only on the specific chipboards
- clock and trigger/shutter input (RJ45 compatible with TLU)
- I2C bus
- clock generator / jitter cleaner — SI5345
- 4 × pulse injection circuits

Pin utilization for the different readout chips — (link to the full table)

	Standard	Differentiial pairs	Single ended inputs	Single ended ouptuts	Clock inputs (diferential)	GTX	Comment
Timepix3							
DataIn	LVDS	1					
EnableIn	LVDS	1					
Reset	LVDS	1					
T0_Sync	LVDS	1					
Shutter	LVDS	1					
EnablePowerPulsing	LVDS	1					
ExtTPulse	LVDS	1					
ClkIn40	LVDS				1		
ClkInRefPll	LVDS				1		
PLLOut	SLVS	1					
DataOut	SLVS					8	
ClkOut	SLVS	1					
DACout	ADC_IN						for slow ADC
DAC_IN	BIAS	1					
	SUM:	**9**			**2**	**8**	
CLICpix2							
CLK_320	CML				1		
CLK	CML				1		
Rst	CMOS		1				
Power_pulse	CMOS		1				
Shutter	CMOS		1				
TP_SW	CMOS		1				
DataOut	CML					1	
ClkOut	CML	1					
CS	CML	1					
SPI_IN	CML	1					
SPI_OUT	CML	1					
C3PD							
SDA	CMOS						on board I2C
SCL	CMOS						on board I2C
I2C_AD	CMOS						fixed with switches
RSTN	CMOS		1				
PWRE	CMOS		1				
TPS	CMOS		1				
BANDGAP	BIAS						bias voltage
ANALOG_IN	BIAS						bias voltage
ANALOG_OUT	ADC_IN						for slow ADC
PIX	ADC_iN						4 x for scope
	SUM:	**4**	**7**		**2**		

CaR V1.0 (resources available using a single FMC connector of the ZC706 board)

The ZC706 board implements only subset of the strand FMC connectivity. In order to profit all features of the CaR V1.0, an additional custom 2FMCs-to-1FMC adapter is needed (Atlas case).

Functionality for the CaR connected directly to ZC706 (CLIC case) includes:

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- 32 $\times$ voltage outputs (0 — 4 V) — DAC7678
- 8 $\times$ current outputs (0 — 100 μA)
- 8 $\times$ voltage inputs (0 — 4 V) — ADS7828
- ADC (~~16 channels~~ 2 channels, 65MSPS/14bit) — AD9249
- high voltage input
- 8$\times$ full-duplex GTX links (only 1 $\times$ GTX in case of the LPC connector)
- ~~22~~ 12 $\times$ general CMOS (~~14~~ 4 outputs/8 inputs) signals with adjustable voltage levels
- ~~17~~ 14 differential pairs (I/O) — CML converters only on the specific chipboards
- clock and trigger/shutter input (RJ45 compatible with TLU)
- I2C bus (through standard FMC single ended lines)
- clock generator / jitter cleaner — SI5345
- ~~4~~ 1 $\times$ pulse injection circuits

Status of the Caribou development

- CaR V1.0 design
  - issue with PADS software (used at BNL for design)
    - ★ design files shared via gitlab
    - ★ at the moment not available at CERN
    - ★ Mentor Xpedition should allow to open schematic and import (**?**) design
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  - finalizing last details of the schematic
    - ★ connectivity optimization to Zynq SoC
    - ★ so far very successful and fruitful cooperation (*thanks for Hongbin and Hucheng*)
  - working already on layout
    - ★ considered size: 4000 $\times$ 6000 mil (10.16 $\times$ 15.24 cm) — not standard FMC width
    - ★ stack-up: 10 layers (4 signal layers)

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