UK community meeting on CMOS
sensors for particle tracking28-29
10 March 2016
Abingdon, UK

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Technology

HR-CMOS

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The problem

NIEL

→ *reduction in minority carrier lifetime*

→ *less time to collect the charge*

→ *need to collect the charge faster*

→ *need to have an electric field in the detecting volume*

→ *Depletion region*

$$\propto \sqrt{V_{bias}\rho}$$

HV **HR**

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ATLAS task force

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Foundry review

Image sensors: lots of pixels but traditionally low resistivity and thin
High-voltage CMOS: not for pixels

Foundry Code	Node	CIS / HV	Max chip size		Stitching	Resistivity	Epi thickness	Backbias	TCAD	MPW	Wafer size	Cost		
										Average frequency		Mask set	Wafers	
													Engineering run	Production
			X	Y										
	nm		mm	mm		Ohm cm	um			Months	mm	US$		
A	180	CIS	25.5	32.5	2D & 1D	>1k	up to 40	In progress	possible	2	200	$125,000	$3,333	$1,100
B	150	CIS	19	24	2D & 1D	Yes	20?	In progress	y	?	200			
F1	150	CIS	25	31	Planned	500 (?)	50	y	?	6	200	$210,440		$2,813
I	180	HV	18.73	20.77	No	10				3	200	$197,755	$7,175	
O	130	HV			No?						200			
R	350	HV	19	24.5	No	20				3	200	$102,709	$4,532	

NB Cost is indicative only. It would depend on exact specification, e.g. how many metal levels, which type of devices, …

The task force selected two foundries, one HV and one HR

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- Goal is to develop pixel detectors for particle physics based on conventional CMOS Image Sensor
- CIS foundries tend to be (a bit) more interested in process changes
- E.g. more choice of starting material (substrates)
- Possibility of stitching, i.e. making sensors beyond the 2cmx3cm of the reticle size. Up to a full CMOS wafer
- Two main limitations:
  1) Pixels in imagers contain only NMOS transistors
  2) Substrates are thin (3-5um) epi and low resistivity
- Needs to develop
  1) Full CMOS (N+P MOS) pixels
  2) Thick, high res and fully depleted substrates

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TPAC

- *CMOS Image Sensor for a digital calorimeter at the International Linear Collider*
- *Requirements:*
  - *Pixel size = 20-60 μm*
  - *S/N = MIPS detection with a noise hit rate < 10^{-5} → noise ~ 20-30 e- rms*
  - *Time stamping with 150 ns resolution (6.7MHz), over 16 bits*
  - *Large area to be covered → MAPS sensor …*
- *… but need a HAPS type pixel: HAPS = Hybrid Active Pixel Sensor or Hyper-Active Pixel Sensor*
- *STFC patent on the deep P-well: how to integrate CMOS electronics in a pixel without compromising performance*
- *Which foundry?*
- *Start working with Tower Semiconductor in 2006 to develop a deep P-well module*

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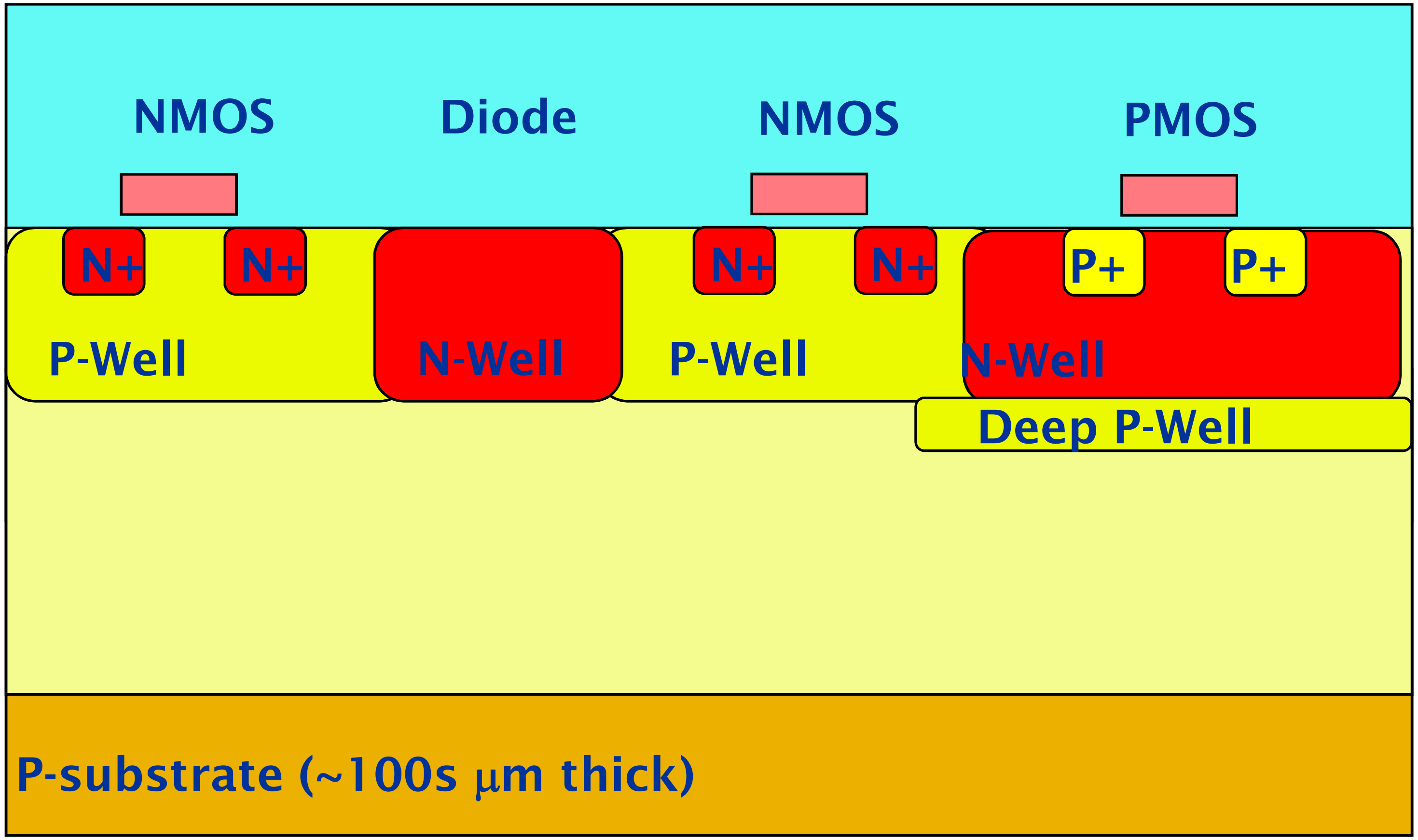
Deep P-well

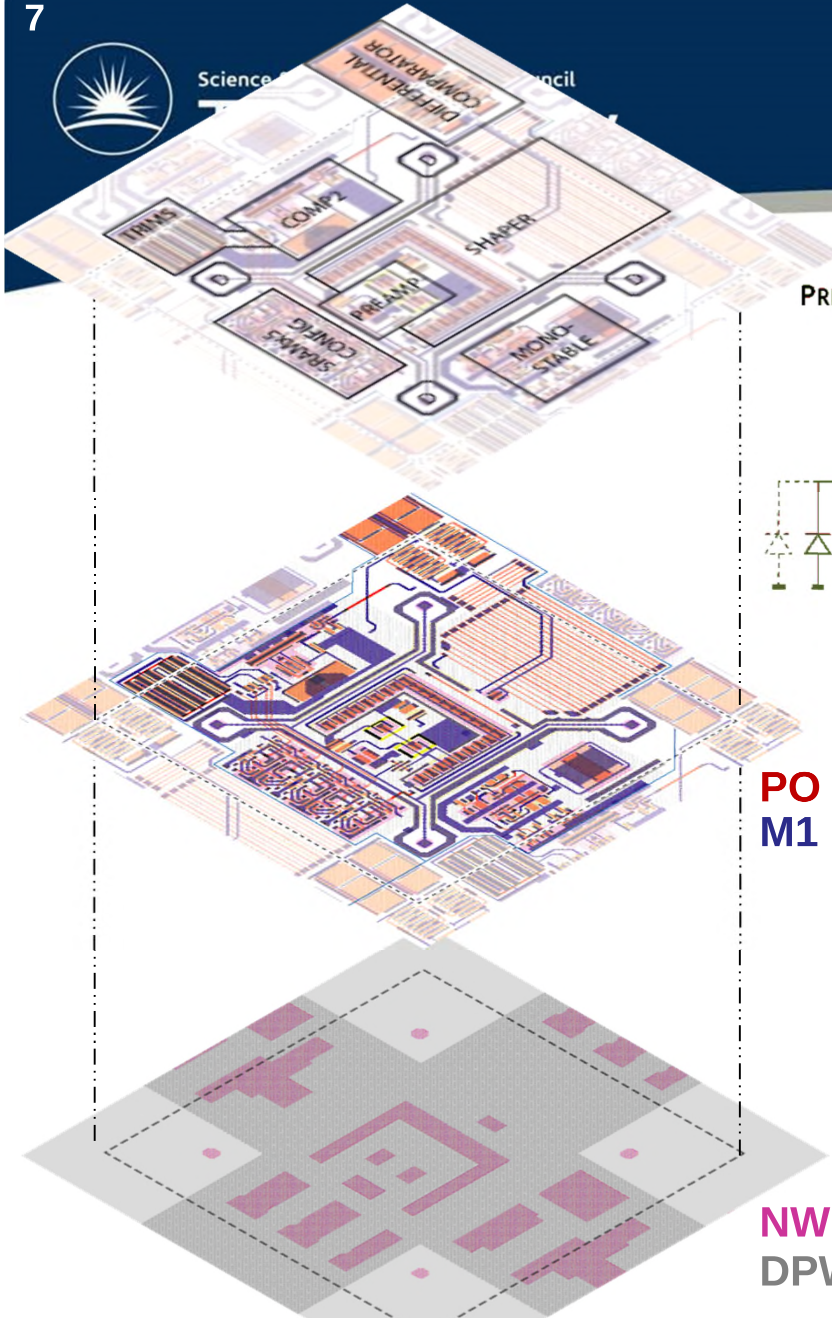


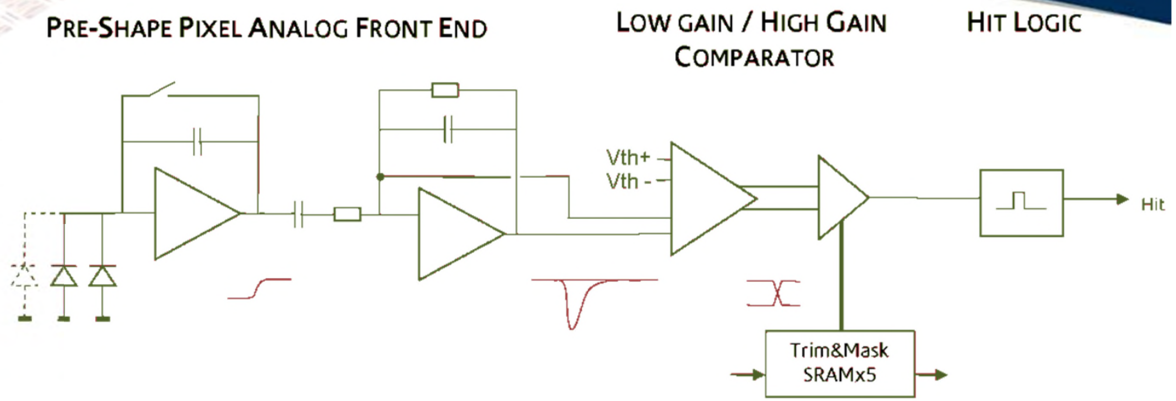
Standard CMOS with additional deep P-well implant. Quadruple well technology.

100% efficiency and CMOS electronics in the pixel.

Optimise charge collection and readout electronics separately!

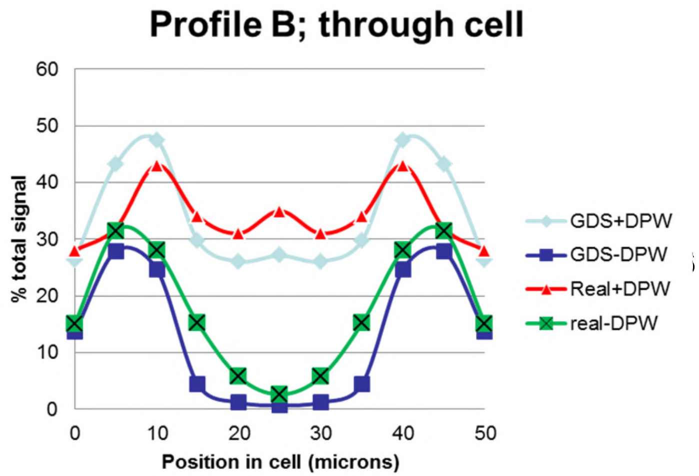
Image Sensor for CAlice





- Gain 136uV/e
- Noise 23e-
- Power 8.9u
- 150ns "hit" wired to rov
- Shaped pul return to ba

- 50um pixel
- 4 diodes



TPAC = Tera Pixel Calorimeter

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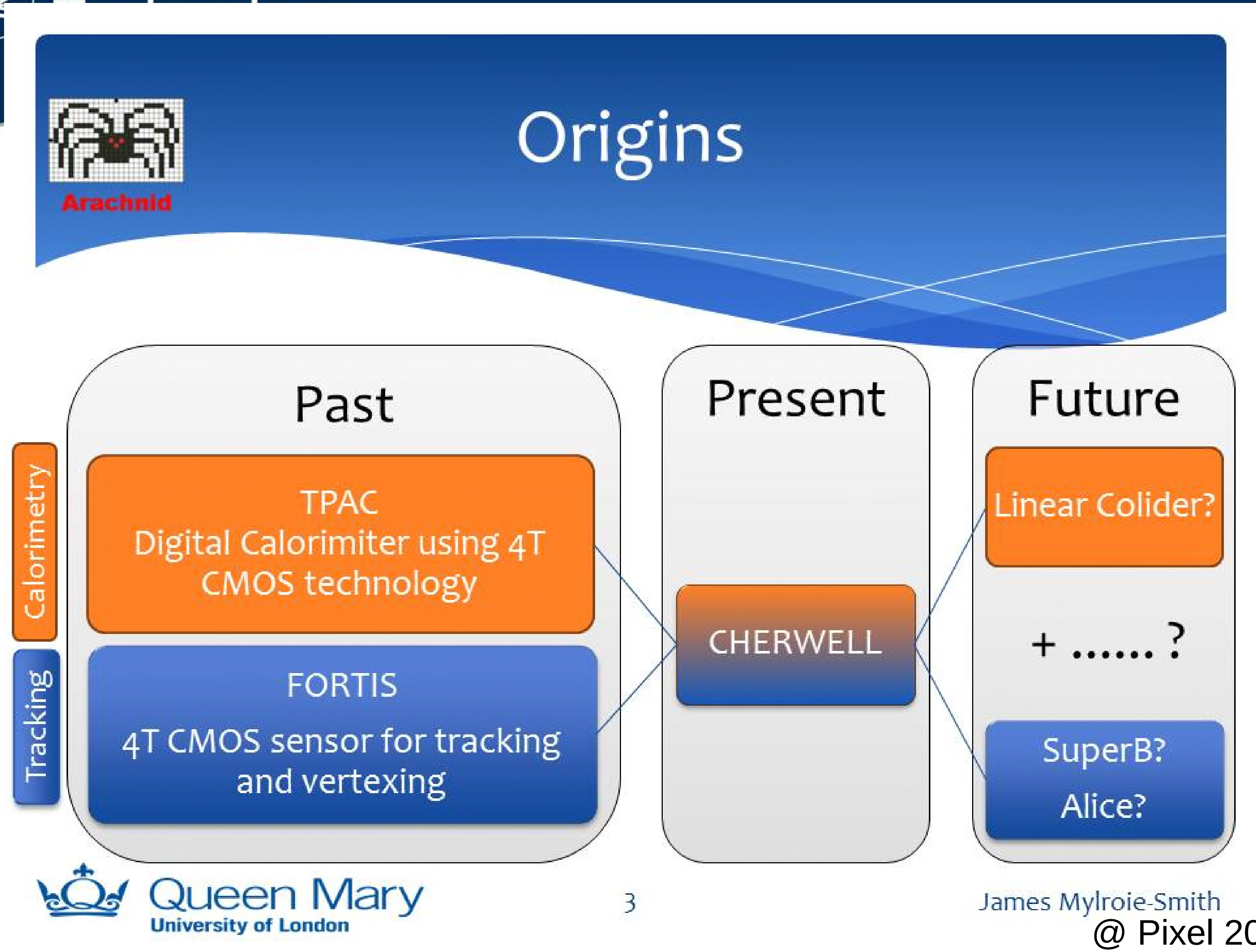
What happened next



@ Pixel 2012

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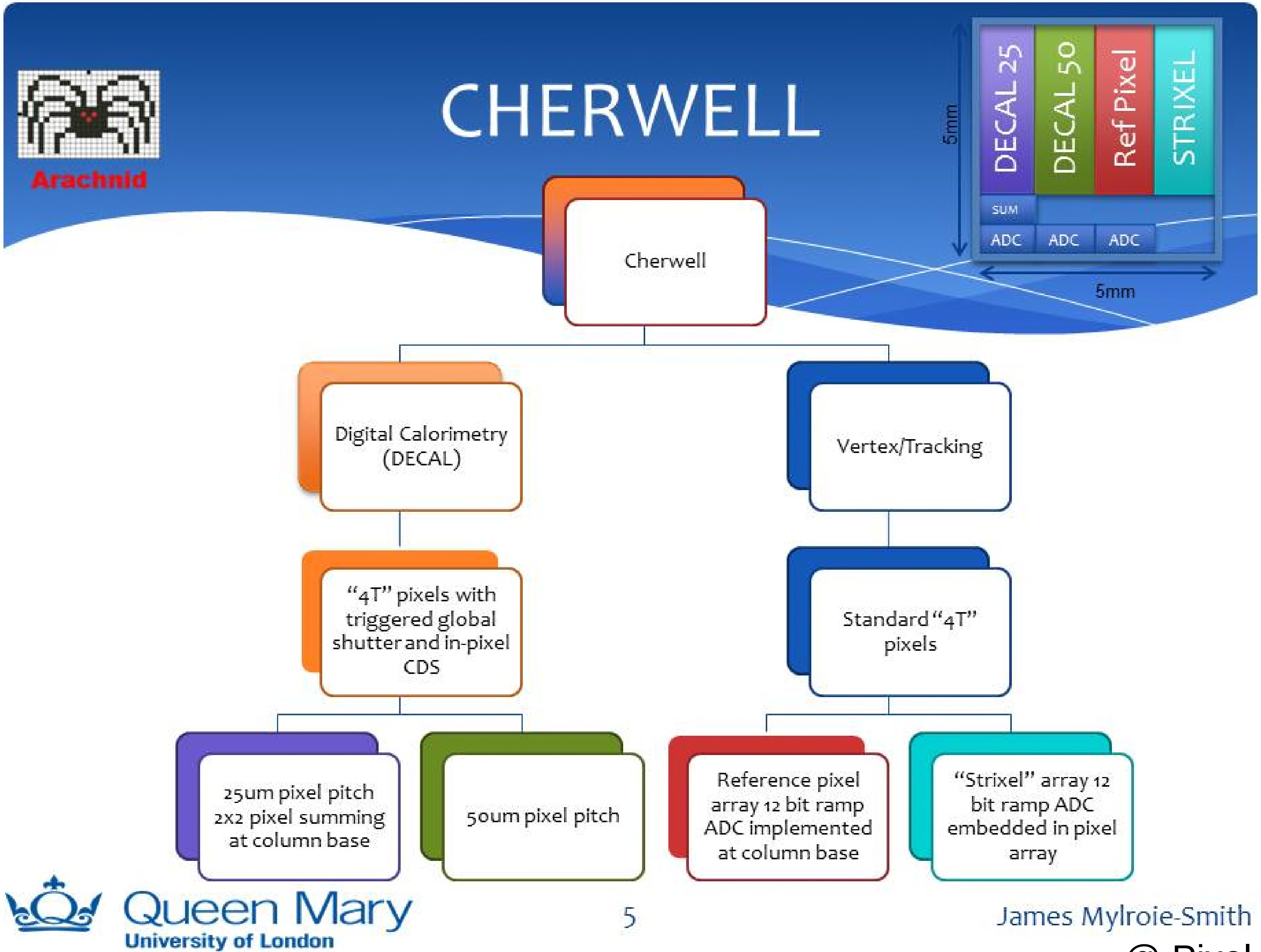
Cherwell



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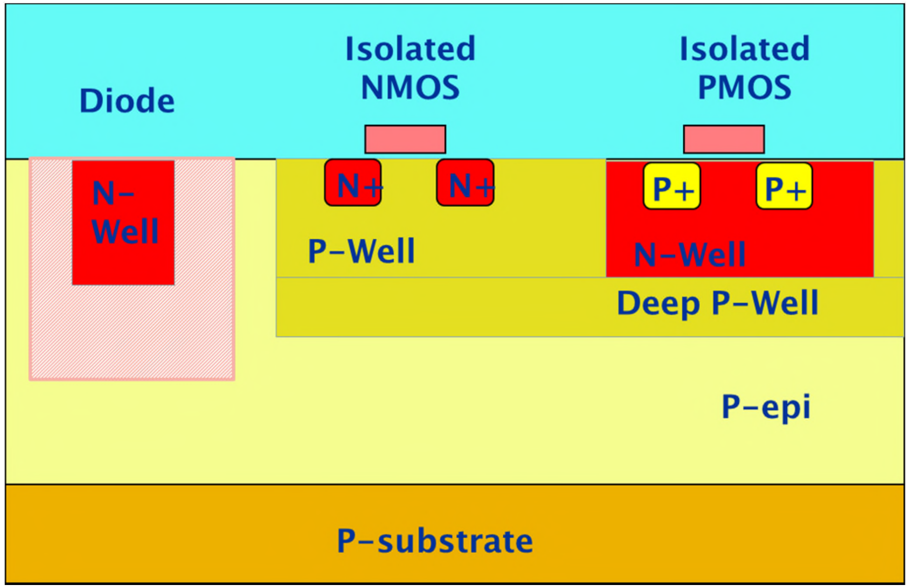
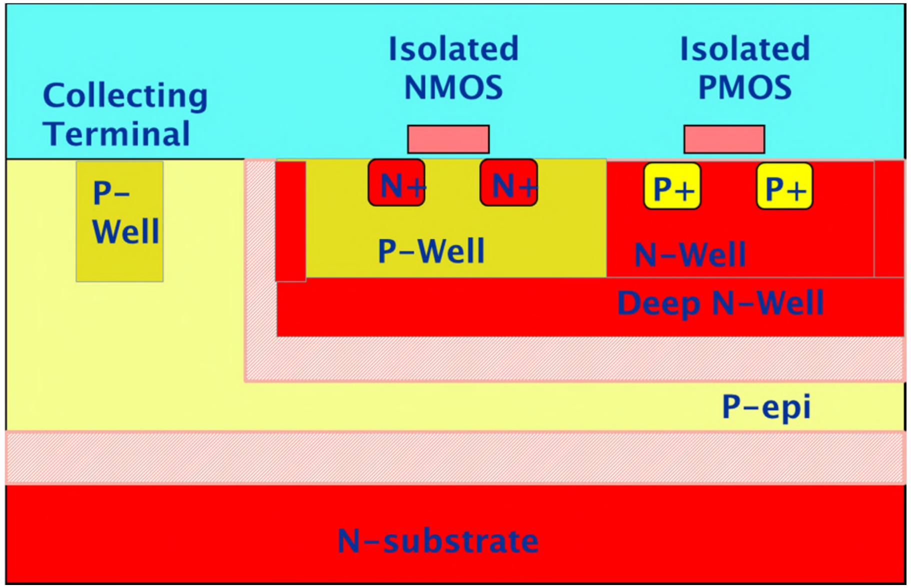
Wafer types for Chess

P on P
aka P epi on P substrate



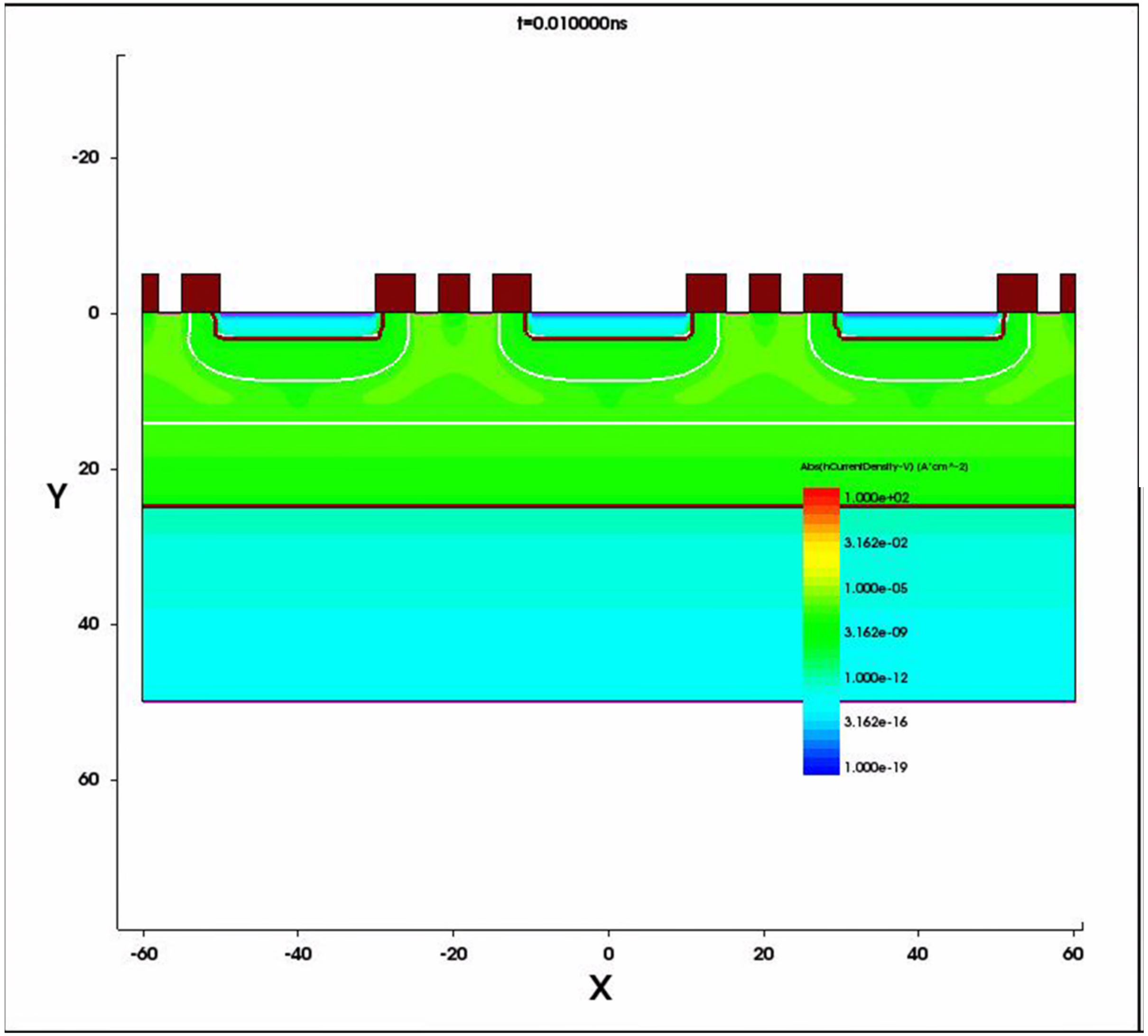
Conventional
Depletion starting from collecting N-well

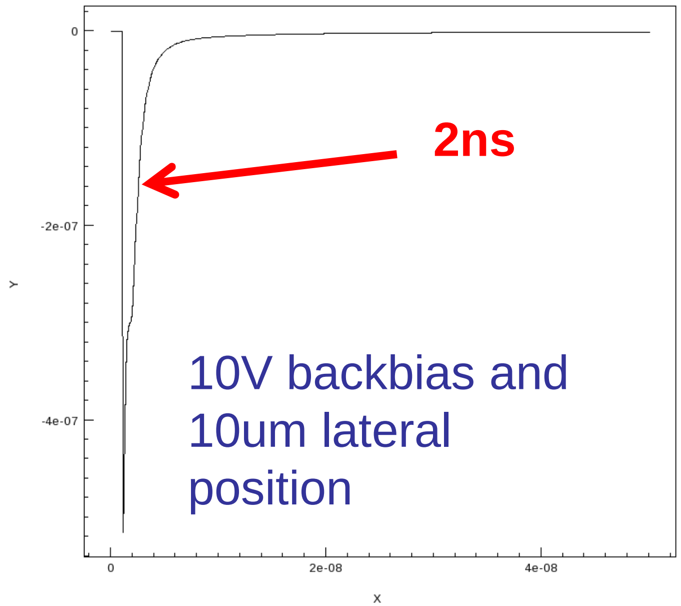
P on N
aka P epi on N substrate

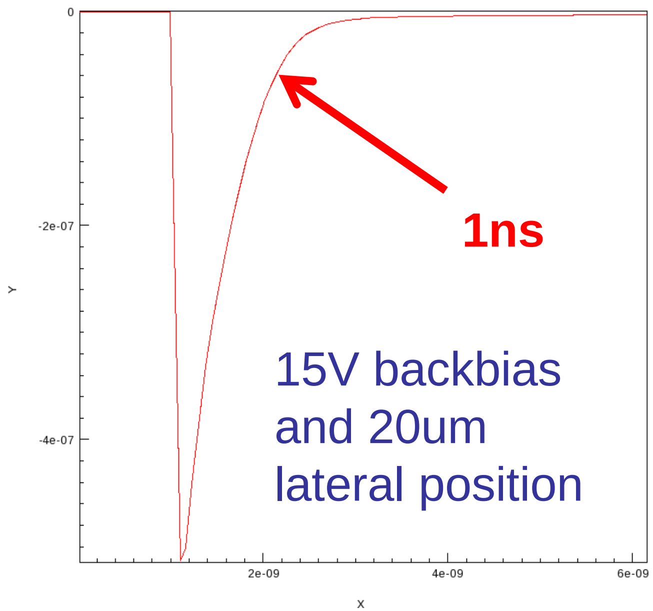


New
Depletion starting from deep N-well and N substrate

Charge collection in PonN







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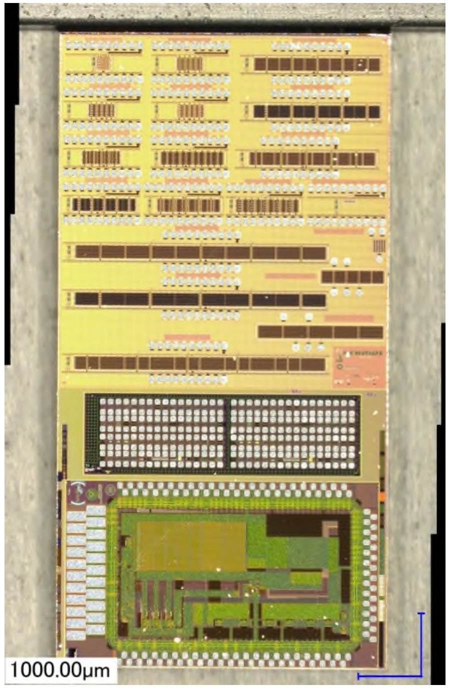
Manufactured Chips
HR-CHESS1

P on P
aka P epi on P substrate



Conventional
Depletion starting from collecting N-well

Inside the chips we have:

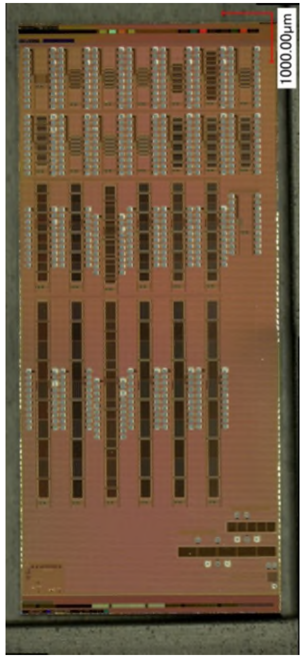
- Passive pixel Arrays
- Active pixels Arrays
- Isolated fast amplifiers
- Individual transistors, resistors, capacitors

Both chips available in splits:

- 5µm (low resistivity)
- 12µm (high/low resistivity)
- 18µm (high resistivity)
- <u>25µm</u> (P on P high resistivity)
- <u>25µm</u> (P on N high resistivity)

Now under test

P on N
aka P epi on N substrate



New
Depletion starting from deep N-well and N substrate

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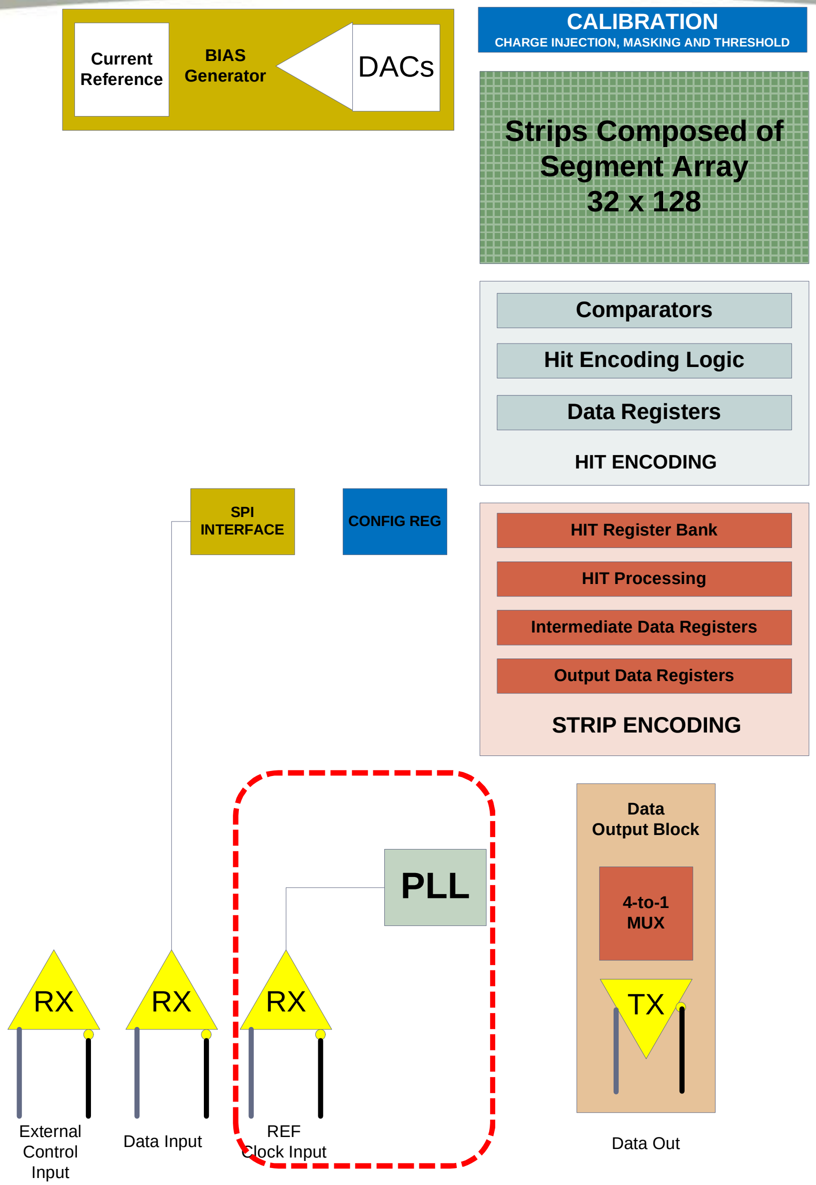
HR-CHESS2 Chip Block Diagram

Design in progress
Goal to tape out in May/June 2016



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PRD 2016

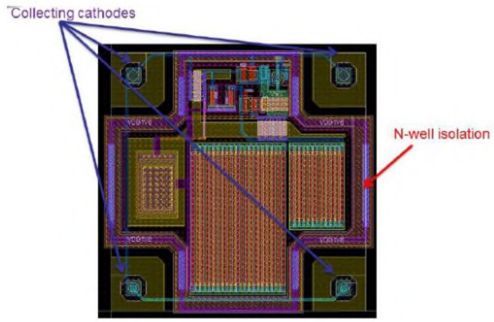
Development towards a Reconfigurable Monolithic Active Pixel Sensor in Radiation-hard Technology for Outer Tracking and Digital Electromagnetic Calorimetry

P.P. Allport[1], D. Das[2], L. Gonella[1*], S. Head[1], K. Nikolopoulos[1], S. McMahon[2], P. Newman[1],

P. Phillips[2], R. Turchetta[2], G. Villani[2], N. Watson[1], F. Wilson[2], Z Zhang[2]

1) The University of Birmingham

2) Rutherford Appleton Laboratory, STFC

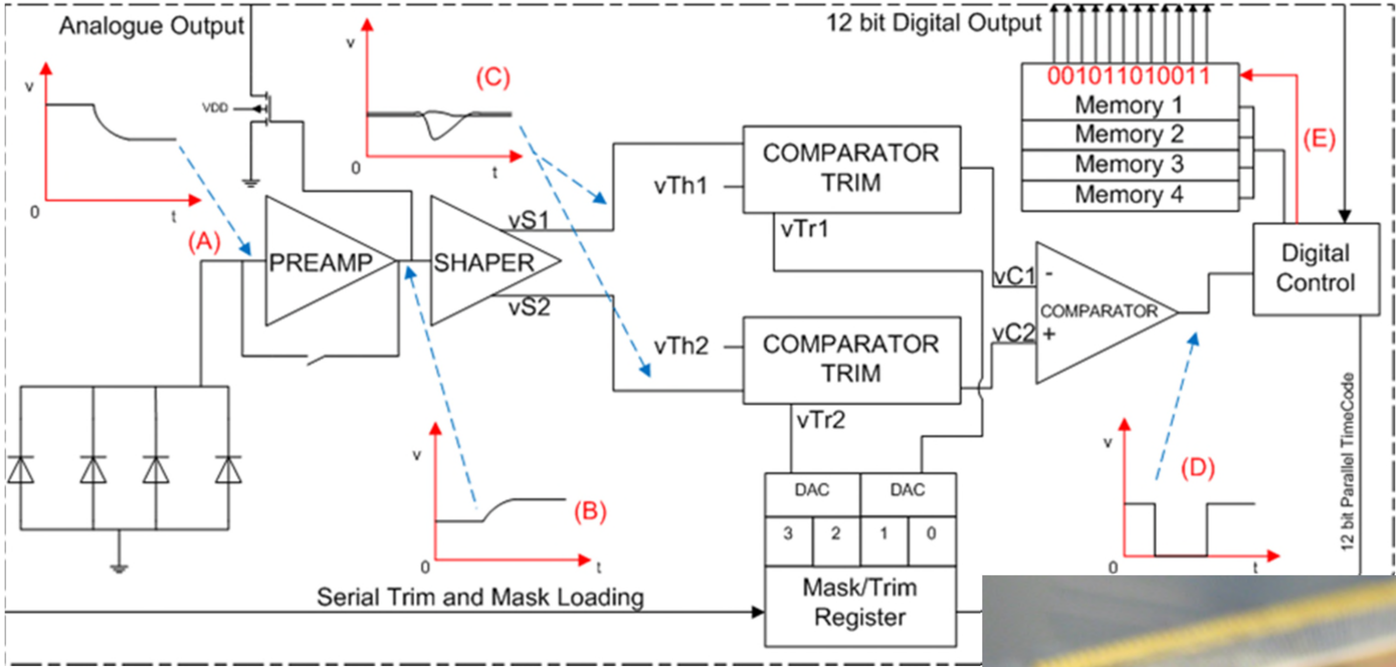


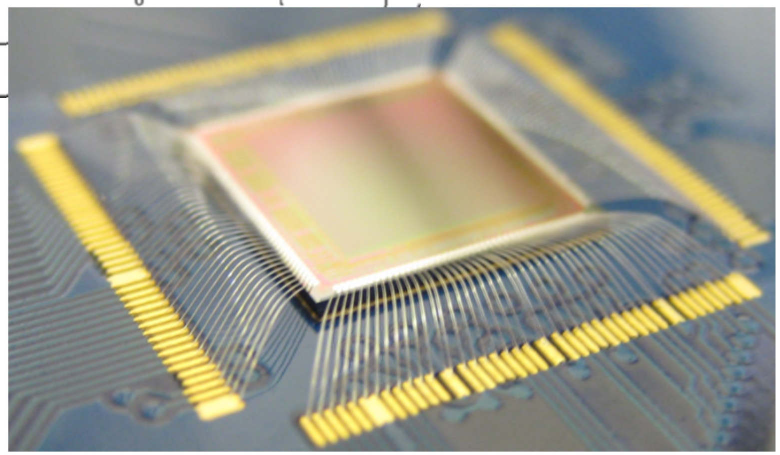
Sensor to be designed and manufactured over the 2-year period

Size: 25mm2 max. Manufactured in reference substrate (thin, low resistivity epi) and thick, high res epi

Target: 50um pitch pixel. With low noise front-end and comparator + test pixels with preamp-shaper and smaller pitch

PImMS – Pixel Imaging Mass Spectrometry





384x384 pixels

70 μm x 70 μm pixel size

Time-code resolution = 12.5 ns

4 event stored in each pixel

12 bit time-code resolution

Coulomb explosion imaging

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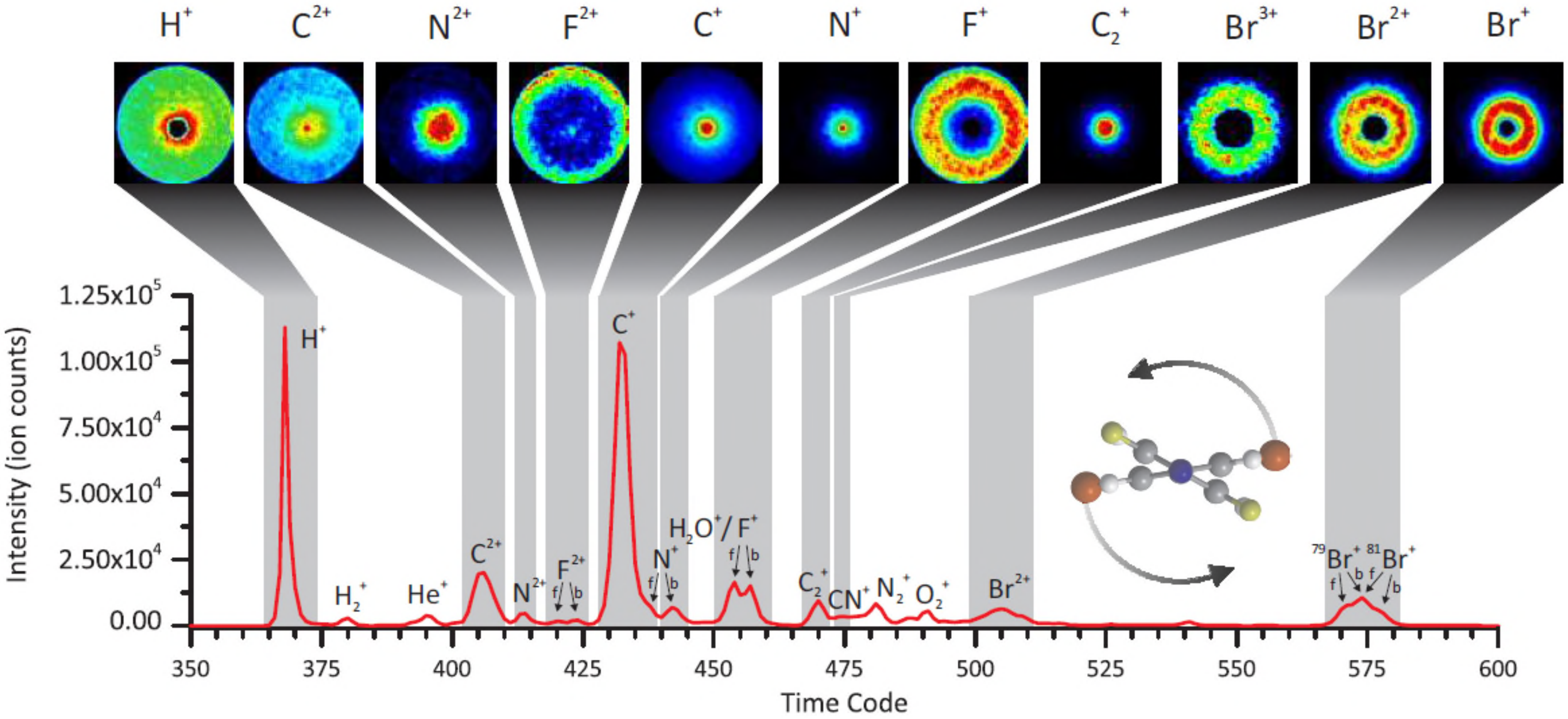
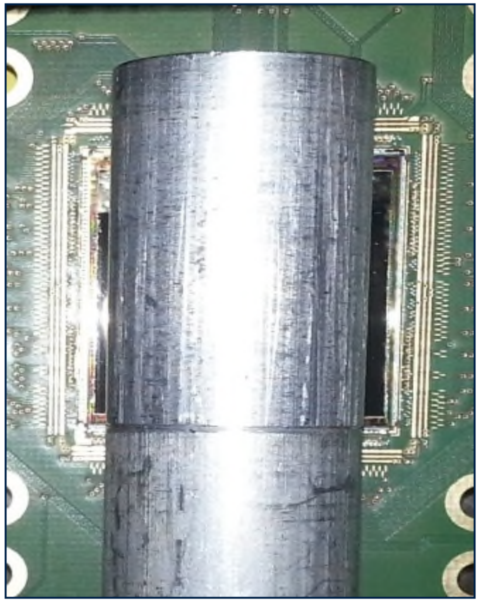
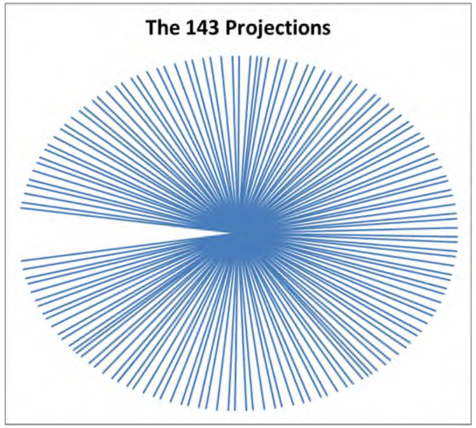
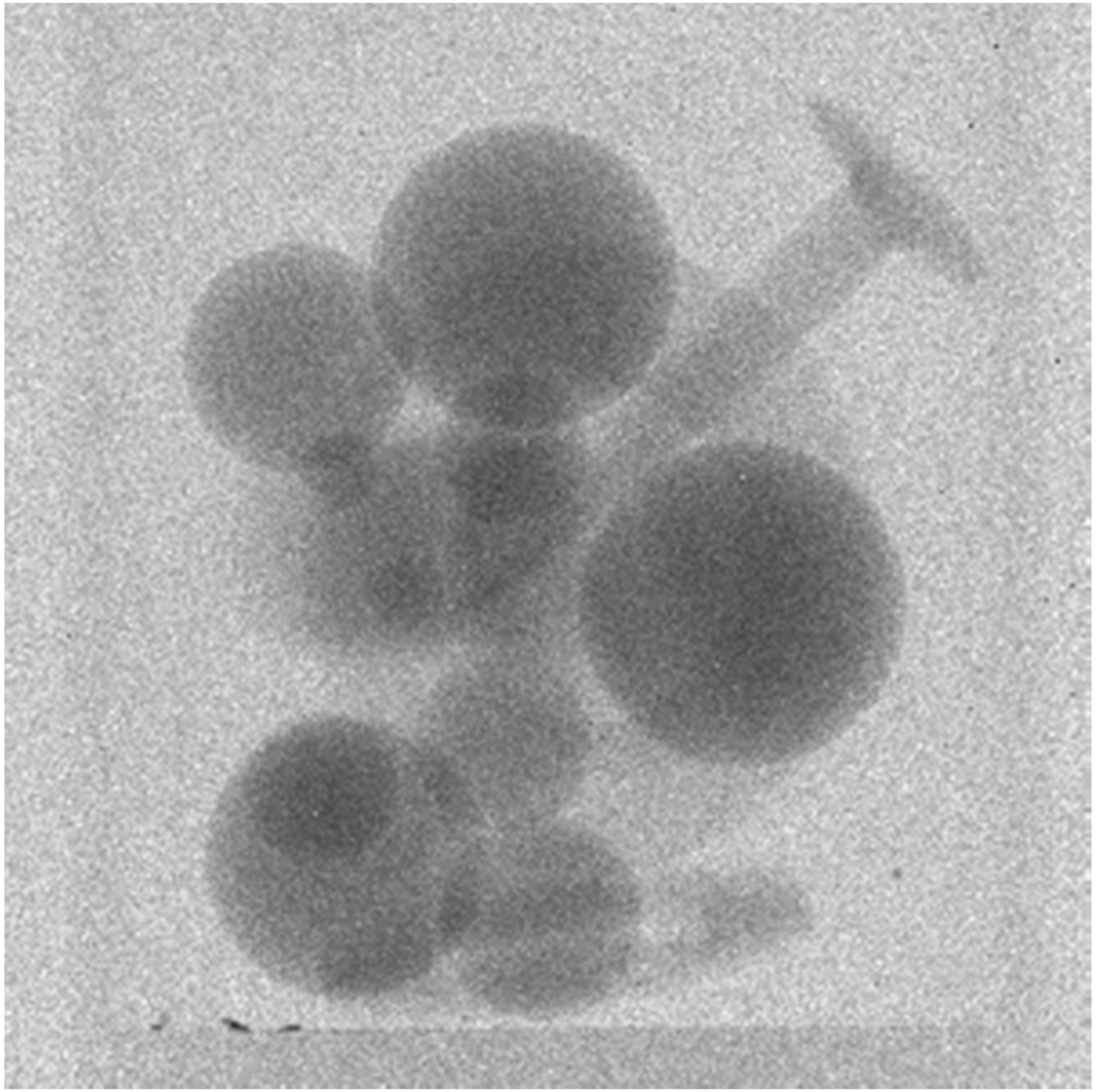


Perpendicular 1D alignment and Coulomb explosion imaging

Neutron tomography







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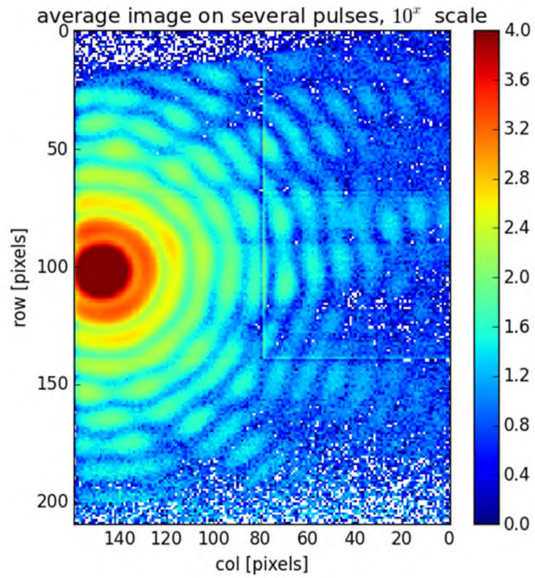
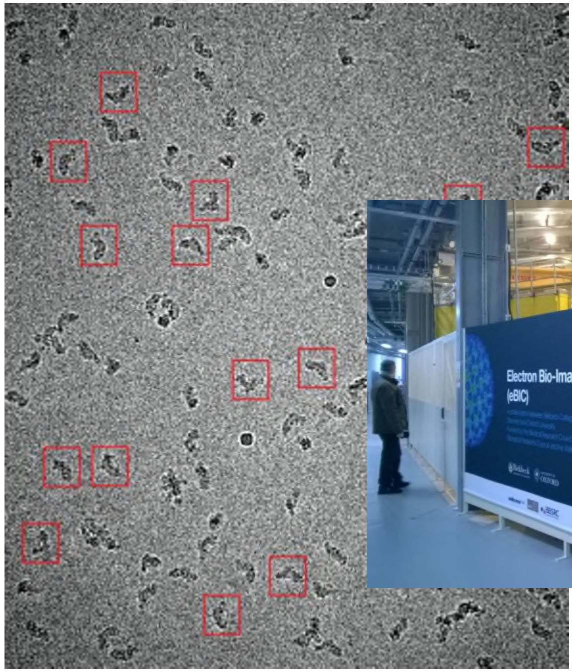
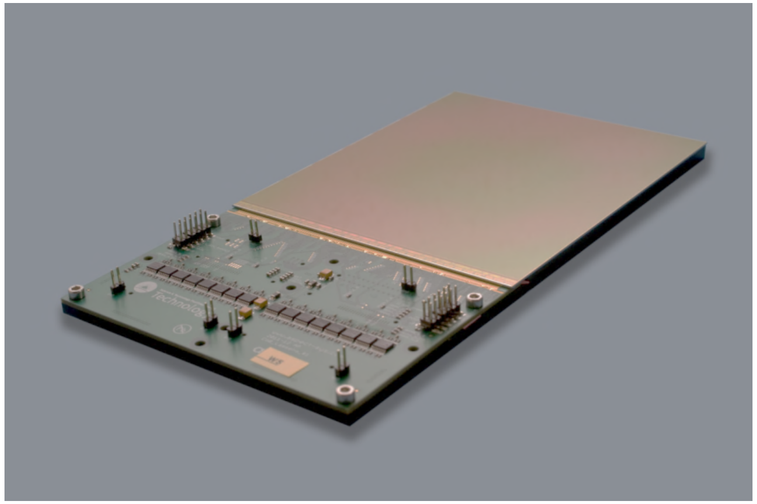
… and also







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Some numbers

Over the period 1999-2010, 61% of the wafers we manufactured were for Particle Physics projects.

Over the period 2010-2015, this ratio became 3.8%.

The size of the group has not changed in the meanwhile.

Many people who worked on particle physics projects until 2010 have since left.

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Conclusions

HR-CMOS: developing a solution for fully depleted, full CMOS pixels, based on standard CMOS Image Sensor technologies.

Development started in 2006 for Calice, and essentially stopped around 2010.

We supported the jump-start of the design for the Alice ITS and the technology is now used there.

It is also used in a variety of scientific sensors, produced for industry and other scientific organisations world-wide.

New development started for Atlas following Task Force conclusions

PRD for Future Colliders starting in June this year