CMOS: A broad overview

J. Dopke (STFC RAL)

UK community meeting on CMOS sensors for particle tracking

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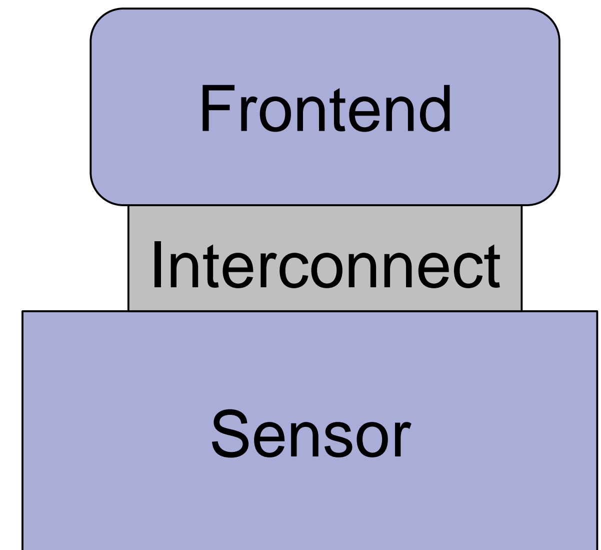
Outline

- Where we come from
- What we mean by CMOS sensors
  - Features for us
  - Features we need
- Technologies
  - Differences and commonalities
  - Fabs
- Summary

Where we come from

- High energy physics community (as well as others) very often relies on hybrid detector assemblies:
  - Two individual pieces of silicon, different feature sizes, extra handling steps for assembly
- Sensor production usually runs on special substrates
  - Limited number of suppliers
  - Production rate usually small



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CMOS sensors

Physics community seeks to tap into potential from semiconductor production:

- Current camera imaging sensors deliver 1um2 pixels for imaging purposes
  - Scientific community very often rests at the 100x100um2
- CMOS production happens in large volumes
  - Many “secure” providers
  - Large wafers used, reduces cost
- Single layer assembly makes it easier to build thin structures (down to 50um)

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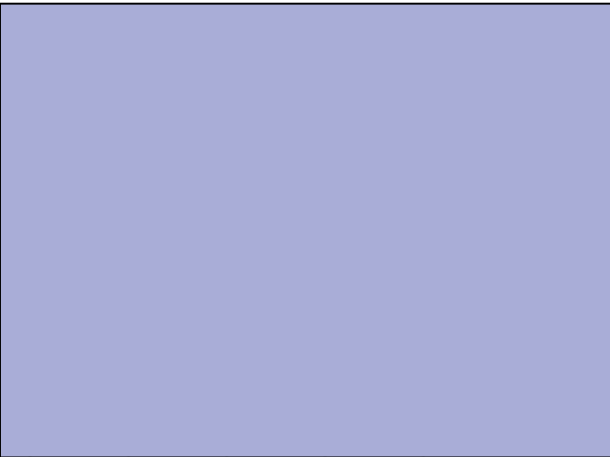
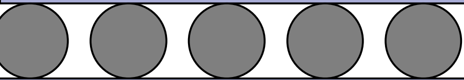
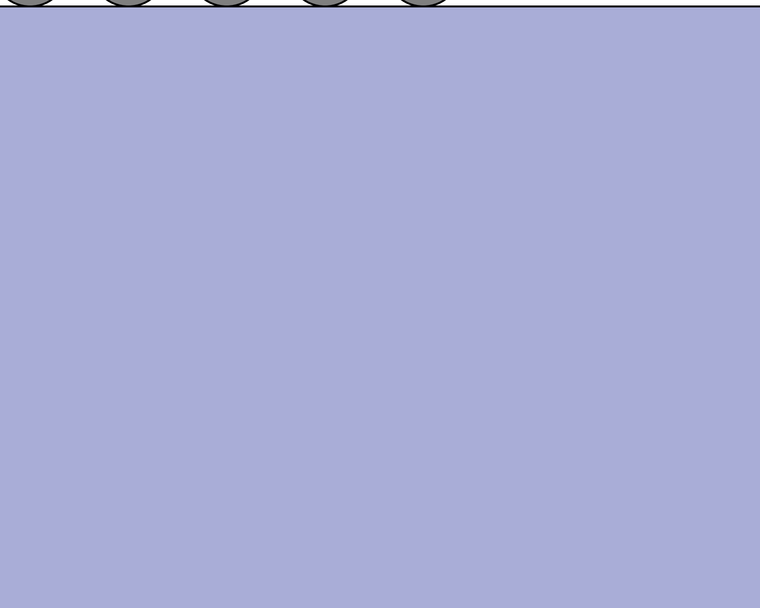
To scale







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CMOS Features

- What we already get from the imaging sensor world:
  - High resolution
  - Low noise
    - Depending on process and implementation

- What we still need:
  - Consistent (and possibly fast) timing
    - LHC based experiments need to associate measurements with bunch timing (25ns spacing)
  - Radiation hardness
    - Ionising dose resistance comes (almost) for free in (most) processes (up to O(50Mrad))
    - Bulk damage changes collection efficiency (not necessarily bad)

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Nomenclatures

- Many processes are either branded as HV or HR
  - A high voltage (HV) process can be delivered on a highly resistive substrate
  - A high resistivity (HR) process can be designed to have high voltage applied to its sensitive volume
- Processes actually differ in
  - Feature size (some allowing for full monolithic implementations - MAPS)
  - Available number of deep-wells/metals
  - Silicon base (Bulk, Epitaxial, Silicon on Insulator)
- Fabs
  - Some come with their own Multi-purpose-wafer (MPW) program
  - Some are available through Euro-practice

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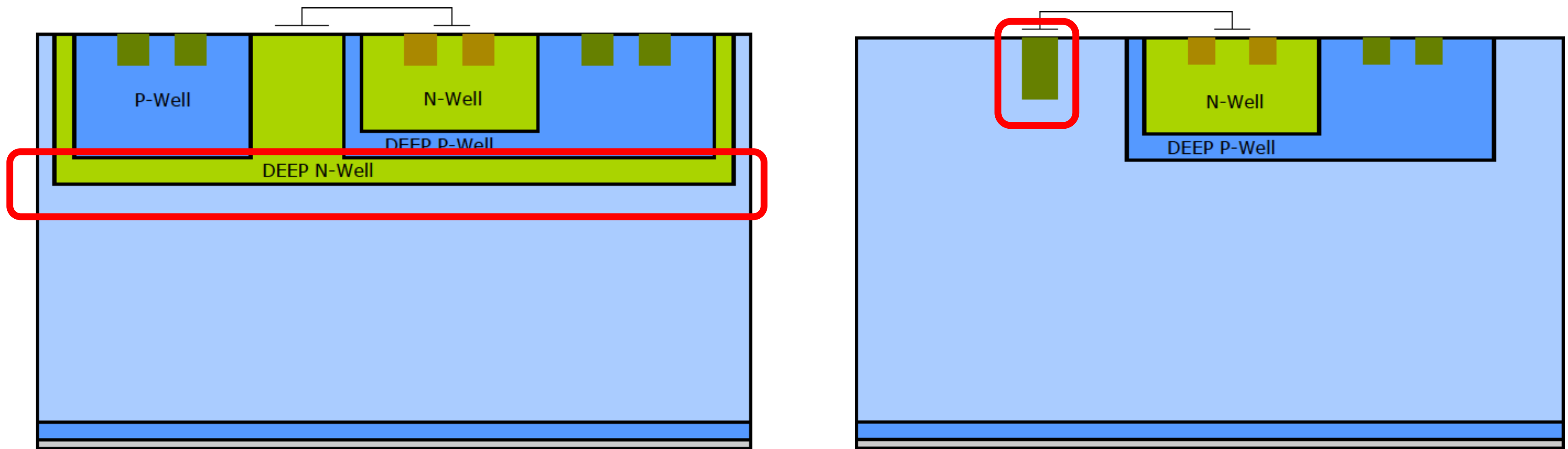
Cross-sections



- Different charge collection electrodes
  - Larger fill factor gives more rad-hardness, but larger noise
- Isolation of CMOS depends on process

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Fab List

- **AMS** (180nm/350nm, 120V design rules)
- *TowerJazz* (180nm, EPI, stitching)
- *Lfoundry* (150nm, HV design rules, stacked deep wells)
- **Global Foundry** (130nm)
- ESPROS (150nm)
- **XFAB** (180nm SOI)

These are all being looked at by various groups in Europe with partial contributions from the UK here and there

MPW through Europractice, *MPW* through foundry

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Design cycles and cost

- Design cycle time depends on
  - Availability of manpower for design **& verification**
  - Availability of MPW runs (reduced cost small size submissions for tests)
    - A submission return can take from 2 months up to … long
- Cost
  - Very much feature size dependant (scales roughly with square of inverse feature size)
  - MPW can be as low as 5k GBP for a minimalistic sample
  - Engineering runs can be as low as O(50k) and as high as O(400k) for the processes we're looking at here

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Testing requirements

- Many scientific endeavours have to operate for years under harsh conditions
  - Temperature cycles to liquid Argon temperatures
  - High radiation environment
  - Extremely long lifetime of the experiments
    - No 2-year warranty business
- Mostly untested in any of these processes hence requires extensive verification
  - Many of these tests take months to conduct (radiation hazard for transport, sheer length of heat treatments…)

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What we need

- Technology is out there, many of us (as will be shown) already touch it
- Can we save effort in a common approach to the subject?
  - Mostly to save money by seeing commonalities in development and not repeating effort, e.g.:
    Radiation testing could be a subject attacked in every submission, based on a test structure in different processes – development time is small, testing time is long but could be (largely) unified for different processes

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Summary … thoughts for the day

- What do people want with CMOS?
  - Radiation hardness always required?
- What has already been done?
  - Which processes do we fancy?
  - Which technologies show promising results?
- Where do we already have expertise?

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