



Hybrid CMOS strip detectors

J. Dopke for the ATLAS strip CMOS group
UK community meeting on CMOS sensors for
particle tracking
10.03.2016, Cosenors House, Abingdon

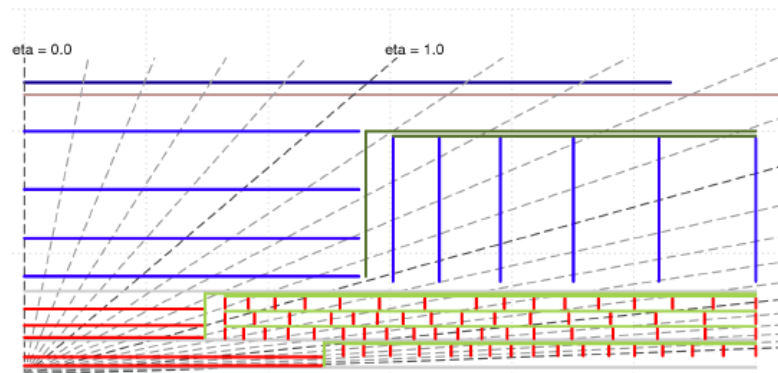
Outline

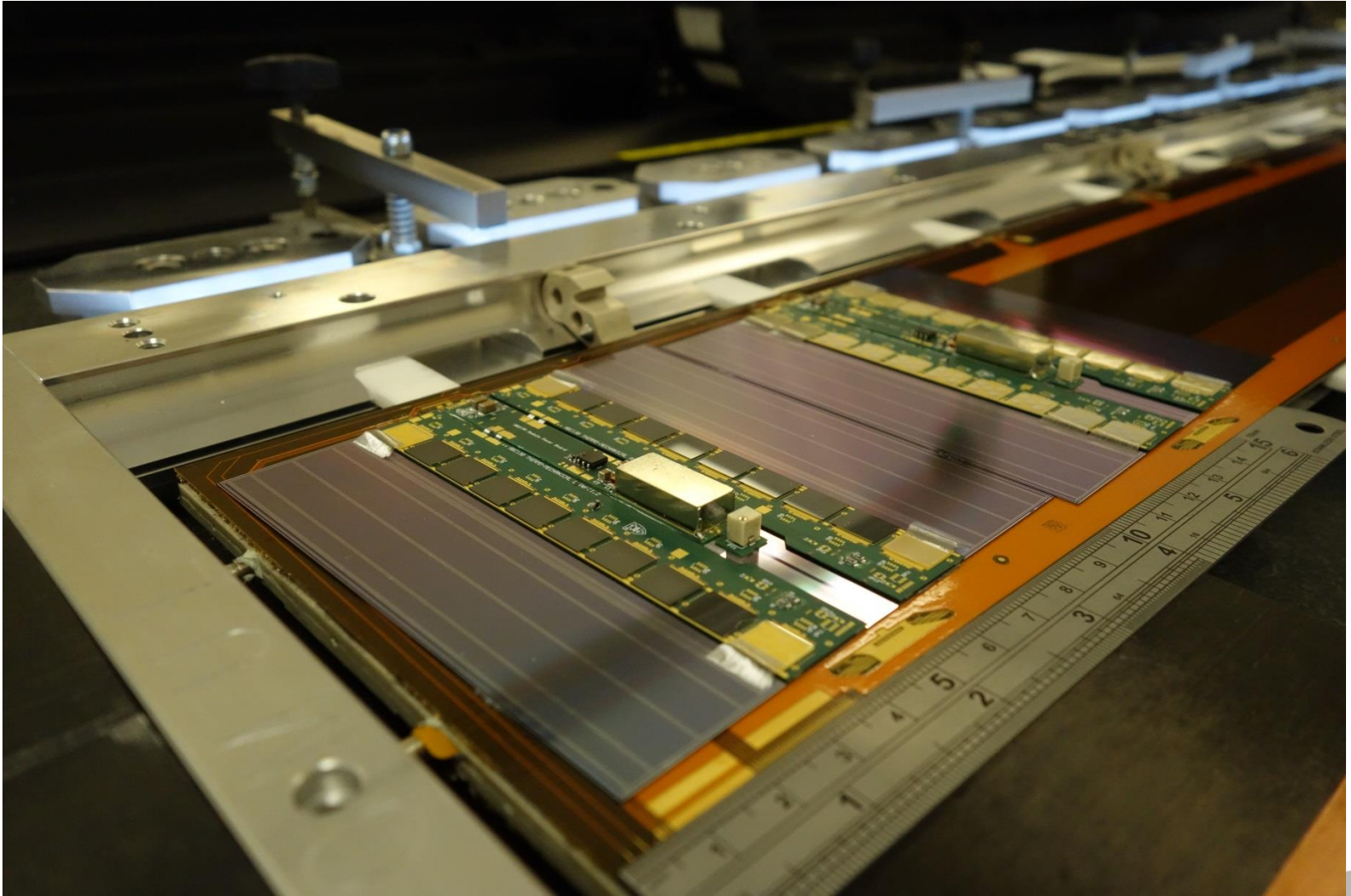
- ATLAS Strip Tracker Upgrade
- CHESS Project outline
- Development lines and current status
 - HVStripV1 and HV-CHESS-1
 - HR-CHESS-1/OverMOS
- CHESS-2 status
- Summary



The ATLAS strip tracker upgrade

- ATLAS tracker upgrade planned for the HL-LHC
- All Silicon tracker
 - 5 Barrel Layers of Pixels
 - 4 Barrel Layers of Strips
 - 6 Strip Endcap disks per side
 - O(1 Million) pixel rings per side
- Strip tracker is now based on double sided carbon fibre supports (thermo-mechanical as well as electrical)
- 14+14 strip modules to be mounted on these two sides with a stereo angle between them
 - Allows z-coordinate measurement
- In total about 200sqm of Silicon surface in strips alone!





CHES Project Outline

- Investigations on possible suitability of CMOS for an ATLAS strip tracker to be used with the HL-LHC started ~2.5 years ago
 - Non-disruptive: The baseline program should not have to adapt to a CMOS implementation
 - No need for major design changes, all support mechanics and most of the readout electronics should still be usable
- Conclusion was a 3 year program for “CMOS HR/HV Evaluation for Strip Sensors” (CHES)
 - 3 Quick submissions
 - Break points every year
- Currently the program is in its second year



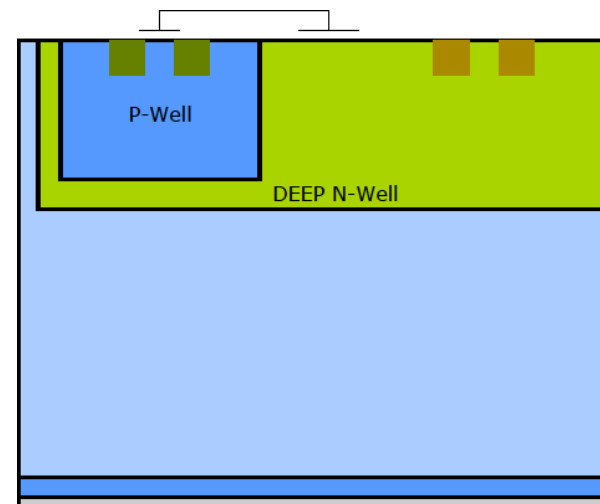
Development Lines

- The program is evaluating two different approaches to CMOS sensors for a strip tracker implementation
 - An imaging fab approach (high resistivity)
 - An automotive approach (high voltage)
- Both will eventually be using bias voltage and evaluate high resistivity substrates, but Fabs are set up differently:
 - HR is based on an epi layer defining charge collection depth
 - HV is based on a backside bias which generates the collection depth



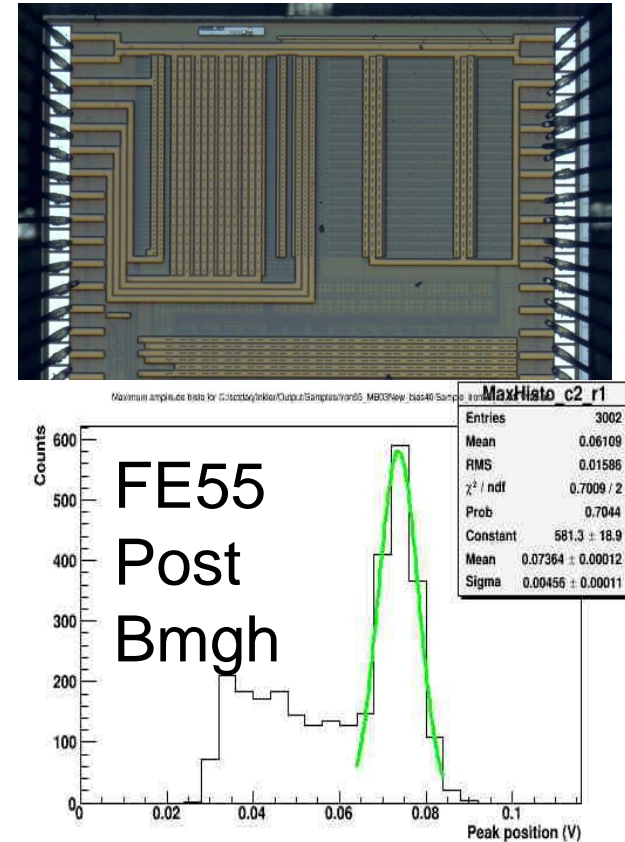
HV line

- Based on AMS 350nm HV process
 - 120V design rules, 4 metal layers
- Initial submission was a strip test chip, HVStripV1:
 - Few simple test structures: transistors, diodes, passive pixels
 - Active (Sub)Pixels for a strip geometry
 - 40x400um dimension
 - Preamp per pixel (two different types)
 - Standard comparator
 - Time-walk compensated comparator
 - Analog output
 - Digital readout bus for two hits per 25ns
- Was submitted before the program even started (Thanks to I. Peric, KIT, Germany), back in hand August 2014



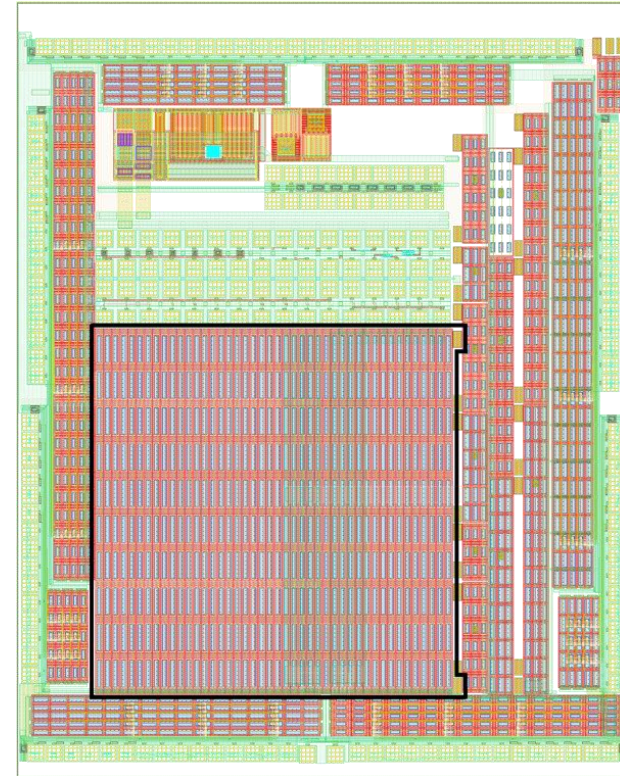
HVStripV1 results

- Tests were performed on passive diode array, as well as active structures
 - All structures were functional after adequate ionising/neutron dose (and even after Birmingham)
 - Depletion depth at fixed bias voltage increases during neutron irradiation
 - Initial diffusion peak is quickly removed, charge collection timing is good



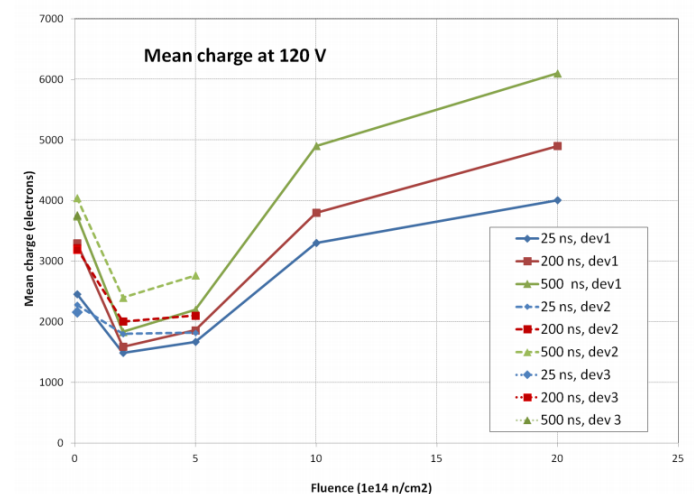
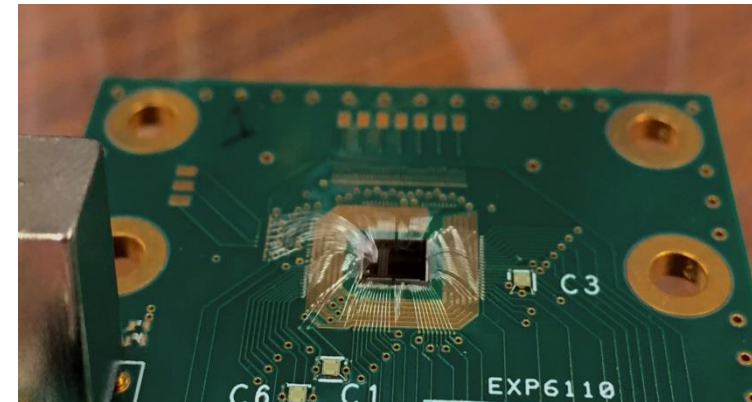
HV-CHESS-1

- Design outline
 - Active pixel arrays of different size
 - 40x100 – 40x800, different fill factors
 - Passive pixel arrays of different size
 - Edge-TCT array
 - Large diode for source measurements
- Submission mid August 2014
- Delivery end of October 2014



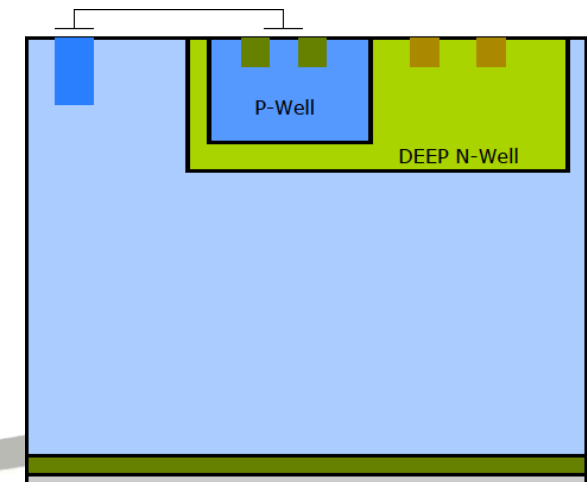
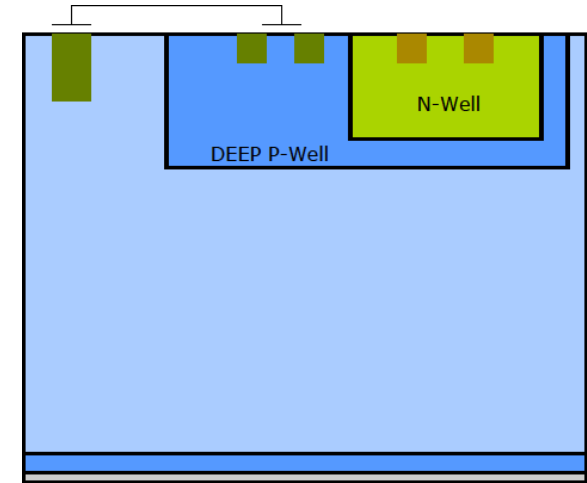
HV-CHESS-1 results

- Initial tests done on bare chips
- Neutron irradiation shows acceptor removal: increase in substrate resistivity leading to larger depletion – chips get better over neutron Dose!
- Gamma irradiation showed good results for amplifier characteristics:
 - Chips need recalibration
 - Timewalk needs to be tackled
- Some test results were not quite understood – Foundry met with us and answered our questions! (Try that with others)



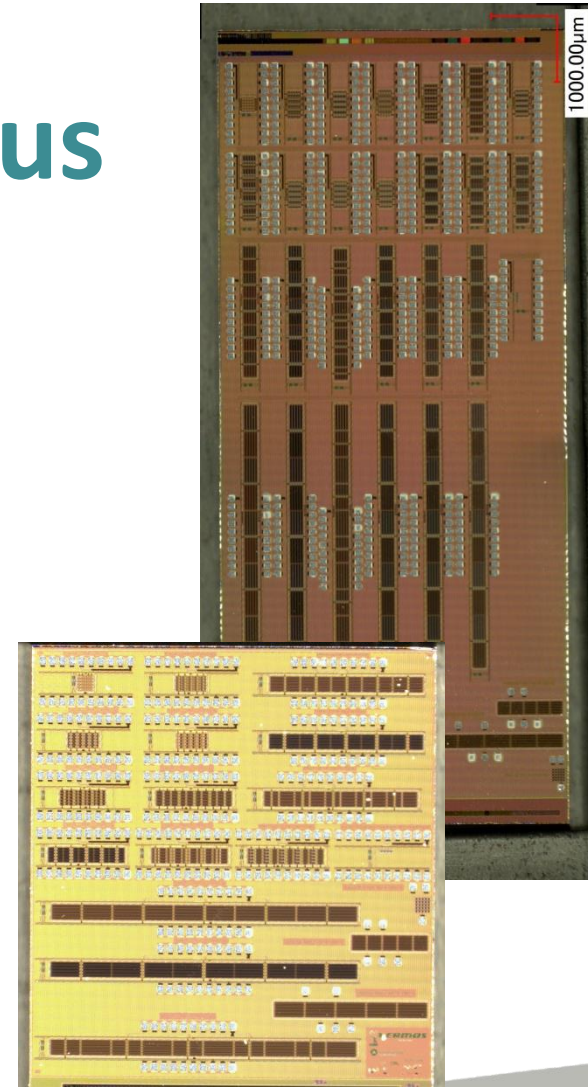
HR-CHESS-1/OverMOS 1

- Design outline
 - Different substrates
 - Depletion mode changes
 - Collected charge changes
 - Different sized arrays
 - Different collection diode structures
 - Passive pixels for (Edge-)TCT measurements
- Effort funded through STFC CFI, submission funded through ATLAS collaborators
- Submission in November 2014
- First samples left foundry early May 2015
 - Final Wafers arrived just before Christmas last year



HR-CHESS-1 status

- Control wafer from the Fab had issues:
 - Deep P-well was missing
 - Otherwise functional chip
- Other wafers took a long time to come through, but are now all in hand
- Initial tests showed functional amplifiers as well as reproducible charge collection from Laser injection
 - Sadly independent of injection position within an array, all pixels respond, turns out to most likely be a problem with missing P-stop between collecting terminals



CHES-2 Status

- The program is coming towards the end of its second year this summer
 - HV-CHES-2 (a large functional prototype) is about to be submitted in AMS 350nm
 - Changes in amplifier design with experience from HV-CHES-1
 - Crosstalk and timewalk are still to be studied on these larger structures
 - HR-CHES-2 is at the schematic/simulation stage and got important feedback from the first submission as well
- Working on plans for building “a module”
 - An object that could replace a strip module



Summary

- Very good progress made towards an ATLAS implementation for an HL-LHC strip tracker based on CMOS active sensors
 - Hybrid approach to reduce the effort needed in the sensor design itself and thereby make it fast
 - Memory/time-tagging circuitry to sit outside, different feature size, all digital circuit
- Cost reduction for silicon production
- Vastly reduces sensor radiation length (less multiple scattering)
- Hopefully better resolution
 - Detector also allows for simple pattern recognition: Large R track seeding much simplified

