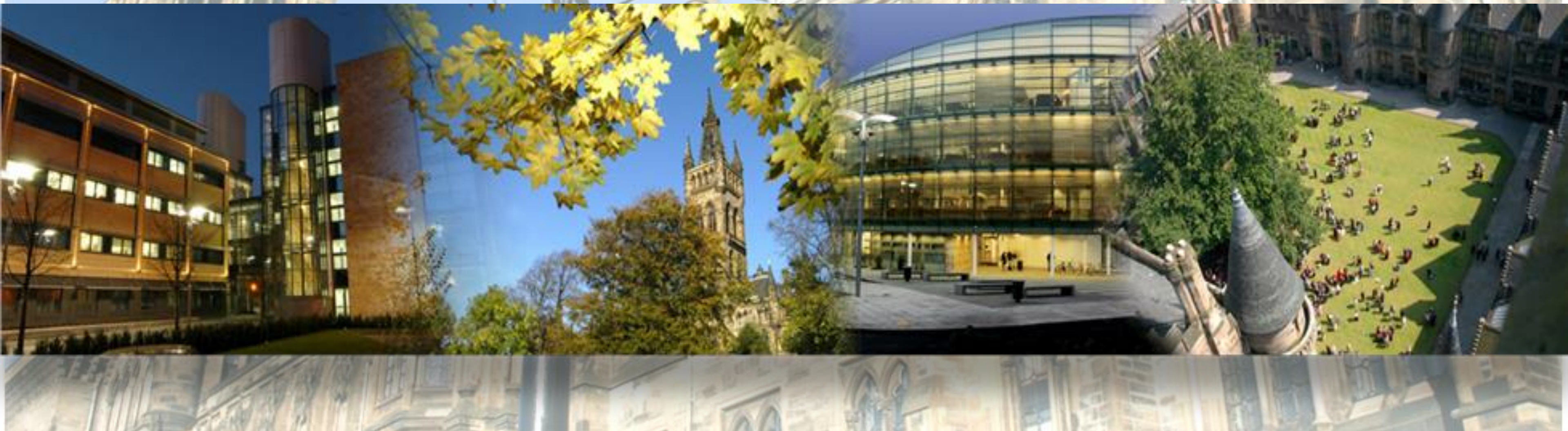
University of Glasgow | Department of Physics & Astronomy

CMOS Hybrid pixel detectors

Richard Bates & Dima Maneuski



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Contents

- Motivation for hybrid CMOS
- Assembly

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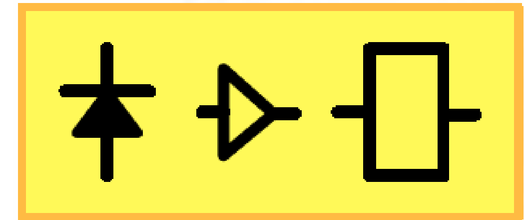
CMOS designs

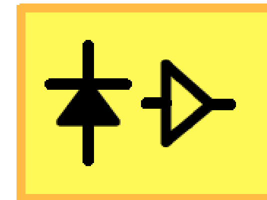
Tomasz Hemperek, ACES, 8th to 10th March 2016

- Depleted Monolithic Active Pixel Sensor
  - HR-material (charge collection by drift)
  - Fully depleted MAPS (DMAPS)

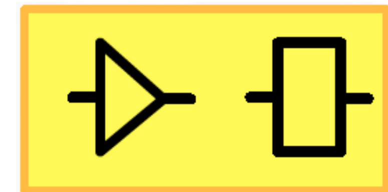


Diode + Analogue + Digital

- Hybrid Pixels with Smart Diodes
  - HR or HV-CMOS as a sensor (8”)
  - Standard FE chip
  - CCPD (HVCMOS) on FE-I4

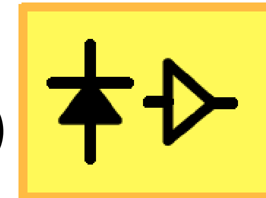


Diode + Analogue

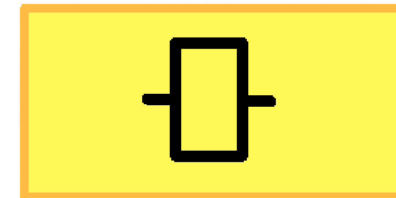


Standard FE (A + D)

- CMOS Active Sensors + Digital R/O chip
  - HR or HV-CMOS sensor + CSA (+Discriminator)
  - Dedicated “digital only” FE chip

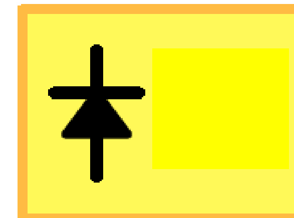


Diode + Analogue

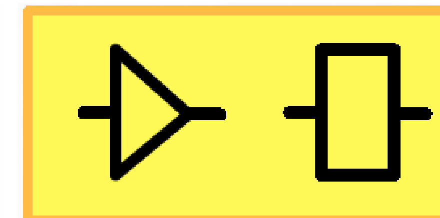


Digital FE

- Passive CMOS Sensor + R/O chip
  - HR or HV-CMOS sensor
  - Dedicated FE chip
  - Low cost C4 bumping and flip-chip



Diode



Standard FE (A + D)

Hybrid CMOS Motivation over planar

- Reduced material
  - CMOS active area is thin
- Sensor Cost
  - CMOS sensors cheap compared to 6-inch FZ planar
- Flip-chip cost
  - Capacitive coupling reduces complexity of interconnect
- Lower Analogue power
  - Capacitive load of pixel reduced
- Less cooling requirements
  - Post-irradiation operation at higher temperatures

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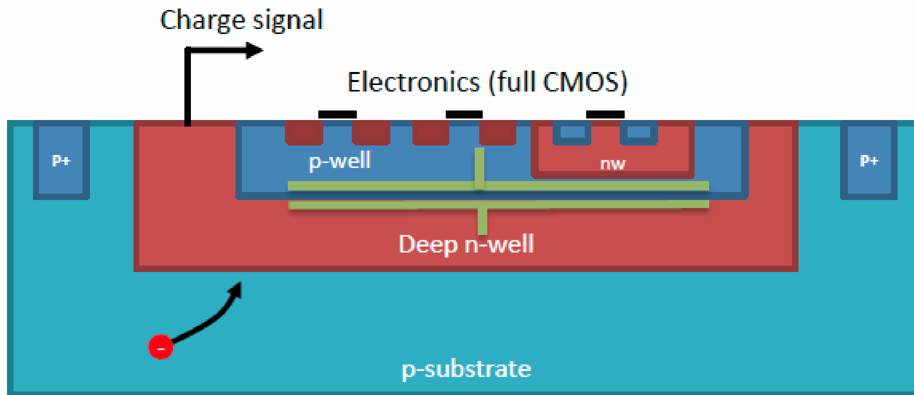
Why not Monolithic?

- Separation of analogue from digital circuitry
  - Better analogue performance
- Build flexibility
  - Smaller sensor pixels that ROIC pixels
    - Use signal size to encode position
  - Large area CMOS with small ROIC footprint
    - The strip sensor shown before but with smaller pixels
- Electronics flexibility
  - Full ROIC CMOS in smallest node
  - Maximum functionality of digital side
- Higher fill factor and more uniform response

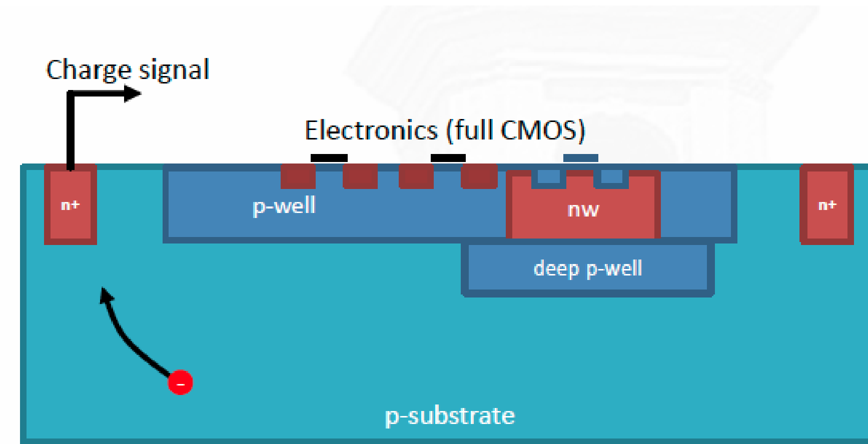
Process options

Electronics inside charge collection well



- Collection node with large fill factor -> rad. hard
- Large sensor capacitance (DNW/PW junction) -> X-talk, noise & speed (power) penalties
- Full CMOS with isolation between NW and DNW

Electronics outside collection well



- Very small sensor capacitance -> lowest power
- Potentially less rad. hard
  - longer drift lengths
- Full CMOS with additional DPW

Larger capacitance makes it more difficult for the readout

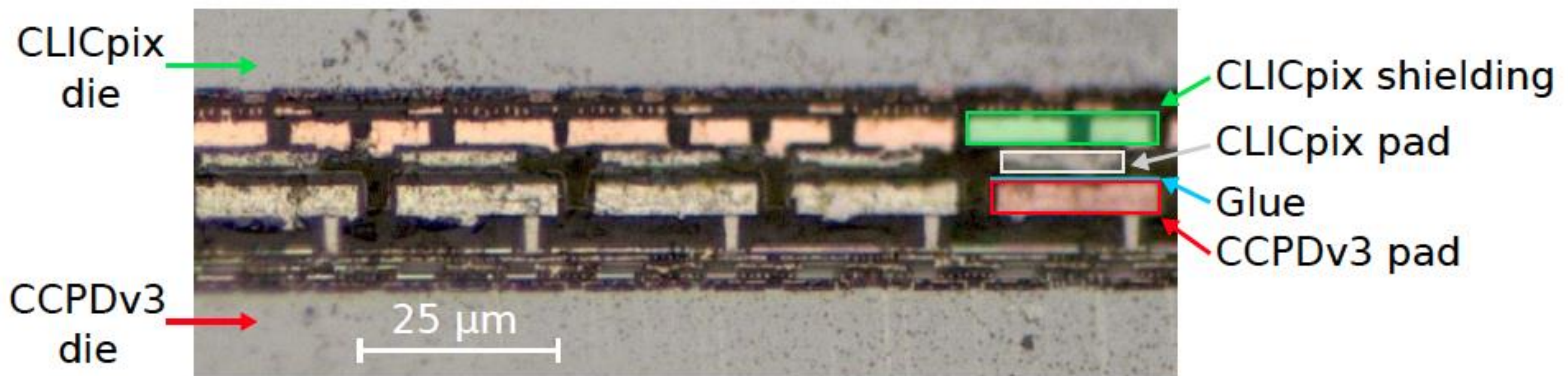
Assembly

- Simply glue the two together
- Control the glue thickness
- Direct bonding
  - Wafer-to-wafer copper-to-copper bond
- The DC connection for power

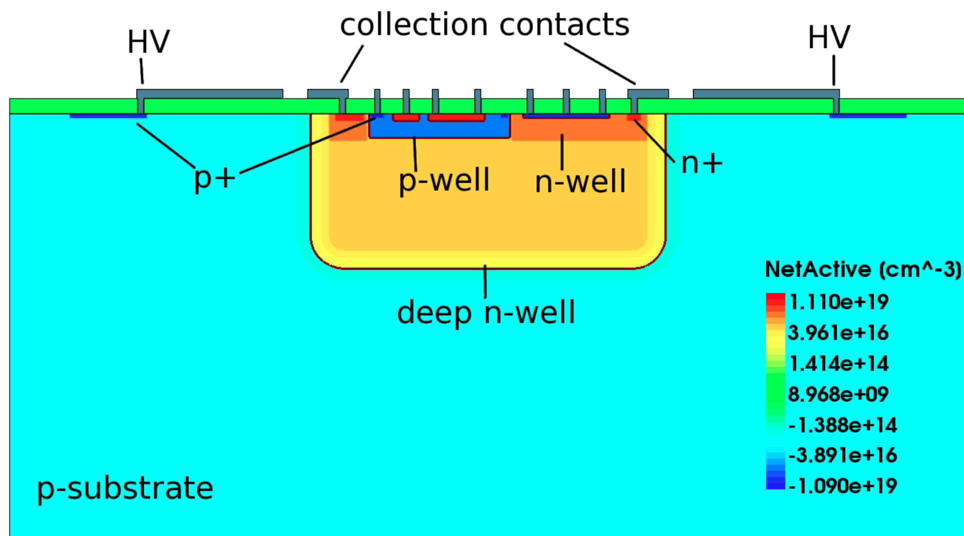
Glue CMOS sensor to ROIC

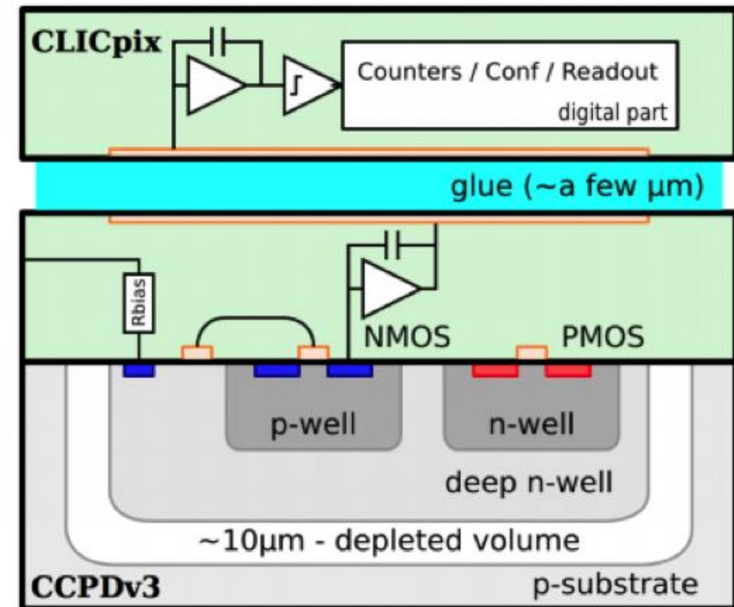
N. Alipour Tehrani, VCI 15th to 19th Feb 2016, Vienna, CLICdp collaboration

- Simple glue layer between ROIC and CMOS sensor
- Use a flip-chip machine to align and flip-chip the die
- Output of the CMOS is capacitively coupled to the ROIC
  - No expensive bump bonds
  - Still needs die to die flip-chip
- Control can be capacitively coupled
- Still require DC power connections



CMOS for CLICpix

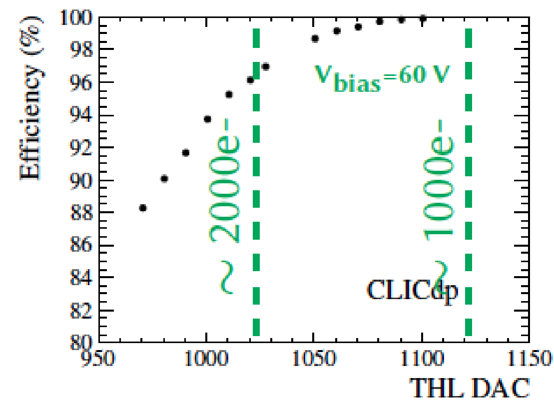


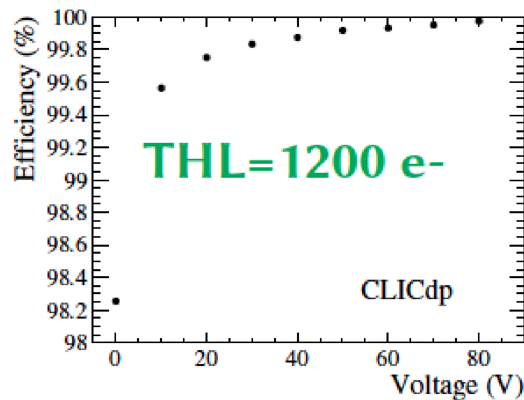


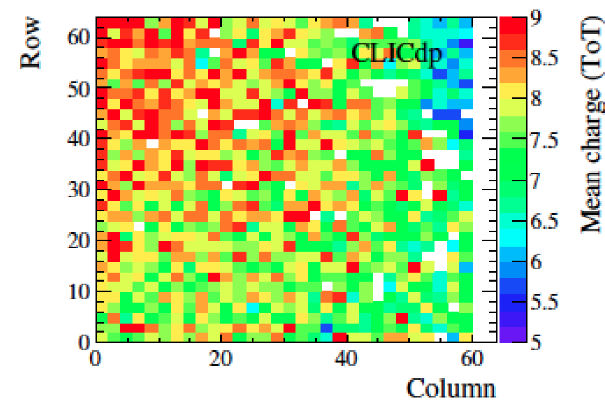
- CCPDv3
- Deep n-well collects charge
  - Shields electronics from substrate -> prevents charge loss to electronics well
- 180nm HV-CMOS process
- Two-stage amplifier in each pixel -> T_{peak} = 120 ns

Results – Cap coupled CLICpix

- Test-beam at CERN SPS (EUDET/AIDA telescope)
- High Detection efficiency (even without Sensor bias)
- Non-uniformity of glue thickness visible in variation of the measured mean charge (ToT) across the matrix
- ~ 6 µm single-point resolution







- Demonstrated AC coupled HV-CMOS smart sensor
- CLICpix2 readout and CMOS sensors under development

SU8 pillars to control glue thickness

A. Gaudiello, Trento Workshop, 22nd to 24th Feb 2016, INFN

- Better control of glue thickness over large area device

Basic process

Spin SU-8 photoresist
Pattern pillars by mask

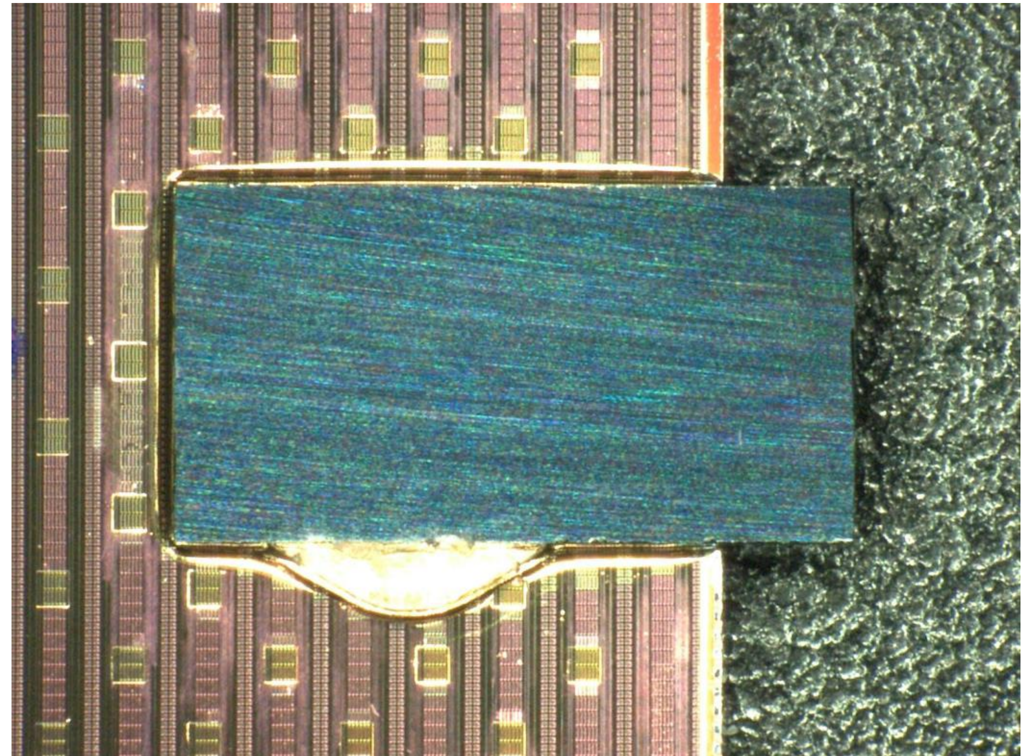
Glue deposition

Align & pressure

Deposition of SU8
photoresist by spinning

Credits: Giovanni Darbo

- Single chip assemblies
  - Glue and SU8 spacer
  - Pillar height ~ 5 µm
  - Device thickness Stdev = 0.6 µm



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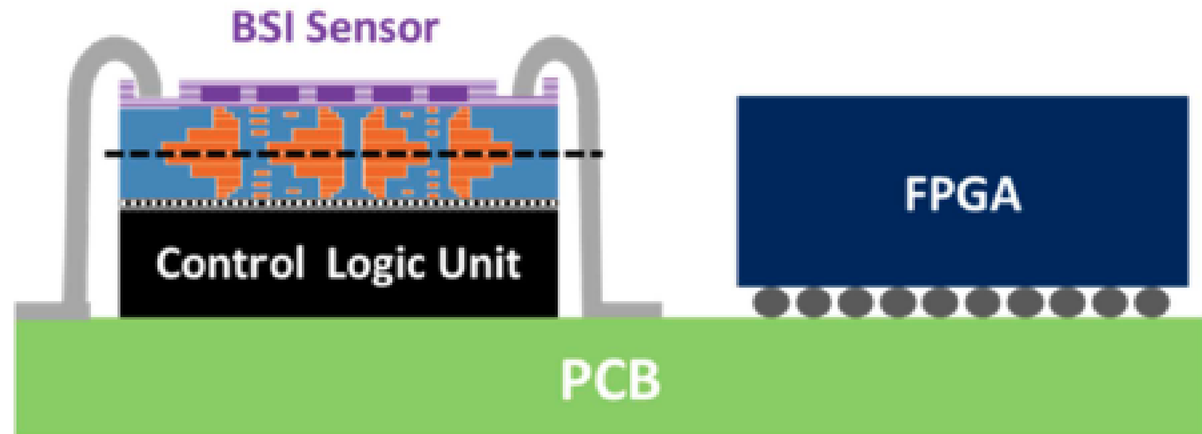
Wafer-to-wafer bond

- Preferred solution for back-illuminated visual CMOS in the modern world

ST Microelectronics & CEA LETI
- - - - bond line between CMOS sensor and ROIC



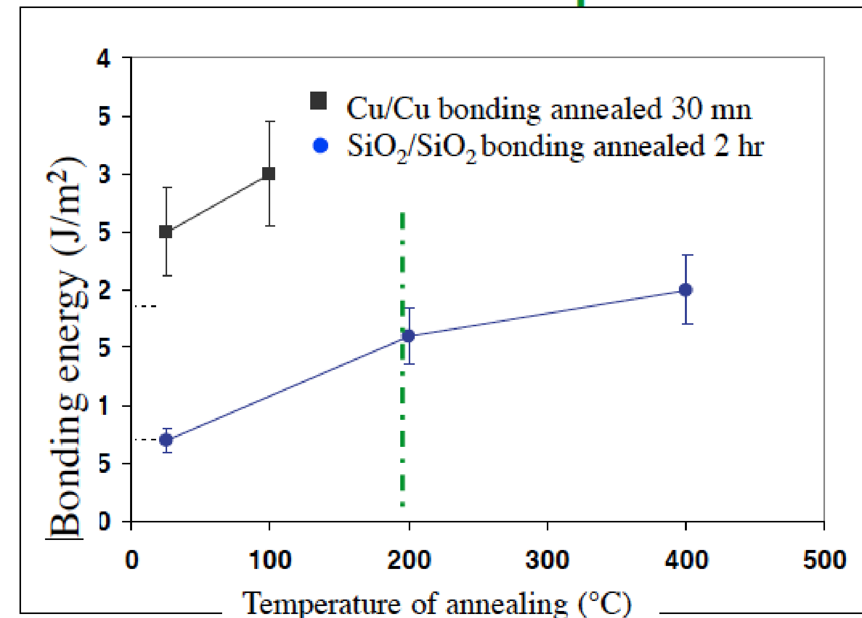
Sony http://www.sony.net/SonyInfo/News/Press.201201/12-009E
ST L. Benaissa et al., “Next Generation Image Sensor via Direct Hybrid Bonding”, EPTC proceeding, 2015

Direct copper to copper bonding

- Wafer level process
- Room temperature process
  - Moderate post bond anneal (200-400C)

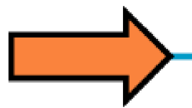
Process

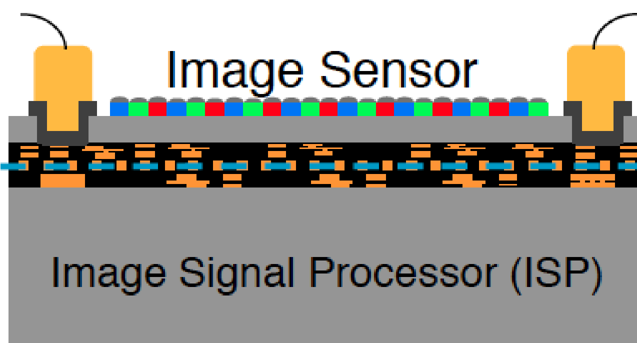
- Copper deposition and oxide growth
  - Copper for metallic conductive bonds
  - No glue or solder required
- Chemical mechanical polish of surfaces
  - Surface roughness RMS ~ 0.5 nm
  - Wet clean / Plasma clean
  - Ion beam surface activation
- Wafer alignment
  - x/y better than 400 nm
- Contact wafer and bond forms
- Anneal to recrystallize copper over bond
  - Increase bond strength – removes bond interface
- Treat bonded device as single wafer
  - Thin CMOS to 10 µm thickness
  - Add TSV last as required



Copper direct bonding

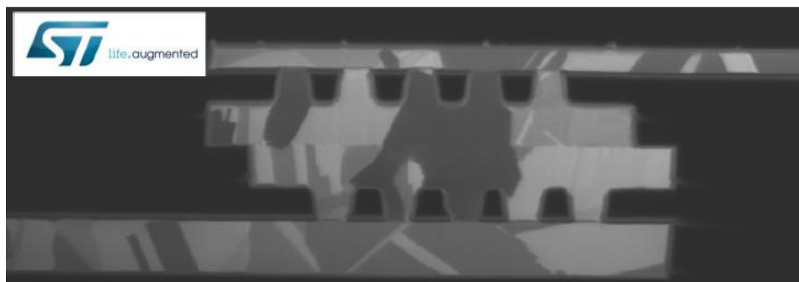
Hybrid bonding interface



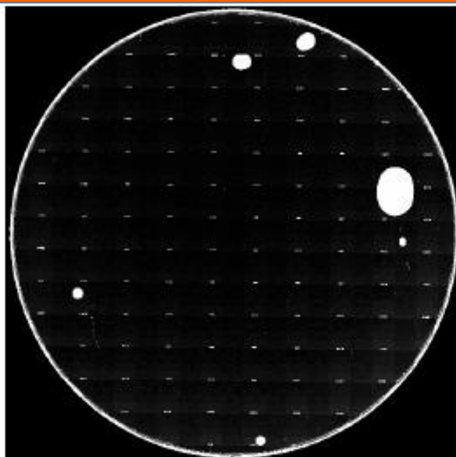


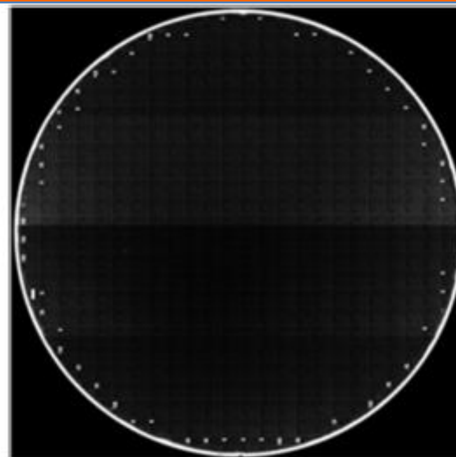
R. Taïbi et al., “Full characterization of Cu/Cu direct bonding for 3D integration”, EPTC proceeding, 2010, pp. 219-225

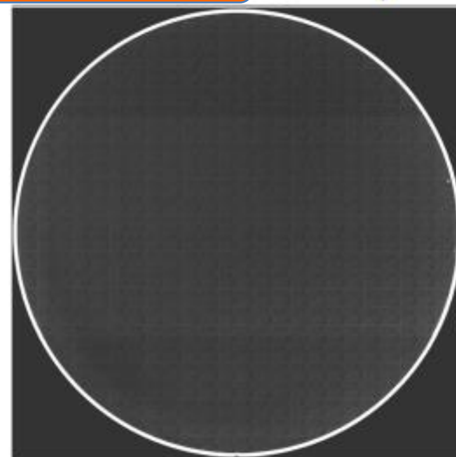
Cu-Cu bond.
Cu crystal growth removing bonding interface



SAM image – improving wafer bond quality: white – void/ black -bond



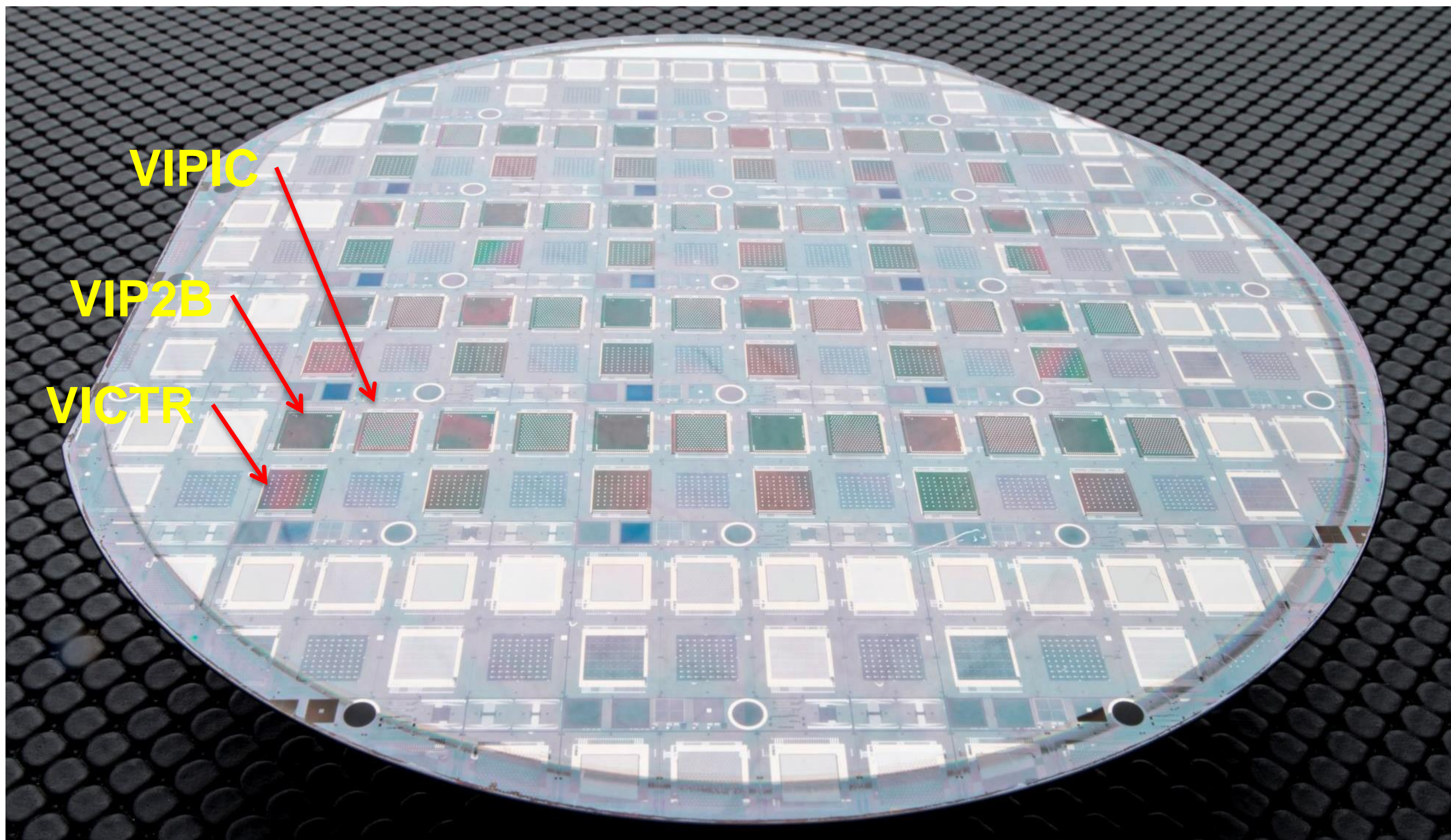




8-inch FZ with pixel ROICs direct bonded

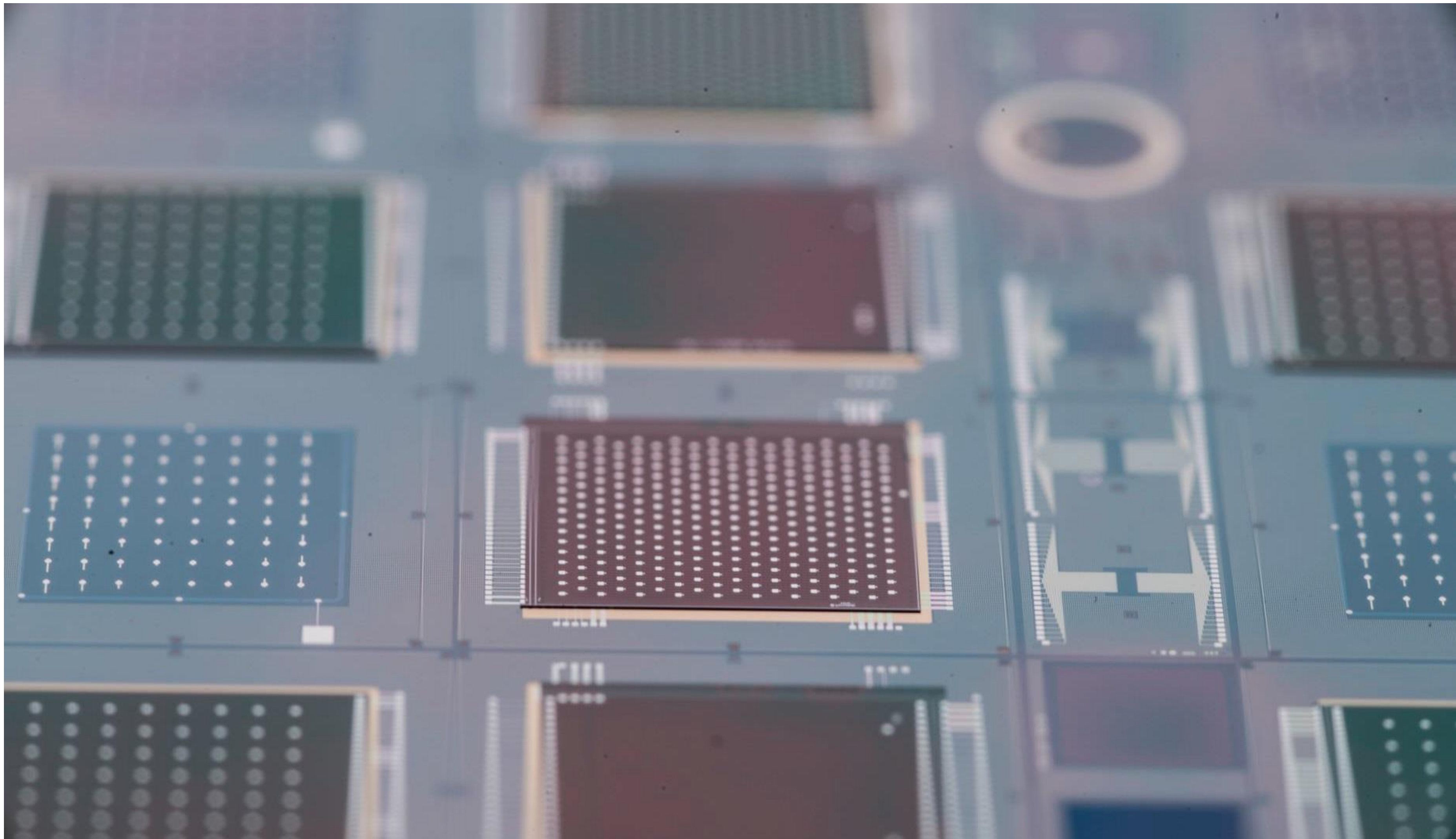
Ray Yarema, CMOS workshop, Sept 15th to 17th 2014, Bonn, FNAL

Bonded with Ziptronix Ni-DBI (Oxide-Oxide Fusion bonding)



VIPIC

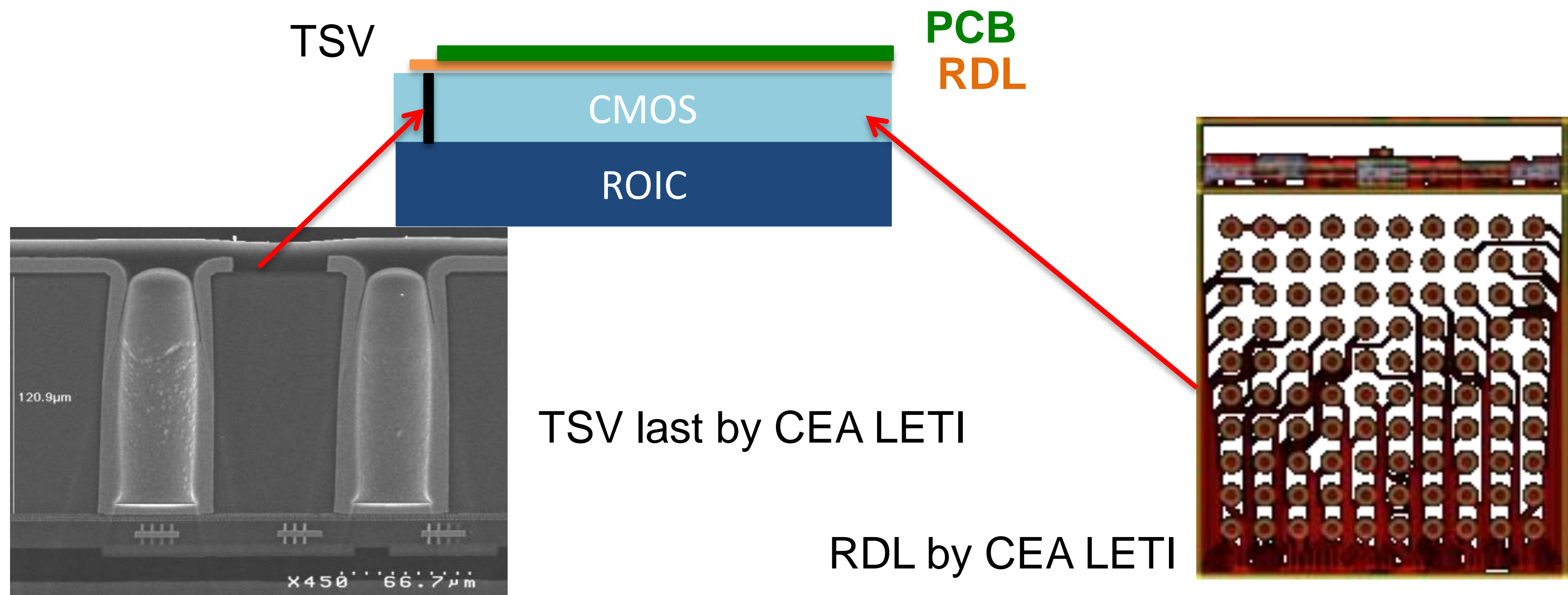
VIPIC is 34 μm thick and has bonding pads on its back to connect to PCB



The DC power connection

- Power via the back of the CMOS/ROIC
  - Through Silicon Via, TSV
  - TSV last for ROIC – Aspect ratio of 3:1
  - Via middle possible for CMOS – 2 µm vias possible

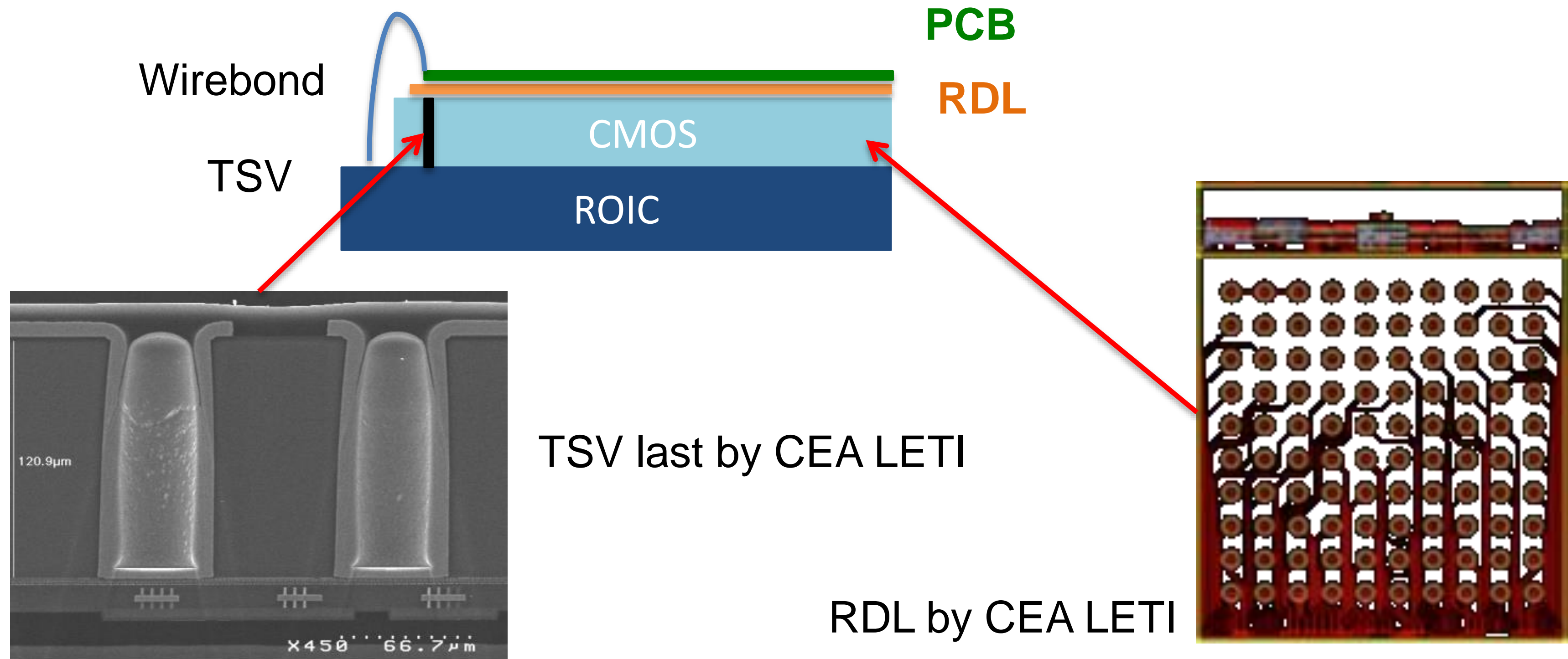
Electrical DC connection between die. TSV on one side



The DC power connection

- Power via the back of the CMOS/ROIC
  - Through Silicon Via, TSV
  - TSV last for ROIC – Aspect ratio of 3:1
  - Via middle possible for CMOS – 2 µm vias possible

AC connection between die. TSV on one side, wire bond the other



The DC power connection

- Power from the front of the CMOS/ROIC
  - Traces on one chip powers both chips
  - Conductive glue used for DC connection for power only