STEP-by-step manufacturing of ULSI CMOS technologies

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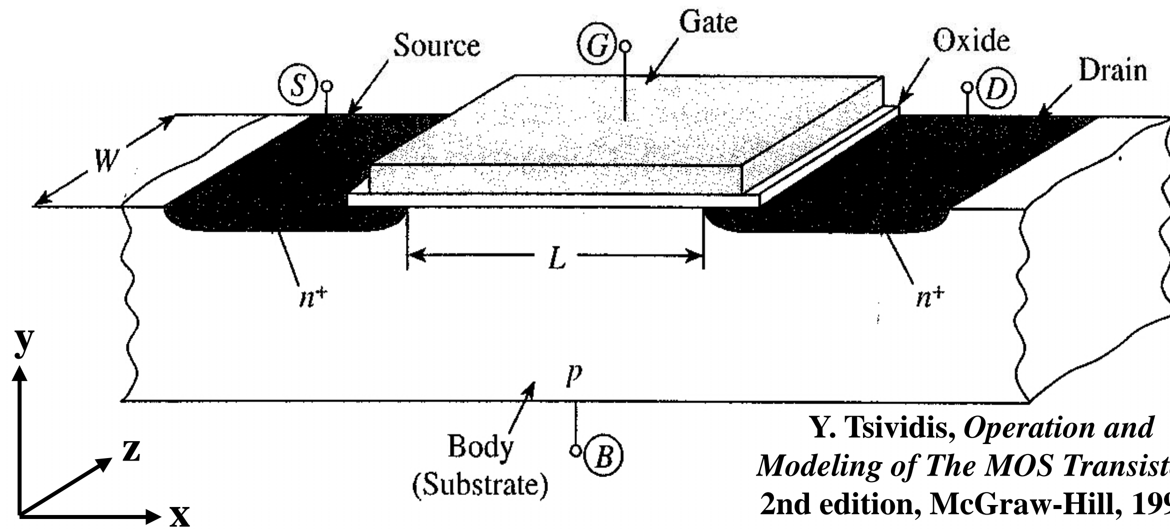
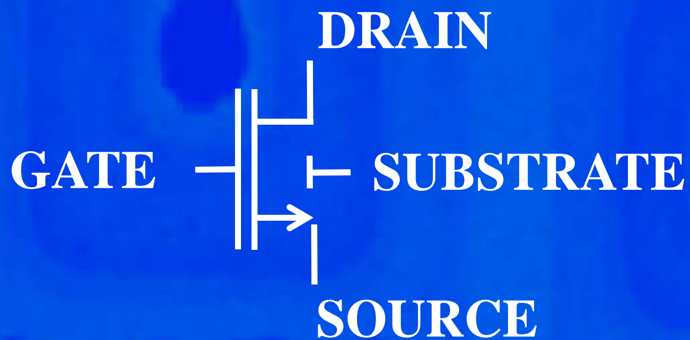
Outline

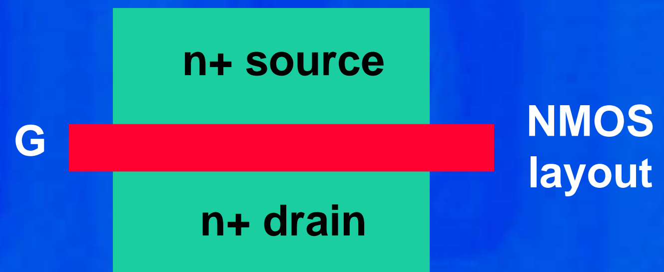
- ✓ Foreword
- ✓ Moore's law
- ✓ Manufacturing of ULSI CMOS technologies
  - Fundamental manufacturing operations
  - Process Flow
    - Front End Of Line (FEOL)
    - Back End Of Line (BEOL)

Foreword: the MOS transistor

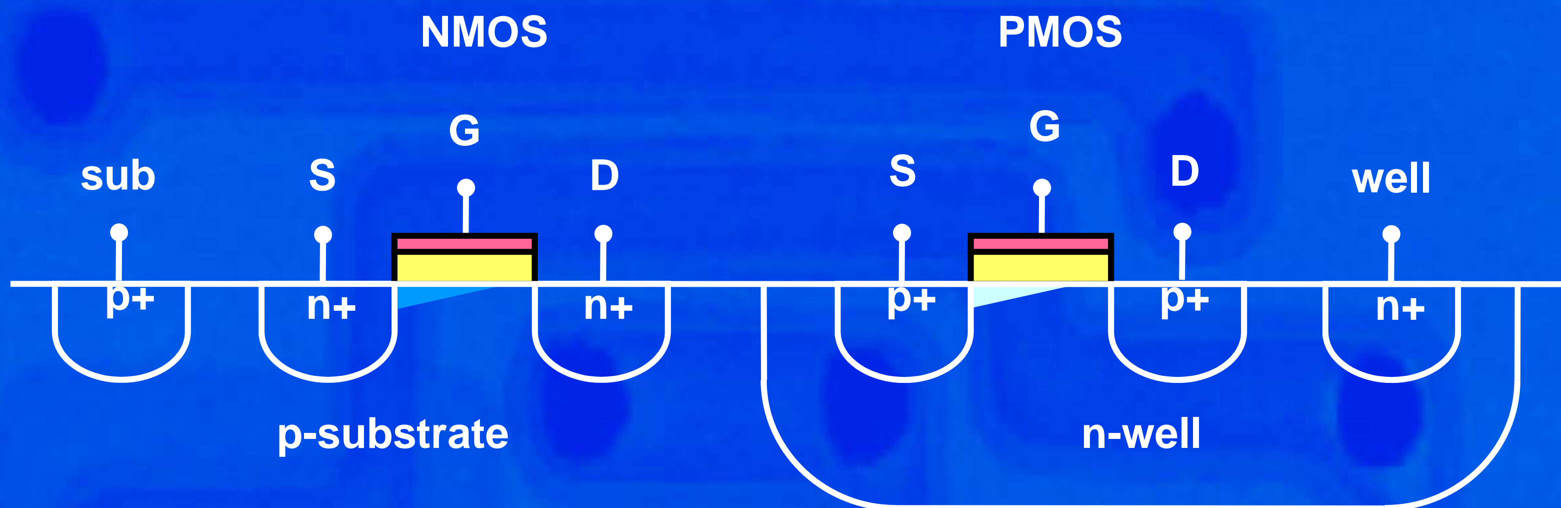


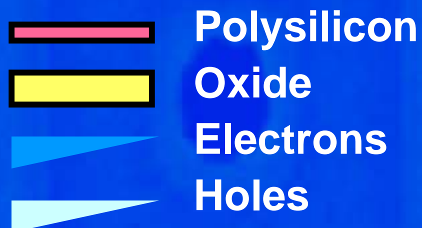
Y. Tsividis, *Operation and Modeling of The MOS Transistor*, 2nd edition, McGraw-Hill, 1999, p. 35

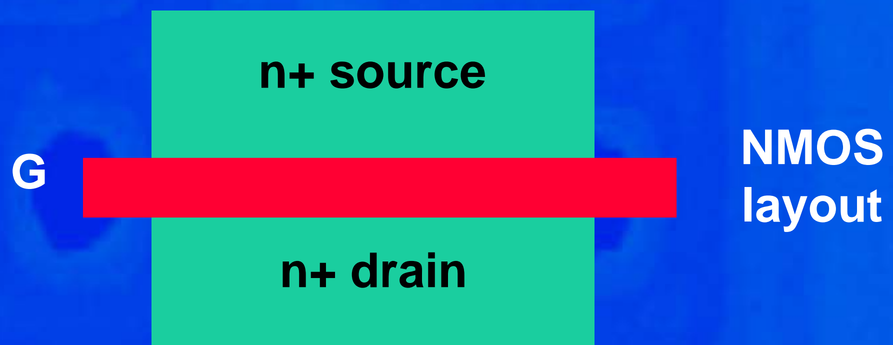




Foreword: CMOS technology



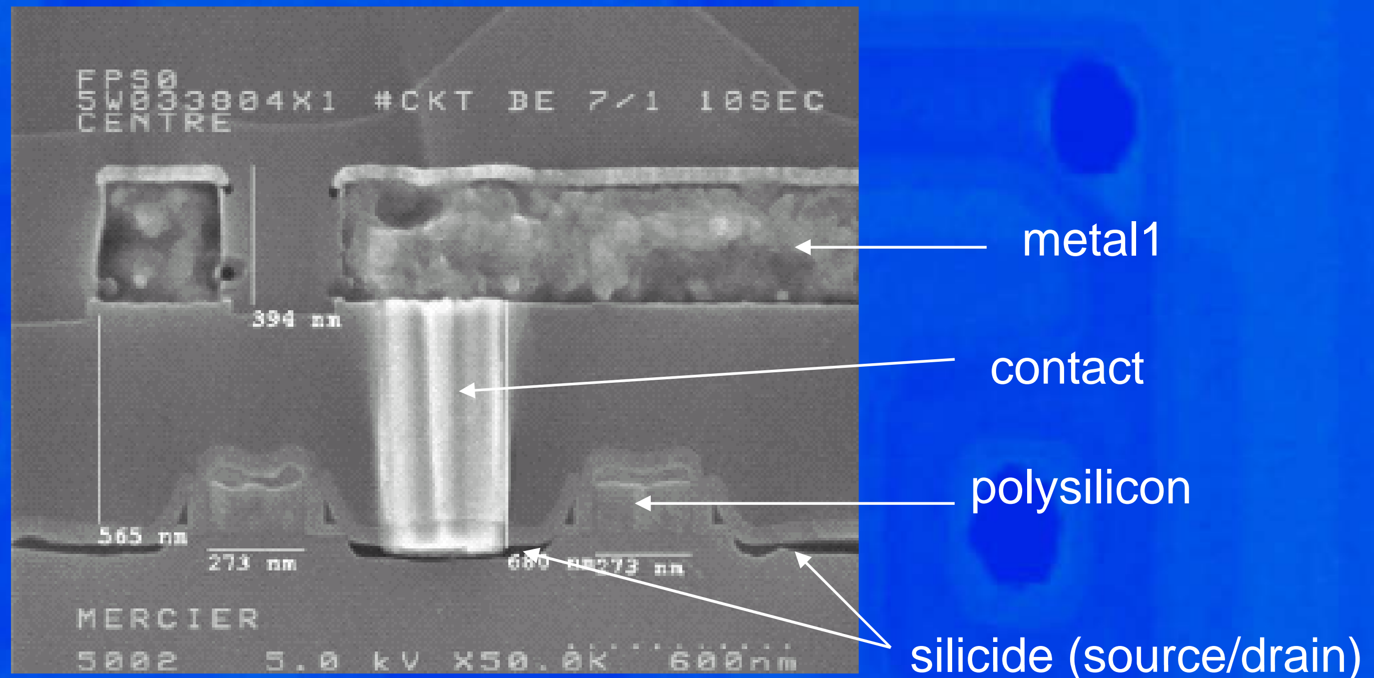




NMOS layout

Foreword: CMOS technology

- ✓ SEM (Scanning Electron Microscope) image of transistors



ULSI technologies: manufacturing

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Moore's law

1965: Number of Integrated Circuit components will double every year

G. E. Moore, "Cramming More Components onto Integrated Circuits", *Electronics*, vol. 38, no. 8, 1965.

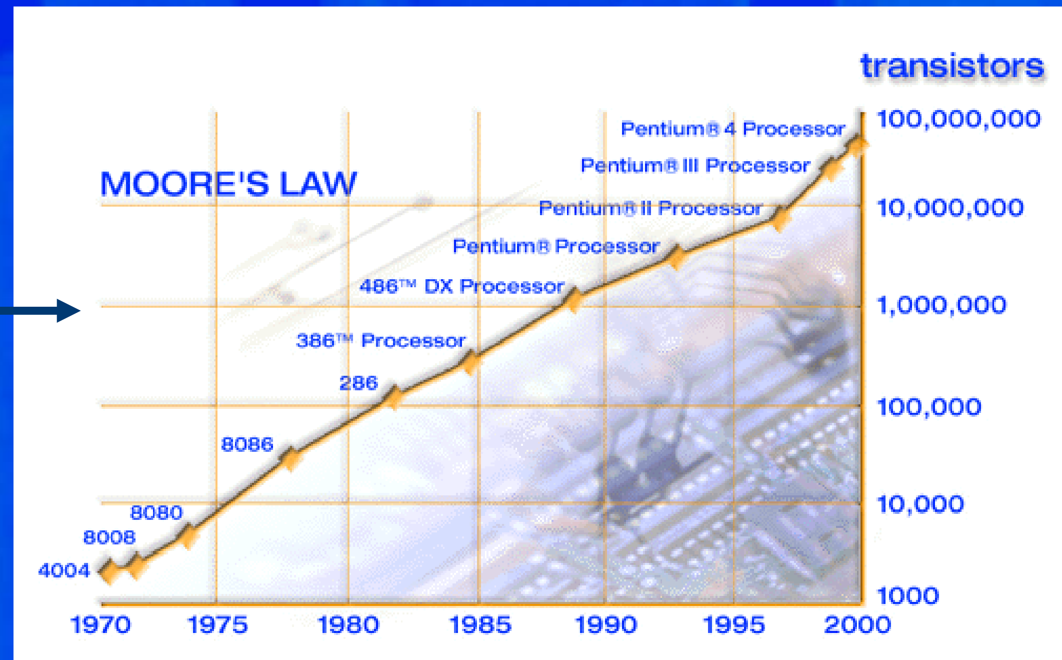
1975: Number of Integrated Circuit components will double every 18 months

G. E. Moore, "Progress in Digital Integrated Electronics", *Technical Digest of the IEEE IEDM 1975*.

1996: The definition of "Moore's Law" has come to refer to almost anything related to the semiconductor industry that when plotted on semi-log paper approximates a straight line. I don't want to do anything to restrict this definition. - G. E. Moore, 8/7/1996

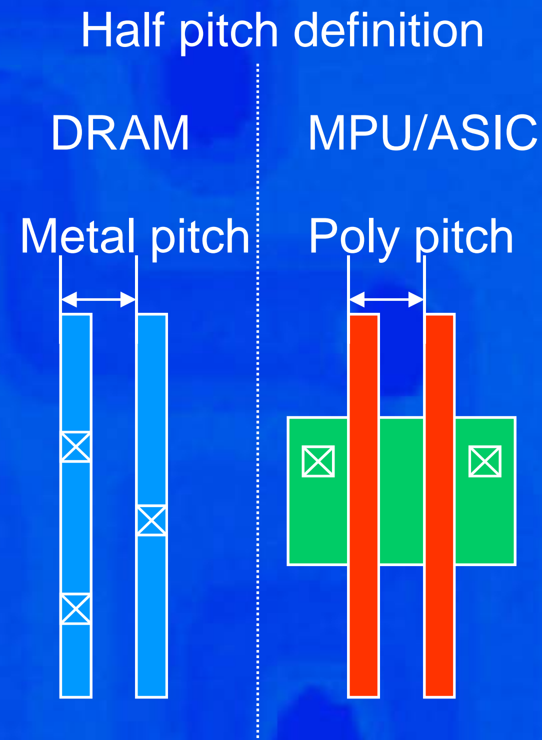
P. K. Bondyopadhyay, "Moore's Law Governs the Silicon Revolution", *Proc. of the IEEE*, vol. 86, no. 1, Jan. 1998, pp. 78-81.

An example:
Intel's Microprocessors



Moore's law fundamentals

- ✓ For every generation:
  - CD x 0.7
  - Area x 0.5
  - Chip size x 1.5
  - Structural improvement x 1.3
  - N of components x 4
  - Clock frequency x 1.4



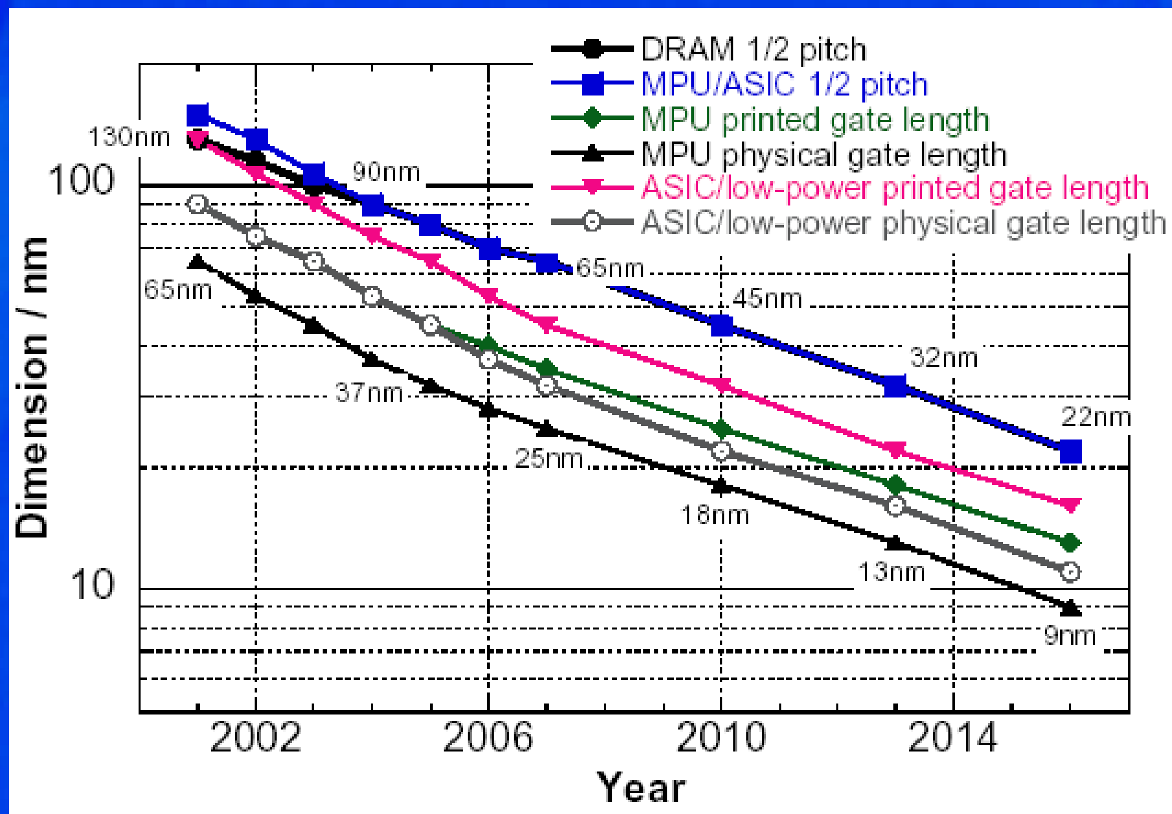
Technology nodes (1/2 pitch):

0.7 0.7

250 -> 180 -> 130 -> 90 -> 65 -> 45 -> 32 -> 22 -> 16

0.5

CMOS technology scaling



This roadmap is 7 years old:
Now 45 nm is in production

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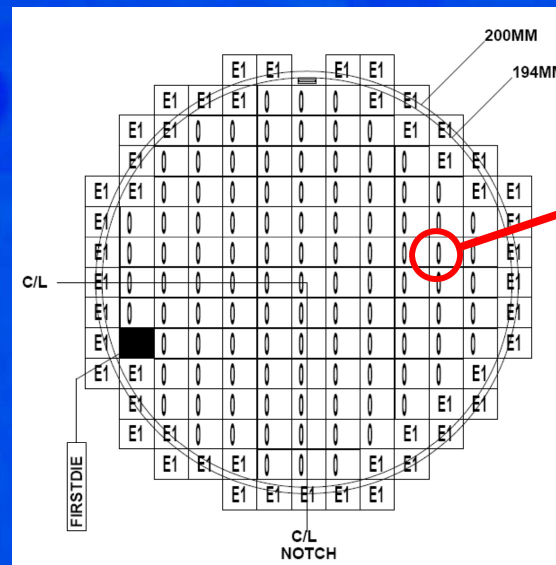
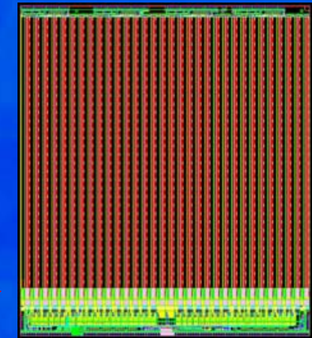
What's in a fully processed wafer?

- ✓ The repetition of a circuit (or a group of smaller circuits assembled in a "reticle") as many times as possible

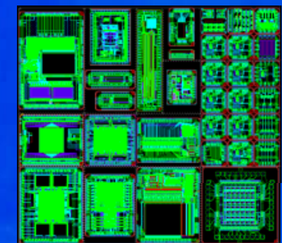
200mm wafer in its "wafer shipper" box, in the 250nm CMOS technology used for LHC



"Step plan", or map of the same wafer in the left picture. Each square is a repetition of the base structure (reticle)



Individual chip repeated in the wafer (or it could be a composition of circuits as in the figure below)



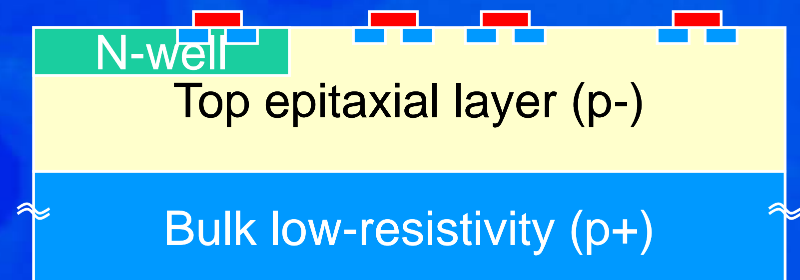
Fundamental manufacturing operations

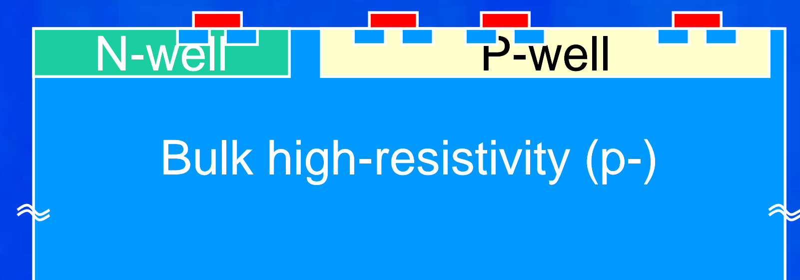
- ✓ Silicon wafer production
- ✓ Wafer cleaning
- ✓ Oxidation
- ✓ Lithography
- ✓ Ion implantation
- ✓ Etching
- ✓ Deposition

Silicon wafer production

- ✓ CMOS Foundries normally purchase substrates (silicon wafers) from other suppliers
- ✓ The wafers can be classified according to
  - Their diameter: 200mm is standard size until 130nm node, from which point also 300mm start to appear. 300mm is becoming the only option for more advanced technologies
  - Their nature: bulk, epitaxial, Silicon On Insulator (SOI)
- ✓ The native thickness of wafers is about 700µm (for 200mm), and they can be thinned after full processing with a process called Back Side Grind (BSG)

Epitaxial: bulk wafer is very low resistivity, top 2-5um are grown and have higher resistivity. Wells and diffusions are implanted on the top layer. For instance, 250nm was typically using this type of wafers.

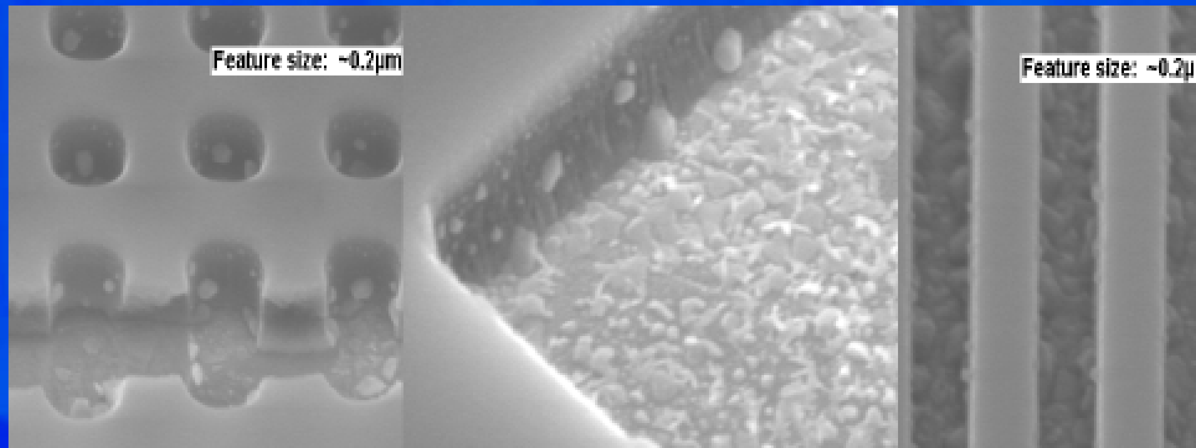




Bulk: all the wafer has rather high resistivity, and twin wells are implanted (n and p wells) on the surface with appropriate dopings for FETs. From about the 130nm node, this type of substrate is used (it is cheaper)

Wafer cleaning

- ✓ Contamination has very strong influence on important technology properties (gate oxide integrity, poly thickness, etc.)
- ✓ Before every processing step, there is the need to removing residual contaminants from previous processing. In modern semiconductor processing, there are about 100 cleaning steps!!
- ✓ Principles of cleaning:
  - Weakening the Vad Der Waals forces sticking the contaminants to the wafer
  - Building repulsion potential around the contaminant particles and the wafer
  - Carrying away the repulsed contaminant particles from the surfaces (for instance, with physical removal mechanism such as brushing, megasonic agitation of liquids, flux of aerosols, etc.)

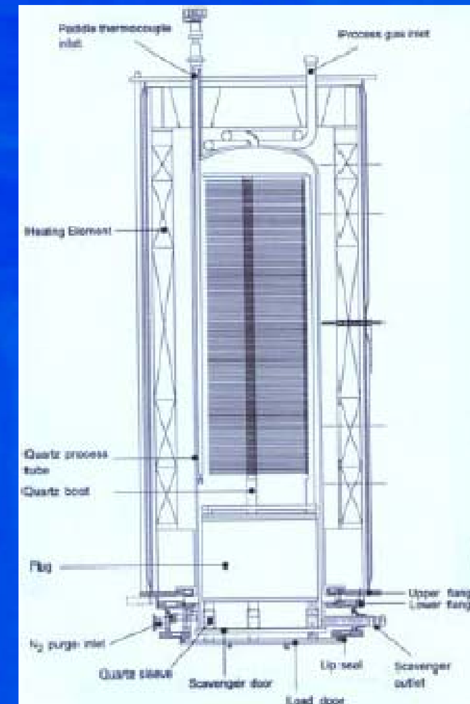


Example:

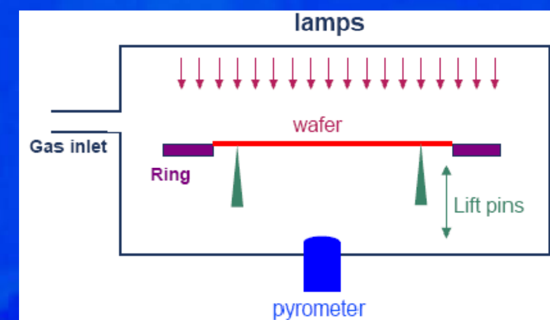
Residual polymers after etch during low-K dielectric processing. They are visible as "bubbles" in the picture and need to be removed before further processing.

Oxidation

- ✓ CMOS technologies are based on the combination of Si and SiO_2 (so far…): it is not surprising oxidation plays a fundamental role in manufacturing
- ✓ Oxide is used for the FET gate, to isolate devices from each other, to isolate metals from each other, to isolate metals from FETs
- ✓ Not all oxides are “built” with oxidation, some are deposited…
- ✓ High-quality oxides, such as the gate oxide, are product of very well controlled oxidation process (often with dopants to modify the properties of the oxide)
- ✓ Oxidation can be performed:
  - In furnaces, mainly vertical, at the batch level (more than 100 wafers at the same time)
  - In Rapid Thermal Processing (RTP) Furnaces that can process only one wafer at a time



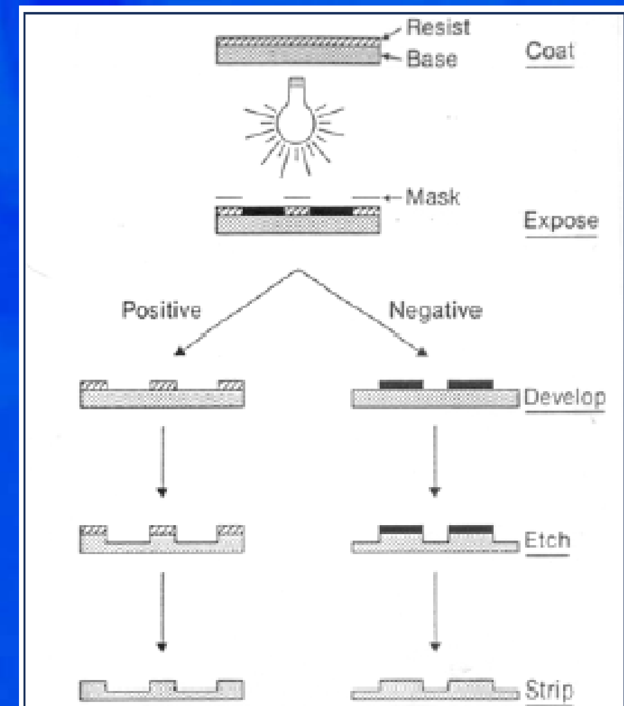
Vertical furnace for 150-175 wafers (100-150 plus dummies on top and bottom to avoid regions where T is not uniform)



RTP furnace. The wafer is heated by lamps, T is read from the back, and the wafer is rotating for better uniformity

Lithography (1)

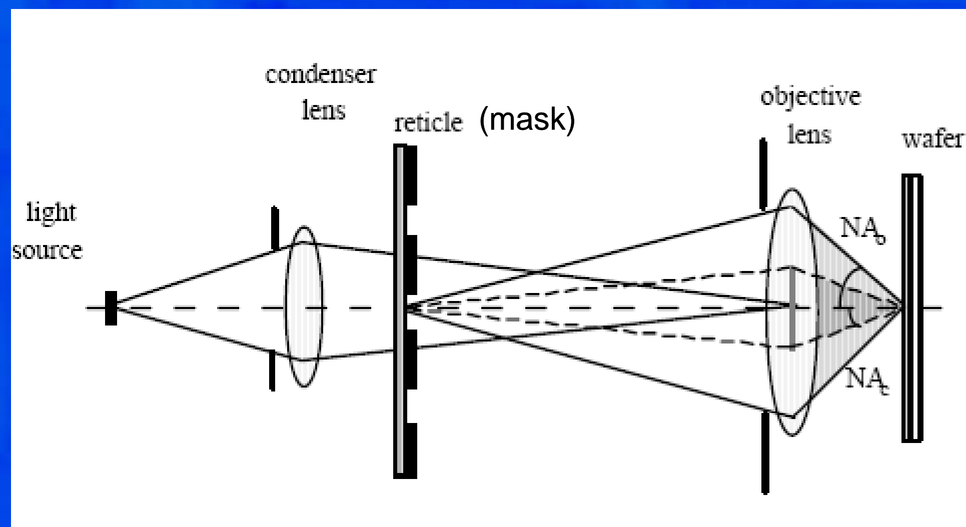
- ✓ Starting from one image of the circuit or combination of circuits (reticle), how to project this image multiple times on the wafer?
- ✓ The projection allows to "selectively" expose areas of the wafer to any given processing step (oxidation, deposition, implantation, etching, …)
- ✓ The projection field is "stepped" across the wafer regularly to reproduce the same image multiple times (actually to fill the whole wafer)
- ✓ The image to be projected – this is actually the "MASK" – is larger than its projection on the wafer, hence not too difficult to manufacture
- ✓ The process is analog to what happens in photography:
  - The wafer is covered with a material called "resist" (Coat)
  - It is then exposed to a source of light that passes through the mask. Hence the image on the mask is projected on the wafer
  - The resist changes properties only in the selected regions exposed to light
  - A "development" removes the resist only where it has changed properties (positive) or it has not changed properties (negative)
  - Now the wafer can be subject to the processing step – for instance implantation or etching – that will only take place where the resist has been removed
  - At the end, the resist will be removed from all areas and the wafer is ready for next processing step (again with selectivity determined by a new lithography step with another mask)



Example of positive or negative lithography associated with an etching step

Lithography (2)

- To improve the resolution of the image, lots of complicated "tricks" can be used:
  - On the light source (dipole, quadrupole, annular, customized, …)
  - On the mask (different types of Phase Shifting Masks, PSM)
  - With techniques such as Optical Proximity Corrections (OPC)

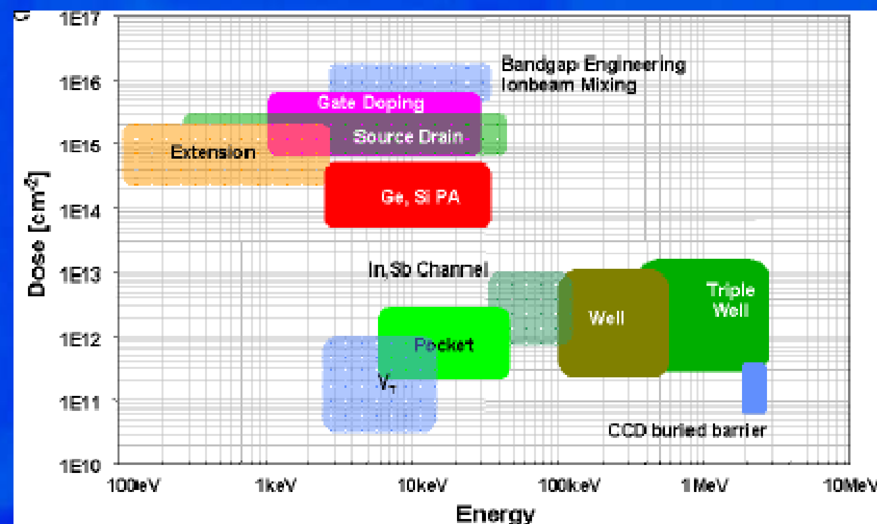


For better resolution with the same light wavelength, "immersion" lithography is used these days. The medium between the objective lense and the wafer is not air anymore, but a liquid

Light sources:
ArF (193nm) down to 65nm node
F2 (157nm wavelength) probably down to 32nm node
EUV (13.6nm wavelength) probably down to 22nm node

Ion Implantation

- ✓ Ion implantation is the standard doping technique in microelectronics
- ✓ Ions are produced in a source, mass separated in a magnet, accelerated in an electric field , deflected to obtain homogeneous doping, the implanted into the wafers
- ✓ Ion implantation produces damage which has to be annealed at high temperatures (800-1050ºC). At these elevated temperatures, dopant atoms diffuse
- ✓ The dose and energy of the ions change considerably with the purpose of the doping. Careful selection of dopant, energy, dose and annealing temperature and time allows the formation of well controlled doping profiles

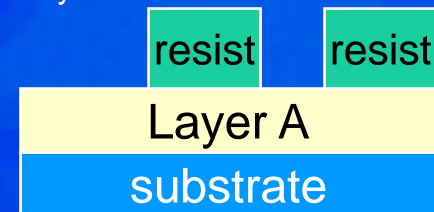


Etching

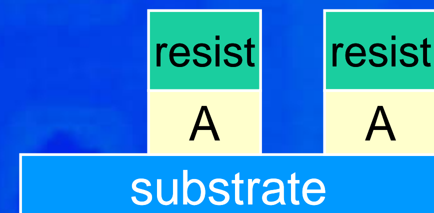
- ✓ Etching allows to removing material from the wafer surface, hence transferring a lithographic defined pattern into the underlying layer
- ✓ The most common etching technique is plasma etching, because it is:
  - Anisotropic – it enables removal of material on one direction with minimal removal on the other directions
  - Highly selective – it can be tuned to remove only one material and let the others virtually untouched
  - …and it has a large throughput, wafers can be processed quickly
- ✓ Plasma etching takes place in a chamber and in the presence of a plasma (gas mixture at low pressure with High Frequency Electric Field; this produces neutrals – atoms, radicals, molecules – ions, electrons and photons). In the plasma, the wafer surface gets quickly negatively charged and ions are accelerated towards it. Both their physical impact and – mainly – their chemistry contribute to remove material from the wafer

Example:

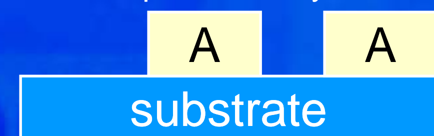
A film has to be "selectively removed" to reproduce a pattern in layer A. Lithography patterns the resist on top of the layer.



Plasma etching selectively removes layer A only, and only vertically. Etching stops when the substrate is reached (different material, or etch stop)



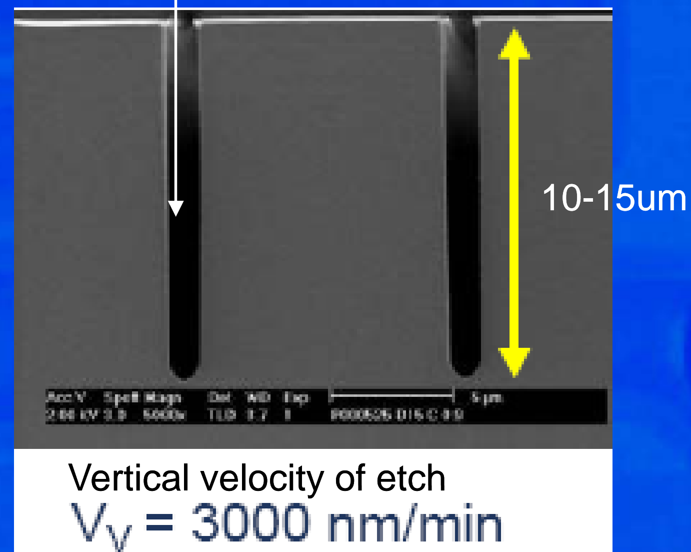
The eventual removal of the resist leaves the patterned layer A



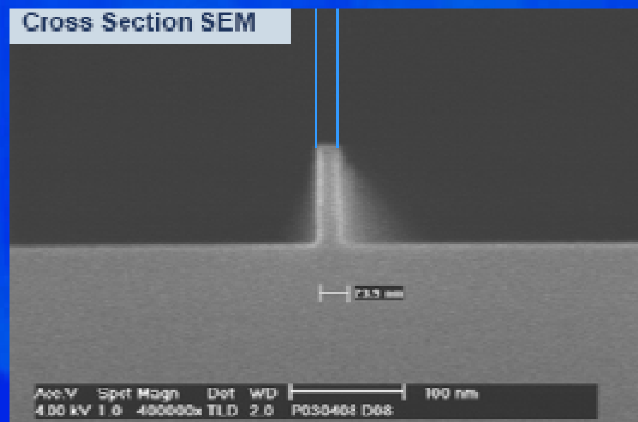
What plasma etching can do…

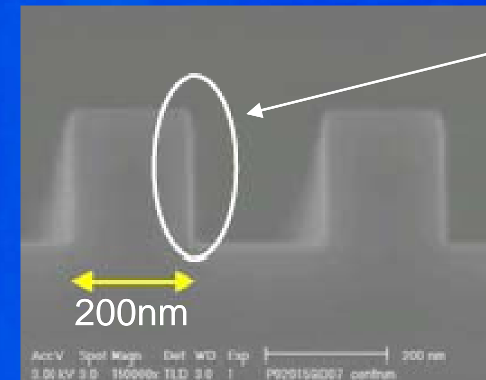
Scanning Electron Microscope (SEM) images

Well, this is anisotropy!



25nm

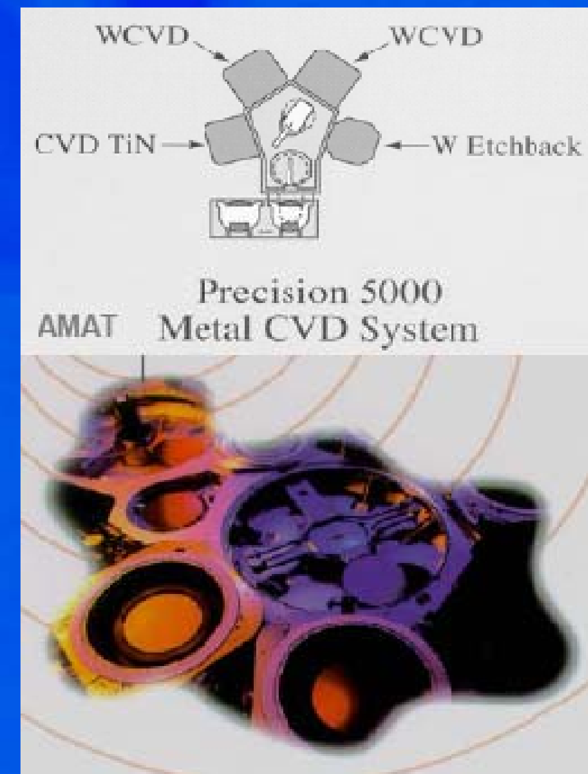




Deposition

- ✓ In wafer manufacturing, one needs not only to "etch" but also to deposit material. For instance, etched holes must be filled…
- ✓ Deposition is performed with either
  - Chemical Vapor Deposition (CVD) techniques (some of which are enhanced by the presence of a plasma in the chamber). There is a large variety of such techniques: APCVD, SACVD, LPCVD, PECVD, HDPCVD, RTCVD, ALCVD…
  - Physical Vapor Deposition (PVD) techniques such as sputtering, evaporation, …
- ✓ In CVD, chemical reactions are carefully selected and enhanced by conditions in the deposition chamber (temperature, pressure, presence of plasma, …)
- ✓ Very often CVD takes place in single wafer cluster tools, where the single wafer moves from chamber to chamber to go through several processing steps

Multi-chamber tool (1 wafer per chamber at a time). In this case, the chamber does operations related to Tungsten (W) deposition for contact/via

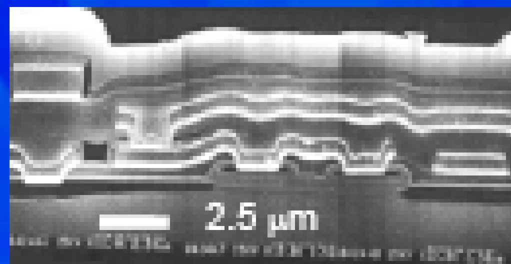


The wafer moves from one chamber to the next in sequence

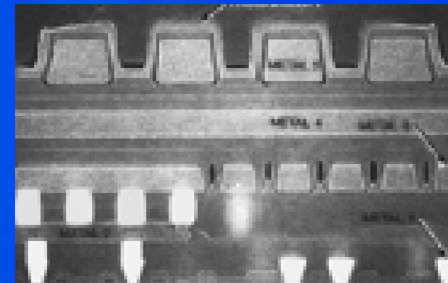
Planarization (1)

- ✓ Processing of modern technologies requires the capability of "etching" holes tens of nm wide and tens of nm apart. Up to 8 levels of metal have to be processed this way on top of each other!
- ✓ This is possible ONLY if the "substrate" is perfectly flat!
- ✓ Chemical Mechanical Polish (CMP) is the planarization process that allows modern technologies to exist
- ✓ For 90nm technology node, it allows better than 50nm planarization on a single die. This is equivalent to leveling a football field homogeneously to within better than 250µm!!!

Before CMP

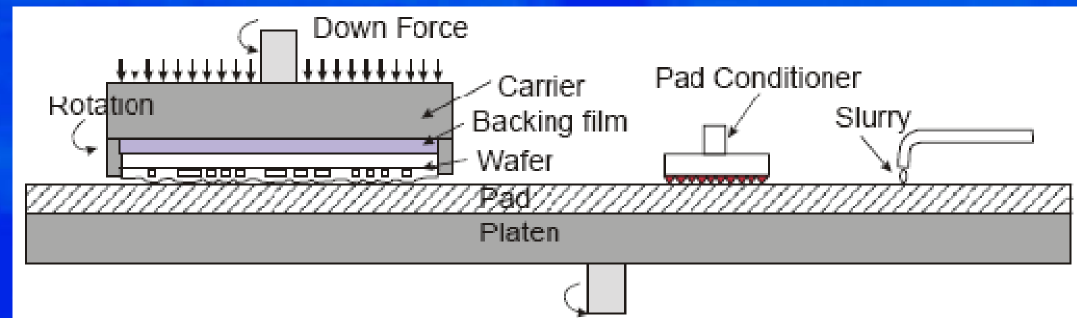


With CMP

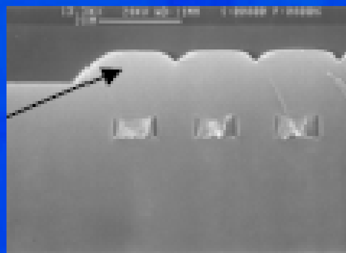


Planarization (2)

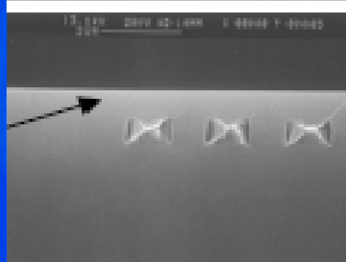
The wafer is positioned "head-down" in the CMP tool, and rotates.
The bottom platen, covered by the polishing (abrasive) pad, rotates.
A dispenser distributes a "slurry" which has a chemical action adding to the mechanical polishing.
The pad is constantly conditioned.

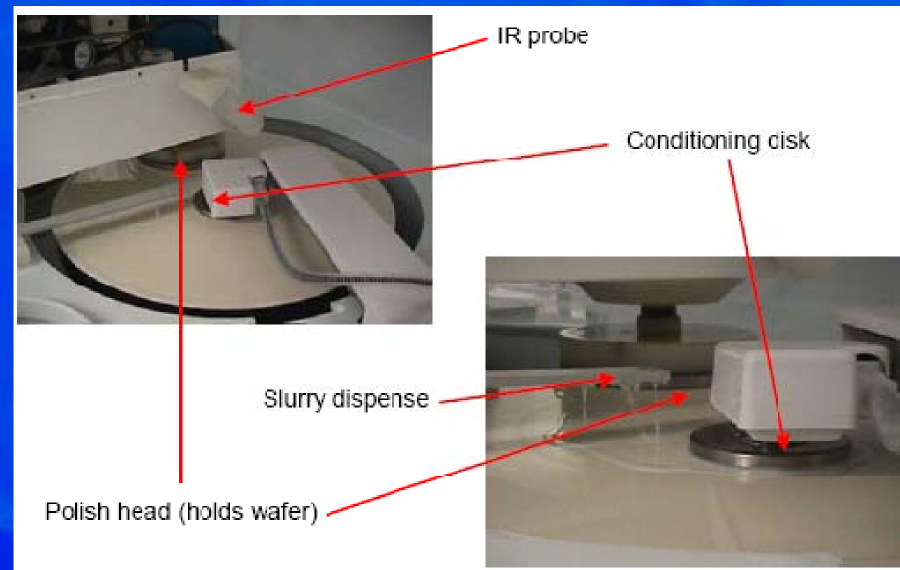


Pre-CMP



Post-CMP





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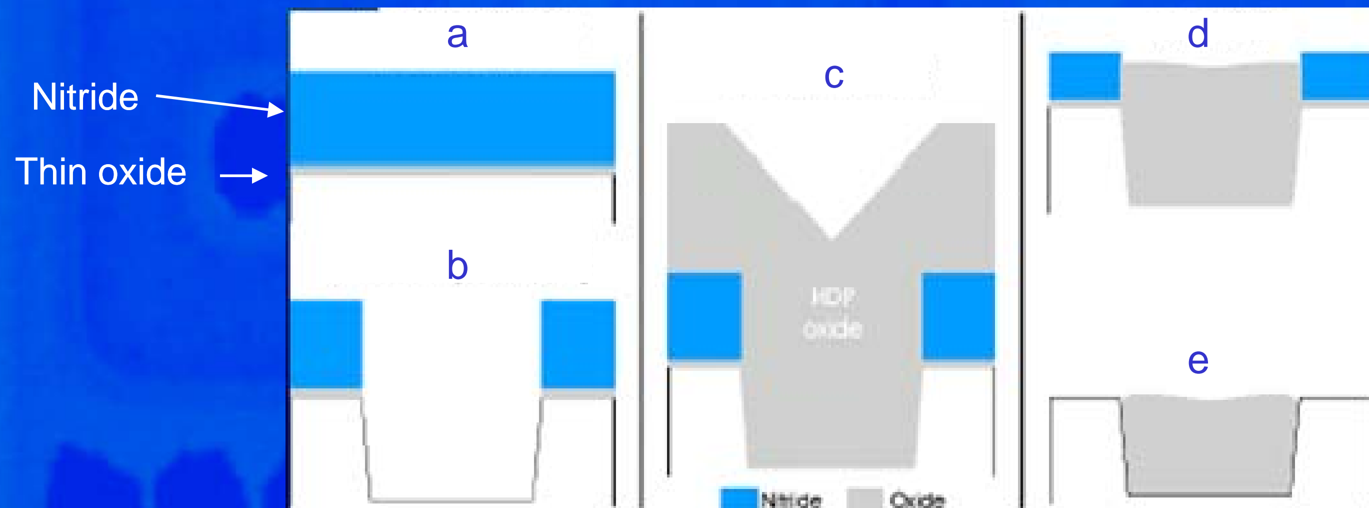
    - Front End Of Line (FEOL): construction of the transistors. The FEOL stops before the Pre-Metal Dielectric
    - Back End Of Line (BEOL)

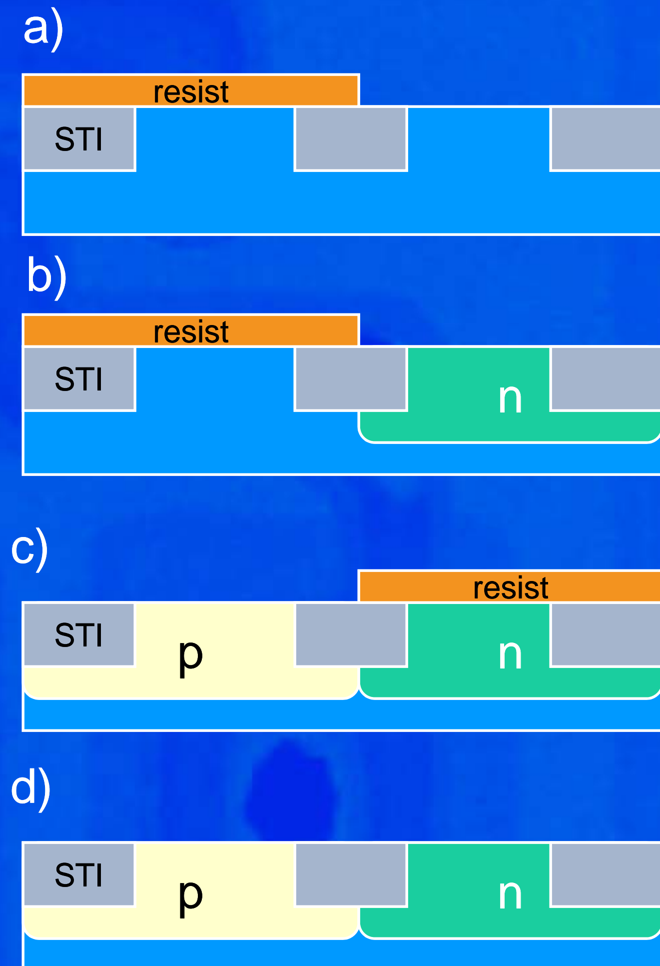
Active Area Module

- ✓ AIM: selection of “active area” (area where transistors will be built)
  - a) Thin oxide growth (thermal). Nitride (Si_3N_4) deposition
  - b) Active area patterning (lithography). Trench etching (STI trench that will isolate devices)
  - c) STI oxidation: thermal at first (thin oxide), then with High Density Plasma (HDP) CVD
  - d) Oxide planarization (CMP). Nitride is used as CMP stop point since CMP rate is much smaller in nitride than in oxide
  - e) Final result after CMP



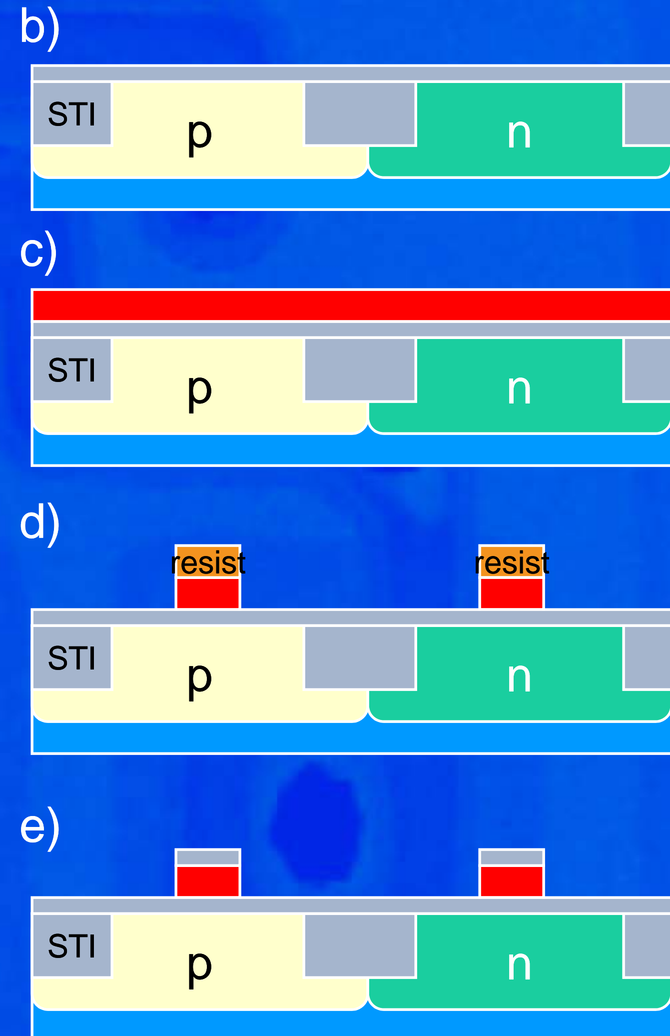
Channel doping module

- ✓ Aim: doping of the wells and doping for the threshold adjust (doping in the area where transistors will be built to fine-tune their Vth)
  - a) Definition of nwell (resist, lithograpy)
  - b) Implant of nwell in two steps: deep implant for well profile (high energy ions), shallow implant for Vth adjust and lateral leakage control
  - c) Strip resist patterning nwell, and repeat a) and b) for pwell
  - d) Well anneal (thermal process where implanted ions will diffuse)



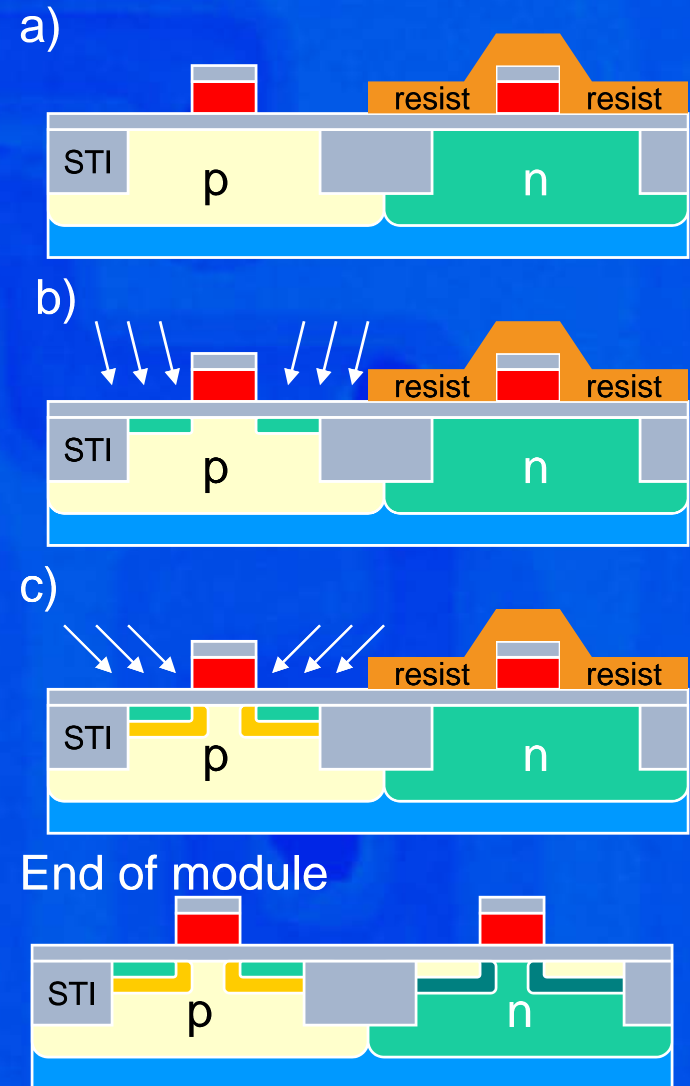
Gate module

- ✓ Aim: growing the gate oxide, deposit and pattern the polysilicon gate
  - a) Remove damaged oxide on top of active area
  - b) Gate oxide growth (nitrided oxide)
  - c) Deposition of polysilicon with CVD
  - d) Gate patterning (resist, lithography, etch)
  - e) Resist removeal (strip). Re-oxidation to cure oxide above Source/Drain areas



Source/Drain extension module

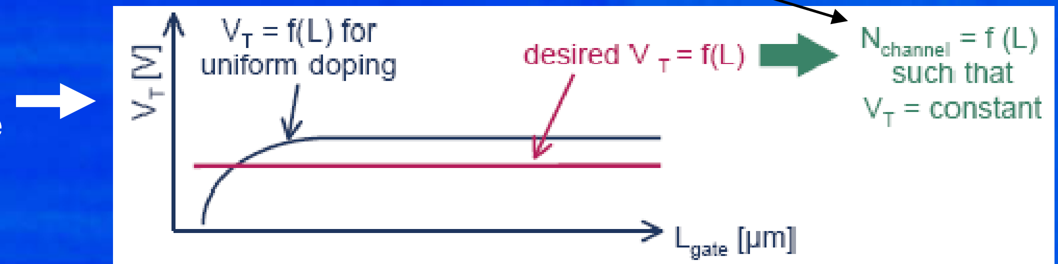
- ✓ Aim: implant the S/D extension and pockets (halo). The two implant are self-aligned by the presence of the poly gate
  - a) Patterning for n+ S/D (resist, lithography)
  - b) Implant of n- for S/D extension, at moderate angle (7 degrees). The extension limits the short channel effect and series R between S/D and the channel region
  - c) Implant of p- for halo, at large angle. The halo changes the channel doping concentration for short channel transistors, hence the Vth dependence on gate length is weakened
  - d) Removal of resist, RTP anneal
  - e) Repeat a) to d) for p+ S/D (all dopings are reversed)



Role of the HALO implant

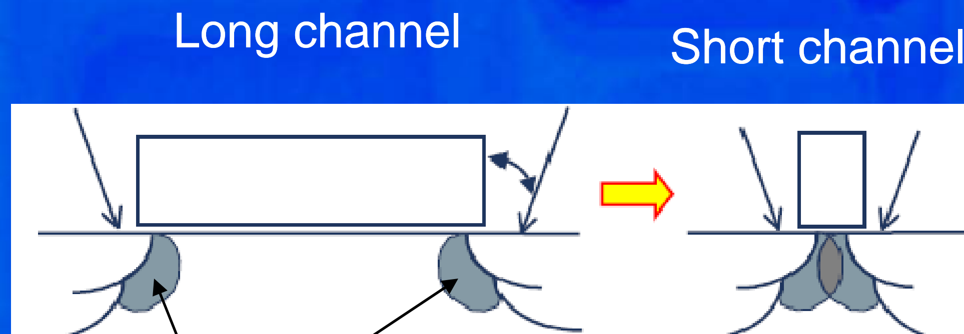
With uniform doping for all gate length L, Vth changes with L (Short Channel Effects). Users wish all FETs with roughly the same Vth irrespective of the L. To achieve that, HALO allows to change doping with L, so that Vth stays approximately constant

$N_{channel}$=dopant concentration in the channel region



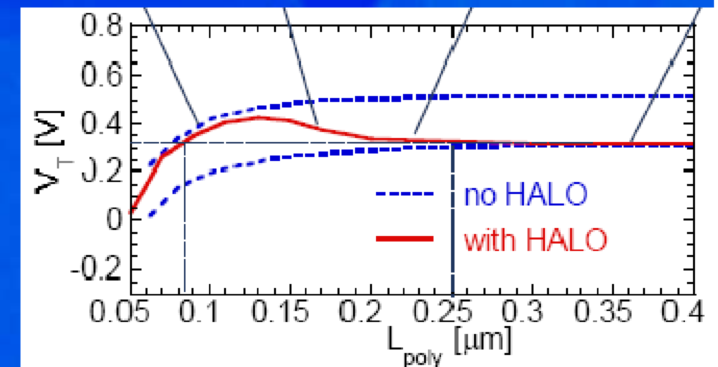
Long channel

Short channel



Halo implant

Here the doping in the channel region is higher, hence Vth is increased



Result:
In the absence of HALO, Vth is either too low for small L or too high for large L. With HALO, the compromise is acceptable

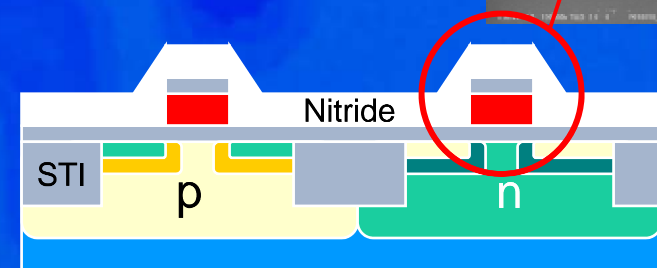
Spacer module

✓ Aim: building the spacer that will allow for self-aligned S/D doping implant

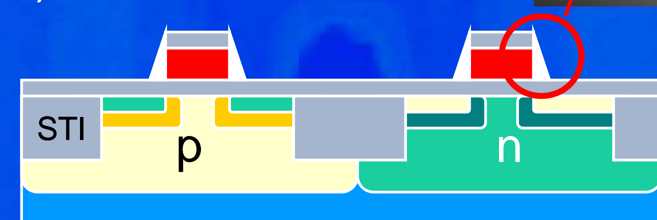
a) Deposition of a thin oxide layer, then a thicker (150nm) nitride layer (both with CVD)

b) Anisotropic etching of the nitride – much quicker in vertical than horizontal direction

a)



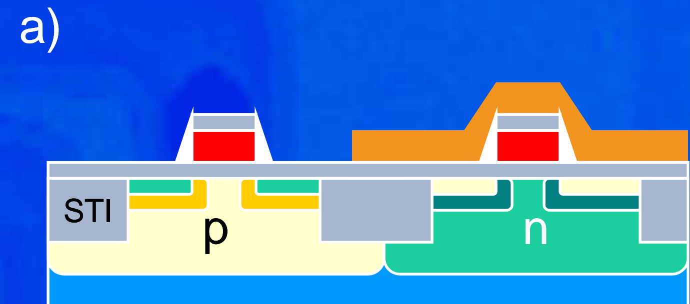
b)



Junctions module

- ✓ Aim: realizing S/D regions for FETs and doping gate electrodes
  - a) Patterning for n+ implant (NFETs)(resist, lithography)
  - b) Implant n+ regions (poly is doped as well)
  - c) Remove resist and repeat a) and b) for p+ implant (PFETs)
  - d) Remove resist. Thermal anneal to cure doping-related damage

a)



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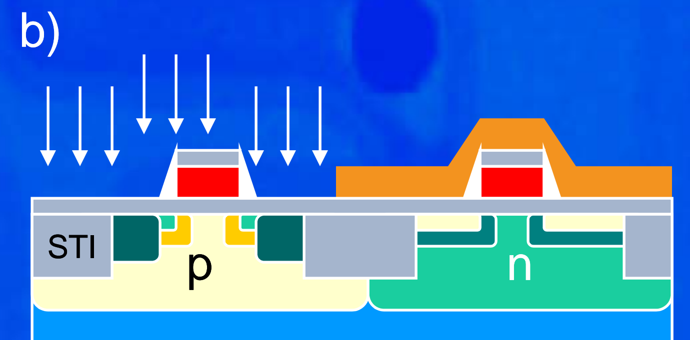
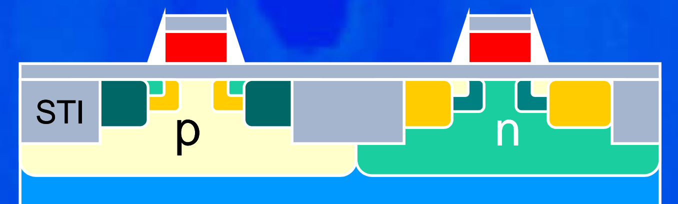
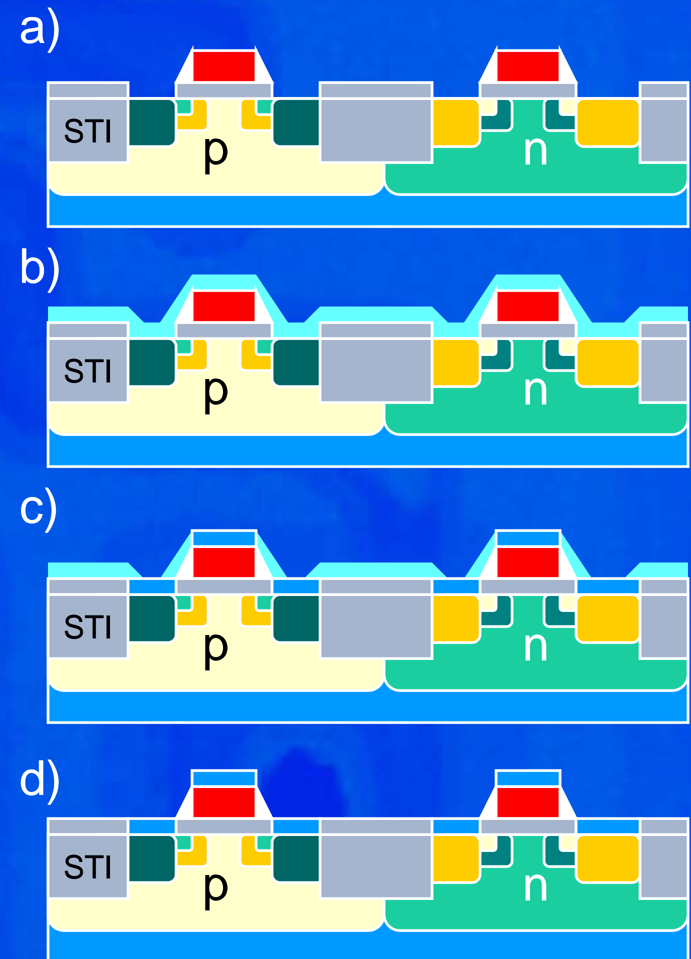


End of module



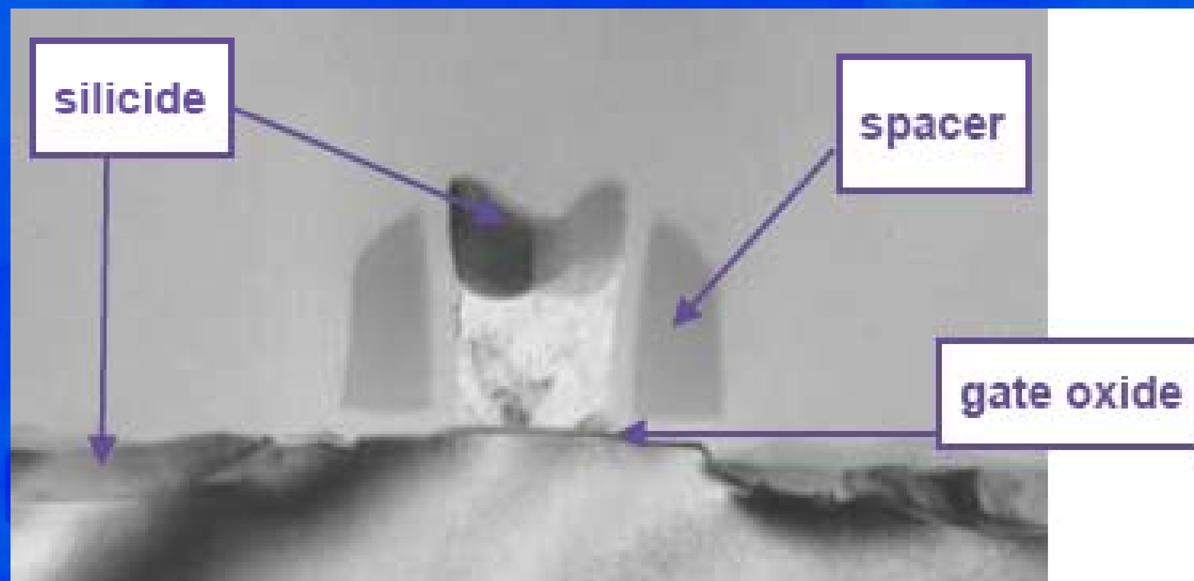
Silicide module

- Aim: Forming a silicide layer (typically $TiSi_2$ or $CoSi_2$, NiSi from the 90nm node) on top of S/D and poly to lower the access resistance
  - a) Etch of the oxide covering the Si
  - b) PVD of the metal (Ti or Co)
  - c) First RTP at lower T (order of 500°C) to form a high-resistivity compound (TiSi or CoSi). Reaction only occurs where metal is on top of silicon. Thanks to the spacers, low risk of short between S/D and poly
  - d) Etch of the metal that has not reacted with Si (selective etch)
  - e) Second RTP at higher T (order of 800°C) to continue reaction and obtain low-R compound ($TiSi_2$ or $CoSi_2$)



End of FEOL

The transistors are ready to be connected with each other and with the outer world!



SEM of a transistor at the end of FEOL

ULSI technologies: manufacturing

Outline

- ✓ Foreword
- ✓ Moore's law
- ✓ Manufacturing of ULSI CMOS technologies
  - Fundamental manufacturing operations
  - Process Flow
    - Front End Of Line (FEOL)
    - Back End Of Line (BEOL): it starts with PMD deposition. Only Copper Metal Processing flow is described here

PMD module

✓ Aim: depositing the Pre-Metal-Dielectric insulating the silicon from the metal layers (this layer has to be a barrier against moisture and mobile ions such as K+ and Na+)

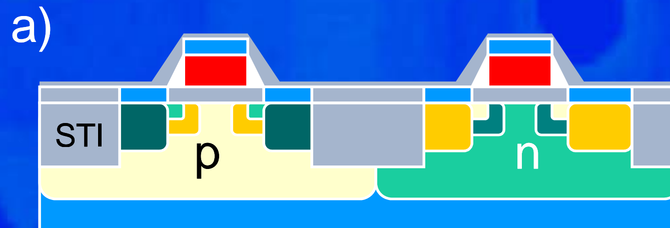
a) CVD of a thin layer of SiON

b) High Density Plasma (HDP) CVD of an Undoped Silicate Glass (USG), an SiO_2. This undoped isolation layer prevents migration of P from the upper doped layer towards Si

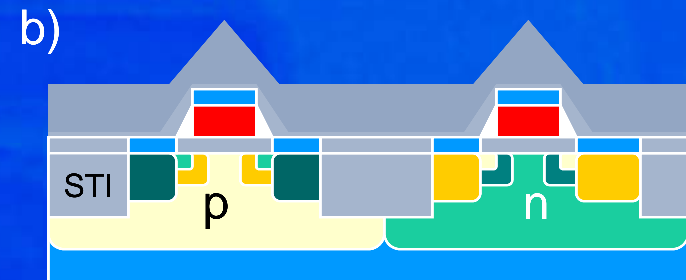
c) HDP CVD of a doped (4.5%) SiO_2 layer, PSG (Phosphosilicate Glass), that is good at capturing mobile alkali ions. This prevents migration of such ions to the Si

d) Anneal and CMP to about 1250nm thickness

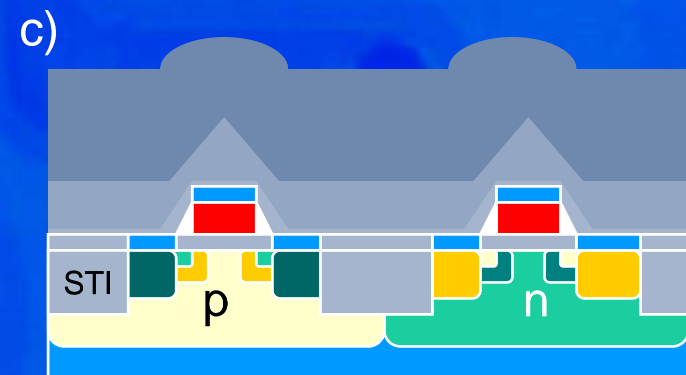
a)



b)



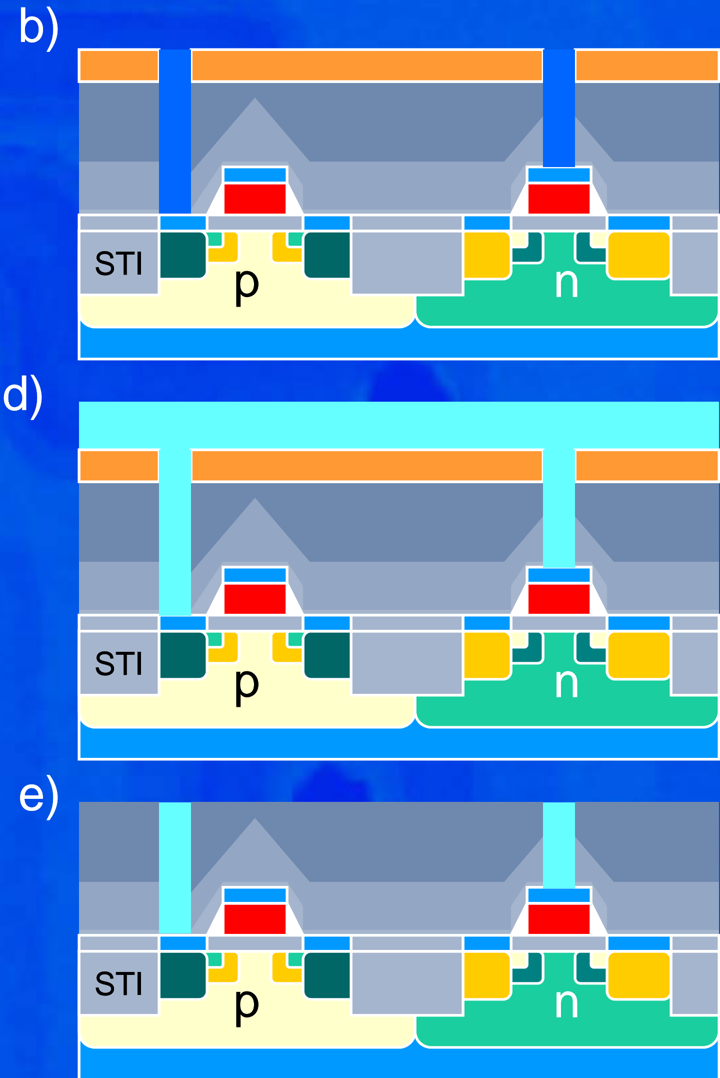
c)



d)

Contact module

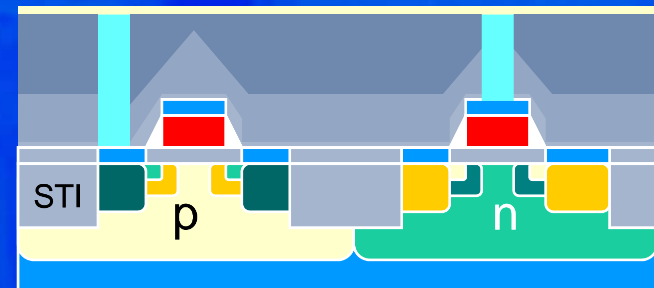
- ✓ Aim: opening the contact holes in the PMD and filling them with tungsten (W)
  - a) Patterning for the opening (resist, lithography)
  - b) Etch of the contact hole. Etching needs to be very selective to stop on silicide (different depth of holes on poly or S/D)
  - c) Deposition (with Ionised Metal Plasma CVD) of a Ti and TiN barrier. TiN helps the following deposition of W, Ti ensures a low-R contact to the silicide. This thin layer Ti-TiN is not shown in the figures to the left, but it is present all around W in the holes
  - d) Deposition of W
  - e) CMP stopping on PSG to leave W only in the holes



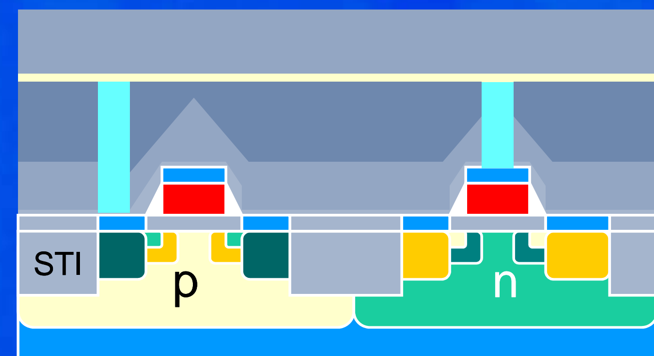
SD IMD1 module

- ✓ Aim: deposition of Inter-Metal Dielectric (IMD) in preparation of the first metal layer (metal1), that will be integrated using the Single Damascene (SD) technique
  - a) Deposition (PECVD) of a Silicon Carbide (SiC) thin layer (as etch stop material for next module, when trenches will be dug)
  - b) Deposition (PECVD) of a SiO_2 layer (IMD)

a)



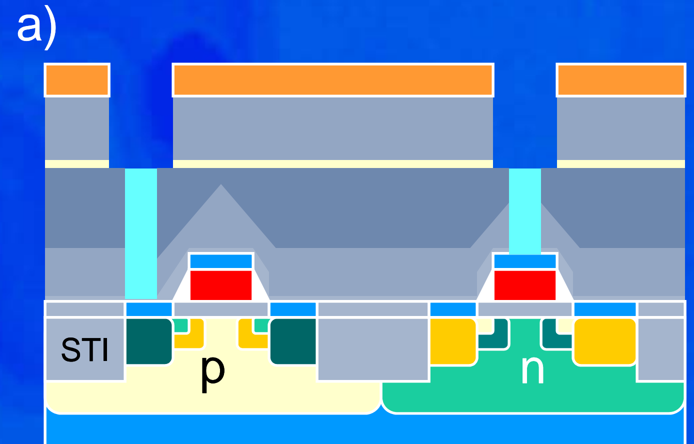
b)



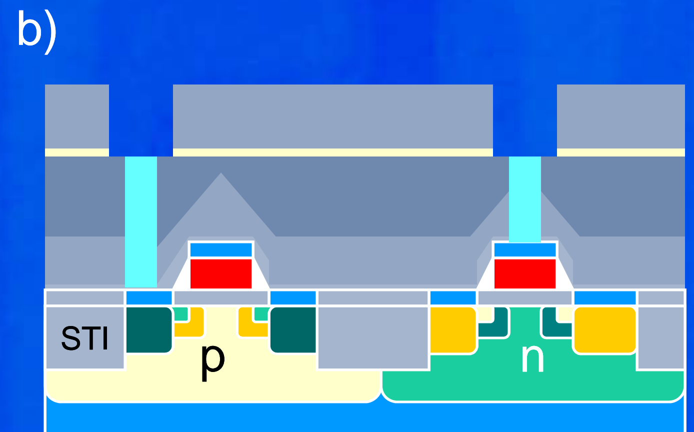
SD Metal1 patterning module

- ✓ Aim: Digging the trench for Metal1 lines
  - a) Patterning for metal1 lines (resist, lithography)
  - b) Etch of oxide and SiC
  - c) Removal of resist

a)

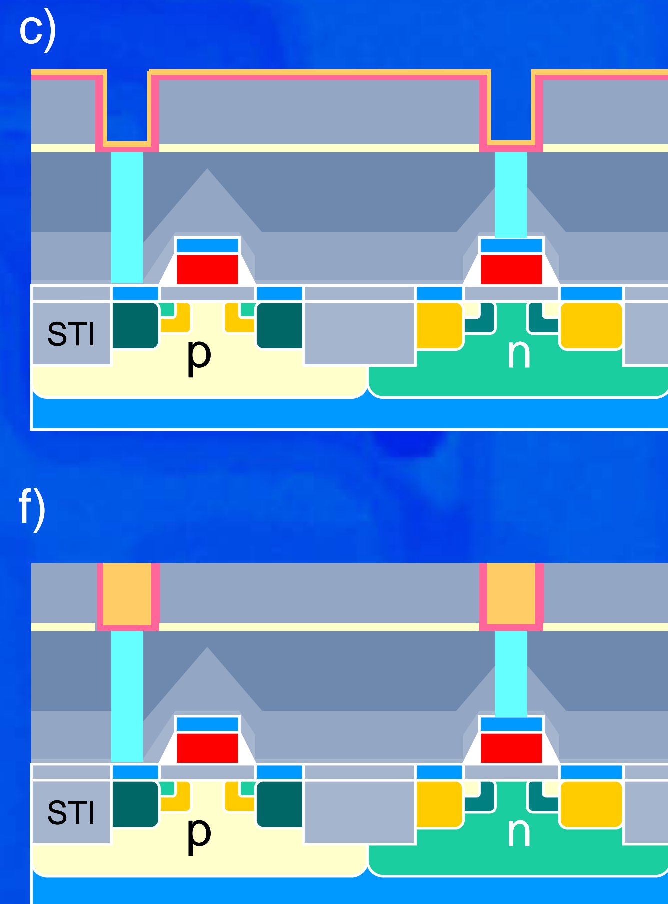


b)



SD Cu Metal1 module

- ✓ Aim: filling the trench with Cu to complete Metal1 layer
  - a) Pre-cleaning of trench with Ar
  - b) Deposition of a TaN/Ta barrier with a PVD technique. This barrier prevents migration of Cu, since Cu has tendency to migrate
  - c) Deposition of a thin layer of Cu with the same PVD technique. This layer acts as a “seed” when later filling the trench with Cu
  - d) Deposition of the bulk of the Cu with electroplating (a form of electrolysis that takes place in a bath rich in Cu salts)
  - e) Annealing for 30” at 250ºC. The annealing is necessary to ensure a change of structure of Cu, that reorganizes in larger grains with lower resistivity
  - f) CMP of the Cu, then of the TaN/Ta barrier. In this phase, it is necessary to have uniform Cu distribution across the wafer to have good results (this drives strict requirements for pattern density)



DD IMD2 module

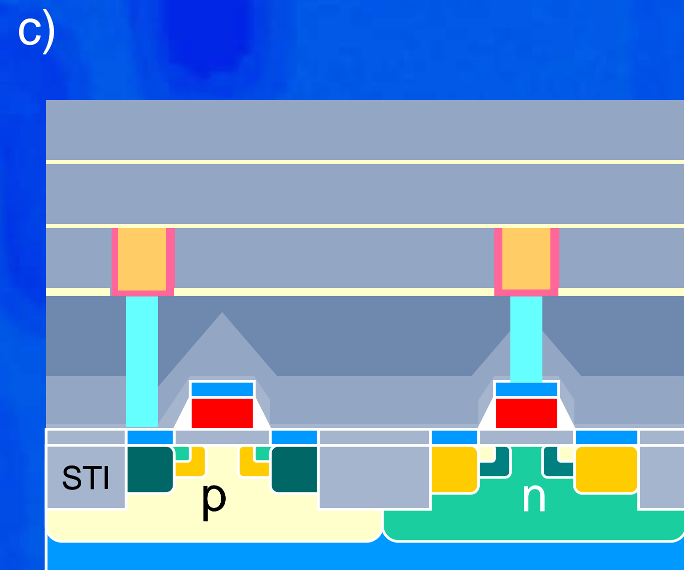
✓ Aim: deposition of Inter-Metal Dielectric (IMD) in preparation of the second metal layer (metal2), that will be integrated using the Double Damascene (DD) technique

a) Deposition (PECVD) of a Silicon Carbide (SiC) thin layer (as etch stop material for next module, when trenches will be dug)

b) Deposition (PECVD) of a SiO2 layer (IMD)

c) Steps a) and b) are repeated

c)



DD Metal2 patterning module (1)

- ✓ Aim: Patterning the dielectric to prepare for the deposition of Cu for M1-M2 vias and for Metal2
  - a) Patterning for Via1 holes (resist, lithography)
  - b) Partial Via1 etch, using the top SiC layer as etch stop
  - c) Removal of resist

b)

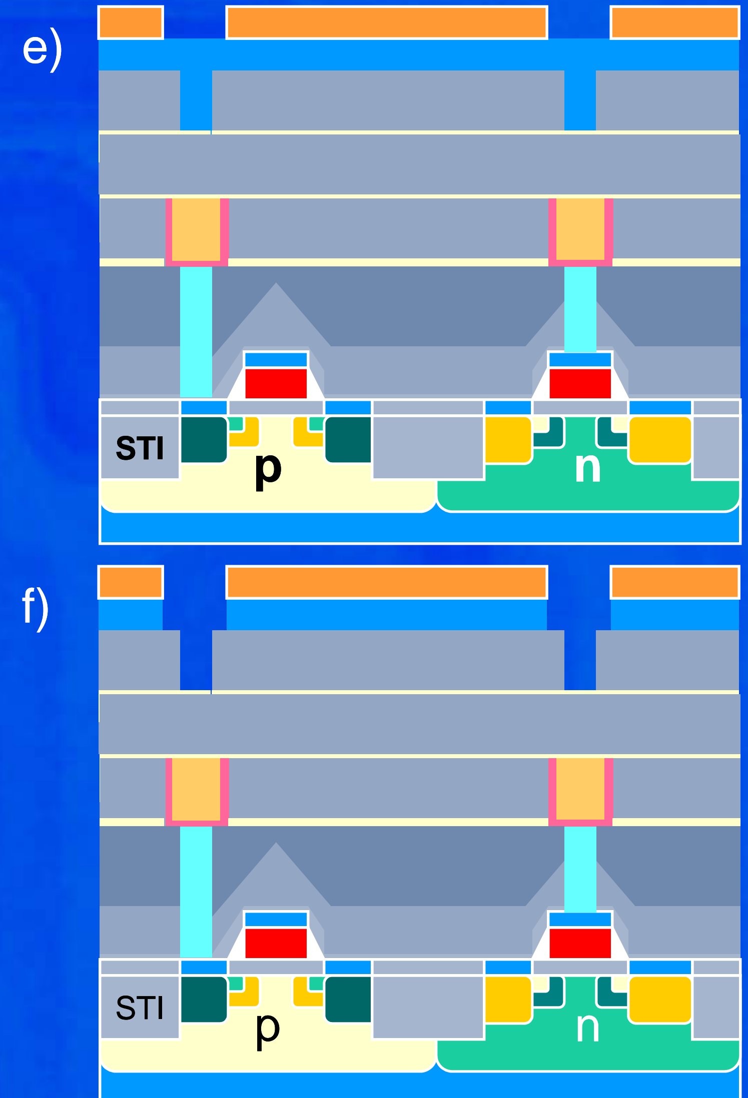
c)

DD Metal2 patterning module (2)

d) Deposition of an "underlayer" (UL) resist (planarized)

e) Deposition of an Imaging Layer (IL) of resist, and pattern of this layer for Metal1

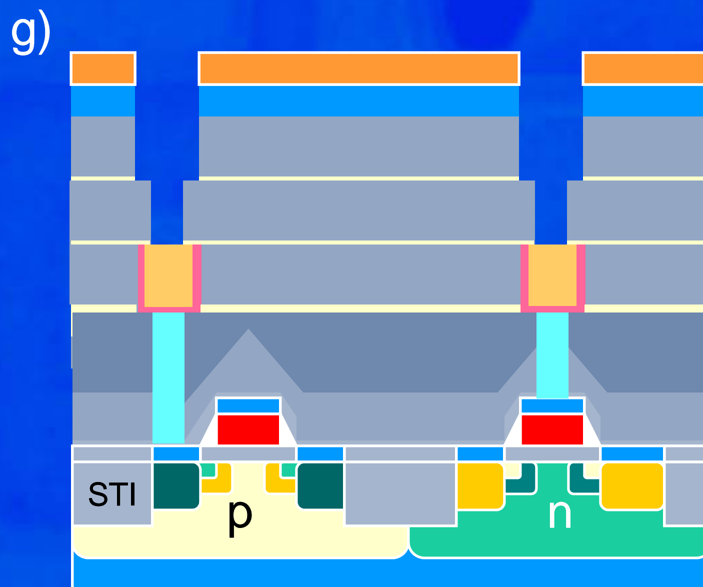
f) Development of the UL resist in plasma, very selectively under openings of IL and until trenches are completely emptied

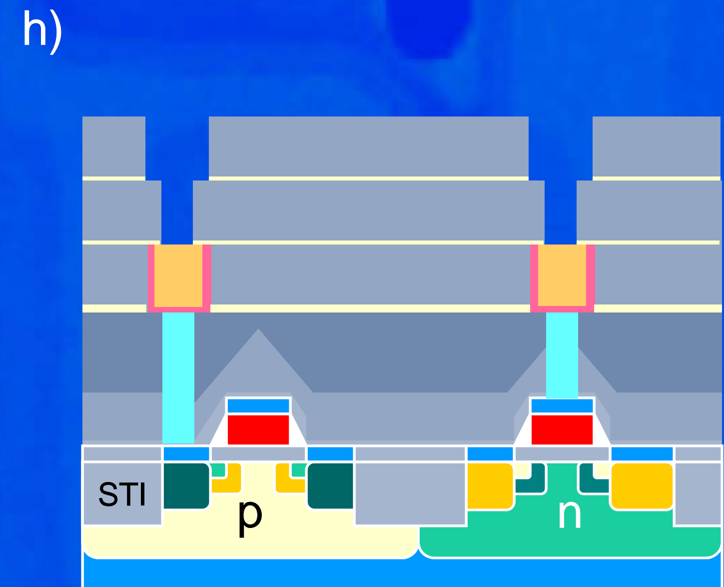


DD Metal2 patterning module (3)

g) Damascene etch of the oxide for both Via1 and Metal2 (SiC layers as etch stop)

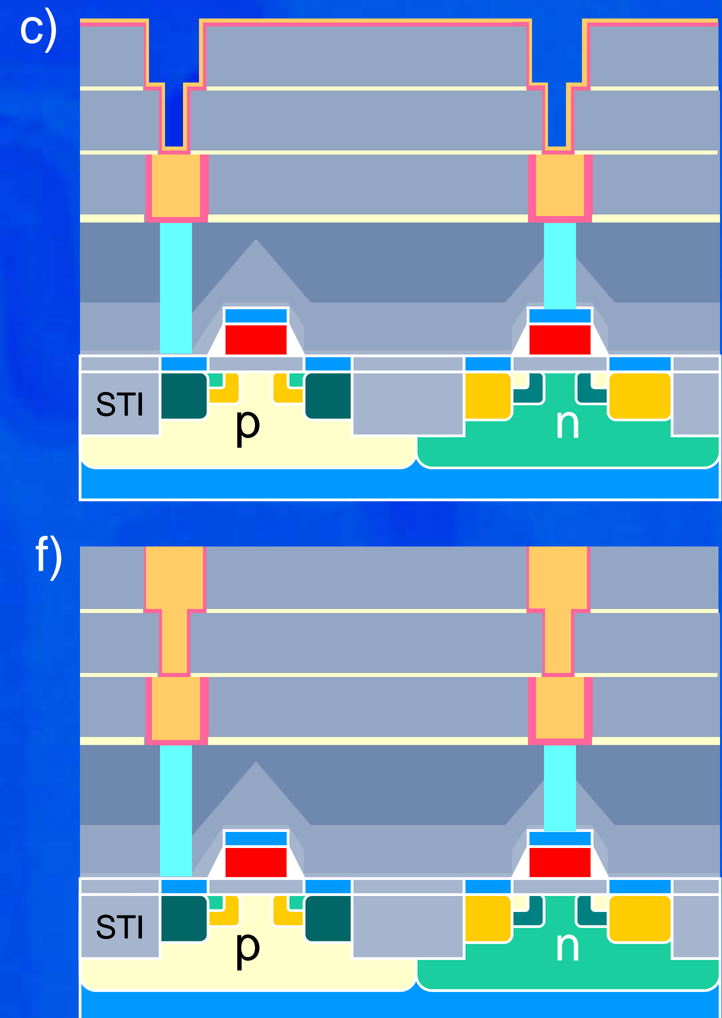
h) Removal of resist





DD Cu Metal2 and Via1 module

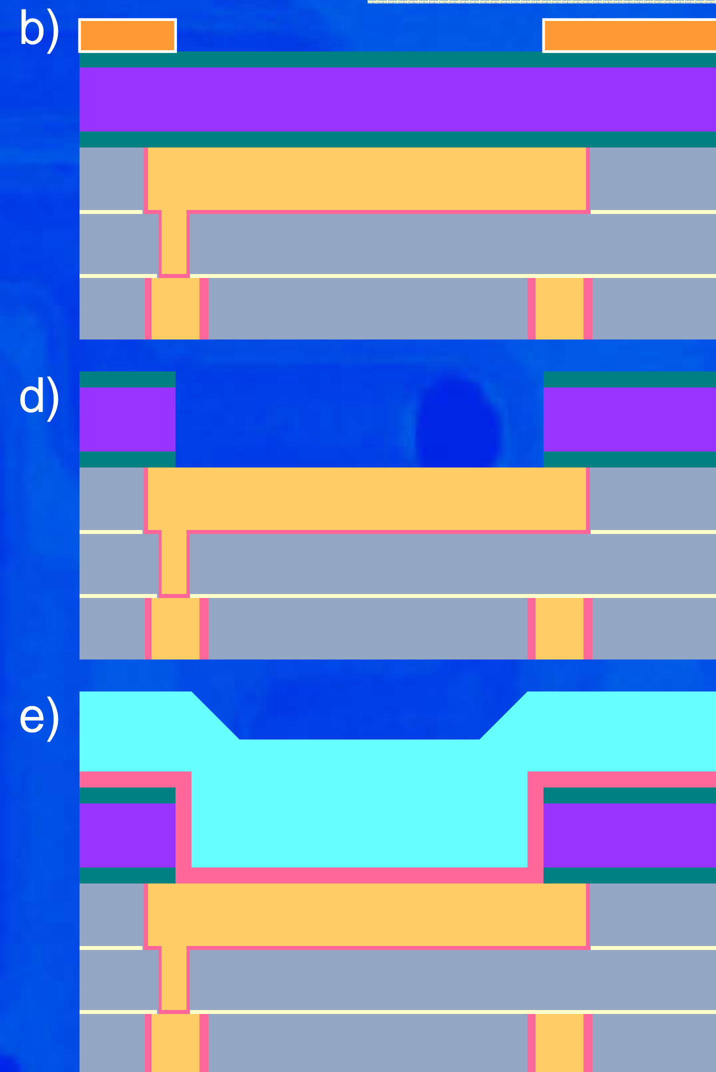
- ✓ Aim: filling the trenches with Cu for both Via1 and Metal2. The procedure is identical to the one used already for Metal1
  - a) Pre-cleaning of trench with Ar
  - b) Deposition of a TaN/Ta barrier with a PVD technique. This barrier prevents migration of Cu, since Cu has tendency to migrate
  - c) Deposition of a thin layer of Cu with the same PVD technique. This layer acts as a “seed” when later filling the trench with Cu
  - d) Deposition of the bulk of the Cu with electroplating (a form of electrolysis that takes place in a bath rich in Cu salts)
  - e) Annealing for 30” at 250°C. The annealing is necessary to ensure a change of structure of Cu, that reorganizes in larger grains with lower resistivity
  - f) CMP of the Cu, then of the TaN/Ta barrier. In this phase, it is necessary to have uniform Cu distribution across the wafer to have good results (this drives strict requirements for pattern density)
- ✓ All other metal layers are processed the same way (Double Damascene)



Passivation module (1)

✓ Aim: at the end of the metal stack (up to 8 levels), the final passivation and the pad opening steps are performed

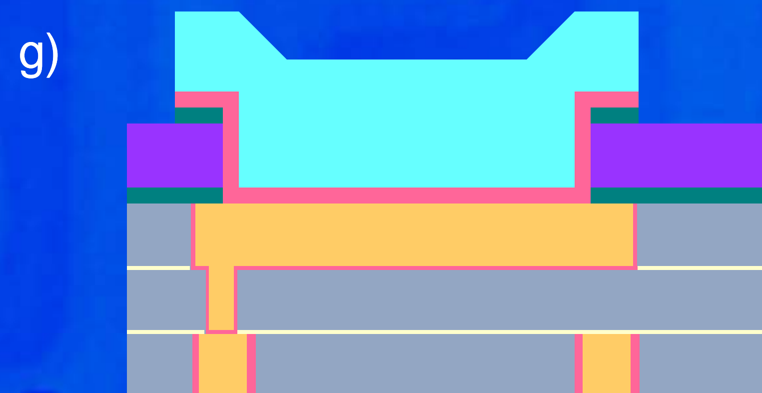
a) Deposition of a stack (SiC, Nitride, SiC)
b) Patterning of the pad opening (resist, lithography)
c) Etch of top SiC layer. Resist removal
d) Etch of Nitride and bottom SiC layer
e) Deposition of TaN (barrier) and Aluminum



Passivation module (2)

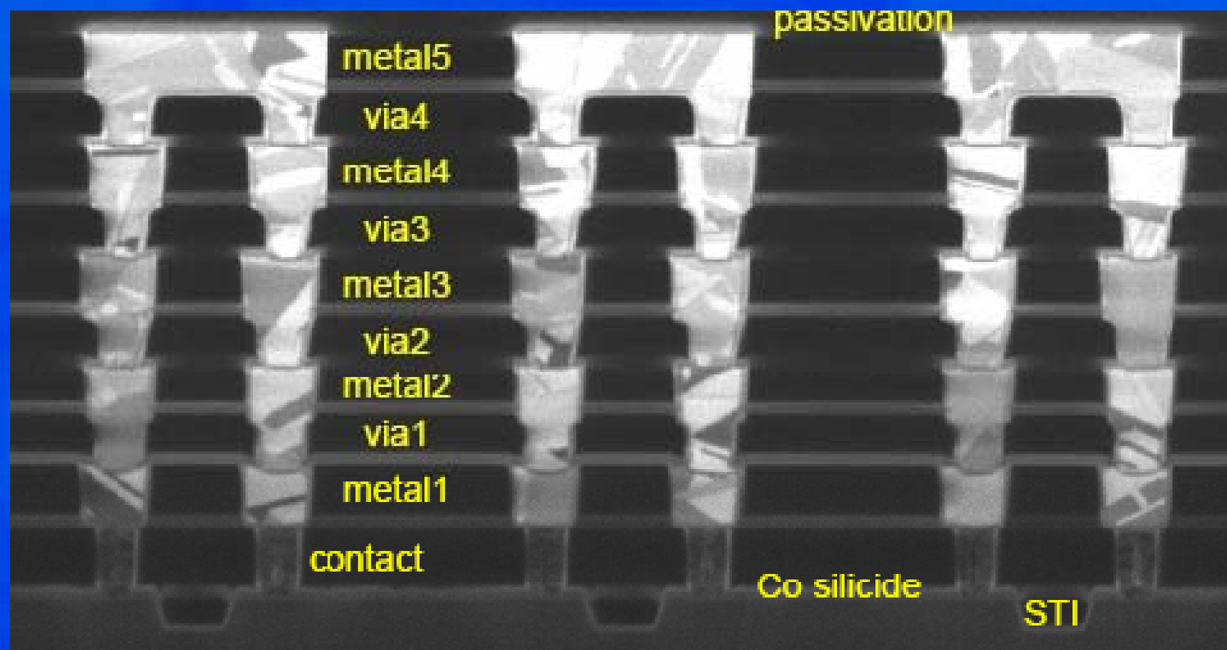
f) Patterning of the Al pad (resist, lithography)

g) Etch of Al and TaN. Resist removal



End of BEOL

The wafers are finished, ready for being thinned, diced and packaged



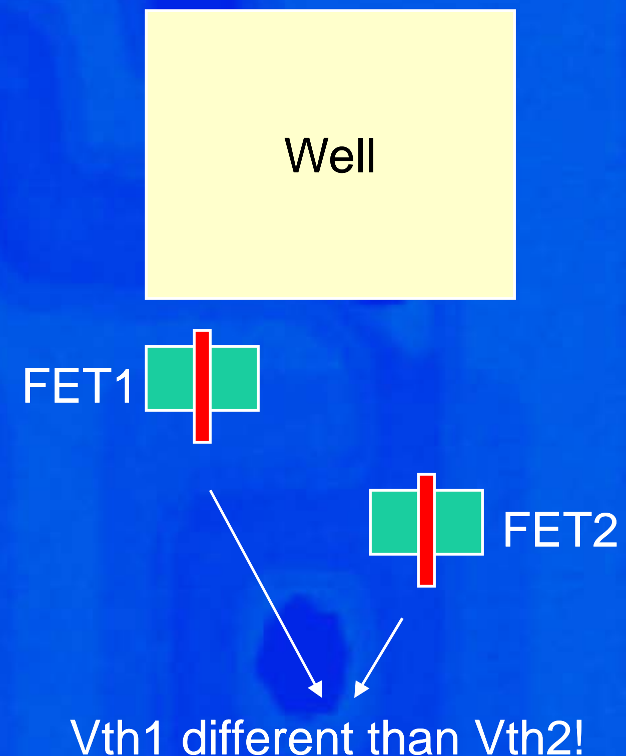
Example: 5 metal stack (all Cu)

Outline

- ✓ Foreword
- ✓ Moore's law
- ✓ Manufacturing of ULSI CMOS technologies
  - Fundamental manufacturing operations
  - Process Flow
    - Front End Of Line (FEOL)
    - Back End Of Line (BEOL)
- ✓ Some consequences….

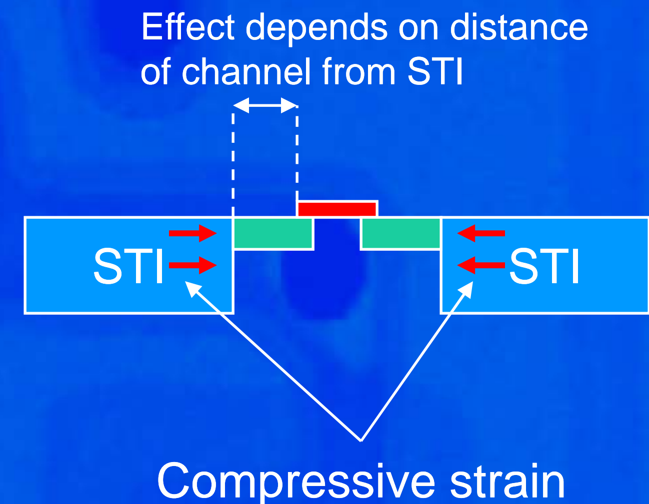
Well proximity effect

- ✓ High energy well implants result in significant scattering of dopants at the well edge, increasing the net doping level and hence threshold voltage for FETs near a well edge
  - The effect is modeled by 1 parameter (which is extracted for post-layout simulations), for estimation – simulation will not be very precise, and it will not depend on the specific layout
  - The use of good design practices for sensitive devices is necessary – place the sensitive devices far from the wells



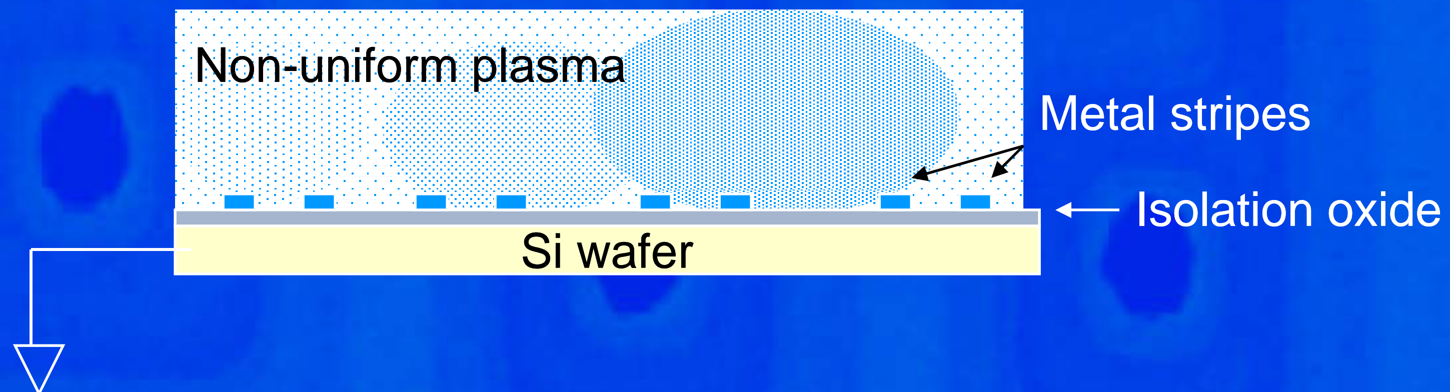
Isolation-induced stress

- ✓ STI induces compressive strain in silicon, which alters mobility of FETs
  - Ids increases for NFETs, decreases for PFETs
  - This effect is modeled for simulation purposes with two parameters, which can be hand calculated (geometric size to measure in the layout)
  - Extraction from layout is fully supported for post-layout simulation



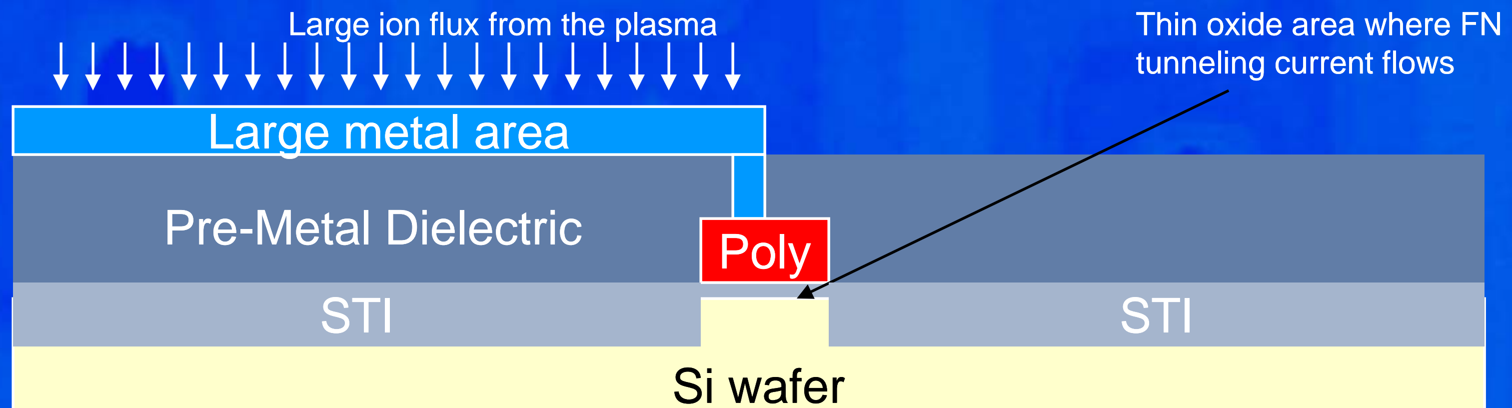
Gate damage due to plasma charging (1)

- ✓ Many processes step for wafer manufacturing take place in a plasma
- ✓ Isolated metal stripes in a non-uniform plasma get charged at different potentials. The wafers substrate is at one only potential (typically grounded), and an electric field builds up in the oxide isolating the metal from the substrate
- ✓ In the absence of any current from substrate to metal, large voltage differences can be reached – exceeding breakdown of the isolation oxide if this is thin (such as the gate oxide)



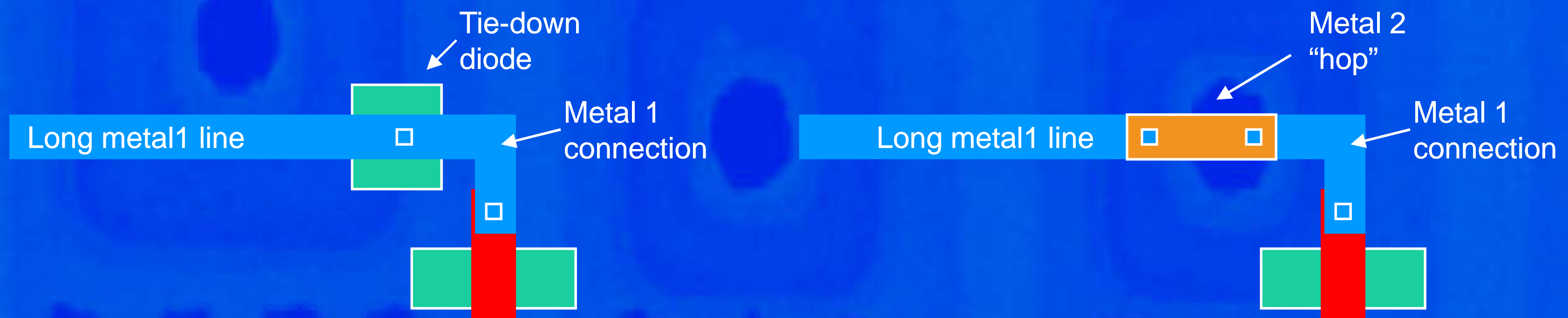
Gate damage due to plasma charging (2)

- ✓ Before the voltage differences reaches breakdown, a current starts flowing across the thin oxide (Fowler-Nordheim tunneling). Current is from electrons injected from substrate to metal
- ✓ This current roughly needs to compensate for flux of positive ions on metal from the plasma. The larger the flux, the larger the current required
- ✓ If large area of metal is exposed to ions, the flux on the metal is large. If the metal is connected to a small area of thin oxide, the FN tunneling current per unit area needs to be large => large voltage across the gate oxide THIS IS CALLED AN ANTENNA!
- ✓ This condition leads to damage to the gate oxide, with consequences on the transistor performance => Vth shift, gate dielectric leakage and increased oxide reliability failure



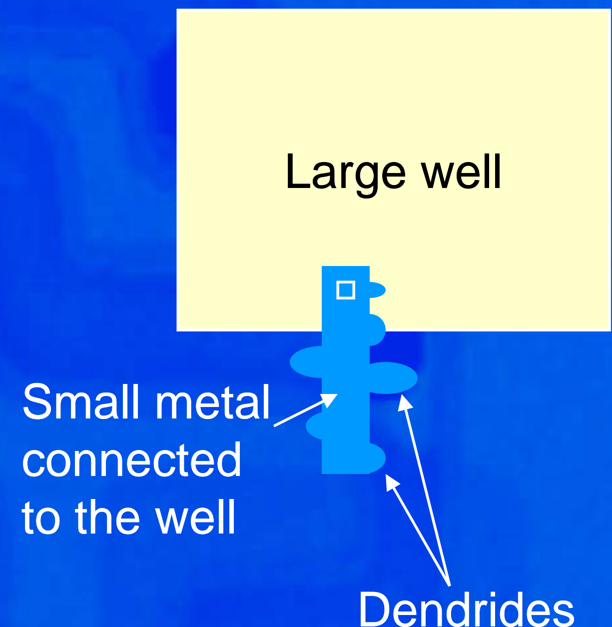
Gate damage due to plasma charging (3)

- ✓ To avoid damage, Design Rules limit the allowable ratio of PC/Metal to thin oxide area. This applies individually to all metal layers (it is not cumulative across layers)
- ✓ Solutions to avoid damage:
  - Add “tie-down” diodes, connected via M1 to the PC (in this case, the limit ratio from the design rules still applies but the tie-down diode area sums – with multiplication coefficient – to the thin oxide area). At wafer processing temperatures, diodes are very conductive and allow current to flow from metal to substrate
  - Introduce “hops” to next metal level. Before the “hop”, only the area of the metal already connected to the thin oxide counts for the antenna. When processing the next metal level, only the (small) area of the “hop” counts for antenna.



Copper dendride formation

- This is a complex effect that can take place during processing of copper metal layers
  - Potential differences built across wells (n and p- wells) can generate currents in the solutions where processing related to a copper metal layer is taking place
  - The induced currents will form “dendrides” around the copper metal line connected to the well, which can lead to shorts to neighbor lines in the same metal level
- To prevent this to happen, Design Rules have been introduced
  - Ratio of metal to well area has to be large

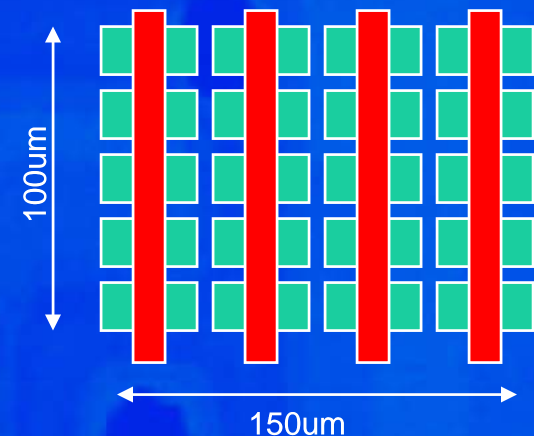


Pattern Density

- ✓ STRICT requirements exist for density of each of the following layers: RX (active area), PC (poly), all metals
- ✓ Requirements are both for the full chip (global rules) and for any small area of it (local rules)
  - Global rules set the limit – upper and lower density – for the full chip
  - Local rules set the limit – upper and lower density – for areas about 100um wide stepped by about 50um across the full design
- ✓ After tape-out, automatic routine at the Foundry will fill in all layers (“filling”), and produce holes in copper layers (“cheesing”). This is unavoidable
- ✓ Some consequences:
  - It is not possible to place “exclude” shapes over area where filling is not wanted. To prevent random metal shapes to be placed over sensitive portion of the design (for instance, where matching is important), cover the sensitive area with uniform metal
  - Some designs that produce excessive local density CAN NOT be manufactured. Example: regions with too large usage of RX. This error is spotted by running a check that predictively estimates the final densities after filling.

Example:

Large array of large transistors (for instance, a large current mirror)



Local RX density migh be eccessive here!
The design HAS to be modified or it will be rejected from fabrication!

To study further…

- ✓ M.Quirk, J.Serda, “Semiconductor Manufacturing Technology”, Prentice Hall, ISBN 0-13-081520-9
- ✓ 1-week course “Silicon Processing for ULSI circuit fabrication”, organized yearly by MTC (Microelectronics Training Center) of IMEC, know also as “Tauber course”
- ✓ To keep updated with newest technologies, attend the IEDM conference (typically in December in either Washington or San Francisco)
- ✓ On the net, to follow latest developments and news from Industry:
  - http://www.fabtech.org/
  - http://www.reed-electronics.com/semiconductor/index.asp?rid=0&rme=0&cfd=1