Super Velo

Theatre of Dreams; LHCb Beyond the Phase I Upgrade
Paula Collins 07/04/16
Special thanks for input to VELO upgraders
Chris Parkes, 2004

SuperVELO: LHCb Beyond the Phase I Upgrade
Main Issues

- 10 x lumi = 10 x data rate
  - rely on miracles from the ASIC, plus all efforts to suppress rate: thin sensors for less hit pixels and less interactions

- 10 x lumi = 10 x radiation hardness
  - thinned, finer granularity sensors essential (extract signal, suppress leakage currents)
  - and/or plan from the start mechanics compatible with yearly changes of the silicon detector

- 10 x lumi = Precision is key
  - thinned sensors (and everything else)

- Timing may become important
  - For which the sensors must be thin
Spot the common theme

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Outline

- Radiation Hardness - Planar Silicon
- Mechanical Issues - Foil and Layout
- Timing: Move to 4D VELO
- New Technologies: Sensors/TSVs
- Conclusions
At SuperVelo fluence levels and even VELO upgrade

- Trapping is very dominant
- “nominal” depletion voltage is unattainable

- New Summary from Tony Affolder here [https://indico.cern.ch/event/487152/](https://indico.cern.ch/event/487152/)
Radiation Damage - Planar Silicon

- Slide from Tony Affolder

State of the art is all from Ljubljana
Measurement to 1e17 possible only by fast amplifier connected to oscilloscope with fine trigger control
Maximum fluence for 4 ke- at 1000 V at 300 µm thickness: 1.6e16
Voltage for 4 ke- at at 300 µm thickness: 3500 V
Thickness will help at bit

\[ b = -0.683 \]
\[ K = 26.4e/V \]

Thinning to 100-140 µm, could buy ~20% more charge
Foil: Material Contribution

Foil contributes a lot of material - impact on low Pt tracks

During VELO Upgrade optimisation we learned some tricks, pixel foil is better than current foil

Foil is extremely non uniform; so far no one complained but will we be systematics limited in future?

What follows is very implausible but are plausible solutions out there?
PLT* Foil - Partial Light Tube

- Very thin ~ 50 um
- short distance between supports
- more uniform radiation length
- simple shape (beam simulations, systematics)
- reduced requirement on precision
- No dangers of silicon clearance to foil, blind insertion

But: in primary vacuum?
May need additional thin, tensioned sheet
Or with decent pumps may survive

*From discussion with P, Lars & Tim
Extreme solution: Instrument the foil

- Main motivation: remove scattering before first measured point, improve IP resolution. Secondary consideration; improve PV resolution
- Modern monolithic devices are thin and flexible
- MAPs can be fully efficient at 25 um
- An instrumented foil could be have a simple round shape
- However the MAPs services, (ASICs, cooling, cabling) can introduce significant material

Advantages:
- individual movement/replacement
- mechanically stable, big choice of material, construction techniques
- decoupling of two VELO sides
- low material before first measured point

But
- foil on average further from IP
- wakefields may be an issue

Blast from the past: Individual roman pots with motorised arms

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Alternative foils
VELO Layout

Dedicated timing planes
(different granularity?)

Or, double (or triple) sided modules a la CMS for tracklet reconstruction

Getting closer
Foil inner radius - not much play
dedicated ASIC design could round inner corners
slim edges can gain us ~10-20%

Keep down material before the second measured point
Keep down material before the second measured point
High momentum tracks: keep the first measured point as precise as possible (i.e. fine pitch and good position information)

\[ \sigma_p^2 = \frac{e^2}{2} \left( \frac{x}{X_0} \right) \left( 0.0136 GeV \sqrt{0.038 \ln \left( \frac{X}{X_0} \right)} + \Delta \sigma \right)^2 + \frac{\Delta \sigma^2 + \Delta \sigma_{\text{ex}}^2}{\Delta^2} \]
Rethink: Replaceable VELO

- Experiments such as NA62 plan to replace silicon “whenever necessary” due to radiation damage

- Access to the VELO is indeed difficult due to vacuum, beam pipe venting and possible contamination, radiation exposure and disposal of irradiated pieces

- But we are not in principle totally inaccessible, and we have a large gradient between the most and least irradiated module positions. Can a total rethink of the mechanical design produced a super velo where the most irradiated parts are replaceable? The cost of the silicon and asics is “minor” compared to the cost of the whole project, due to the small number of sensors

Can we foresee more imaginative solutions?
- Slot in/ slot out cassettes for module replacements, or replacement of entire half?
- Operational garage positions with conveyer belt style bringing modules to the hottest regions?

If we go this way - significant R&D effort on mechanics must start very soon…
Magnetic field, a path well trodden

- BTeV design already implemented a magnetic field
  - reject imprecise low momentum tracks and improve discrimination of vertex trigger
  - Photon conversions become nicely visible
  - With all information in trigger is it necessary? No particular objection from VELO side as long as patrec not excessively complex: tracking arguments needed
Module Material Budget

- Upgrade Currently just below 1% per module (perpendicular)
- cf 0.2% X0 for CLIC with ultra thin silicon and ASICs, CFRP/SiC supports
- cf 0.3% for ALICE upgrade (vs current impressive 1.12%)
- NA62: uchannel cooling with ultra thin material budget
- For us: factor 2 may be a goal
Timing from the VELO: what is possible?

2D strips $\rightarrow$ 3D pixels $\rightarrow$ 4D pixels with timing

- Current pixel pattern recognition is "rolls royce" due to the minute occupancy at the Upgrade. At the Upgrade of the Upgrade how are we affected by a factor 10?

- Vertex fitting with time tagged tracks - could 10 ps be useful at pixel/track level? (study from Giovanni Punzi, [link](https://agenda.infn.it/getFile.py/access?resId=0&materialId=slides&contribId=15&sessionId=9&subContId=2&confId=7567))

- Misassociation of B vertices with primary vertex will become significant at Upgrade of the Upgrade. Use of time information would certainly help; is 100-200 ps enough? Can this information also help triggering?

- Can timing information be used to attack ambiguities when extrapolating from one plane to the next to make track stubs?

- Could VELO timing be used in combination with the TORCH by providing a $t_0$ of the primary vertices. 10 ps would be sufficient to time tag most primary vertices and a worse resolution could still be helpful (Roger Forty)
Timing from the VELO: what is possible?

2D strips $\rightarrow$ 3D pixels $\rightarrow$ 4D pixels with timing

- In all cases the achieved resolution will be a combination of what is possible from the electronics + sensor combination.

- Remember that this has to happen while live streaming a tremendous data rate, providing excellent resolution with tiny pixels, with a lightweight radiation resistant device capable of operating at low temperature in a vacuum.

- Many reviews exist e.g.
  - timing below 100 ps is “non trivial”; 10 ps is a “barrier” to break
  - silicon, diamond most reasonable options for LHCb; $<$ 100 ps is “non trivial”
### ASIC for HEP, state of play

<table>
<thead>
<tr>
<th>Feature</th>
<th>Timepix3*</th>
<th>VeloPix*</th>
<th>TDCPix</th>
<th>FEI4a</th>
<th>Super VeloPix?</th>
</tr>
</thead>
<tbody>
<tr>
<td>Readout type</td>
<td>Continuous, triggerless, ToT</td>
<td>Continuous, trigger-less, binary</td>
<td>Continuous, trigger-less, binary</td>
<td>Triggered</td>
<td></td>
</tr>
<tr>
<td>size</td>
<td>1.96 cm²</td>
<td>1.96 cm²</td>
<td>1.62 cm²</td>
<td>3.83 cm²</td>
<td></td>
</tr>
<tr>
<td>Timing resolution/Power consumption</td>
<td>1.5625 ns, 18 bits</td>
<td>25 ns, 9 bits</td>
<td>75 ps**</td>
<td>triggered</td>
<td></td>
</tr>
<tr>
<td>Pixel matrix, pixel size</td>
<td>256 x 256</td>
<td>256 x 256</td>
<td>45 x 40</td>
<td>336 x 80</td>
<td>50 um x 250 um</td>
</tr>
<tr>
<td>Radiation hardness</td>
<td>N/A</td>
<td>400 Mrad, SEU tolerant</td>
<td>SEE tolerant</td>
<td>250 MRad, SEU tolerant</td>
<td></td>
</tr>
<tr>
<td>Peak hit rate</td>
<td>80 Mhits/s/ASIC 1.2 khits/s/pixel</td>
<td>900 Mhits/s/ASIC</td>
<td>210 Mhits/s/ASIC</td>
<td>1.5 Ghits/s/ASIC 50 khits/pixel (on ASIC)</td>
<td></td>
</tr>
<tr>
<td>Energy resolution</td>
<td>~2 keV</td>
<td>N/A</td>
<td></td>
<td>6 keV</td>
<td></td>
</tr>
<tr>
<td>Max data rate</td>
<td>5.12 Gbps</td>
<td>20.48 Gbps</td>
<td>~12 Gbps⁻¹</td>
<td>160 Mbps (triggered)</td>
<td></td>
</tr>
<tr>
<td>Technology</td>
<td>130 nm CMS</td>
<td>130 nm CMOS</td>
<td>130 nm CMOS</td>
<td>130 nm CMOS</td>
<td>65 nm CMOS</td>
</tr>
</tbody>
</table>

*Tuomas Poikela, Pixel 2014
**Currently sensor adds >150 ps
***dynamic phi pairing to cope with rate
ASIC for HEP, state of play

- Sensor signal amplified and shaped
- Single threshold crossing time digitised by TDC
  - embedded in ASIC or external

- For more accuracy; sample and digitise full waveform with multiple samples
- Sampling and digitisation can be decoupled e.g. DSP

- Timewalk can affect the crossing of the threshold for different amplitude samples, or in case of changing shape
- Can correct using pulse amplitude (offline)
- CFD (constant fraction discriminator) can compensate

IRL: Timing jitter (external/internal) signal variations (amplitude, shape), electronic linearity etc…
NA62 GTK

• Study of very rare Kaon decay: $K^+ \rightarrow \pi^+\nu\nu$

• Time tag the $K^+$ tracks to match the $\pi^+$ track in the RICH

• GTK: three stations of hybrid silicon pixels with $\leq 200$ ps rms resolution per station

• Sensor area: 60 mm x 27 mm readout by 10 TDCpix chips

• Pixel dimensions 300 x 300 $\mu$m$^2$

See M. Fiorini, F. Marchetto
https://indico.cern.ch/event/487152/
GTK Timing

- Timing with DLL based TDC in the periphery - one timing register shared per 5 pixels
- 210 Mhit/s/chip
- 4 x 3.2 Gbit/s serialisers
- CMOS 130 nm technology
- Offline ToT compensation

lab result with laser

Beamtest result with particles

NA62 datataking result

75 ps

200 ps
Difference can be partially attributed to sensor:

- Landau fluctuations

Differences in signal shape (particles hitting in different points experience different weighting fields)

lab result with laser

Beamtest result with particles

NA62 datataking result
Timepix3/VeloPix

- Timepix3 already has a timing feature
- When the output of the amplifier exceeds the programmable threshold, the discriminator rises and starts the local asynchronous 640 MHz clock
- The clock is stopped by the rising edge of the global 40 MHz clock
  - The Medipix ASIC family will now move to 65 nm
  - 65 nm will bring more functionality for the same power (must stay in uW range per pixel)
  - Can we exploit the 65 nm
    - smaller pixels
    - greater speeds (x10 “conceivable”) - also can split columns
    - include timing functionality e.g. extend Timepix3 oscillator concept: rough timing?
    - TSV will allow more processing per pixel

Testbeam result: timewalk corrected resolution ~ 1.6 ps

A. Nurnberg, Timepix3 timing resolution in testbeam,
Sensors for Timing

Thin detectors have a role to play - and are good for radiation hardness - but even then:

• extra gain is needed for reasonable timing resolution
• straggling still an issue
• Time response of irradiated sensors not well known

• LGAD sensors proposed and manufactured by CNM

• doping layer to introduce a high field region to induce avalanche and increase gain factor 10, still low gain compared to sipms or APDs

• Thin, parallel plate, high resistivity, electric field, low leakage current (shot noise) several runs achieved with various gains

SAMPLEC + Fast Si/Diamond: currently ~40 ps resolution obtained (laser). Fast timing key element of ATLAS AFP project: quartz based cherenkov detector coupled to MCP-PMT (34 ps in beam test)
Tracking with precise timing (1)

- INFN Bologna, Cagliari, Ferrara and Milano LHCb Groups and INFN TIFPA plan to pursue an R&D program within INFN and the Italian Minister of University and Research.
- Propose to build an innovative silicon pixel detector with embedded tracking capabilities. Main features:
  - Radiation hardness \( >10^{16} \) 1 MeV n_{eq}/cm²
  - Time resolution \( \sim 20 \) ps, spatial resolution better than 40 \( \mu \)m
  - Tracklet reconstruction
  - Fast track finder for real-time tracking
- Significant expertise in many different areas
  - Sensors, front-end ASIC design, TDC design, FPGA-based read-out and trigger systems, data acquisition systems
Silicon pixel sensors

- FBK (Fondazione Bruno Kessler, Povo, Trento) produced pixel sensors for different experiments (e.g. ATLAS, NA62)
  - Excellent interaction to tailor production
- FBK and INFN are partner institutions of TIFPA (Trento Institute for Fundamental Physics and Applications)
  - Special conditions apply to INFN for selected production lots
Bump bonding issues

- Traditionally the cost issue has been sidestepped due to the small area of the VELO
- however we start to suffer yield problems when we go thin (even at current pitch) and situation is worse at lower pitch

For current upgrade we already saw bowing issues
- solved by handle wafer process (slow, expensive)
- possible solutions with stress compensation layers may be possible

Solder bumping standard pitch currently 50 um
R&D is currently looking to push these technologies down to about 10 um bumps on 20 um pitch
Some of this R&D is part of the ongoing intense 3 packaging effort but some way to go
see for example summary talks from CPIX14
Radiation Damage - non planar
3d, slim edge, and exotic..

Similar charge performance to planar
(with less power)
Possible improvement with smaller cells
Etching smaller columns for 50x50 µm²
cells not trivial
Implies thinner sensors, less charge
Capacitance could become an issue

Fast signal, full depth, low V_{dep}
What about monolithic devices?

In contrast to hybrid pixel detectors, the sensitive volume and part or all of the circuitry is combined in one piece of silicon. The generated charge is collected on a dedicated collection electrode.

Commercial CMOS processing (many foundries, larger wafer diameter, low cost per area, stitching
Thin detectors ~ 50 um
Great precision and small pixels
No bump bonding nightmares

Traditional MAPS solution
charge collected by diffusion
Few transistors per pixel
rolling shutter readout

not good for our speeds and our environment
e.g. DEPFET @ BELLEII, 20 us / frame
Steady increase in HEP

ALICE

BELLE II

STAR

Depfets for Belle:
50 x 75 micron thinning of matrix area to 75 micron
0.21# X0 per layer
More speed and radiation tolerances out of monolithic devices

**Example: HV CMOS**

CMOS process with deep n-well collection electrode

- Structures realized in 0.18 and 0.35 μm CMOS
- Substrate resistivity ~ 10 Ohmcm
- **Biasing of the substrate up to ~100V** → homogeneous depletion layer (~ 14 μm deep)
- First stage amplification in pixel and additional electronics (e.g. discriminator etc.) possible
- Radiation tests with FEI-4 glue bonded indicate radiation hardness up to $10^{16}$ n$_{eq}$cm$^{-2}$

D. Münstermann, VERTEX 2013

D. Münstermann, VERTEX 2013

FCG-hh meeting - P. Riedler, 4.2.2015
The variety of packaging solutions offered by industry is staggering and already today widely sufficient for most and perhaps all HEP applications

Except that:

- There is a huge fragmentation of suppliers
- Entry fees are high
- Our volumes are pathetically small

Under Bump Metallisation is deposited on the front side of the wafer. This is identical to the step used normally by the bump bonding suppliers and will permit the finished die to be flip chip assembled to sensors which have been bumped with a solder bumps.

The front side of the wafer is bonded using a temporary adhesive to a dummy support wafer. The wafer is then thinned to 120 um (2 times the diameter of the TSV opening).

Vias are drilled in the wafer using deep reactive ion etching and the vias are coated conformally with an insulating layer.

Contact holes are etched through the insulation in the bottom of the vias and a 5um thick Cu layer is deposited on the side of the vias and on the back side of the wafer. The Cu layer is then etched to form the redistribution layer on the backside.

The back side of the wafer is passivated and the openings for the BGA contacts etched. An UBM metallization is deposited on the BGA contact pads the same way as on the front side.

The wafers are released from the support wafer and transferred onto a dicing tape. Finally the wafers are shipped for subsequent dicing and flip chip assembly.
Back to the ASIC: TSVs

- Project with Ultra thin TSV processed Timepix3 underway with encouraging results
- Tiling of large areas for low mass detectors
- Bond wiring not needed
- Surprising benefit: nice flat chips!

Ultimate application for VELO: combine TSV stacking and microchannel cooling?

https://nanoheat.stanford.edu/
Conclusions

Thin, Planar, Silicon still the most attractive option
• light, thin, highly segmented, ease of processing, non magnetic, vacuum resistant, radiation hard...
• watch out for dependency on few suppliers

3D integration is the holy grail
• liberation from wire bonding, bump bonding
• ability to add local processing e.g. cluster formation, timing…
• However development is slow, and costs high...

For the ASICs + sensors, the speed seems achievable, but how many other extra features can we pack in?
• Timing (at reduced granularity? 100 ps?)
• segmentation (approach ~few um?)

Global design - need a real effort not only on the sensor technology but also the mechanics
• many incremental improvements possible
• Quantum step with foil design?
• Pattern recognition and trigger issues to be explored
Focusing on the ASIC/sensor
• We have a superb design team in place which has just completed the VeloPix design
• Closely linked to CERN and Medipix support, where the steps are being taken now to migrate to 65 nm technology
  • sharing of blocks e.g. periphery
• Plus, potentially, a possibility to develop and test fast sensors - a critical item for us, to establish what our limits really are for our baseline, electron collecting, irradiated sensors
Can we exploit this opportunity - without detracting from the ongoing, critical upgrade work