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SHIPDAQ update

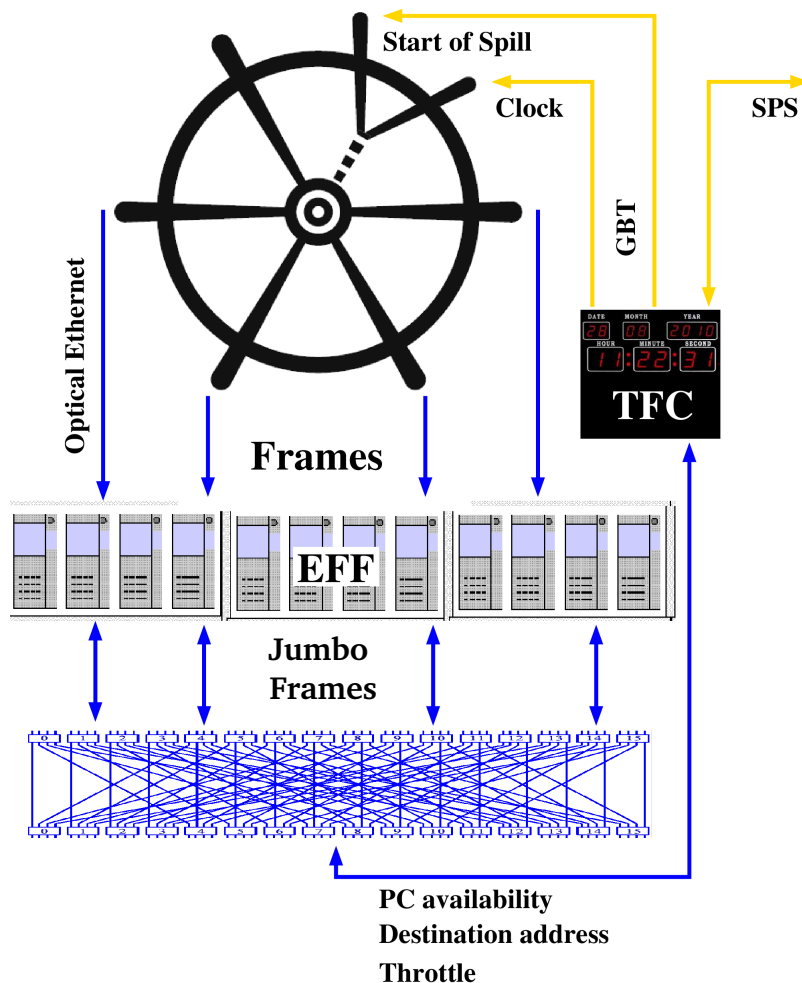
On the behalf of the SHIPDAQ team (CERN, NBI, UCL, UU)

Richard Brenner (Uppsala University)





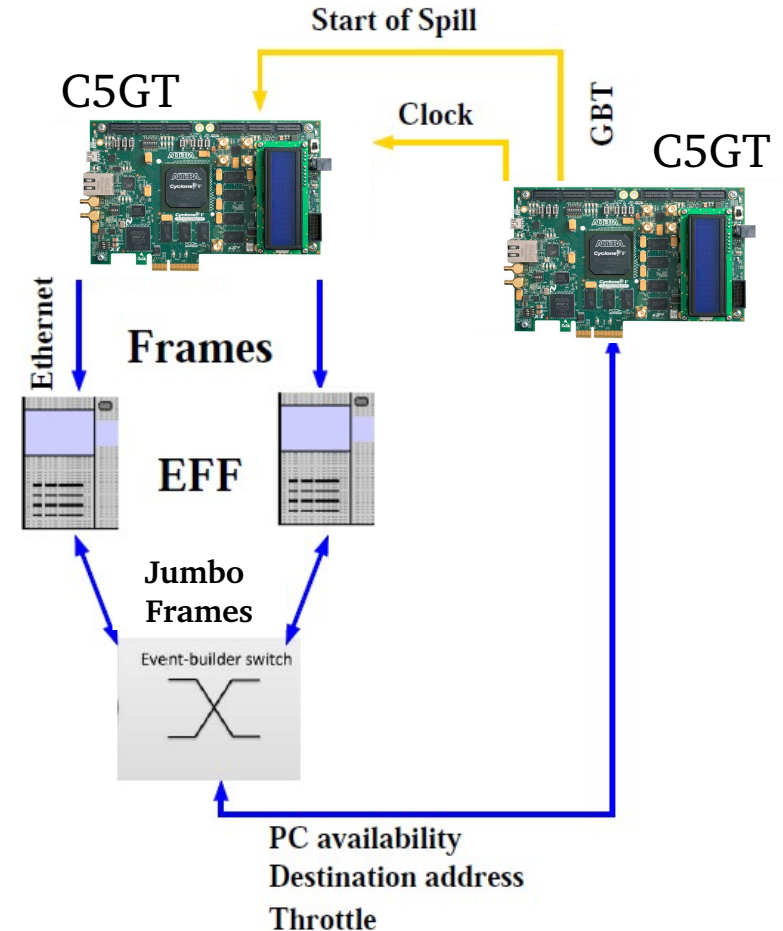
Architecture



- In line with current TDAQ architectures developed for LHC experiments → minimal data processing on-detector.
- Low data rate and non critical latency constraint in SHIP compared to LHC.
- No timing from bunch structure in SHIP requires good timing on-detector.

Demonstrator for TDR

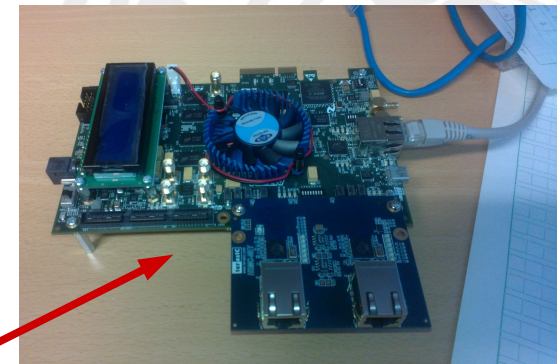
- Goal:
 - Demonstrate distribution of timing and control with GBT.
 - Transmission of time stamped FE data on Ethernet to EFF
- No timing from bunch structure in SHIP requires good timing on-detector.
- Definition FE data frames.
- Use mid-range FPGA hardware to build an affordable system.



Work in progress

”CHEAPDAQ”

- Work started on demonstrator TFC-FE in Uppsala
 - Two master students Filos Vasilelos and Jiheng Chen
 - Supervised by senior engineer Leif Gustafsson
- Cyclone V GT FPGA Development Kit from Terasic purchased by NBI for the project
- GBT-FPGA package downloaded from CERN GBT Project



The FPGA

Towards first milestones

- Preparations → summer 2016
 - *Evaluation and high speed interfaces on FPGA ongoing.*
 - *Evaluation of GBT and Ethernet between nodes.*
- *Milestone 1- fall 2016*
 - *Definition of the common readout protocol - based on preparations and updated input from SHIP detectors.*