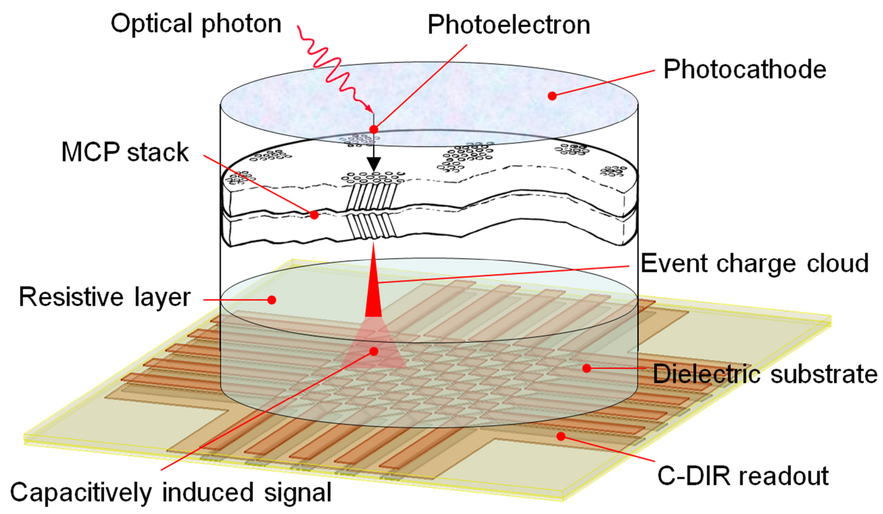
Picosecond imaging using a capacitive charge division readout

T M Conneely[a, b], J S Lapington[b]

(a) Photek LTD, 26 Castleham Road, St. Leonards-on-sea, TN38 9NS
(b) University of Leicester, University Road, Leicester, LE1 7RH

The Capacitive Division Image Readout (C-DIR) is a novel imaging readout for MCP based resistive sea detectors. Resistive sea detectors operate by capacitively coupling the output from the MCP to a readout anode through a ceramic back plate. One of the advantages of this technique is that the readout anode and electronics remain outside the detector vacuum, hence are isolated from the high-voltage inside the detector and do not require vacuum feed-throughs.

The capacitive nature of the resistive sea signal coupling allows a new kind of charge sharing readout anode, which uses purely capacitive coupling between a discrete array of electrodes on the anode to divide the charge between four readout nodes. Compared with traditional devices such as the wedge and strip s, C-DIR reduces the capacitive load for amplifier inputs, allowing the use of high speed amplifiers allowing detectors to sustain a high event rate

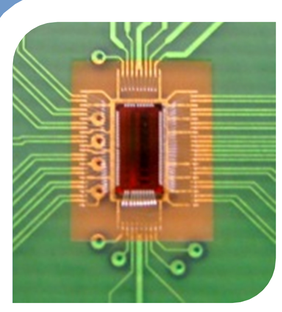


Readout Electronics

NINO ASIC

Originally an 8 channel differential amplifier /discriminator developed at CERN. The time over threshold technique can provide pulse height.

- 10 ps RMS jitter on the leading edge
- >>10 MHz maximum rate
- The time-over-threshold technique uses the discriminator output pulse width to determine the event charge

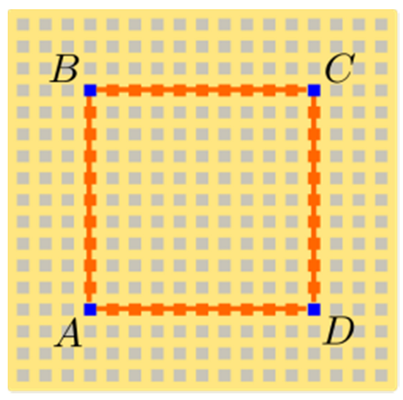


High Performance Time-to-Digital Convertor A programmable TDC developed for ALICE time-of-flight RPCs at the LHC

- Two modes of 100 ps LSB resolution with 32 channels or 24.4 ps LSB resolution with 8 channels.
- Default maximum rate is 2.5 MHz per channel, can be increased beyond 10 MHz using higher logic clock.

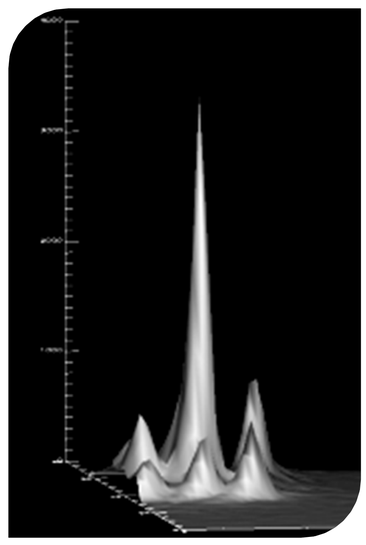
Prototype Results

To prove the C-DIR anode concept a simple pattern was manufactured, this was a square array of pads on FR4 PCB board, using a border of higher capacitance as charge collectors (achieved using SMT capacitors). Each readout node is connected to a NINO input, and a CAEN HPTDC module is used to measure the discriminator outputs leading edge time and pulse width.



Imaging Performance

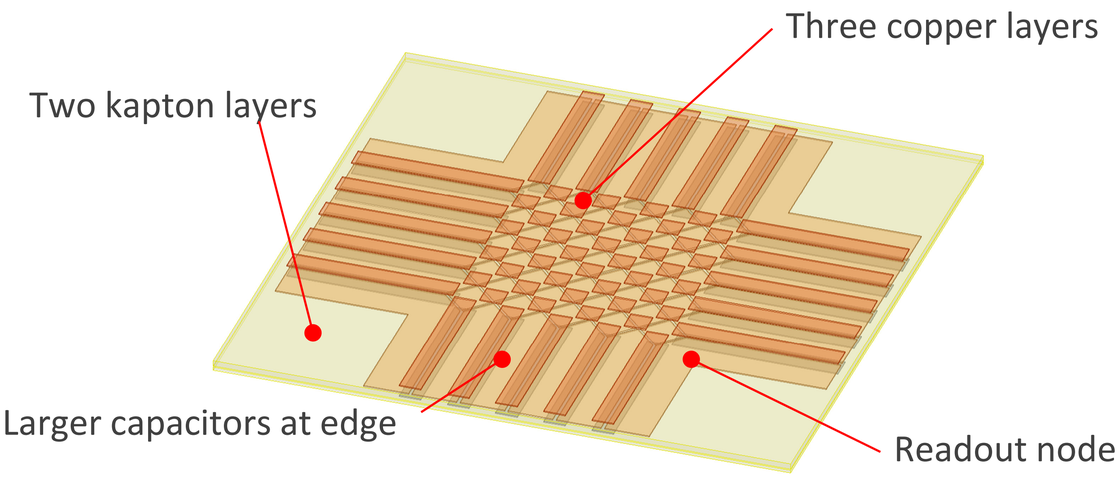
To demonstrate the imaging performance of the prototype, a 3×3 1 mm pitch mask was used (with a 50 µm central hole, and 25 µm bordering holes). The detector was then illuminated with a pulsed laser, attenuated to single photon levels. The FWHM of the detector response was approximately 300 µm, as the anode was 3×3 cm this gives a 100×100 pixel device with <50 ps event timing.



Prototype Limitations

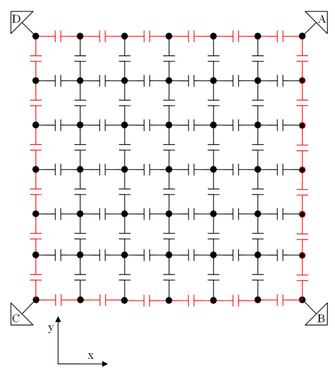
- USB readout noise from the CAEN HPTDC module, leading to a high threshold
- Low charge collection efficiency limiting spatial dynamic range

Optimised C-DIR pattern design

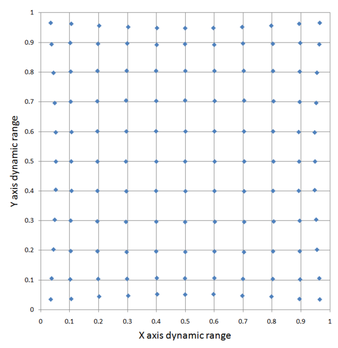


- Simple to manufacture – using standard flex PCB
- Higher capacitance at edges maintains readout linearity
- 8 pF preamplifier input capacitance for a 25.4 mm2 pattern
- ~85% charge collection efficiency

Effective equivalent circuit



Simulated linearity using FEA model



HPTDC Module

We are currently developing our own modular HPTDC device,

- A modular architecture, allowing multiple HPTDC boards
- One HPTDC board will provide 64 Channels with 100 ps LSB resolution or 16 Channels with 25 ps LSB resolution
- LVTTL or LVDS inputs supported natively, with adapter boards possible for supporting other logic standards
- USB readout and control
- On-board FPGA for control and data processing

The design will become a general purpose TDC box suitable for bench top experiment, and will be used for the HiContent and IRPICS detectors also being developed between the Leicester of University and Photek Ltd.

University of Leicester

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