The Belle II DEPFET vertex detector: current status and future plans

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On behalf of the DEPFET Collaboration

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Outline

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SuperKEKB

- KEKB machine upgrade
- Belle II Vertex Detector

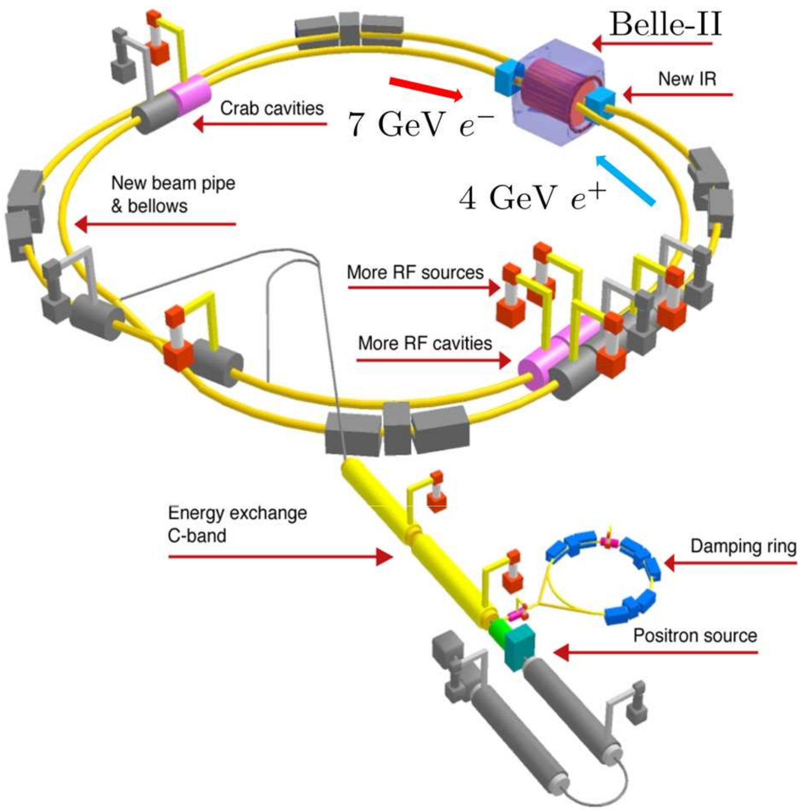
DEPFET

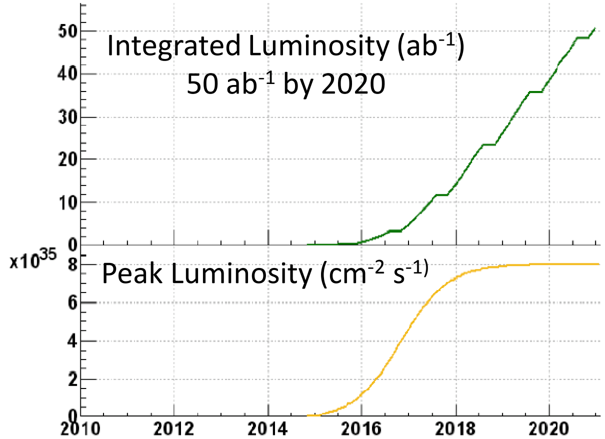
- Fundamentals
- System elements

Belle II PXD

- Detector layout
- Sensor tests
- Thermal studies

KEKB upgrade plan: SuperKEKB Flavour Factory



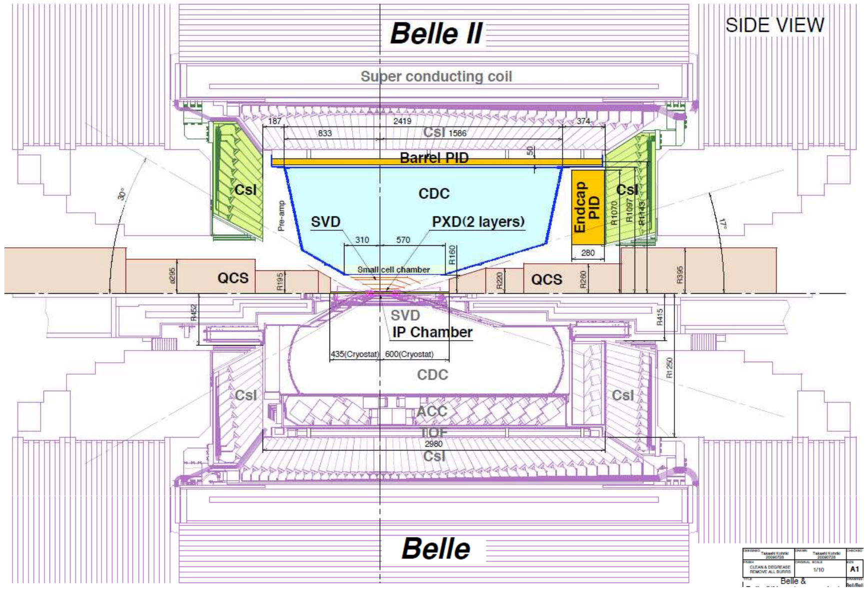


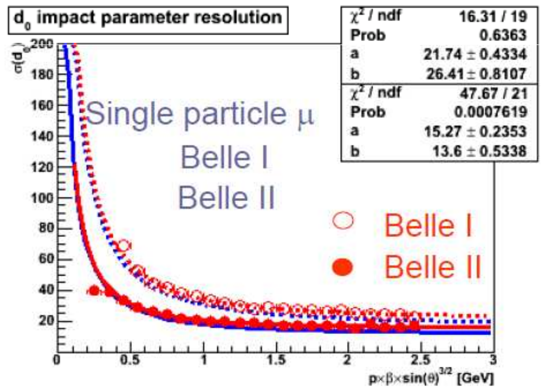
Beam parameters		KEKB		**SuperKEKB**		units
		LER	HER	LER	HER	
Beam energy	E_b	3.5	8	4	7	GeV
Vertical beam size	d_V	0.94	0.94	0.048	0.056	µm
Horizontal beam size	d_H	150	150	10	11	µm
Beam currents	I_b	1.64	1.19	3.60	2.60	A
Luminosity	**L**	**2.1 x 10^{34}**		**8 x 10^{35}**		**$cm^{-2}s^{-1}$**

- Asymmetric energy (4 GeV, 7 GeV) e^+e^- collider at the $E_{cm} = m(\Upsilon(4S))$ to be realized by upgrading the existing KEKB machine
- Final luminosity $8 \cdot 10^{35} cm^{-2} s^{-1}$, 40 times higher than the existing KEKB Factory
- Luminosity will be achieved by squeezing the beams (nano beam)

Belle II PXD group has decided on DEPFET as baseline

Belle II Silicon Vertex Detector





At such high luminosity, we will collect higher number of events but…

- Higher background
  - →Radiation damage and occupancy and fake hits
- Higher event rate
  - → Higher rate trigger, DAQ and computing

DEPFETs for the two innermost layers (L0+L1)

	Belle	Belle II
# layers	4	6
Inner radius (cm)	1.5	1.4
Outer radius (cm)	8	14

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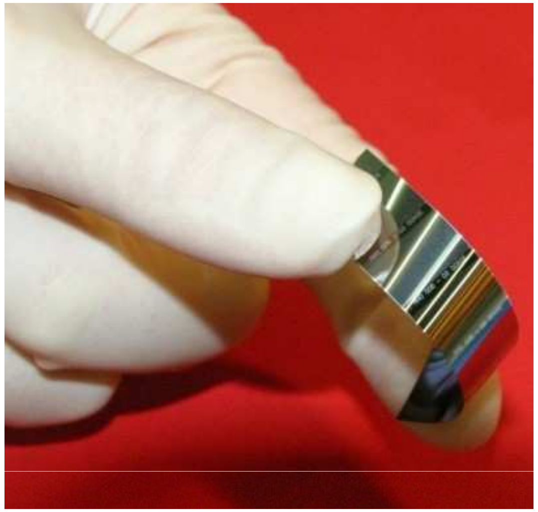
Belle II requirements

	Belle II
Occupancy	0.4 hits/μm^2/s
Radiation	> 1Mrad/year
Frame time	20 µs (continuous r.o. mode)
Momentum range	Low momentum (< 1GeV)
Acceptance	17^o-155^o



The combination of resolution, mass and power is a substantial challenge

- Required spatial resolution (~10µm) → Moderate pixel size (50 x 50 μm^2)
- Lowest possible material budget (0.19% X_0/layer)

→ The DEPFET technology can cope with this challenging requirements

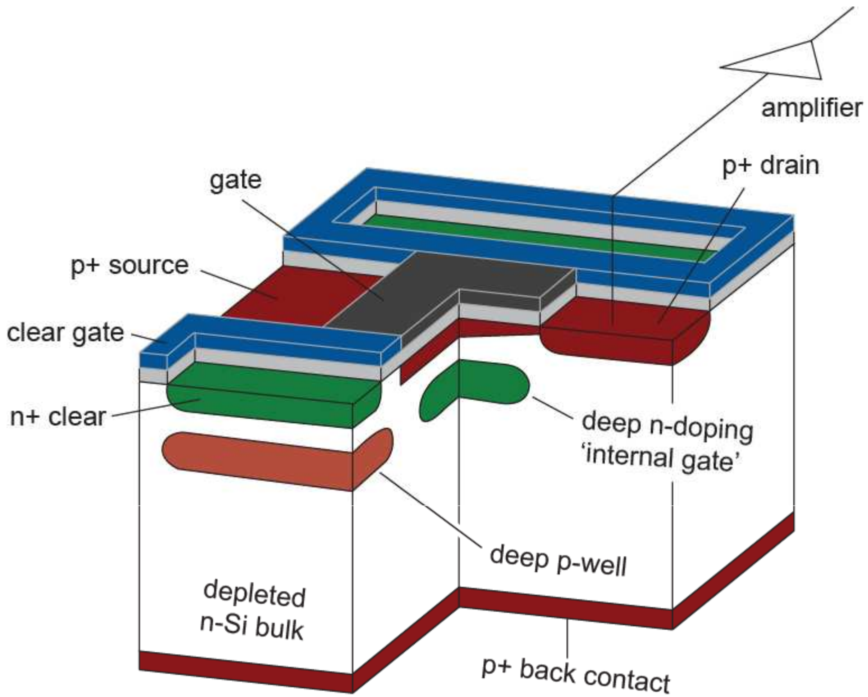
Tight schedule to develop a complete detector system by 2015

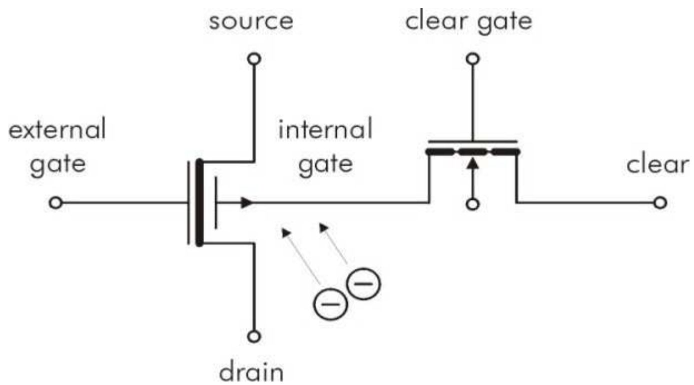
DEPFET – DEpleted P-channel Field Effect Transistor

- Each pixel is a p-channel FET on a completely depleted bulk (sideward depletion). Charge is collected by drift
- A deep n-implant creates a potential minimum for electrons under the gate (internal gate)

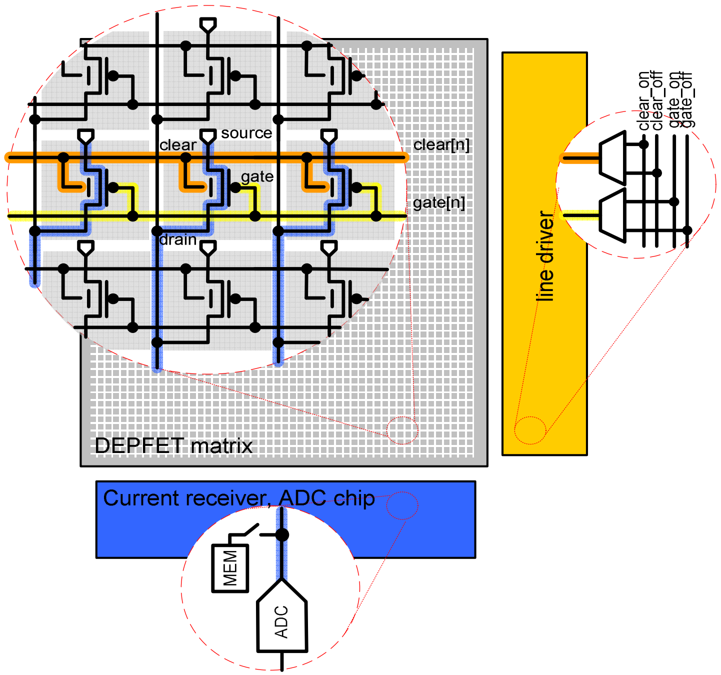
- Signal electrons accumulate in the internal gate and modulate the transistor current (g_q≈400pA/e^-)
- Accumulated charge can be removed by a clear contact

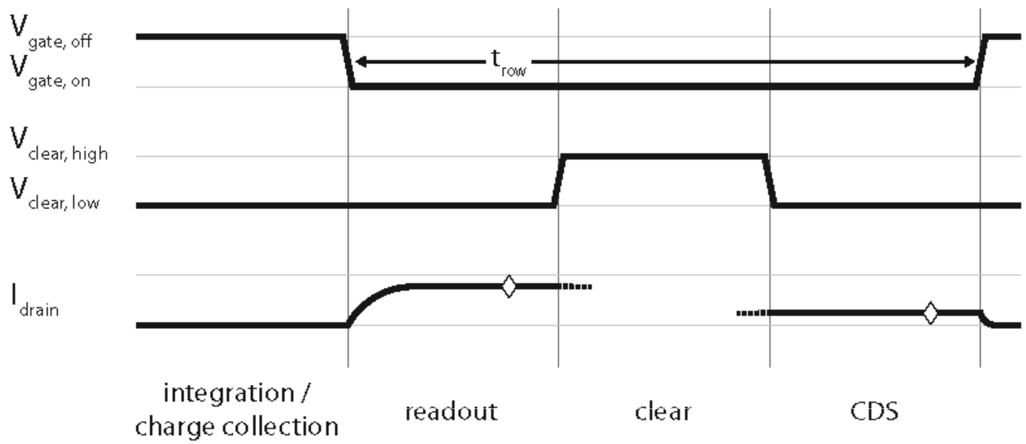
- Detection and internal amplification
- Good signal-to-noise ratio
- Low power consumption
- Thin detectors





Operation mode: Row wise readout





Row wise readout (Rolling Shutter)

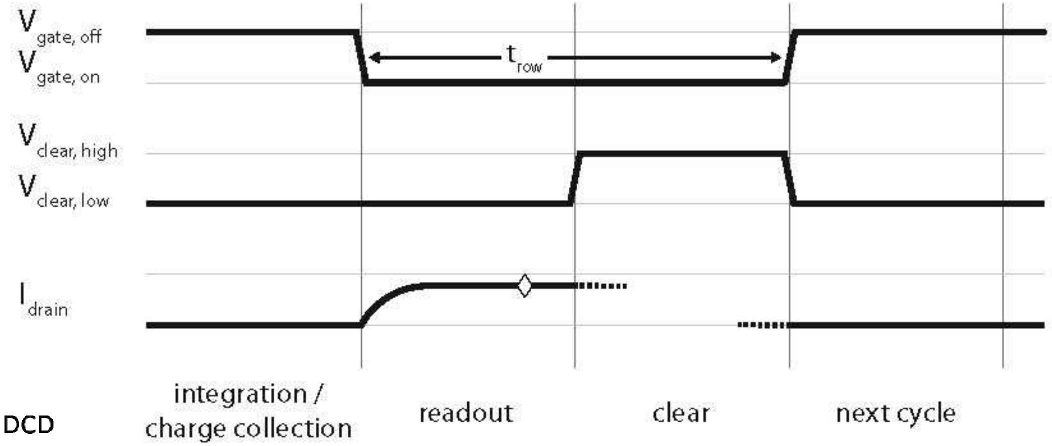
- (If CDS) Select a row, read the current, clear the DEPFET and read the current again. The difference is the signal.
- Single sampling with pedestal substraction afterwards (Baseline)
- Low power consumption: Only one row is active at a time; Readout on demand.
- Steering chips needed (Switchers) and limited frame rate.

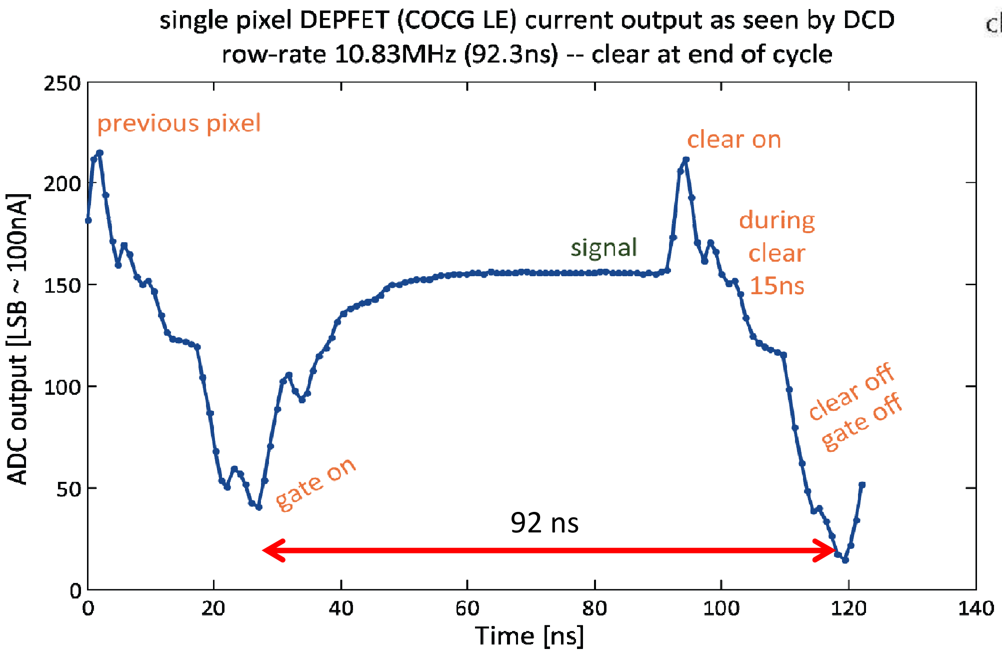
Single sampling

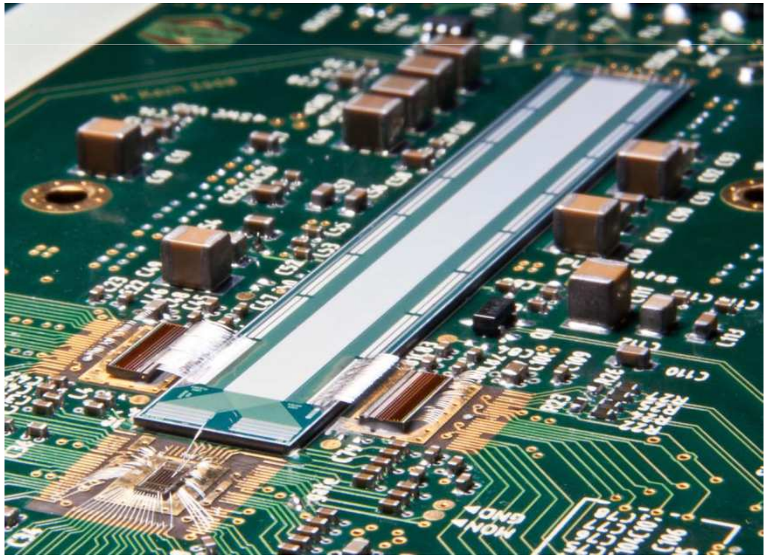
Abandon CDS in favour of speed, move clear to end of cycle

PXD readout time: 20 µs (50KHz frame rate)

Read-clear cycle: 100 ns



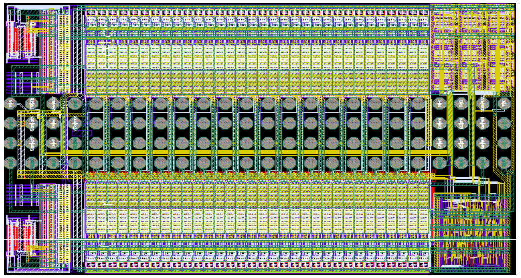




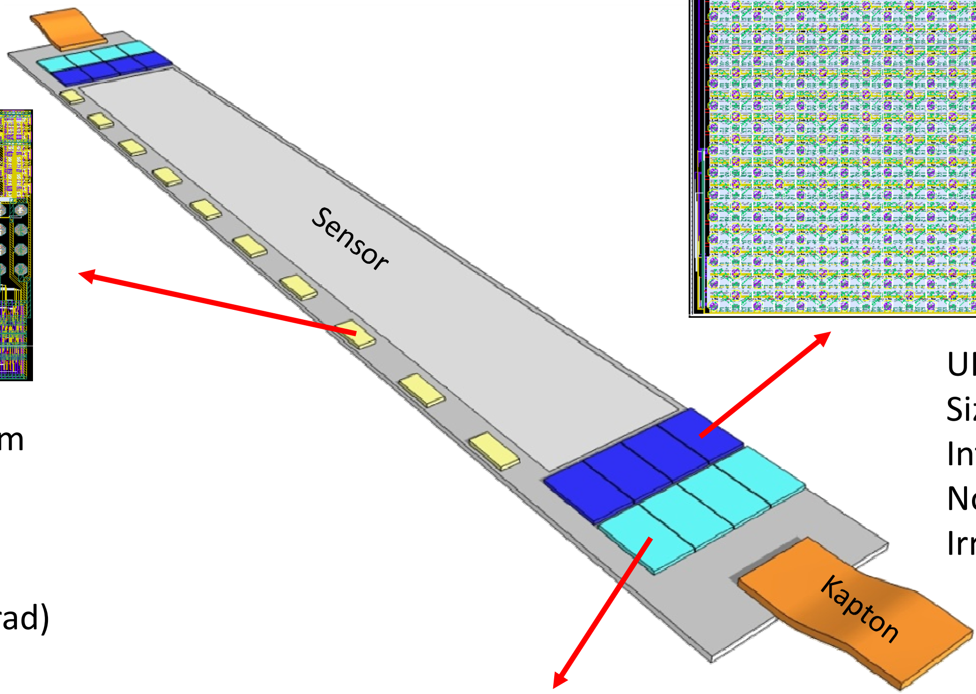
92 ns row time. The sampling could be even reduced further without compromising the signal settling

DEPFET auxiliary ASICs

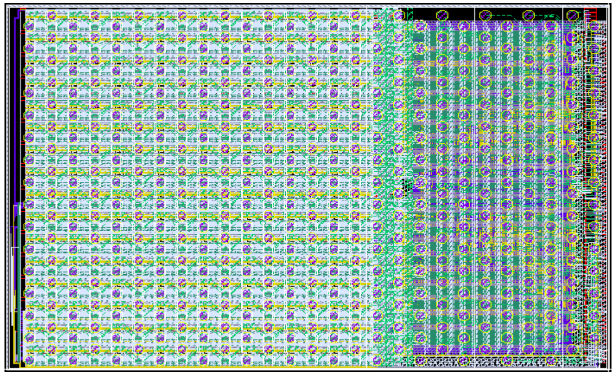
SwitcherB
Row control



AMS high voltage 0.35µm
Size 3.6×2.1 mm^2
Gate and Clear signal
Fast HV up to 30V
Rad. Hard proved (36Mrad)

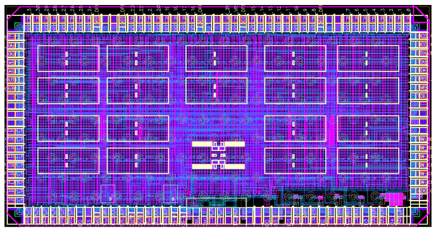


DCDB (Drain Current Digitizer)
Analog frontend



UMC 180nm
Size 3.3×5.0 mm^2
Integrated ADC
Noise 40 nA
Irradiation up to 7Mrad

DHP (Data Handling Processor)
Processor



IBM CMOS 90nm
Stores raw data and pedestals
Common mode and pedestal correction
Data reduction (zero suppression)
Timing signal generation

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Off-module signal flow

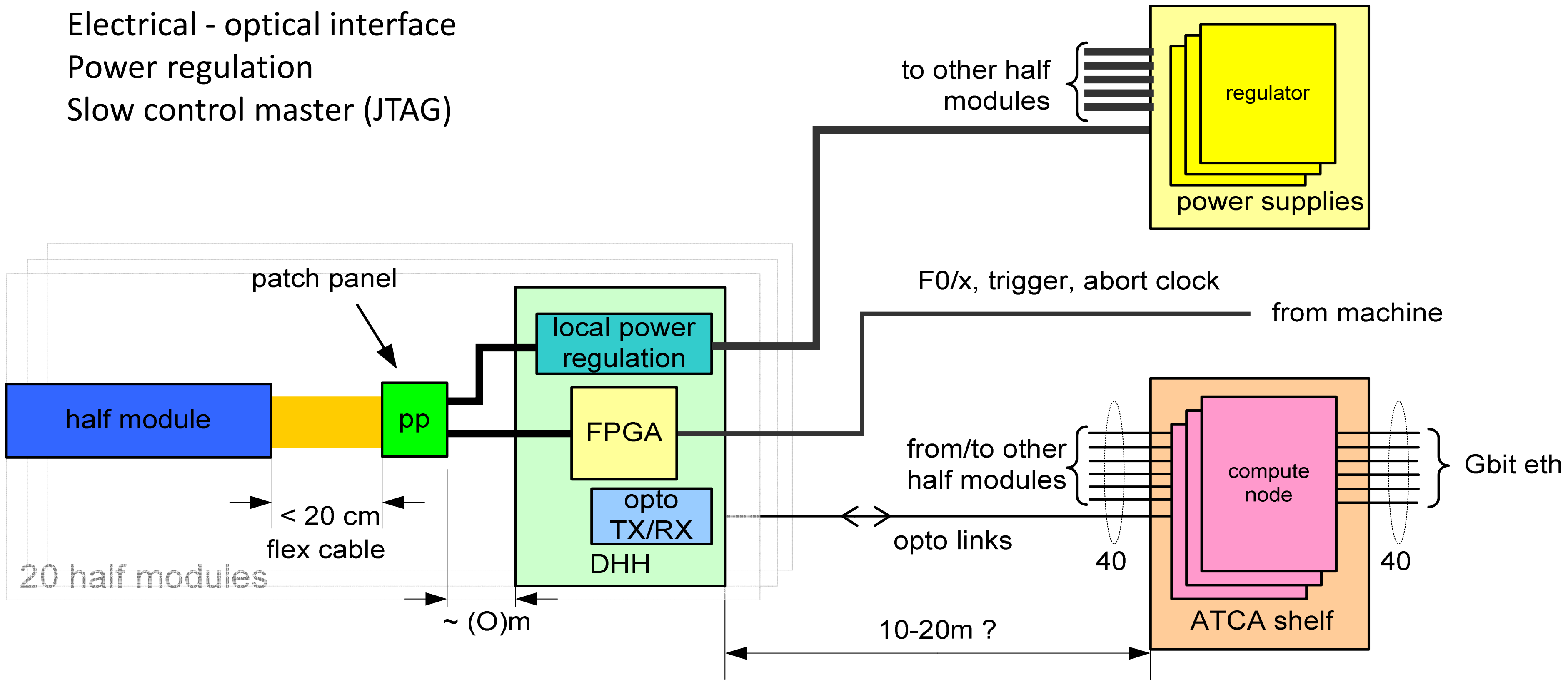
DHH (Data Handling Hybrid): interface of the ladders with the outside world

Impedance matching

Electrical - optical interface

Power regulation

Slow control master (JTAG)



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Optimization: Full simulation chain

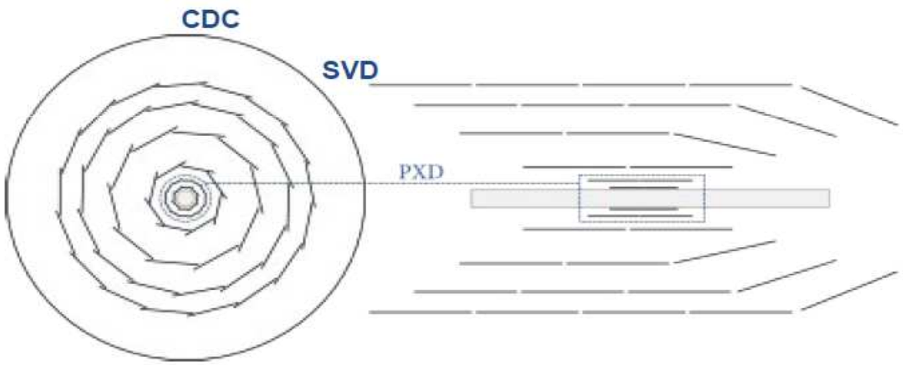
Detector simulation → PXD/SVD Simulation → Track reconstruction → Analysis

Detector simulation
Particle gun (single event)
EvtGen (physics event)
Mokka geometry

PXD/SVD Simulation
Ionization points
Signal points
Electronic noise
Digitization and clustering

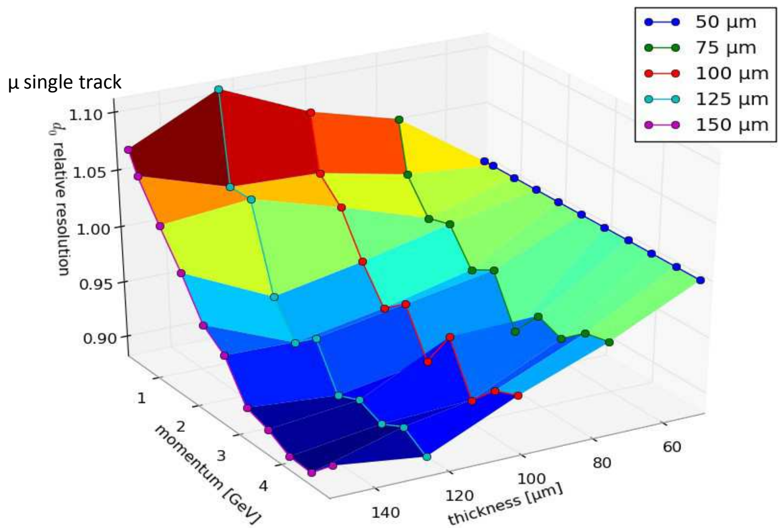
Track reconstruction
Marlin tracking
PXD+SVD+CDC

Analysis
Physics channels



- Digitizer (Geant4) tuned with TBeam data:
- Electric noise
- Electric field in Si (charge collection time)
- Lorentz angle in magnetic fields

Optimization studies:
- Sensor thickness
- Pixel size
- Inner layer radius



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Optimization: Full simulation chain

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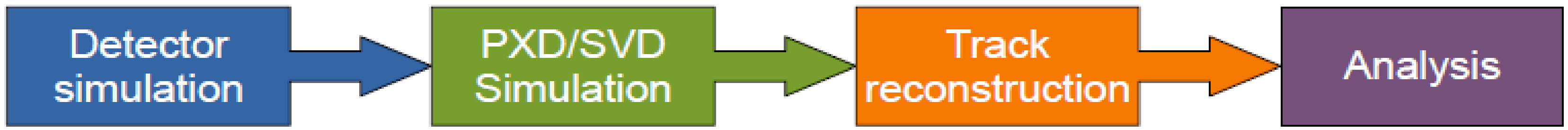
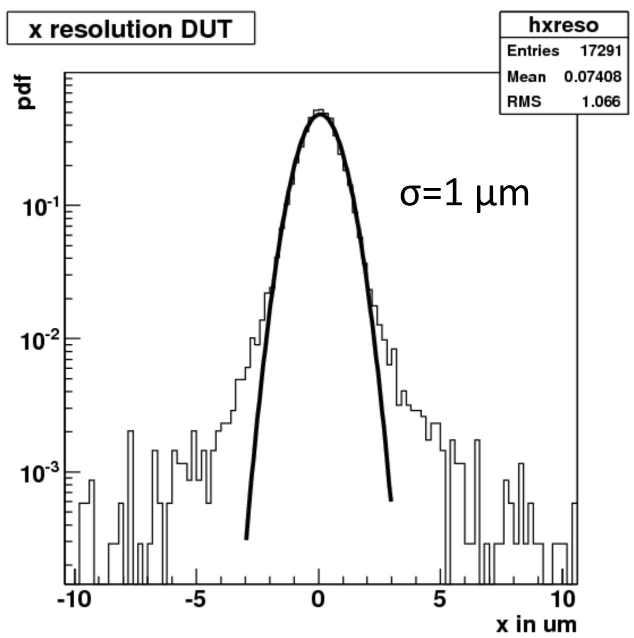


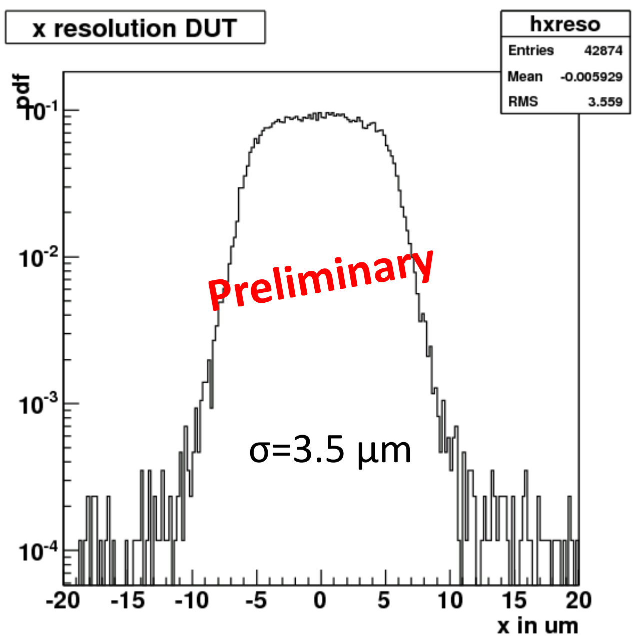
Detector simulation	PXD/SVD Simulation	Track reconstruction	Analysis
Particle gun (single event) EvtGen (physics event) Mokka geometry	Ionization points Signal points Electronic noise Digitization and clustering	Marlin tracking PXD+SVD+CDC	Physics channels

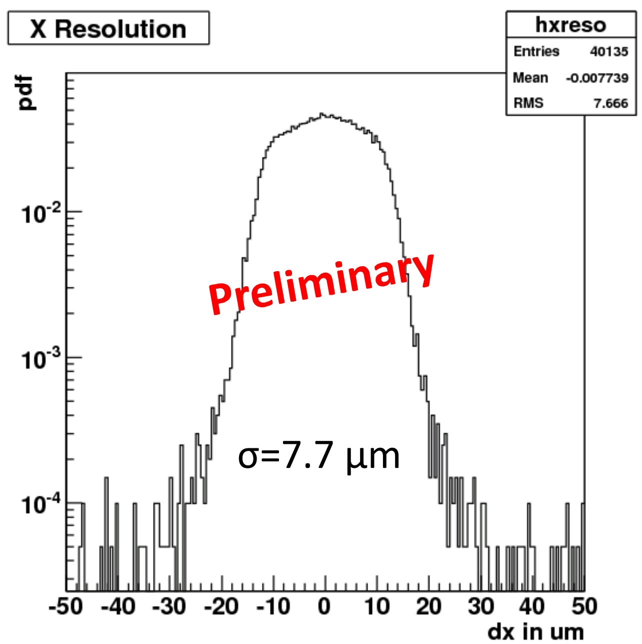
Test Beam Data
$20 \times 20 \times 450\ \mu m^3$
Single point resolution: 1 μm

ILC (Sim)
$20 \times 20 \times 50\ \mu m^3$
Single point resolution: 3.5 μm

Belle II (Sim)
$50 \times 50 \times 75\ \mu m^3$
Single point resolution: 7.7 μm







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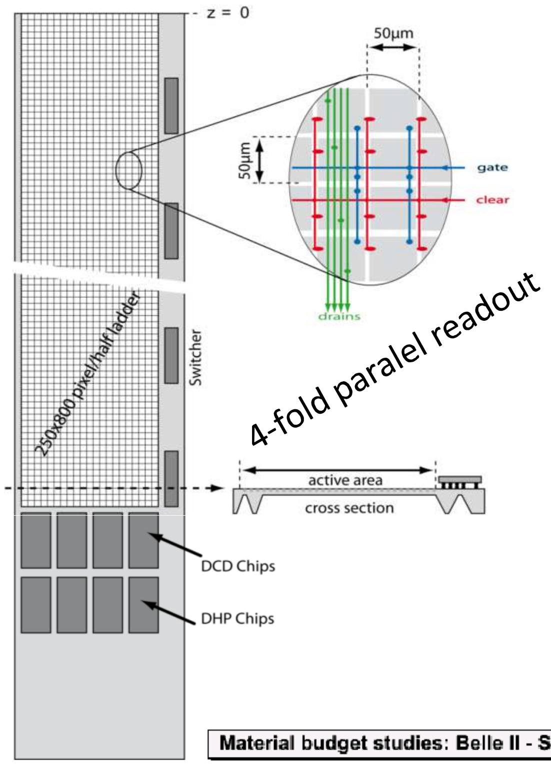
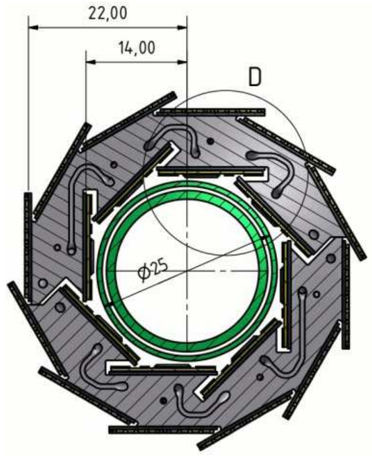
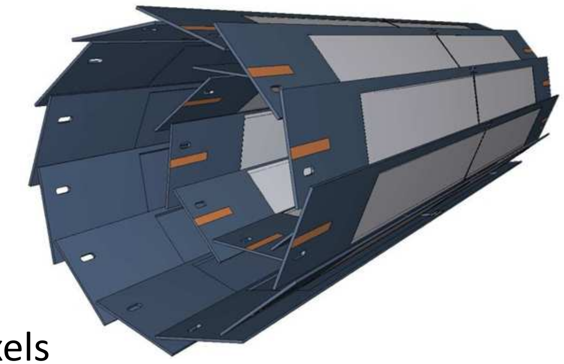
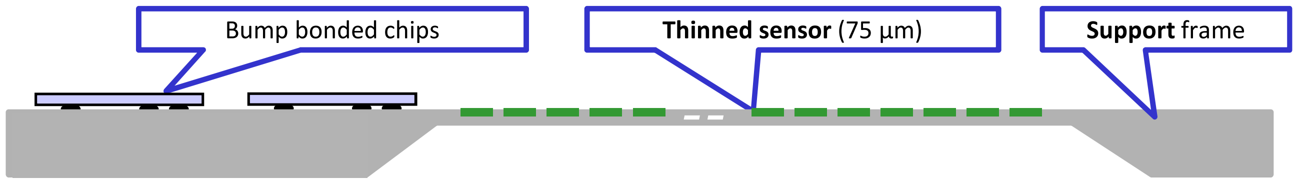
The Belle II PXD layout

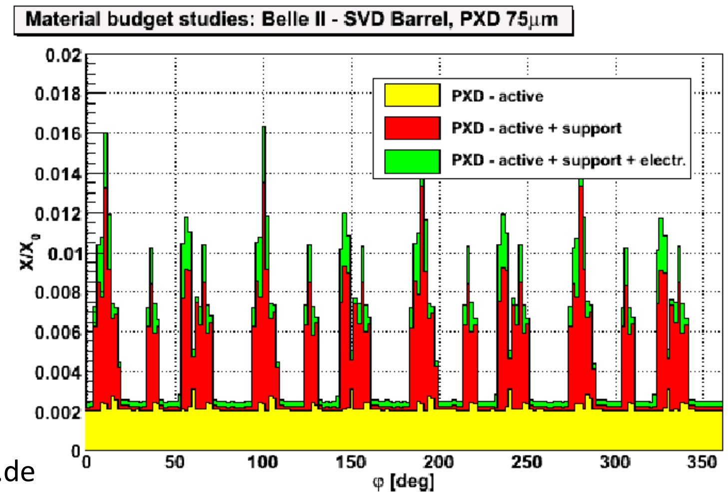






8 Million pixels
Close to the IP
Low material budget





	Inner layer	Outer layer
# ladders	8	12
Radius	1.4 cm	2.2 cm
Pixel size	50x50 μm^2	50x75 μm^2
# pixels	1600(z)x250(R-ϕ)	1600(z)x250(R-ϕ)
Thickness	75 µm	75 µm

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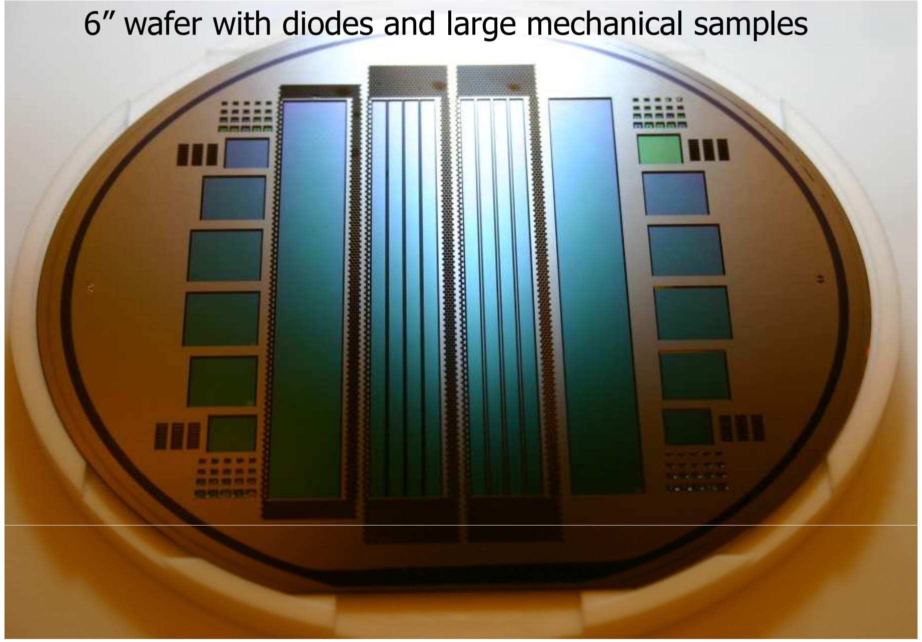
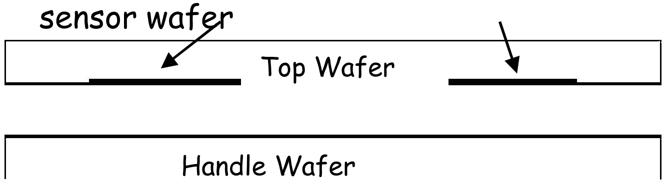
Thinning technology

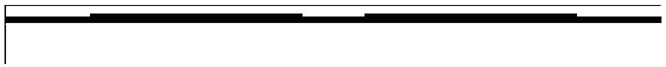


6” wafer with diodes and large mechanical samples

- **Sensor: Thinned down to 75µm**
- **Balconies: Etched grooves**

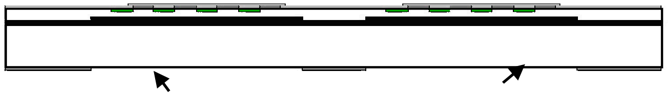
a) Oxidation and back side implant on sensor wafer



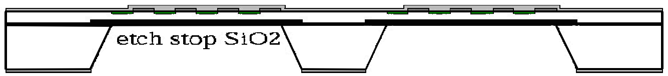


b) Wafer bonding and grinding/polishing of top wafer. Thin sensor side to desired thickness

c) Process DEPFET on top side ➔ passivation



open backside passivation



d) Anisotropic deep etching opens "windows" in handle wafer. Structure resist, etch backside up to oxide/implant

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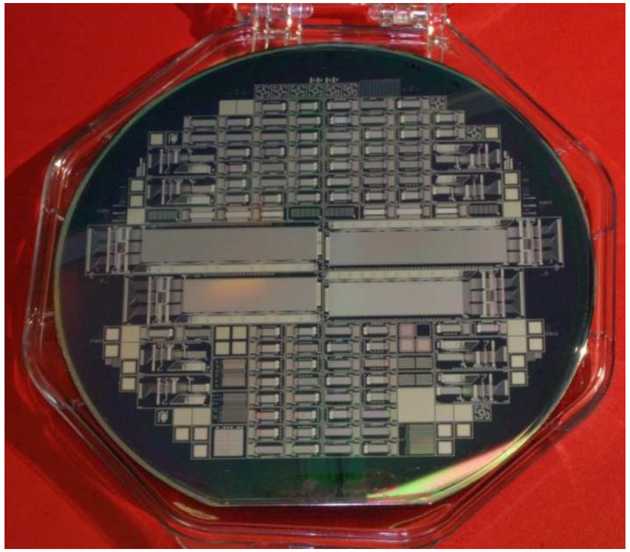
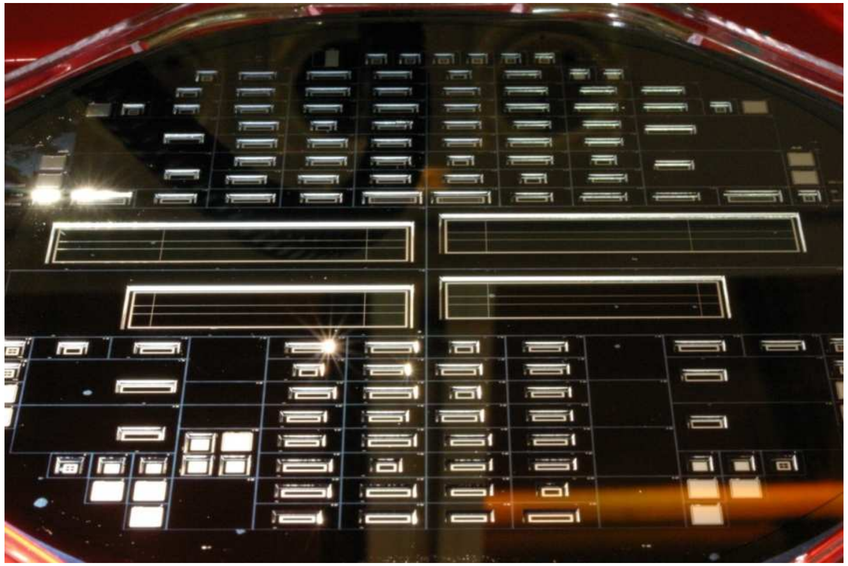
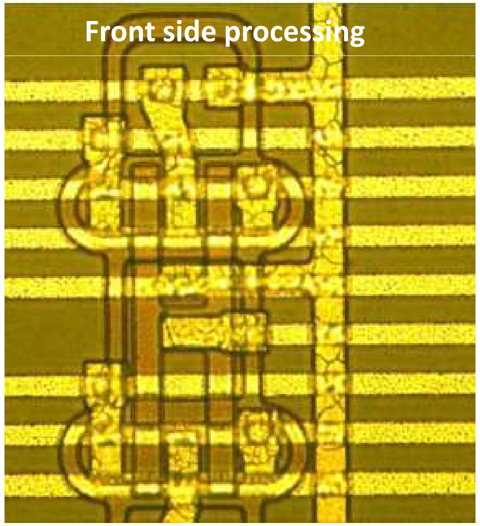
PXD6 prototype production



8 wafers with 50 µm thin sensors
- Small test matrices to test different pixel sizes from 50 to 200 µm
- Design variations: short gate lengths, clear structures
- Full size sensors –half ladders for prototyping
- Technology variations on the wafer level





90 steps fabrication process:
9 Implantations
19 Lithographies
2 Poly-layers
2 Alu-layers
Back side processing

First thin DEPFET sensors produced!

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Test platform

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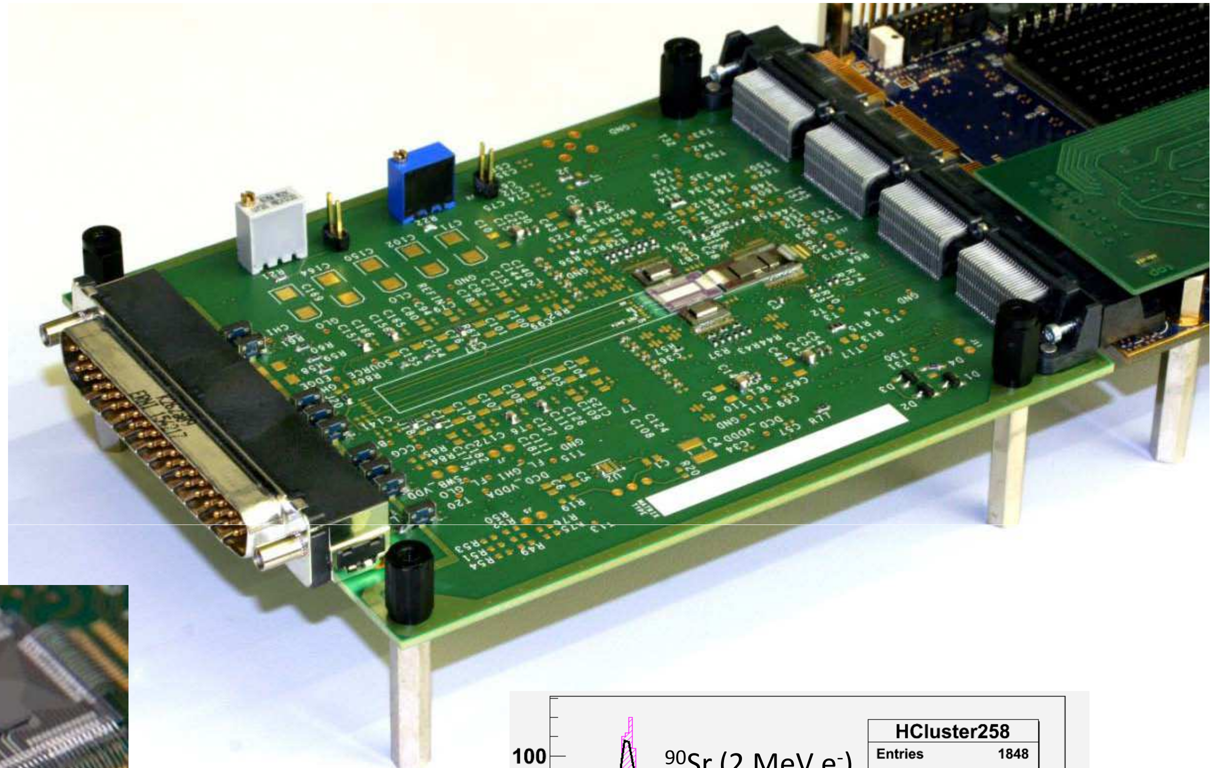
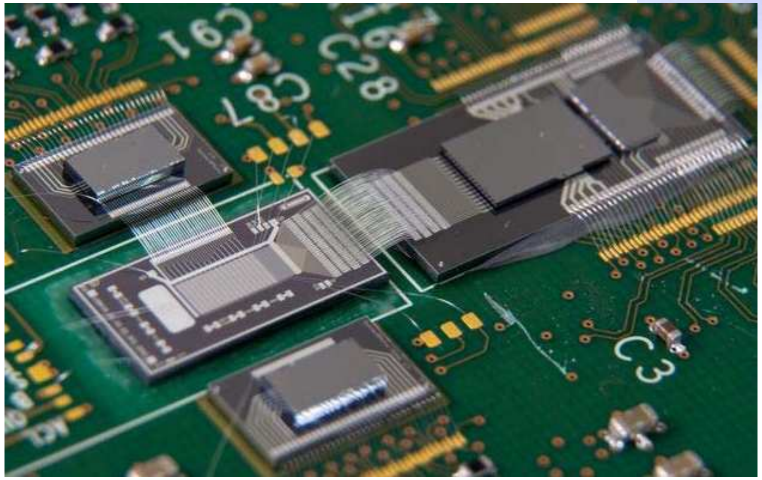
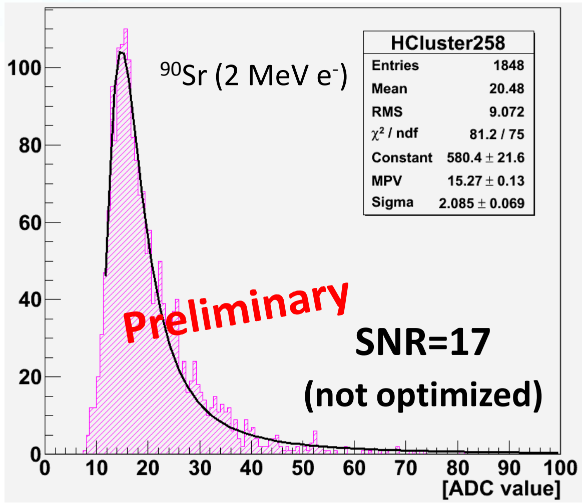
Belle II design
Sensor 32x64 pixels
50x75x50 μm^3
SWB and DCDB at full speed
DCDB readout at 320MHz
100 ns row time

Close to final specs!







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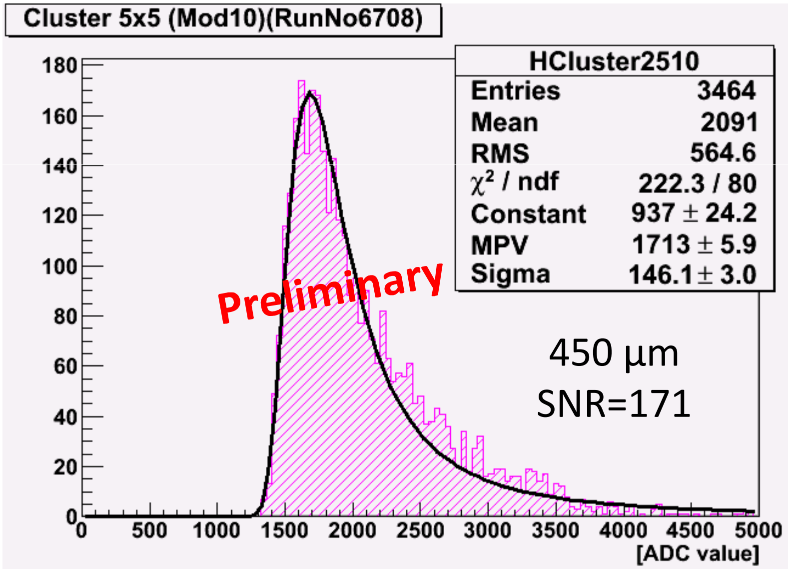
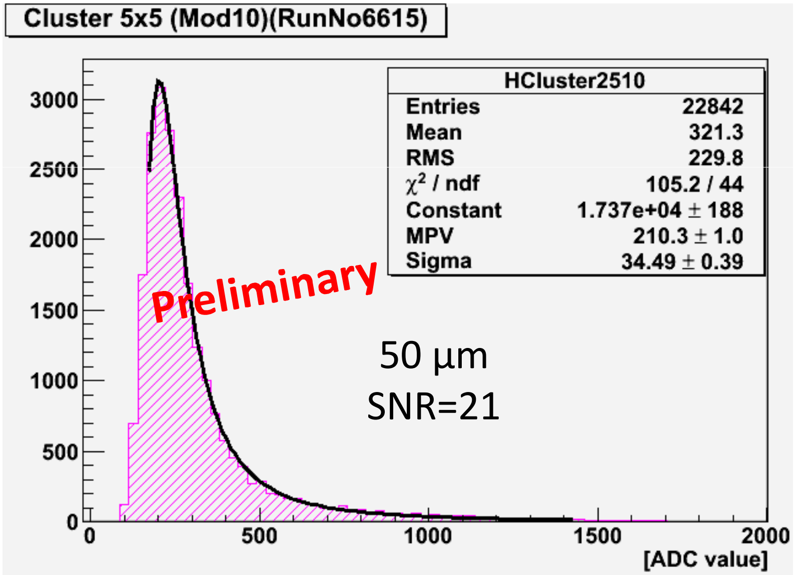
^{90}Sr source test

Belle II design: Thin and thick sensors
32x64 pixels
L=6 µm
Pixel pitch: 50x75x50 µm^3
CURO readout



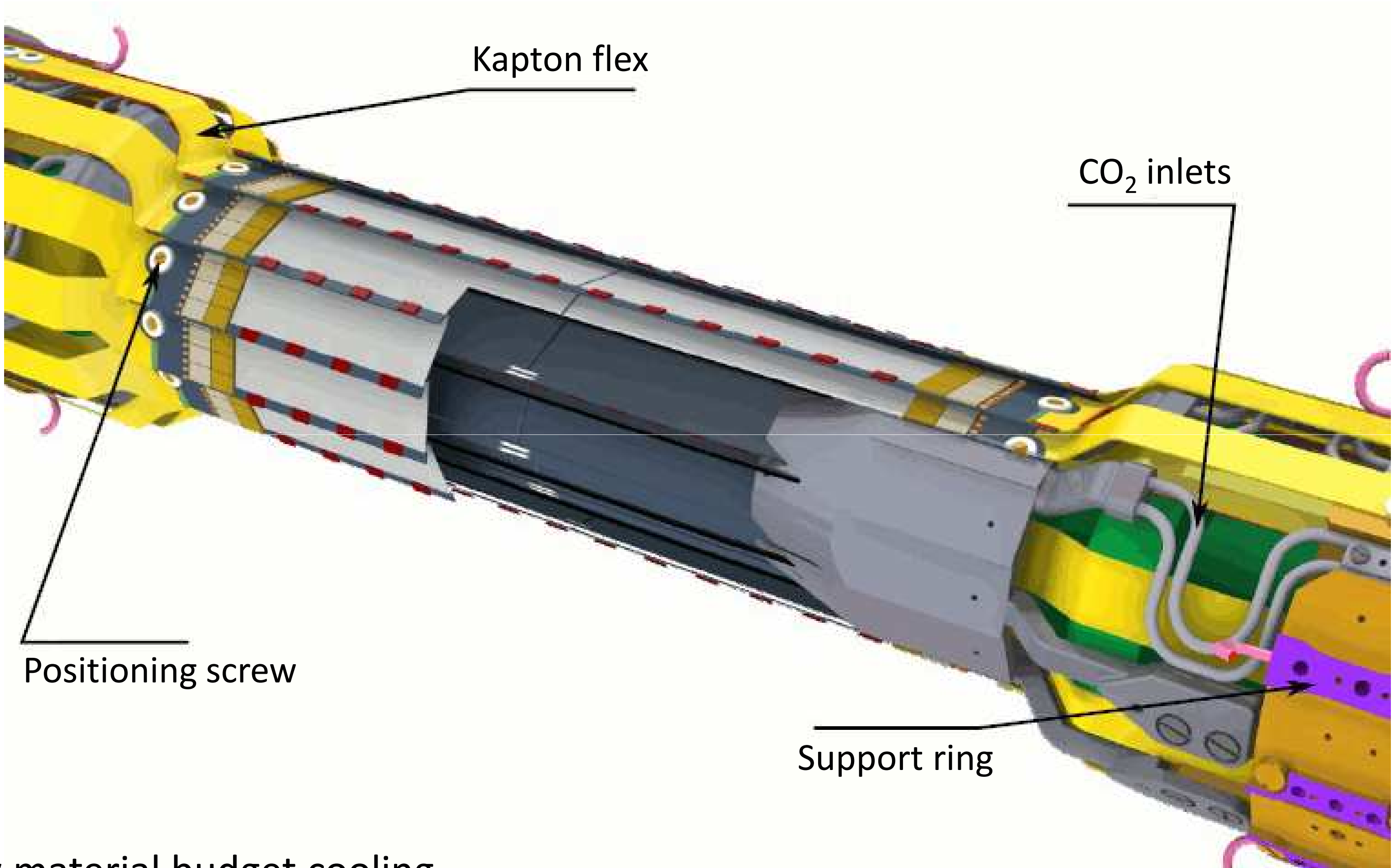
Thick (450 µm)



Thin (50 µm)

Signal(450µm) : Signal(50µm): 8.2 As expected!

Mechanical design



- Low material budget cooling
  - Massive structures outside the acceptance to cool down the readout chips
  - The center of the ladder rely on cold air

Thermal studies: mock up

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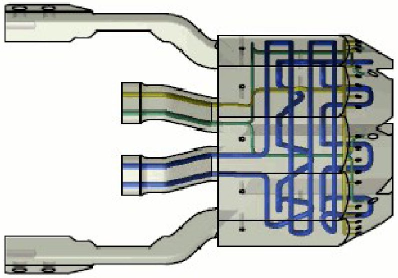
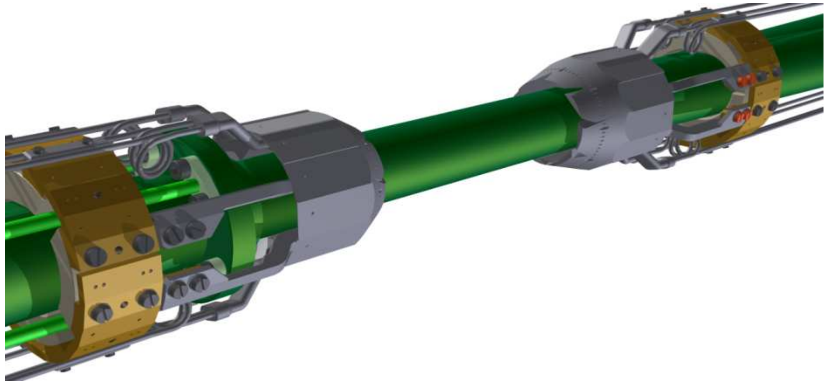
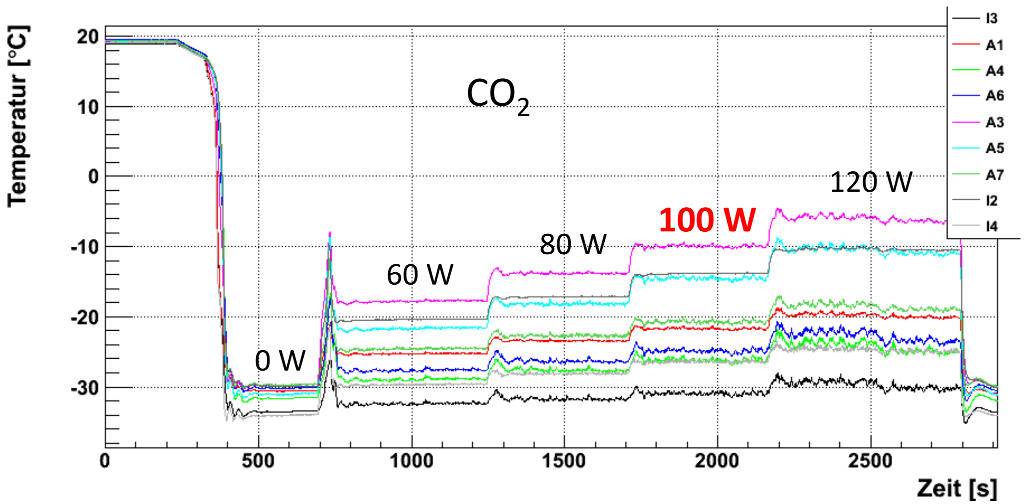
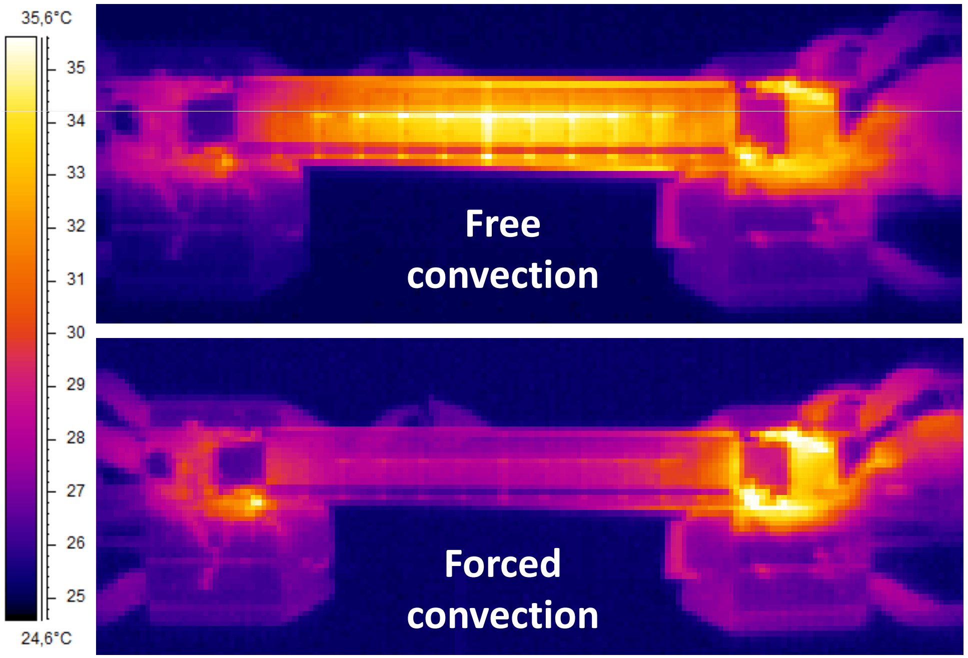


- Stainless steel
- Fast sintering
- Blue: CO_2 capillaries
- Yellow: Air channels







Cooling prove of principle

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Summary

- A new super flavour factory, SuperKEKB is currently being built in KEK (Japan)

- To fully exploit the high luminosity, the detector will be upgraded (Belle II)

- The pixel detector will be made of DEPFET sensors

  → High resolution, low power consumption, low material budget

- The DEPFET PXD entered the construction phase

  All the aspects are being considered (although not treated in this talk)

  → Thin sensors (50 µm) produced and read at full speed (100ns sampling time)

  → Cooling principle being proved

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Thank you very much!

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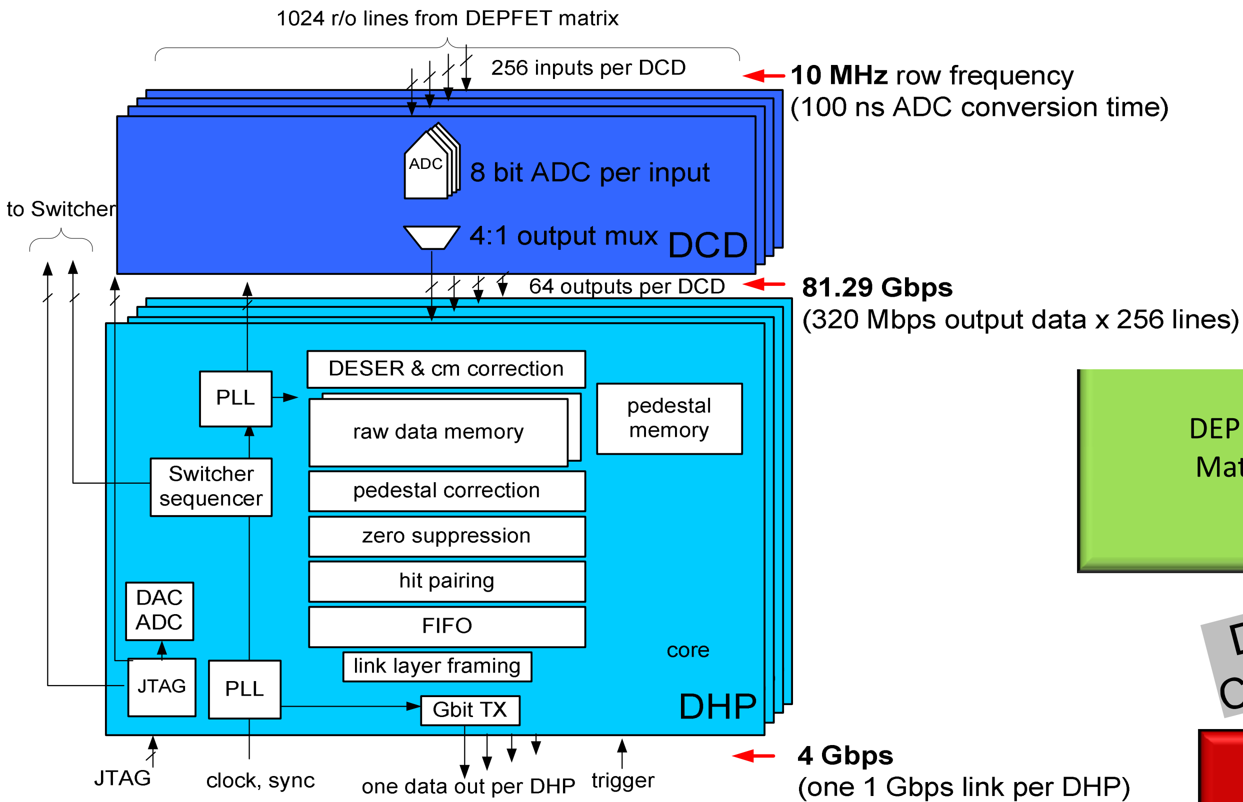
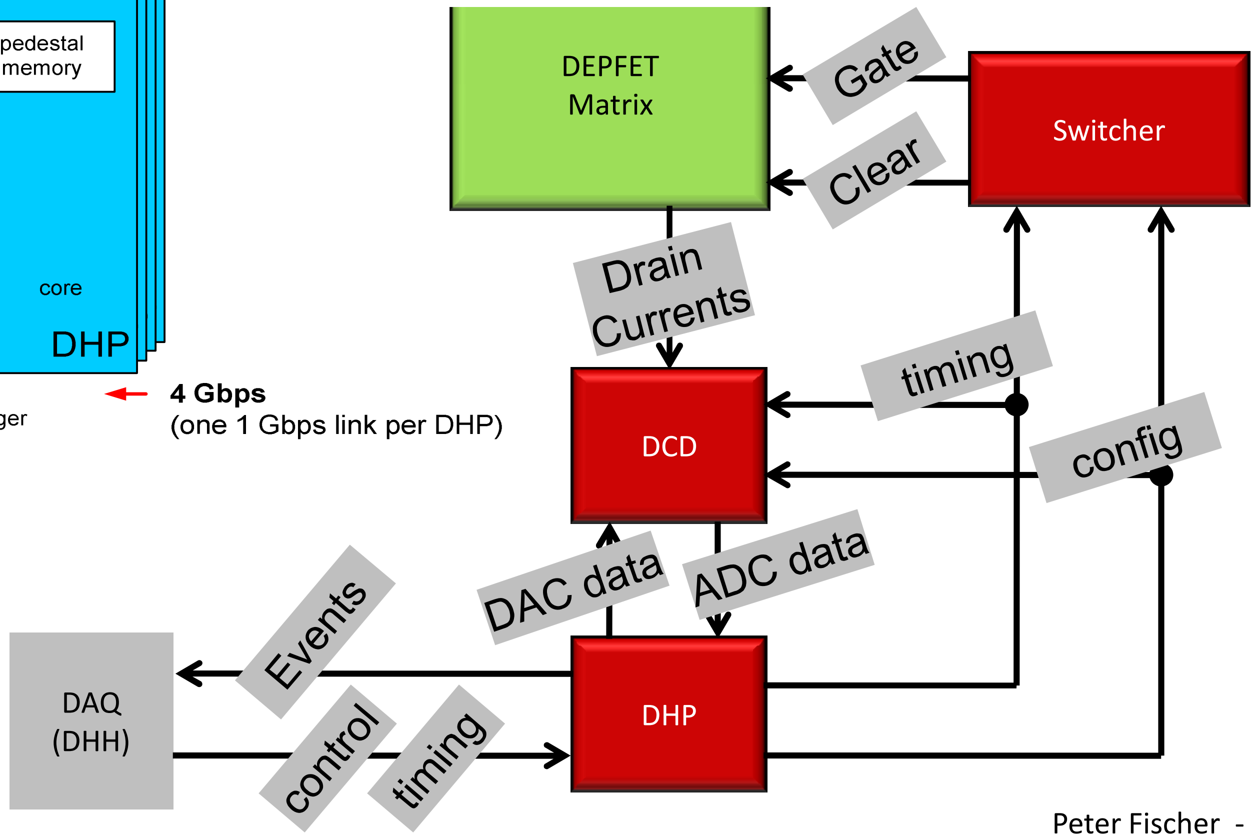
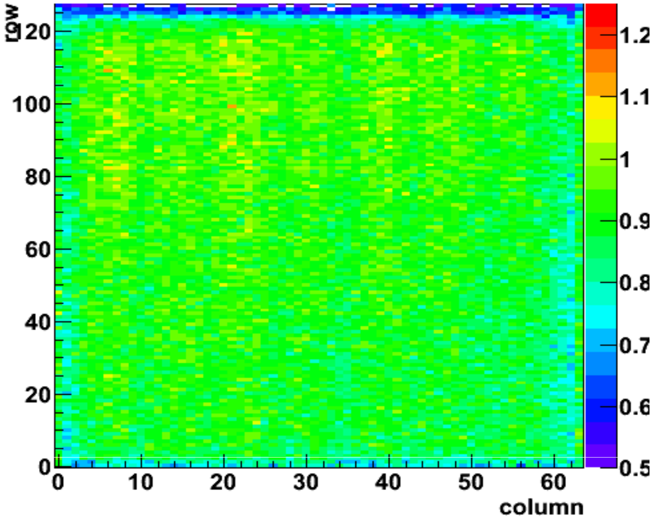
In-module signal flow

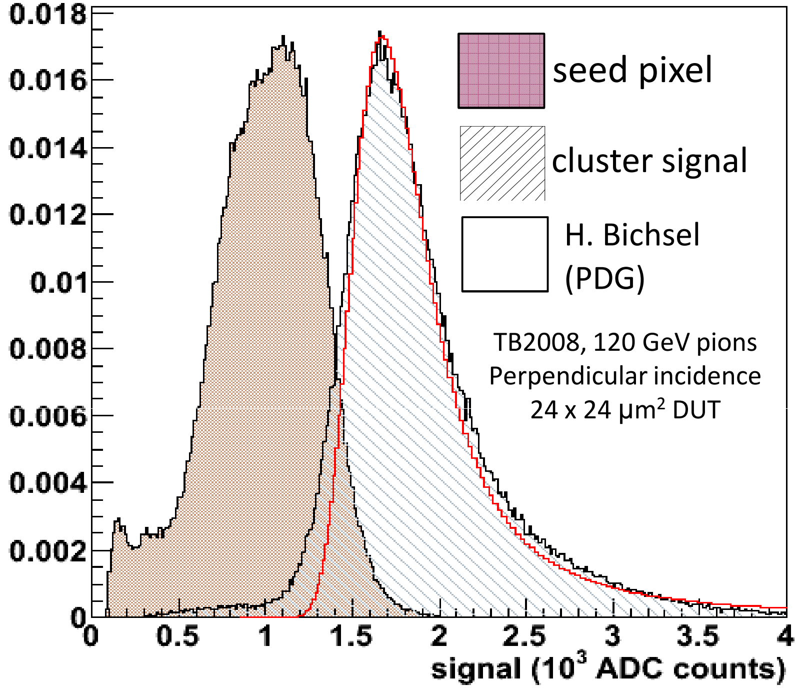




TB 2008 and 2009 results

Gain map: Deviation from average seed signal





- 64x128, 24x24 μm^2 Common Cleargate (TB2008)
  MPV=1715 ADC counts
  g_q=363pA/e$^-$

- 64x256, 32x24 μm^2 Capacitative Coupled Cleargate (TB2009)
  MPV~2400 ADC counts
  g_q~500pA/e$^-$

- 64x256, 20x20 μm^2 Common Cleargate, Length$_{Gate}$=5μm (TB2009)
  MPV~3100 ADC counts
  g_q~650pA/e$^-$ (2x previous g_q, as expected)

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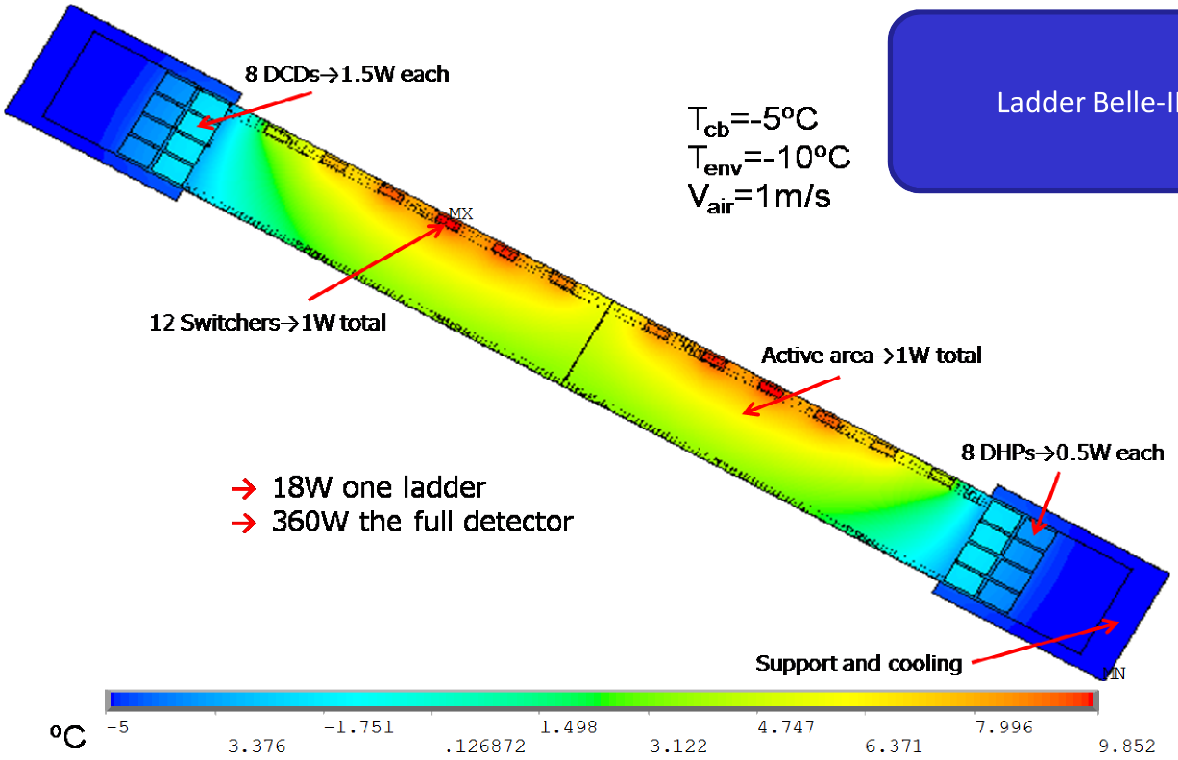
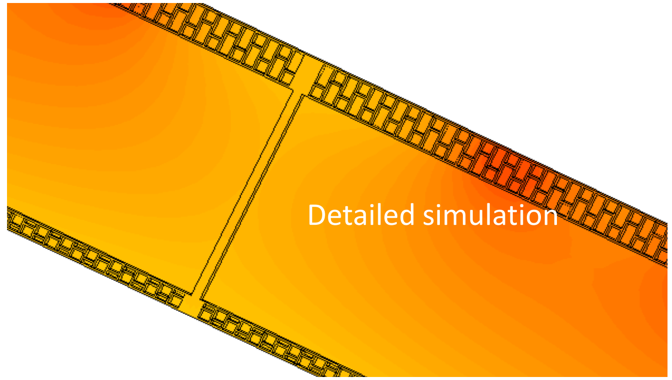
Finding the optimal environment

Ladder Belle-II PXD





- Implement the full Belle-II ladder geometry in f.e- software
- Apply the loads to the different elements (DCD,DHP,SW,Sensor)
- Find an optimal cooling solution (find T_{env} and T_{cb}) for the current upper limits on the temperatures:
  - T_{max} (Sensor)<30ºC
  - T_{max} (Chips)<60ºC

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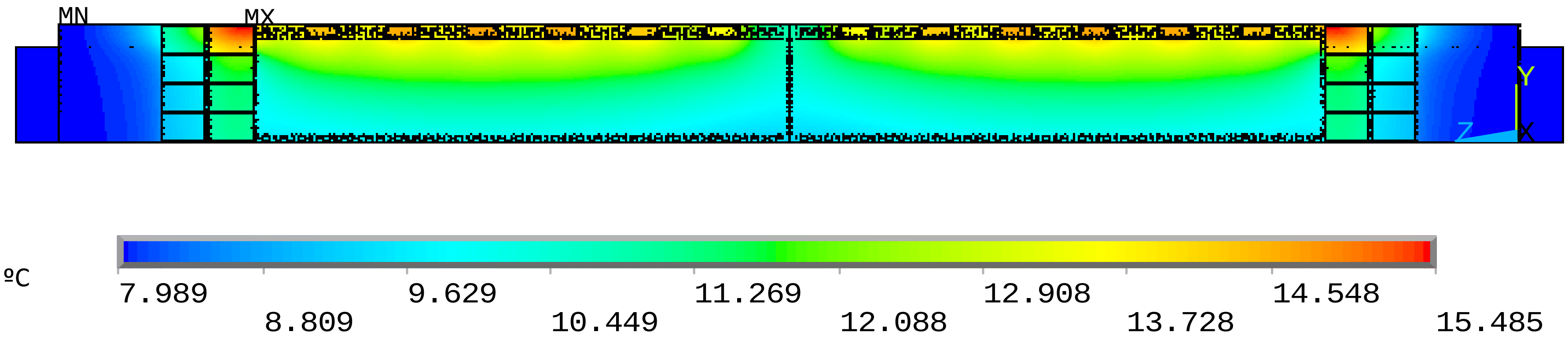
Thermal studies

Temperature distribution along the ladder



Reasonable environment conditions

T_{env}=-5ºC
T_{cb}=8ºC

→ $T_{Laddermax}$=15.5ºC

- The end of the stave will be cooled by CO_2 inside the cooling block
- The center will be cooled by blowing cold air

→ Both, SVD and PXD subdetectors will be isolated of the CDC