

Fast, low-noise, and low-power, electronics for the analog readout of non-linear DEPFET pixels



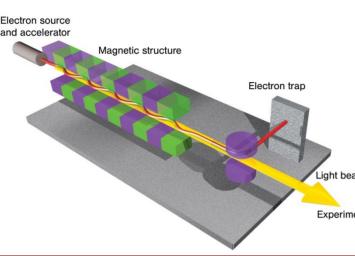
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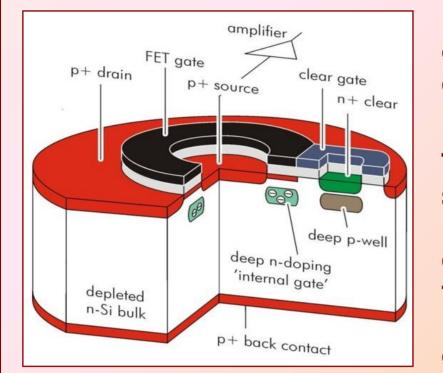
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> The European XFEL project

The XFEL (X-ray Free Electron Electron Source Laser) under construction in Hamburg (Germany) will produce ultra short pulses of high intensity, coherent light, providing macro-bunches by mean of SASE (Self Amplified **Spontaneous Emission).**



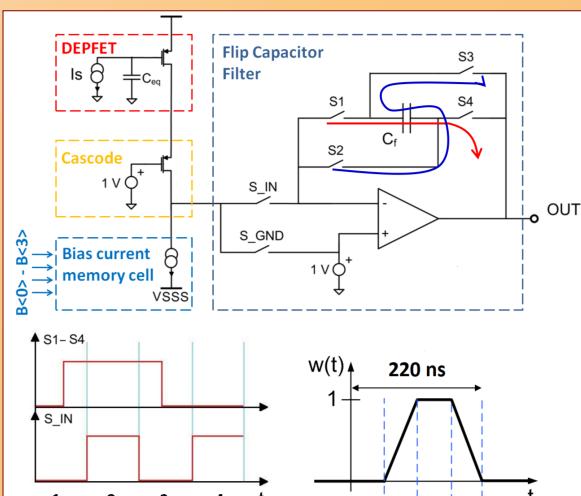
The XFEL will probe atomic arrangements like snapshots after an external perturbation or as a function of an intrinsic excitation. Moreover, due to the coherence and high intensity of the pulses, the project will give the possibility to solve complicated structures.



DEPFET based Active Pixel Sensor (APS) matrix is a new detector concept for X-ray imaging and spectroscopy applications. This detector can provide excellent energy resolution and high speed read-out, combining the advantage of random pixel accessibility.

To cope with the extremely high dynamic range requested (from single photon counting @ 1 keV up to 10^4 photons @ 10 keV) a new **DEPFET Sensor with Signal Compression (DSSC) is under** development at MPI Halbeiterlabor in Munich (Germany). To obtain the non-linear characteristic the potential under the challenge progressively extends under the source, thus reducing the steering effect on the channel current

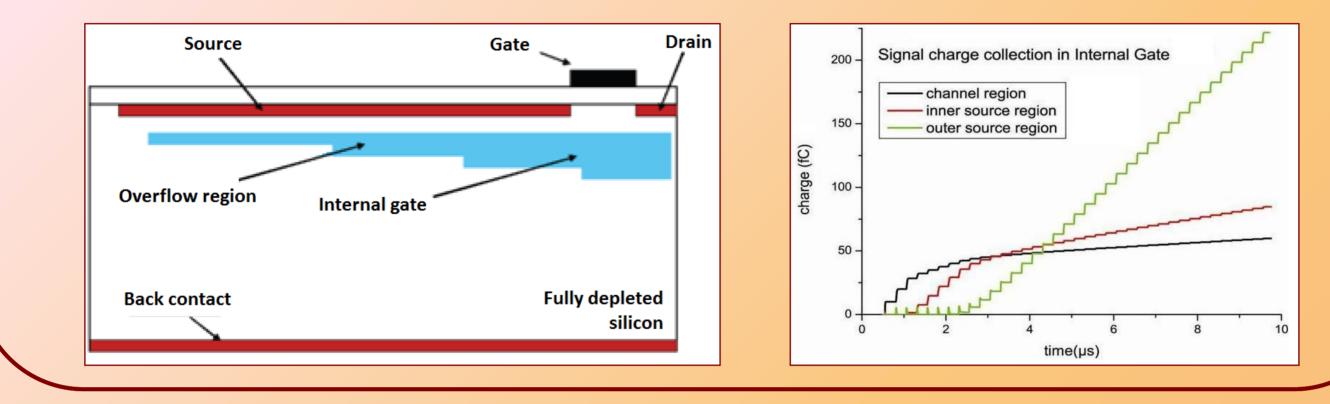
> The current readout approach



The challenging aspects in the XFEL imager design come both from laser characteristics and from project specifications in terms of data acquisition and resolution.

The fast readout speed required by the XFEL beam structure (pulses 220 ns apart) forces to have one electronic channel per pixel. Each will provide analog filtering, digital conversion and storage.

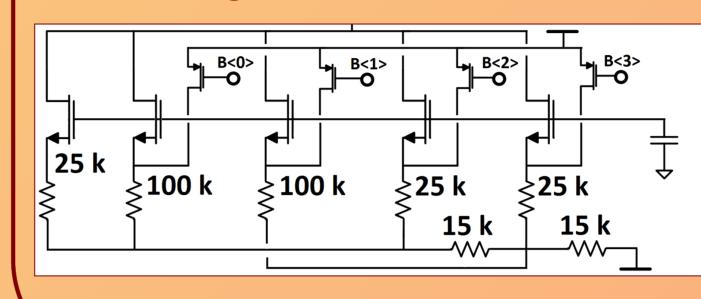
To cope with the short amount of time available, a current readout approach is foreseen. In order to remove the baseline and properly filter the 1/f noise, the filter implements a trapezoidal weighting function by flipping the feedback capacitor before the second integration (Flip



1 2 3 4 t $\overleftarrow{\tau}$

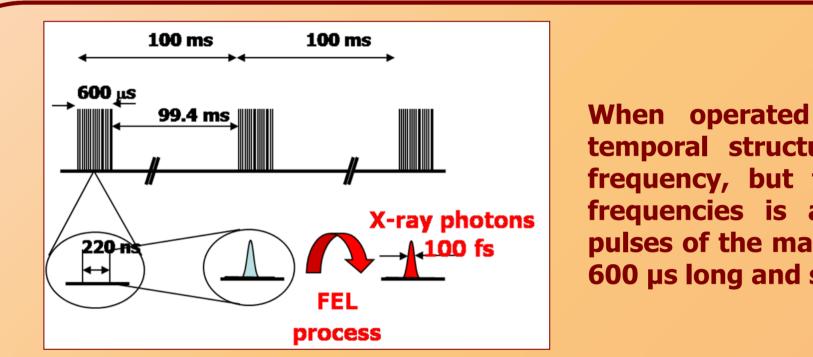
Capacitor Filter, FCF, solution).

The DEPFET is biased fixing the Vgs. The low source resistance of the input cascode moves the pole determined by the stray capacitance on the detector output at high frequency and the circuit can be operated at high frame rate. A current source subtracts the bias current of the sensor to maximize the dynamic range. The input signal to the filter is represented by the detector current variations due to collected charge.



To comply with process mismatches and threshold shifts after irradiations the circuit must be able to track the value of the detector bias current. A coarse regulation of the current is achieved setting once the 4 bits of the pseudo DAC. Later on, before every macro-bunch fine adjustment is obtained setting the gate voltage of the active branches by mean of a negative feedback loop. The same amplified used for the filtering phase is employed to close the loop.

> Readout timing strategies

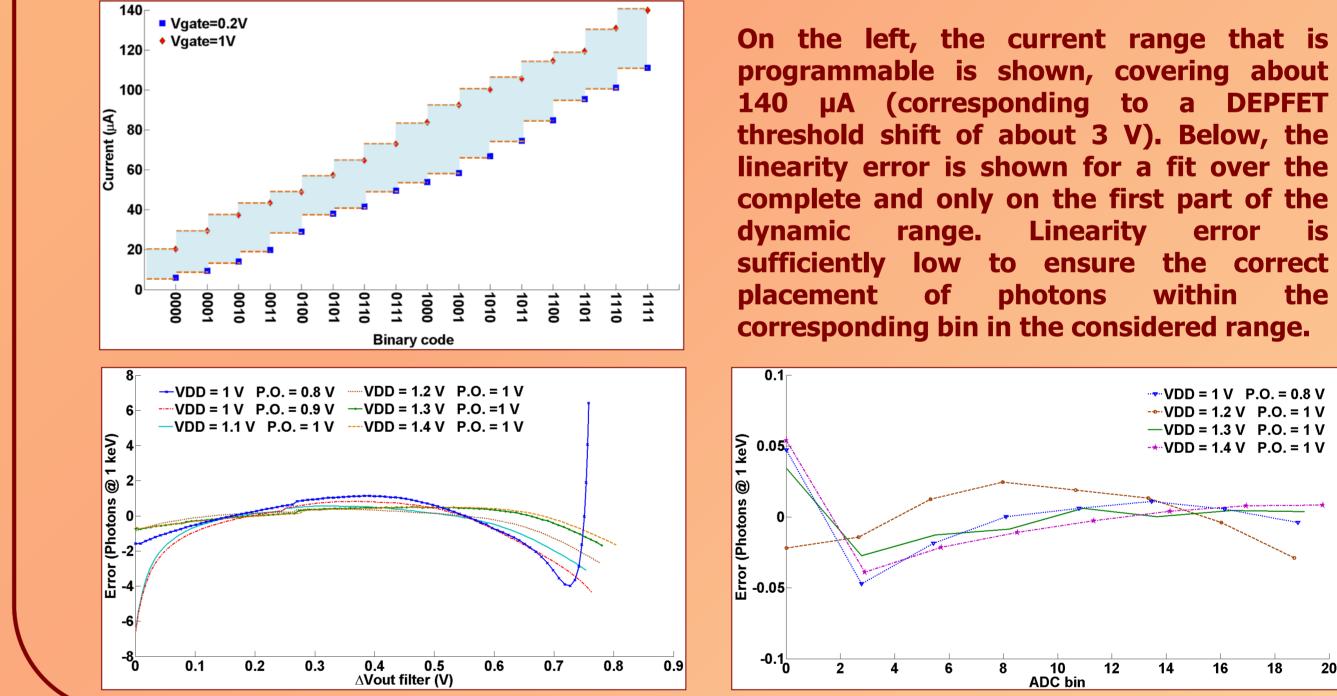


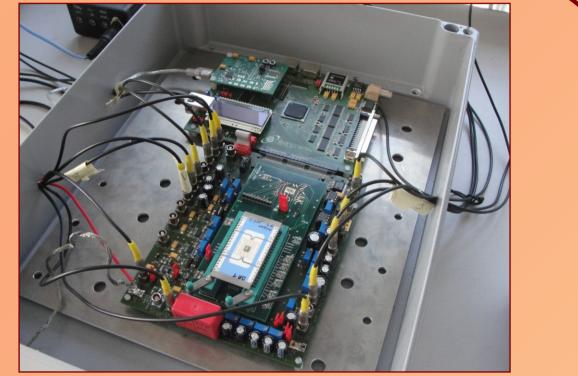
When operated at maximum speed the XFEL temporal structure demands 4.5 MHz operation frequency, but the possibility to work at lower frequencies is also foreseen by skipping X-ray pulses of the macro bunch. The macro-bunches are 600 µs long and separated by 99.4 ms.

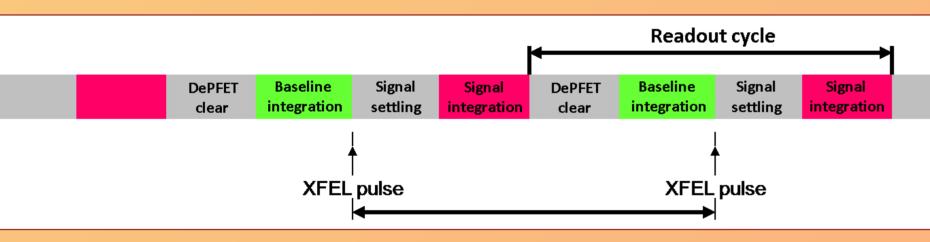
Two approaches to readout XFEL pulses are possible. The first solution consists in having two integrations (baseline and signal) in every readout cycle. The duration of each integration represents the shaping time of the associated weighting function, and is called tau. This approach leads to quite short integrations, especially at the high frame rate of 4.5 MHz.

> Experimental setup and meaurements

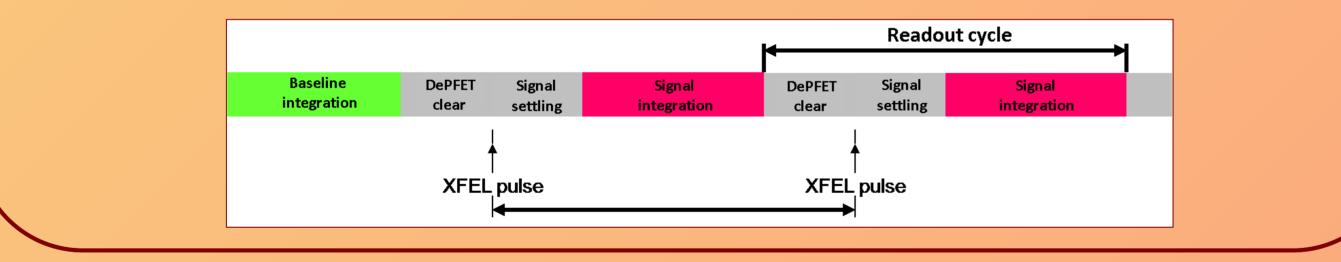
A dedicated setup has been designed to test performances of the FCF, both alone and together with a single pixel linear DEPFET. A first board carries the chip and a DEPFET matrix, and is connected to a second one which delivers the bias voltages and digital signals for the operation of the system. A VIRTEX II FPGA regulates the global timing, programs the on-chip digital sequencer and handles the communication with the PC.







Therefore, an alternative solution has been proposed, in which a single baseline integration per macro bunch is foreseen. Then, between subsequent pulses a single, longer signal integration is performed, with consequent improvement in noise performances.





(a. u.) 8.0

0.6

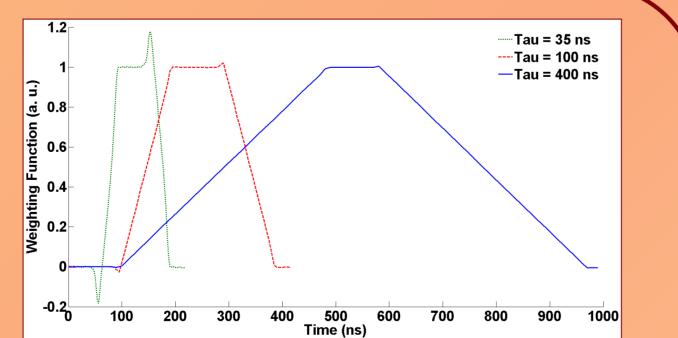
_____ _____0.4

ອີ 0.2

-0.2

0.5

The weighting functions for the double integration readout scheme are shown in the top figure. Three different integration times (65 ns, 100 ns and 400 ns) are shown. Final baseline value is within 1% for all cases, which is completely adequate for XFEL operation. Spikes are due to the finite time response of the power supply to which the signal current is sent between integrations in



— 1 Cf

---- 2 Cf

---- 4 Cf

---- 3 Cf

3.5

Measurements with a DEPFET detector

The performance of the filter was tested at room temperature with standard technology linear **DEPFETs and a 55Fe radioactive source.** The gain of the DEPFETs specifically employed in these tests was measured as approximately 350 pA/el.

 10^{2}

10¹

10⁰∟ -2

10⁸

-1

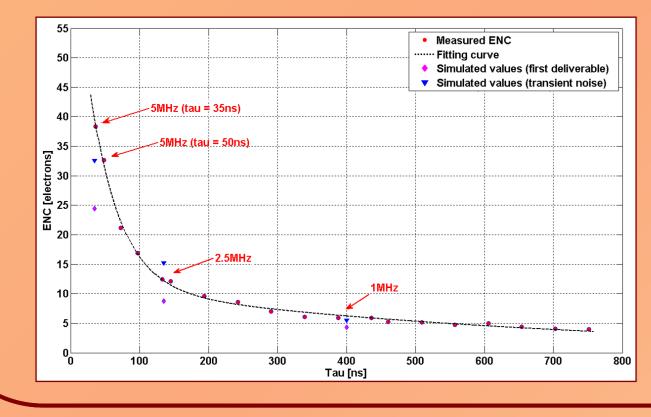
As an example, the measured spectrum for the operating frequency of 1 MHz and the double integration readout scheme is shown top on the right. From the fitting of the noise peak a noise level of 13 el was extracted. This 10^⁴

Λ	FWHM Noise = 110.3eV Noise = 13.0el
	FWHM MnKa = 178.3eV FWHM MnKb = 106.4eV

Energy (keV)

stabilizing the reference voltage.

The single integration weighting functions for different values of the feedback capacitance and for an operating frequency of 1 MHz are shown in the bottom figure. An exponential tail corresponding to the bandwidth of the current source programming loop is visible. Flattop gets longer for pulses more distant from the baseline measurement, leading to different 1/f filtering efficacy, that was measured and proven negligible.



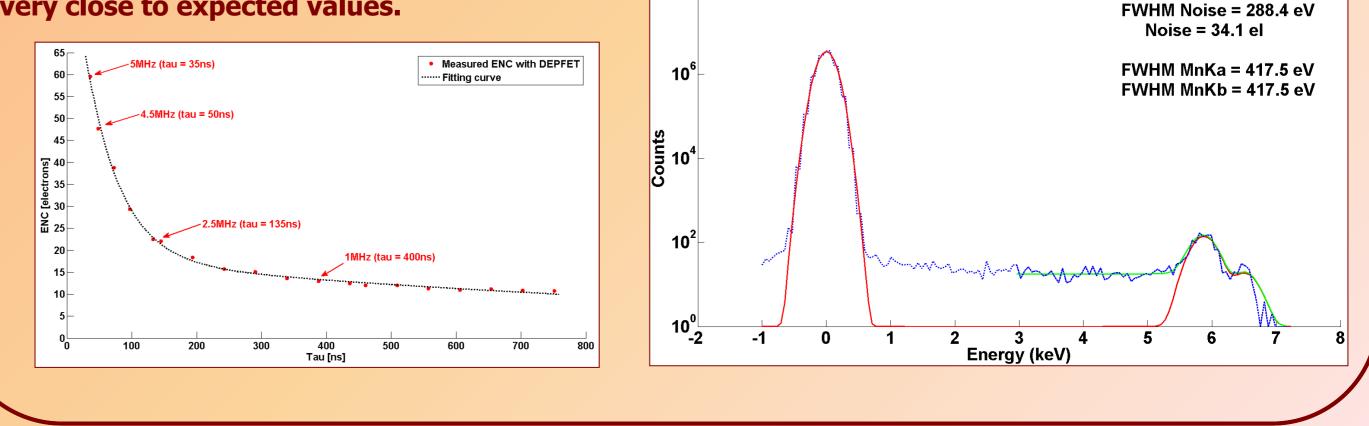
Measured noise is reasonably consistent with the theoretical noise levels and gets higher for short integrations, as expected since the dominant source of noise is white. Measured values for the single integration readout scheme show that the noise increase observed for pulses far from the end of the programming phase is negligible. At 4.5 MHz a remarkable improvement with regard to the double integrations readout scheme was observed (measured ENC of about 17 el).

Time (μs)

2.5

noise level is adequate for single photon un 10³ resolution @ 1 MHz operation and in agreement with expected values.

The noise of the complete system for different integration times is shown below. For the single integration readout scheme, an ENC of only 34 el at the maximum frequency of 4.5 MHz was measured, with an integration time of 70 ns. The relative spectrum is shown bottom on the right. Measured performance is very close to expected values.



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