Wir schaffen Wissen – heute für morgen

EIGER a new single photon counting detector for X Ray applications: performance of the chip.

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PSD9
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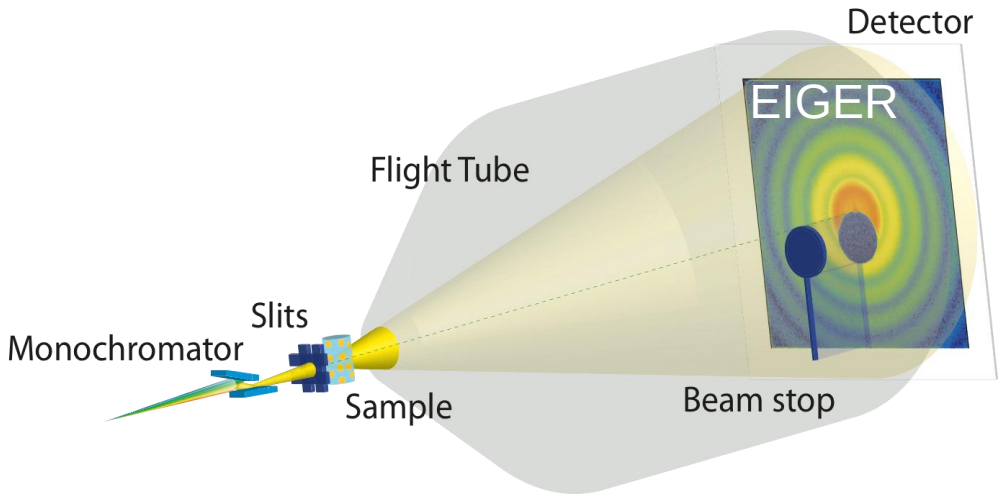
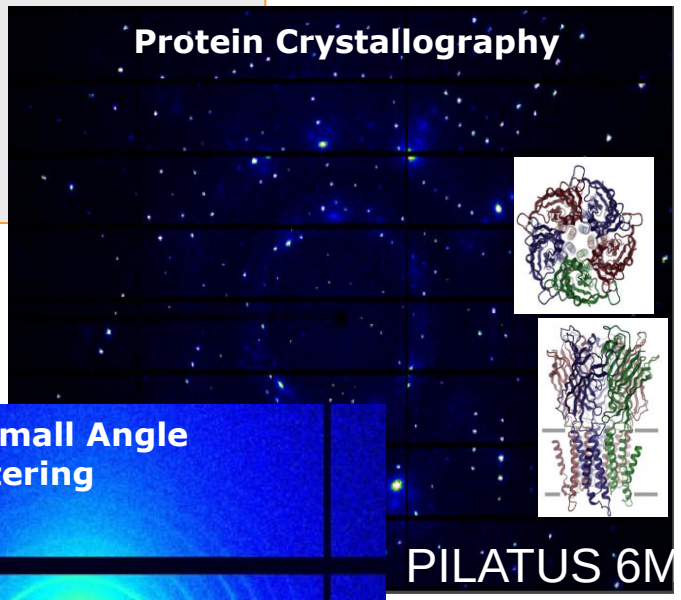
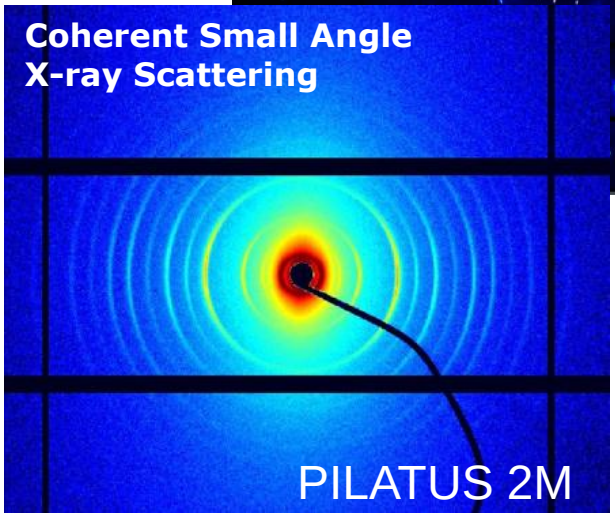
September 2011

Physics focus

- EIGER is a single photon counting pixel detector for synchrotron applications
- aimed towards diffraction experiments
  - Protein Crystallography
  - Coherent Small Angle X-ray Scattering
  - Coherent Diffractive Imaging
  - X-ray Photon Correlation Spectroscopy







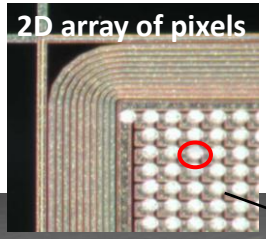
Requirements for an ideal detector

EIGER, designed by PSI-SLS detector group, was optimized to satisfy the main requirements for an ideal detector for synchrotron radiation applications:

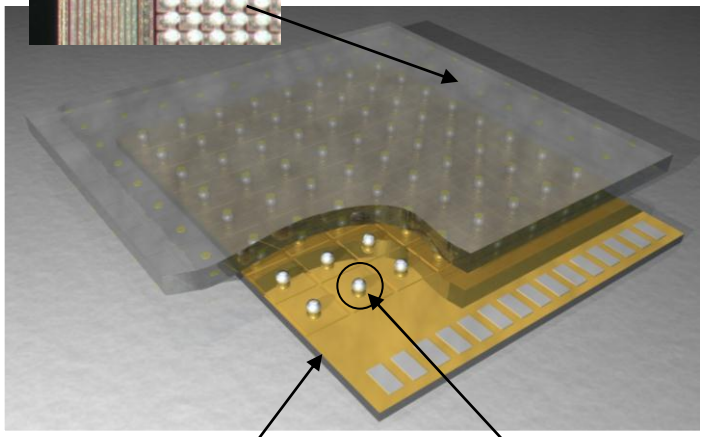
- Single photons sensitivity and no intrinsic noise
  - single photon counting detector
- Good spatial resolution
  - Small pixel size (75x75µm^2)
- Fast Frame Rate ~tens kHz
  - Simultaneous exposure and readout
  - Negligible dead time (~ 3µs)
  - Frame rate up to 22kHz in 4 bit mode
- Detector that can be made as large as possible
  - Modular detector system
  - Data transfer parallel at half module level
  - Projects for EIGER 16M Pixel (~32x32 cm^2)
- High dynamic range
  - Count rates up to 1-2 million counts/pixel/second
- No spatial distortion and uniform response
  - for X-ray energy range few keV to 20 keV

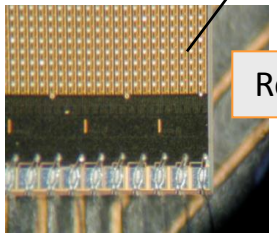
Chip Size	19.3x20.1 mm^2
Pixel Size	75x75 µm^2
Pixel Array	256x256 = 65536
Technological process	UMC 0.25µm; Rad tol. Design >4MRad
Sim. Analog Parameters	Gain: 44.6 µV/e- 30ns peaking time Timing: 151ns (Ret.to 0@1%) Noise: 135e-rms Static Power: 8.8µW/pixel(0.6W/chip)
Count Rate	3.4x10^9 xray/mm^2/s
Transistors Matrix Periphery Transistor density	28.44M >120 000 430/pix
Nom. power supplies	1.1V(analog), 2V(digital), 1.8V(I/O)
Counter	binary, configurable 4,8,12bit, double buffered
Readout speed	~22kHz@4bit mode
Threshold adjustment	Yes 6 Trim Bits
Analog out for testing	Yes
Overflow counter	Yes

EIGER: Hybrid Detector



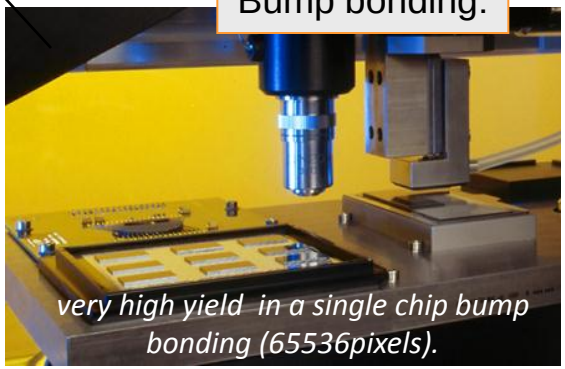
Silicon sensor

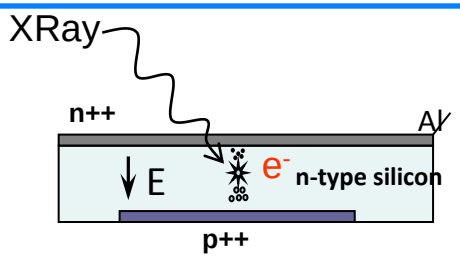




ReadOut chip

Bump bonding:





(A) Silicon Sensor:

Photon - Charge Conversion

(B) Read Out Chip:

Signal amplification and counting

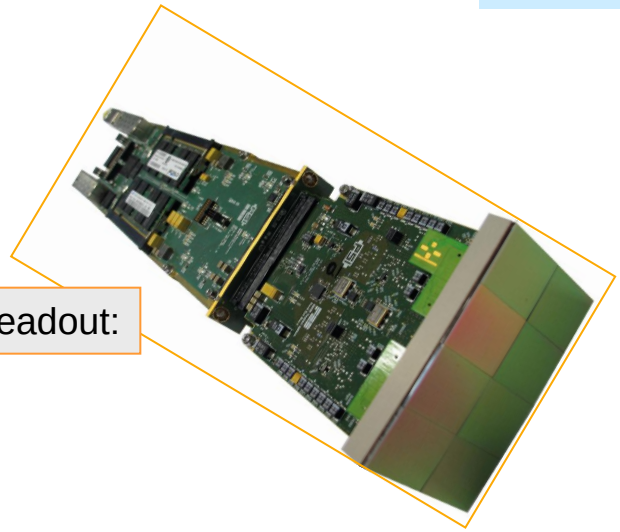
(C) Readout Electronics

Digital Data Processing/ Temporary storage

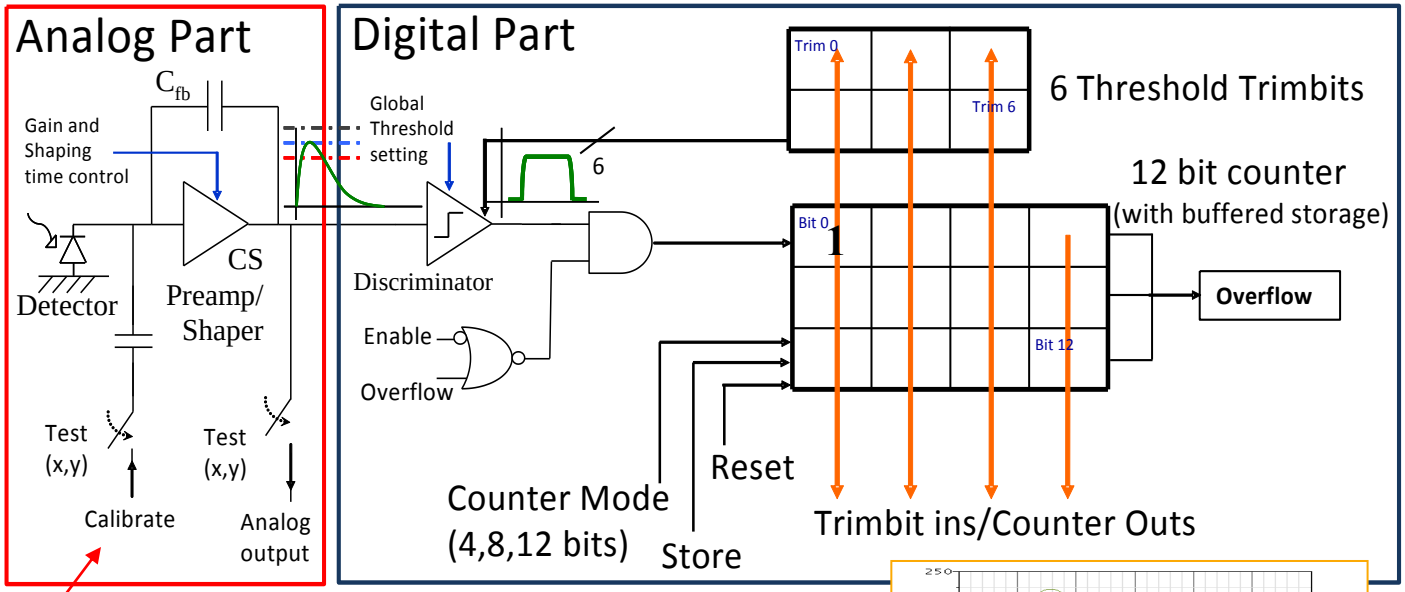
(D) Computer

DAQ and Readout Software

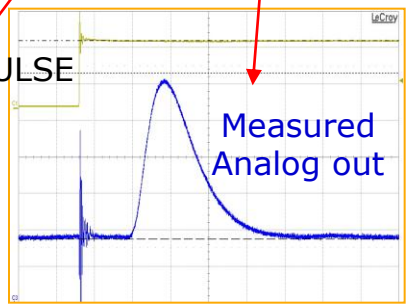
Readout:

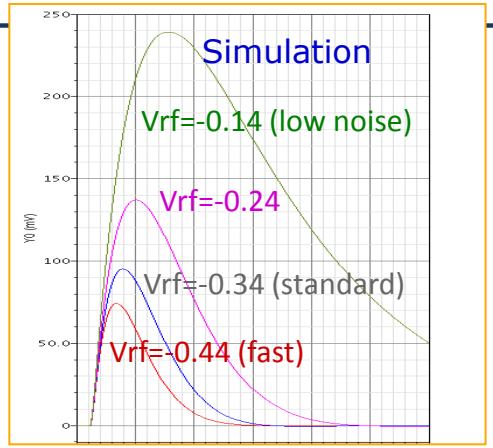


EIGER Pixel Cell



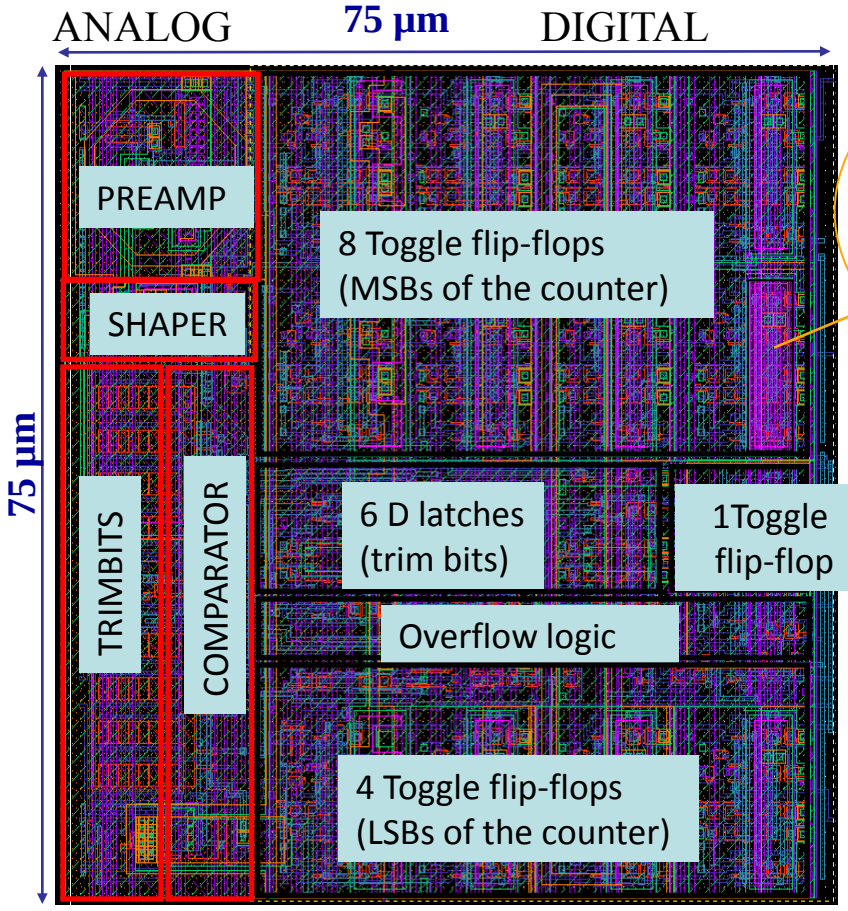
TEST PULSE

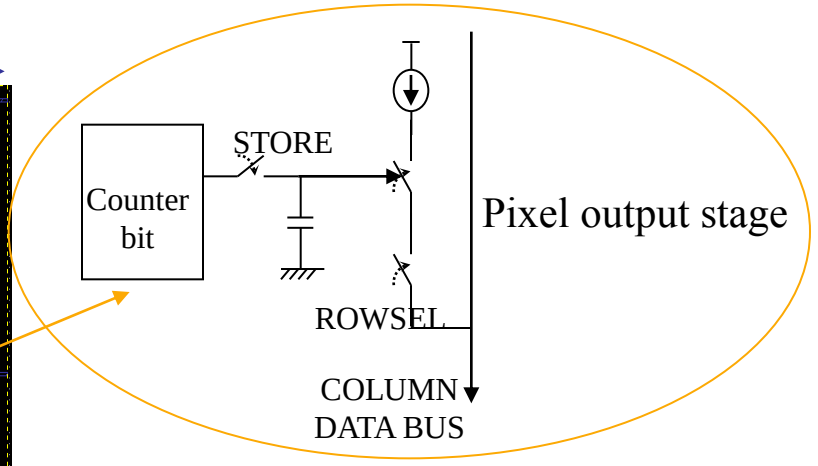




(t=50ms/div)

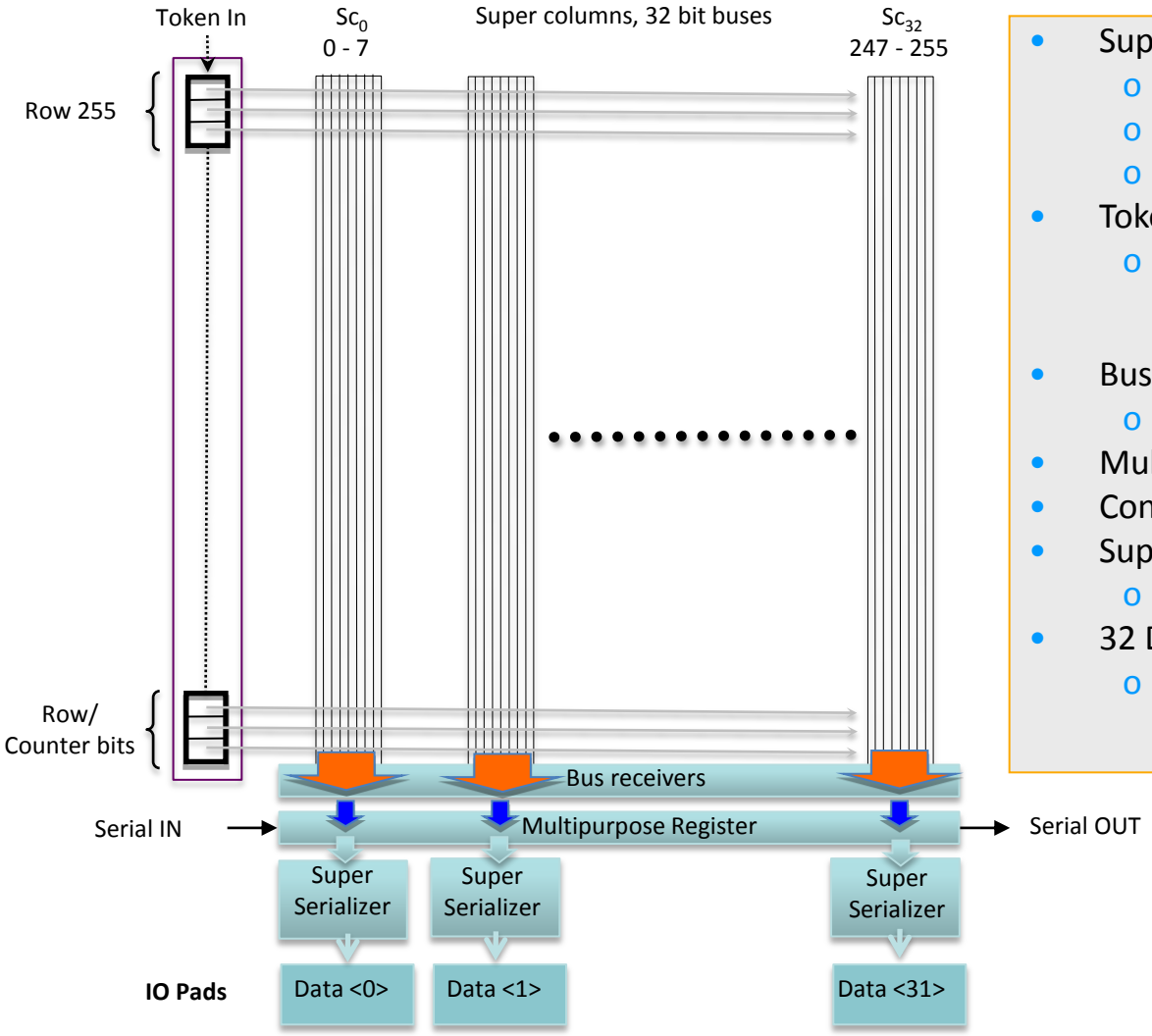
EIGER Pixel on Silicon





- Bump bond connection
- Preamp (TWELL)/shaper
- Comparator
  - Global threshold plus pixel trimming (6 bits)
- 12 bit counter
  - Counter logic
  - Buffered storage
  - Trim latches
  - Overflow logic

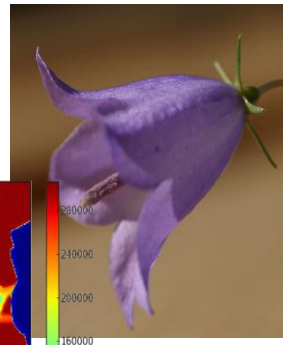
EIGER readout architecture



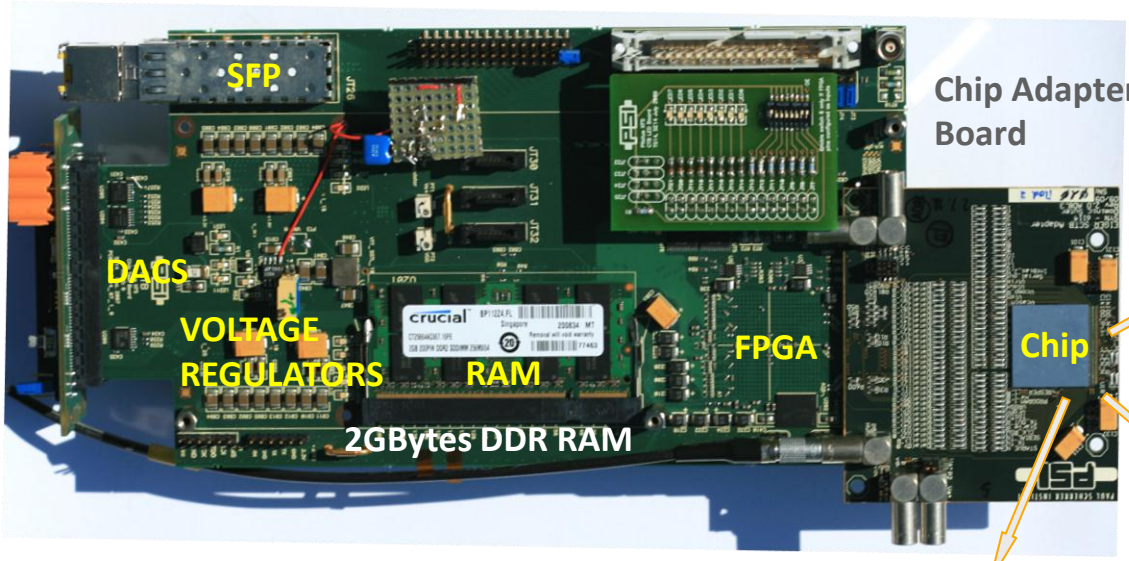
- Super column structure
  - 8 columns/super column
  - 32 super columns
  - Current mode data buses
- Token Shift Register
  - Connects 4 bits of the counter storage cells or trimbits of a row to the bottom register
- Bus receivers
  - Perform I/V conversion
- Multipurpose register
- Configurable serial/parallel I/O
- Super serializer
  - Serialize data sent to the pad
- 32 Data pads
  - 100 MHz DDR,TWELL

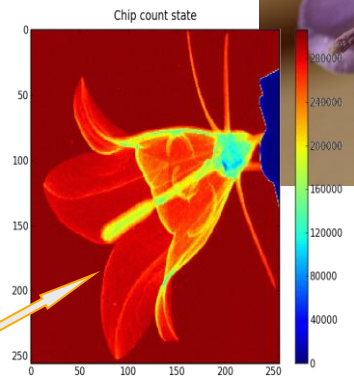
EIGER Single chip test Setup

First high quality image 02.09.09

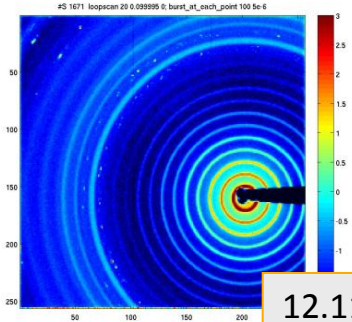


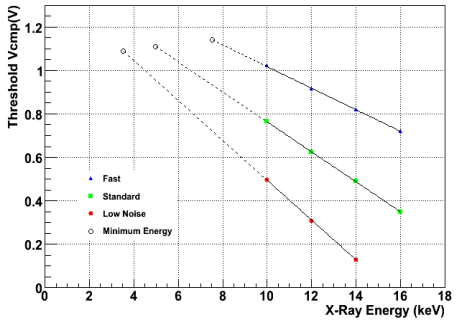
Standard Ethernet Data Link





Silver behenate calibration image.





EIGER Calibration and Characterization

12.11.2010 first time at the SLS-cSAXS beam line

Single chip calibration plan

❑ The samples

- several single **chips** tested with an **XRay tube and Fluorescence samples** for Trimming and Calibration.
- **1 chip tested** at the **PSI-Optics beam line** in two different periods (25-27/02/2011 and 17-21/03/2011). E=10-16KeV

Identify three modes of operation

- Fast
- Standard
- Low Noise

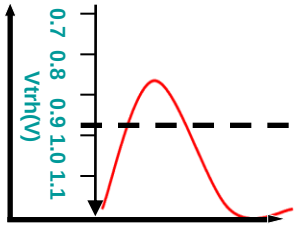
❑ Single Chip Calibration Plan

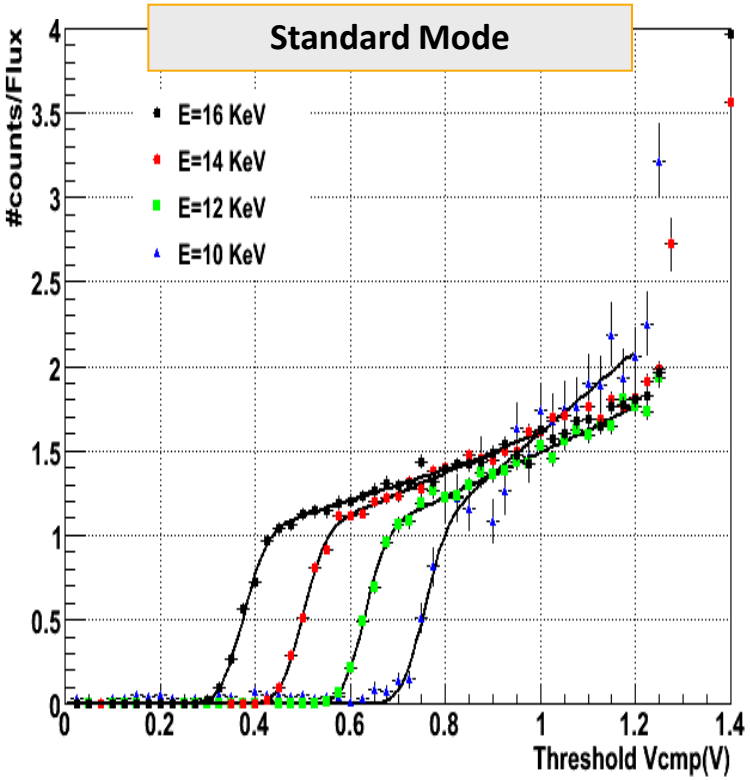
- **Start with DACs settings from simulation**
- **Optimize the DACs**
- **Define a threshold trimming procedure**
- **Measure different detector characteristic**
  - Energy calibration
  - Noise
  - Threshold dispersion
  - Rate Capability
  - Minimum Energy
- **Irradiation tests** performed at the beam line:
  - pixel region irradiated up to a dose of ~6MRad
  - row and column periphery up to a dose of ~7Mrad

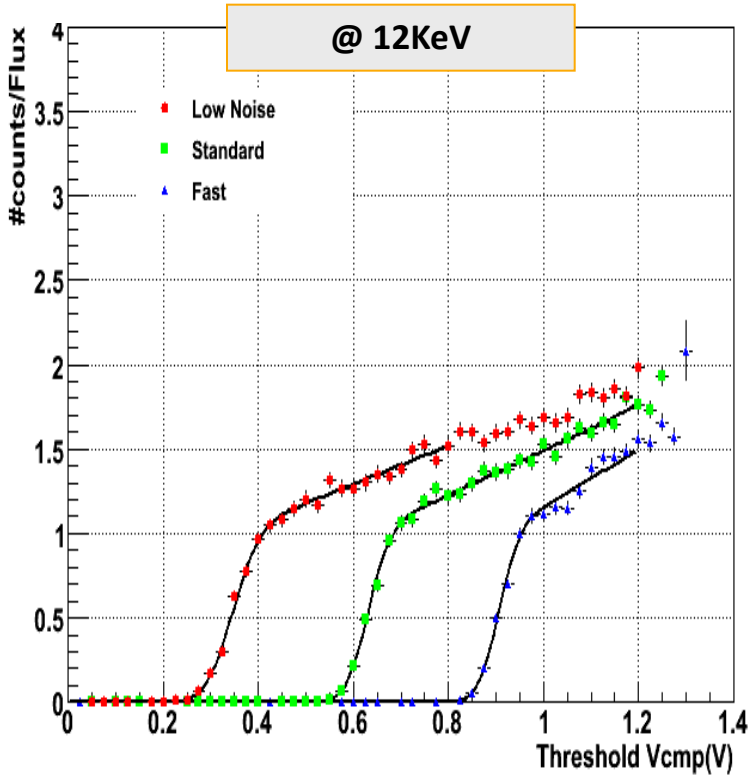
Following Results

Energy Calibration

- **Energy Calibration:** Monochromatic beam at the Optics Beam line: **10,12,14,16KeV**
- **Threshold scans:** Number of counts in each pixel vs Threshold







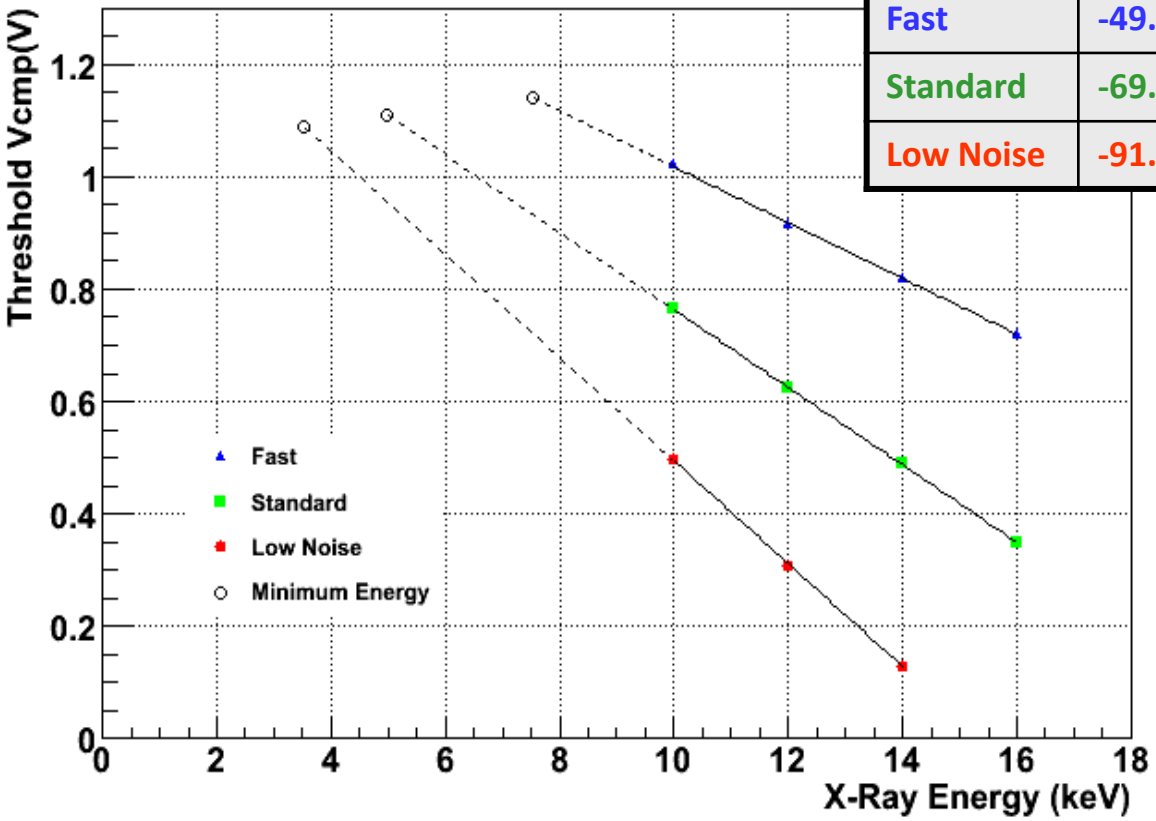
Fitting Function: Scurve·ChShar

$$n(V_{cmp}) = \frac{1}{2}\left(1 + erf\left(\frac{V_{cmp} - a_0}{\sqrt{2}a_1}\right)\right)(a_2 + a_3 V_{cmp})$$

a_0 inflection point; a_1 noise
a_2 flux; a_3 charge sharing param.

Energy Calibration

Energy Calibration plot

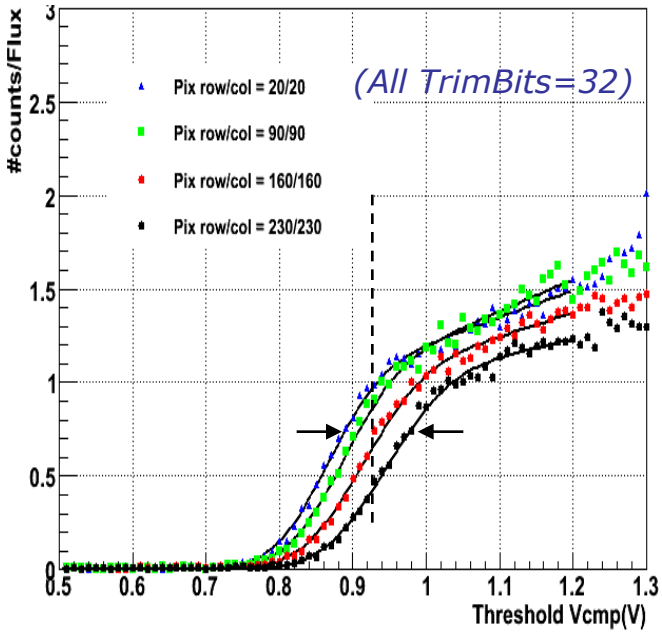


Operation Mode	Slope (mV/keV)	Offset (mV)	Minimum Energy Threshold (keV)
Fast	-49.60±0.02	1514.2±0.3	7.5
Standard	-69.02±0.04	1454.0±0.4	4.9
Low Noise	-91.7±0.1	1412±1	~4

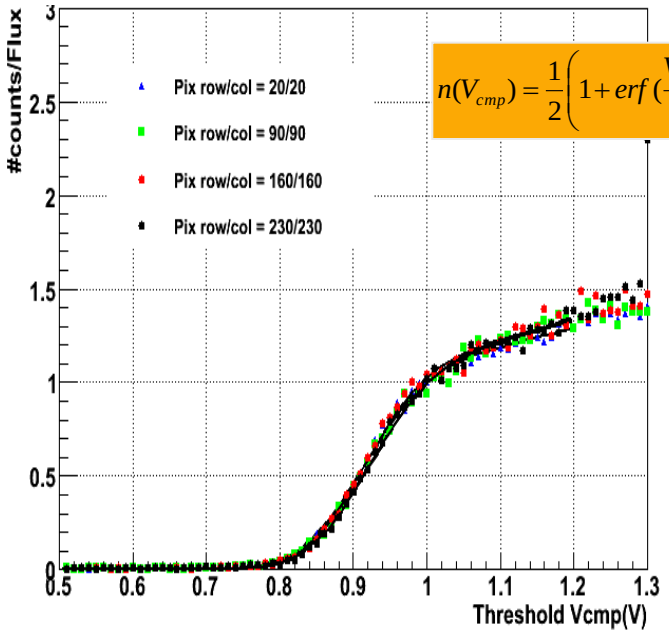
Data Analysis: Trimming

- **Trimming**: XRay tube and Fluorescence screens (Cu Screen **8KeV**)
- **Threshold scans:** **Standard Mode** of operation

Before Trimming



After Trimming

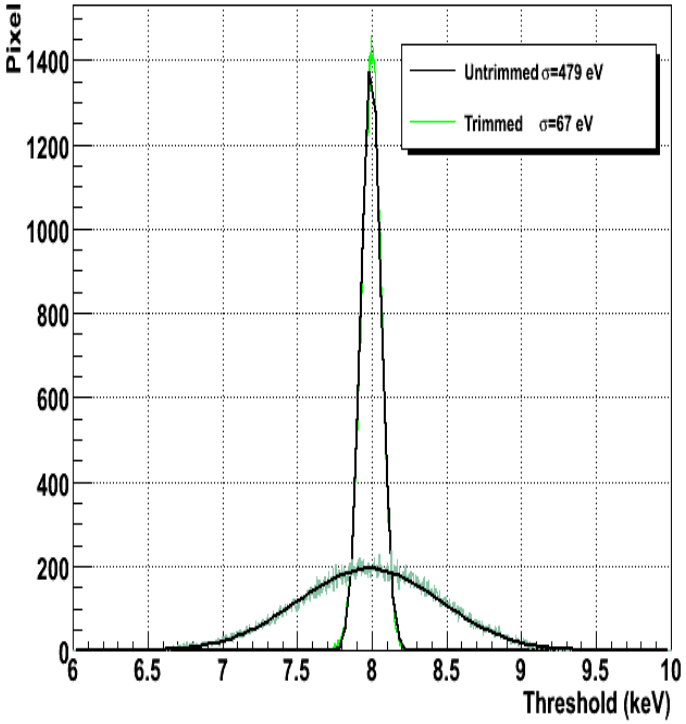


Threshold dispersion

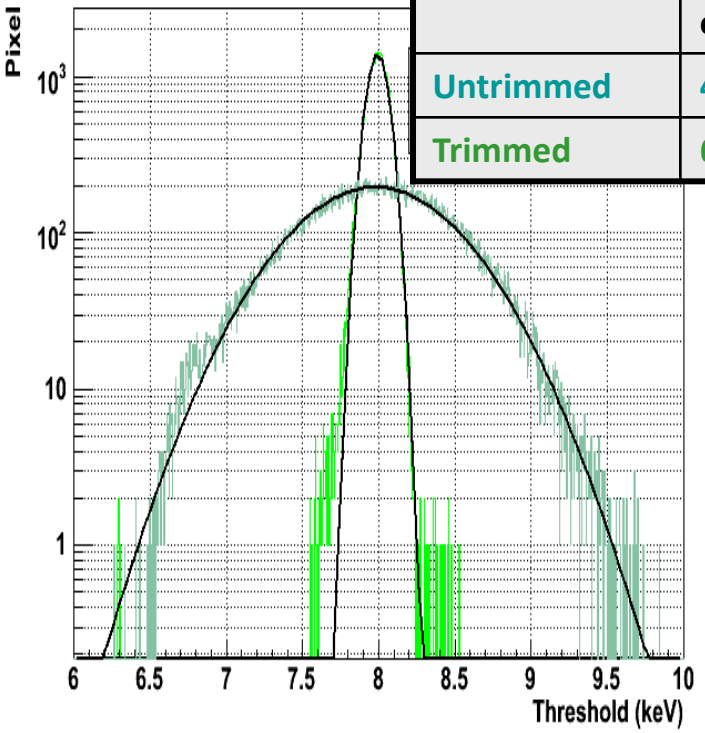
❑ **Threshold distribution**: **Standard Mode** of operation

$$n(V_{cmp}) = \frac{1}{2}\left(1 + erf\left(\frac{V_{cmp} - a_0}{\sqrt{2}a_1}\right)\right)\left(a_2 + a_3 V_{cmp}\right)$$

Threshold dispersion



Threshold disp. (LogY)

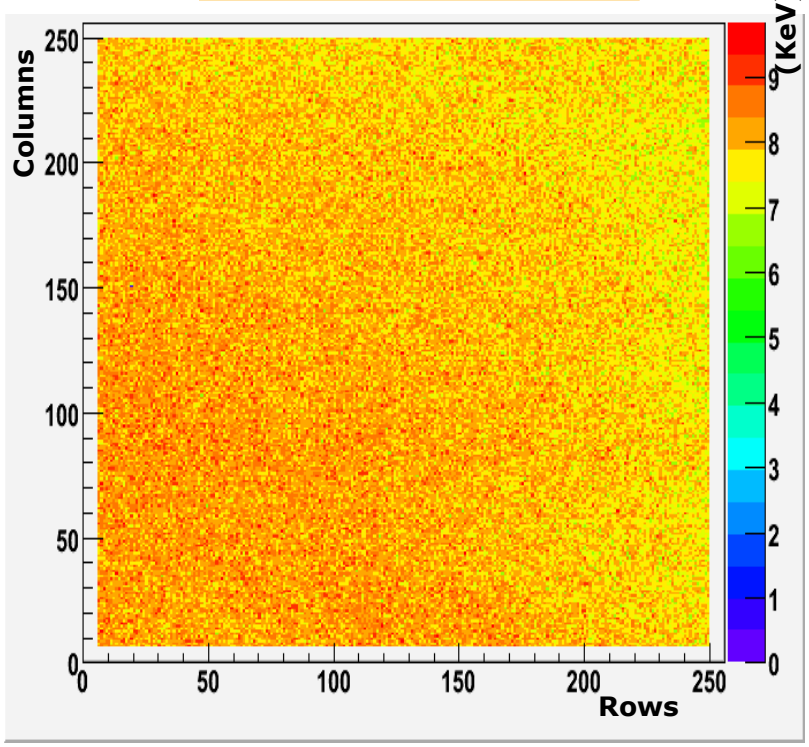


	σ(eV)
Untrimmed	479
Trimmed	67

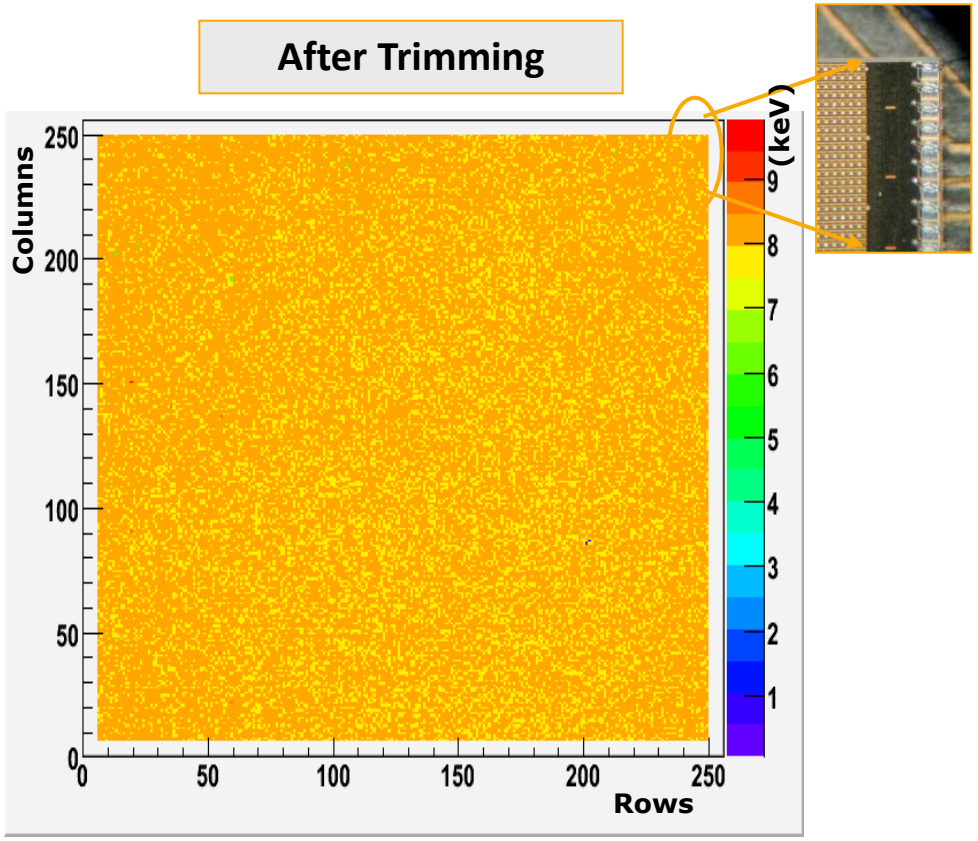
Threshold Map

- **Threshold maps**: **Standard Mode** of operation

Before Trimming



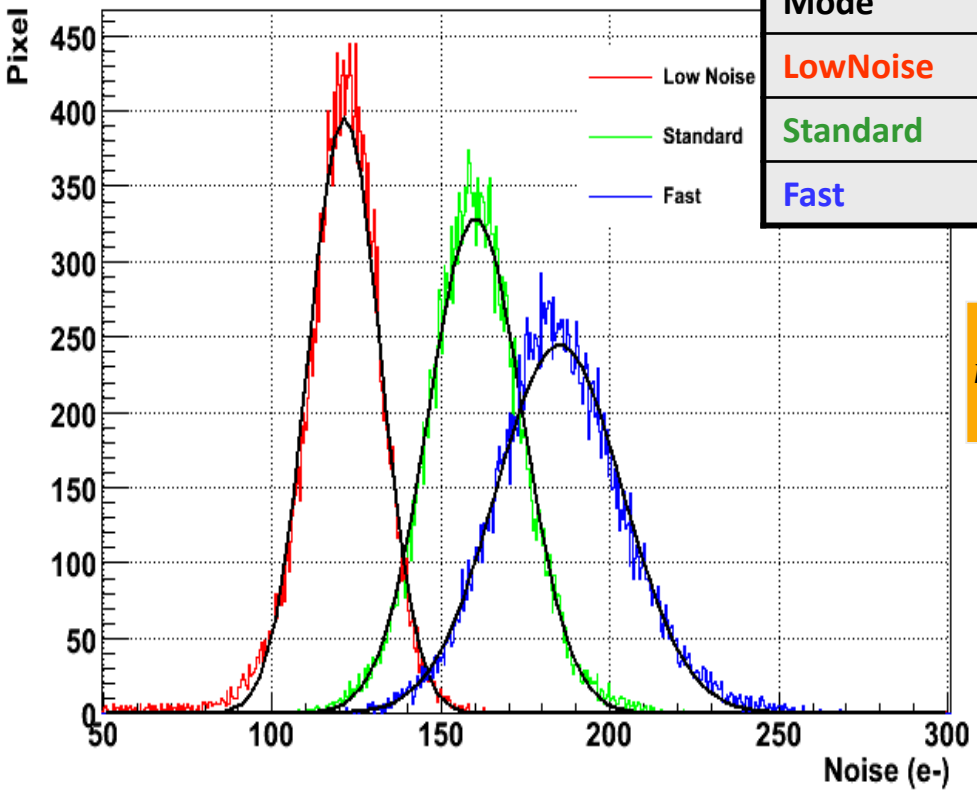
After Trimming



Noise

- **Noise distributions:** monochromatic beam at the Beam line

@14KeV

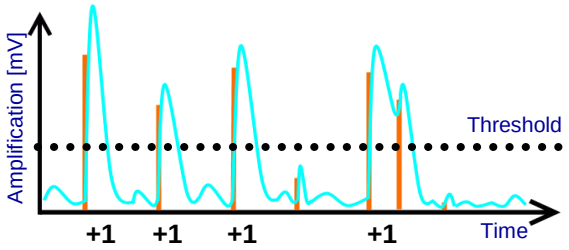


Operation Mode	Noise(e-)	Sigma (e-)
LowNoise	121.1±0.07	10.7±0.06
Standard	160.1±0.08	13.9±0.07
Fast	185.0±0.1	18.7±0.09

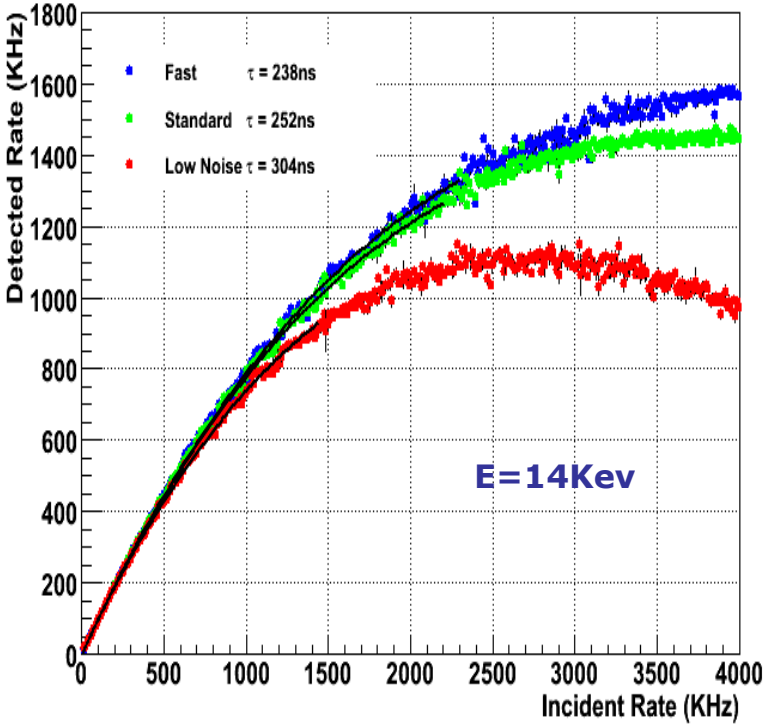
$$n(V_{cmp}) = \frac{1}{2}\left(1 + erf\left(\frac{V_{cmp} - a_0}{\sqrt{2a_1}}\right)\right)\left(a_2 + a_3 V_{cmp}\right)$$

Rate Capability

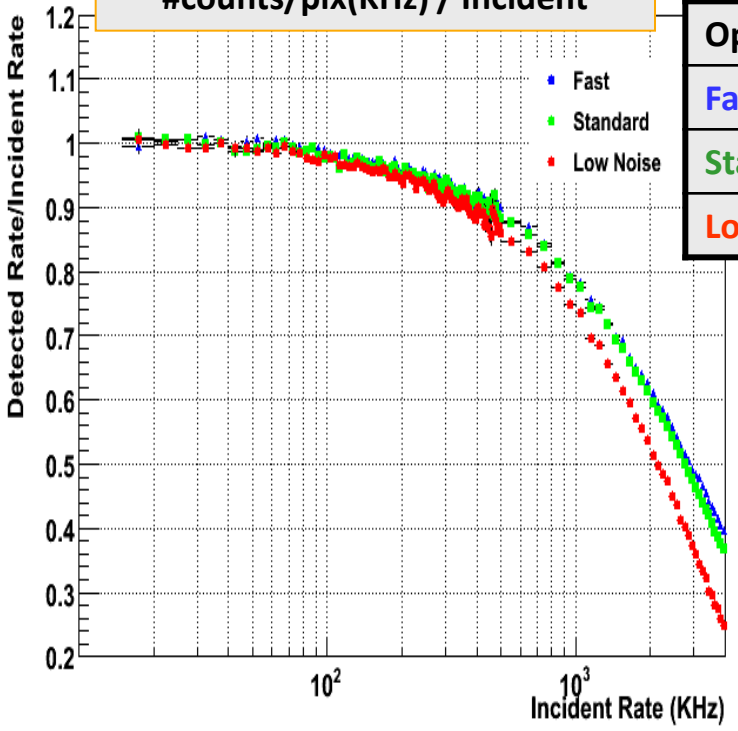
- **Rate Capability:** monochromatic beam 14KeV
- Scattering of direct unfocused beam on carbon
- Al. filters to reduce the flux
- In each mode of operations Vcmp set @ half energy



#counts/pix(KHz)



Rate Correction: #counts/pix(KHz) / Incident

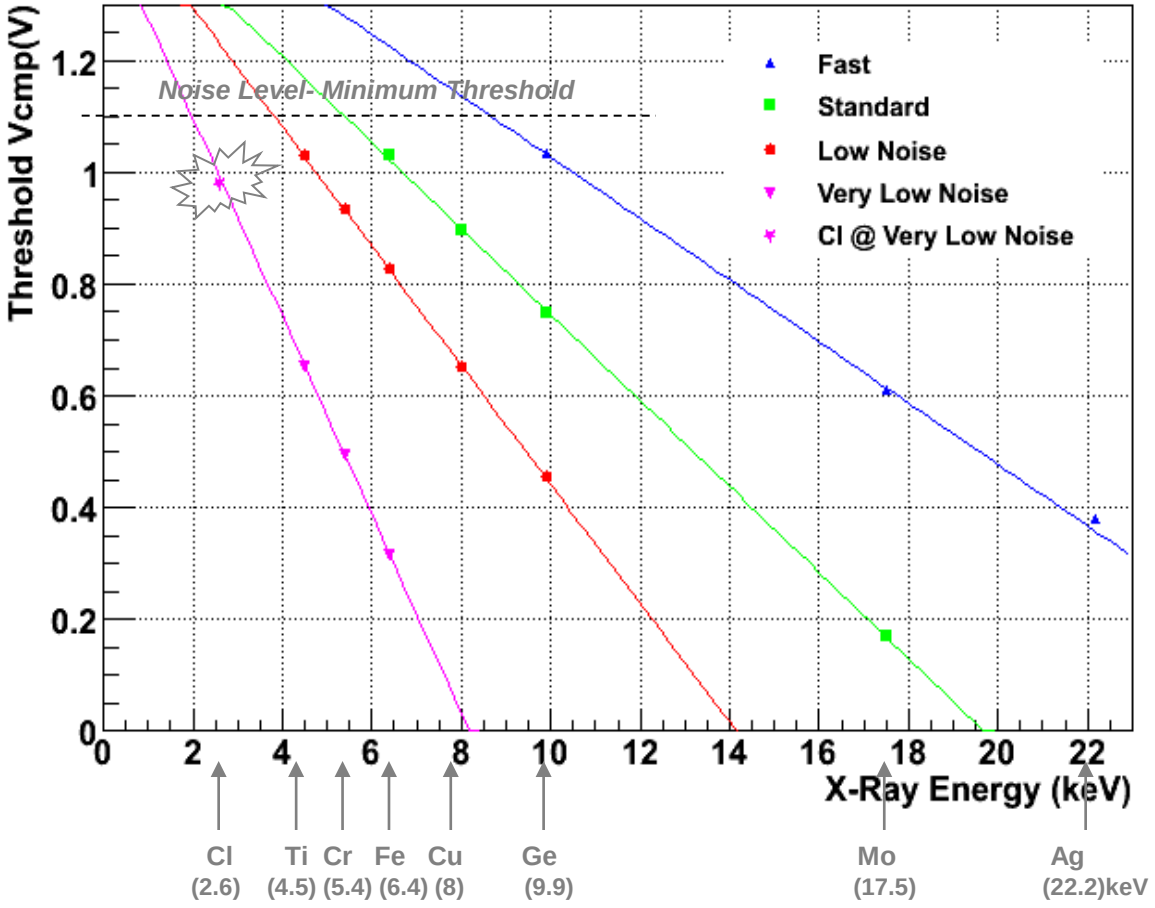


Op. Mode	T(ns)
Fast	238.2±0.2
Standard	251.6±0.3
LowNoise	304.2±0.8

$$N_{\det} = N_{inc} \cdot e^{-N_{inc} \cdot \tau}$$

Low energy operation

- **Energy Calibration**: XRay tube and Fluorescence samples: from Ag (22KeV) to Ti (4.5KeV) and Cl (2.6KeV)
- **One new mode operation** (Fuchsia)**:** "Very Low Noise" i.e. "Very High Gain of the Preamp."

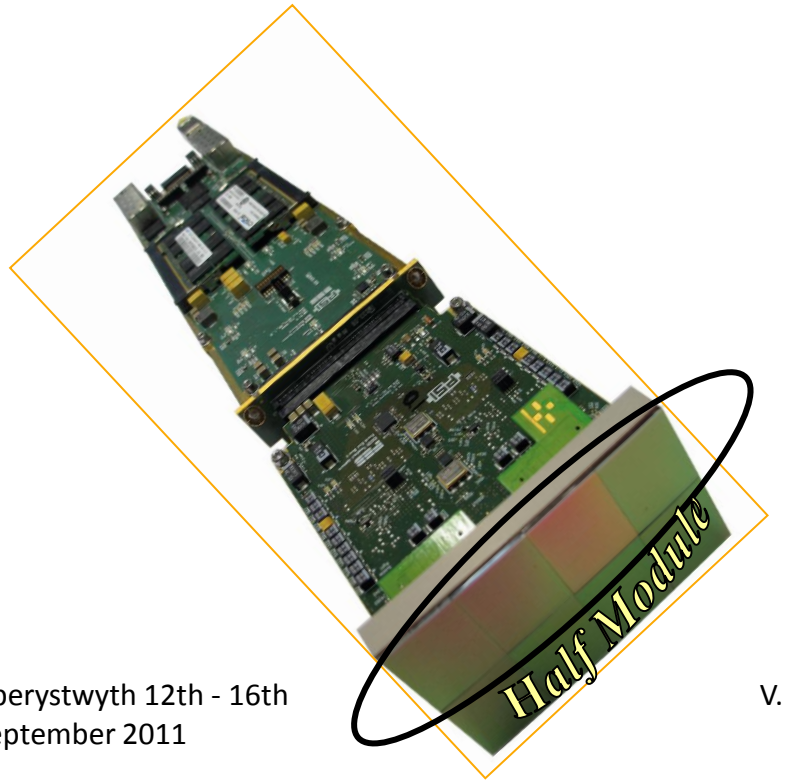


- good performance of the chip at low energy:
  - comparator is linear down to low energies
  - minimum threshold Vthr ~1.1V; safe operation of the comparator @ 1V
  - threshold energy as low as 2.5keV can set in the highest gain mode
  - a further higher gain could also be investigated
  - rate capability of "lower noise-higher gain" operation mode to be measured (good feedback from simulation)

From Single Chip to Module

EIGER Module:

- 2x4chips, 500k pixel
- 38 X 77 mm^2 Sensitive area
- Full Module flex high density interconnect board
- Front and Backend Boards
- Parallel readout on half module base
- 8 GB on module data storage



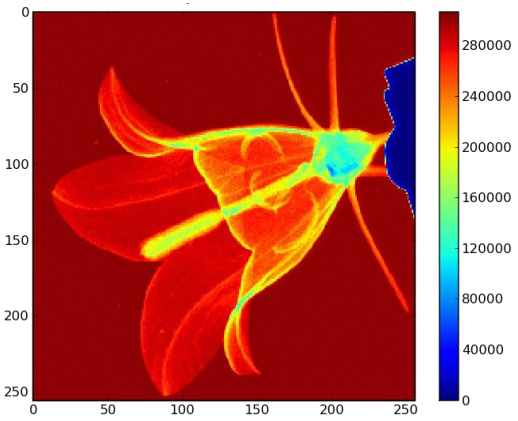
Steps towards the module read out:

- Boards have been produced and tested
- Firmware and software are ~ready
- Flex PCB; received May2011; first test OK

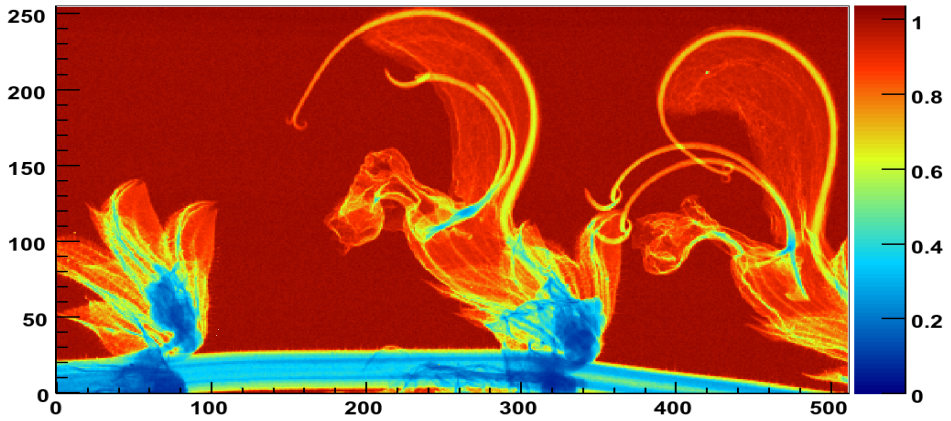
o first Half module connected to the final readout system in May 2011
o two chips read out simultaneously in May 2011
o first half module pictures on the 8th Sep. 2011

First Images (Flat field corrected)

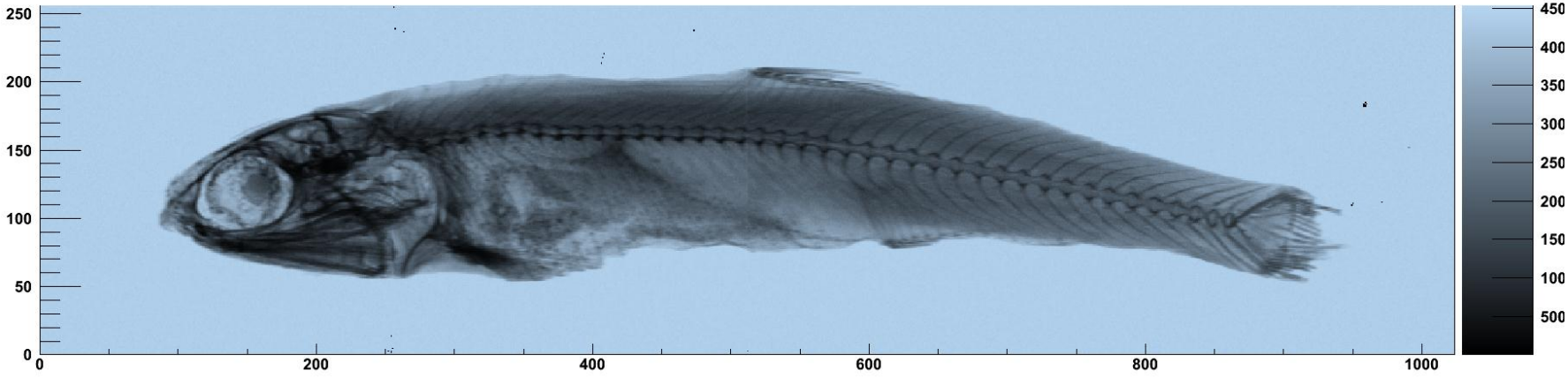
First **1 Chip** image;
02.09.09 Size~2x2 cm^2



First **2 Chips** image;
10.05.11 Size~2x4 cm^2



First **4 Chips** image; 08.09.1 Size~2x8 cm^2

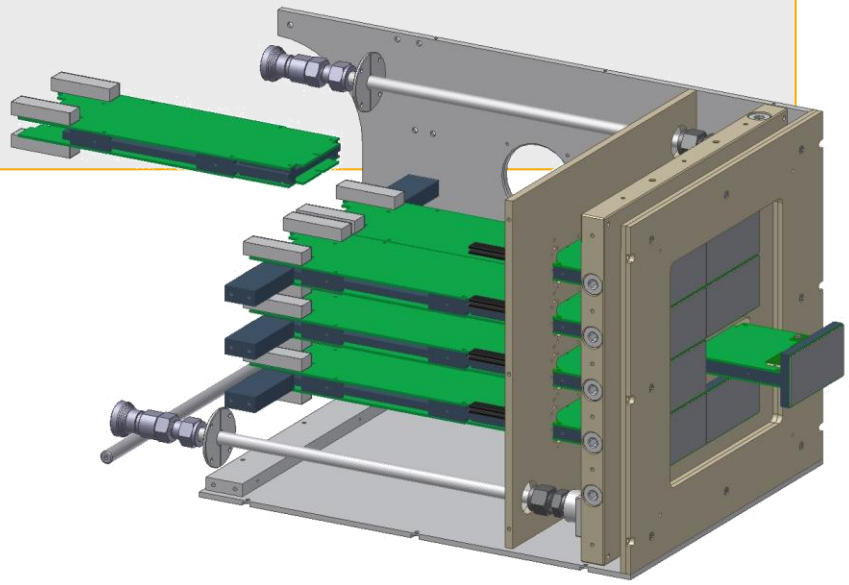


EIGER 4M

EIGER 4M pixels:

8 EIGER modules assembled together for a 4 million pixel detector:

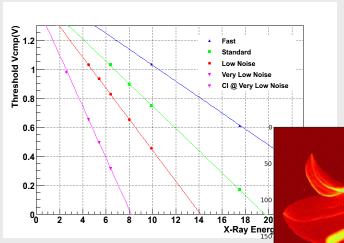
- 8x8 chips
- 2x4 modules
- ~16x16 cm^2

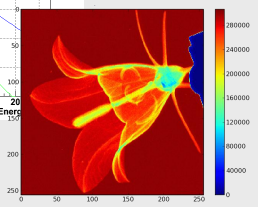


	Detector Specification			Data Size		Data Rate	
	Modules	Chips	Pixels	Bit	Byte	Gbit/s	MByte/s
Chip		1	65'536	524'288	65'536	6.3	750
Half-Module	0.5	4	262'144	2'097'152	262'144	25.2	3000
Module	1	8	524'288	4'194'304	524'288	50.3	6000
4M Detector	8	64	4'194'304	33'554'432	4'194'304	402.7	48000
9M Detector	18	144	9'437'184	75'497'472	9'437'184	906.0	108000
16M Detector	32	256	16'777'216	134'217'728	16'777'216	1610.6	201000

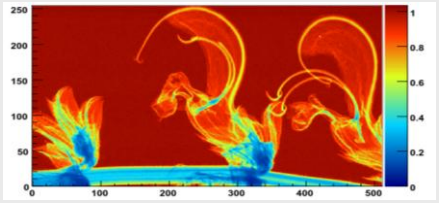
Conclusions

- The Eiger chip is operational since the end of 2009
  - First x-ray images achieved a 22 kHz frame rate
  - Detailed calibration in 2011 on several single EIGER chips
- Very good performance of the chip
  - Inflection point dispersion of ~70 eV
  - Noise sigma ~580 eV or 160 e-
  - Minimum Energy threshold ~2.5 keV
  - Irradiated chip, up to a dose of ~7Mrad, can be calibrated and works at full speed.

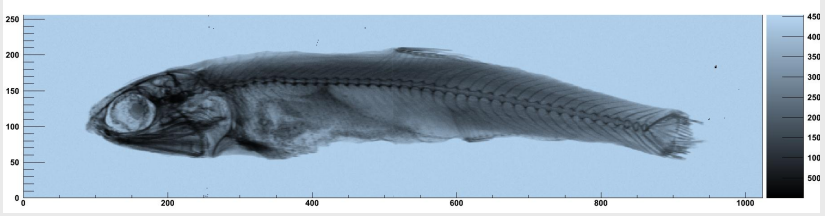




- Chips tested up to now are out of foundry specifications
  - the same chip design has been produced a second time and are within the foundry specifications
  - it is currently being prepared for wafer testing and bump bonding
  - from simulation we expect to have improved performances: lower noise and faster speed!
- First experiments at SLS beam line
  - Time resolved experiments on proteins
  - X-ray Photon Correlation Spectroscopy



- We are working towards modules
  - Front and Backend Boards produced
  - Firmware and software ready
  - First 2 chips XRay images May 2011
  - First 4 chips XRay images 8th Sep. 2011



- Larger Detector Systems are coming soon

Many thanks to the PSI SLS Detector Group

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Wir schaffen Wissen – heute für morgen

PSD9
9th International Conference on POSITION SENSITIVE DETECTORS

Aberystwyth
12th - 16th
September 2011

Backup Slides

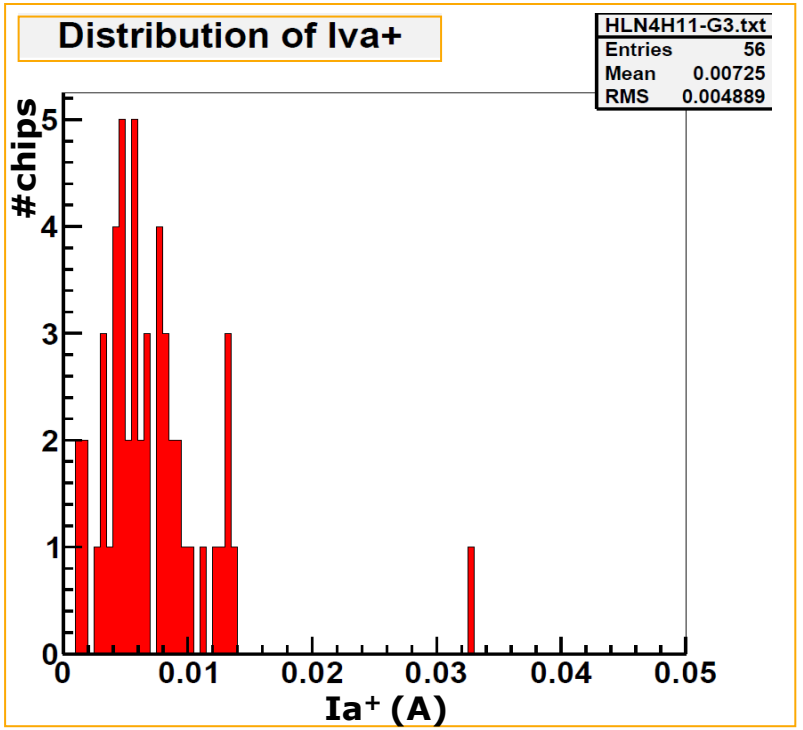
Further considerations

- Distribution of Ia^+ for a nominal Va^+ settings (1.14V) measured on the chips in one wafer *(Wafer test setup)*

- For the chip under test:
  Ia^+ ~ 8mA; $Iash^+$ ~ 91mA
  Ia^+/pixel ~ 122nA; $Iash^+$/pixel ~ 1.40µA

- Ia^+ and $Iash^+$ are lower then expected
  from sim. nom. ~ 182mA
  /pixel ~ 2.78µA

- Simulation: Lower analogue currents:
  - LOW power chip
  - BUT higher noise
  - Slower preamp.!



The present configuration can be defined as **"LOW POWER"** chip!