# Knowledge Exchange Towards High-k Dielectrics, CMOS and Solar Cells

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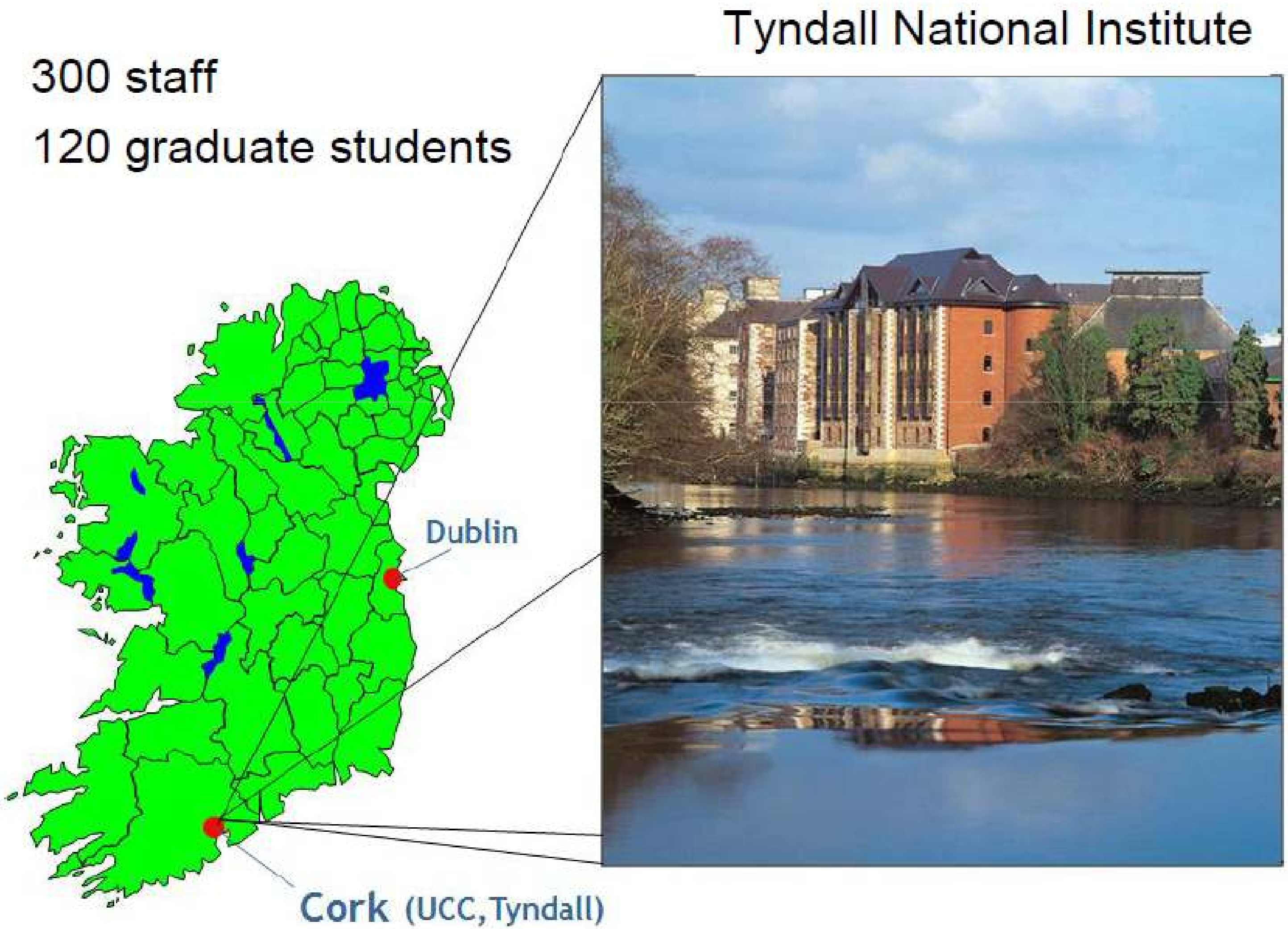
# Outline

- Introduction
  - Field background
  - FORME project
- Knowledge exchange protocols
- Atomic Layer Deposition
  - Results
  - Applications
- Conclusion

# Tyndall

- 300 staff
- 120 graduate students



# Tyndall

new c.5,600m$^2$ state-of-the-art research building opened in 2009

Annual revenue 2010 ~33M€

# Tyndall

new c.5,600m$^2$ state-of-the-art research building opened in 2009

Queen’s visit May 2011

# AMSG

**Advance Materials and Surfaces Group**
*Innovation through materials design*
*and process development*

Prof Martyn Pemble

**Thin films and surface structures, CVD, MOVPE and ALD**

- Growth and modification of novel thin film systems and surface structures by chemical vapour deposition (CVD) metal organic CVD (MOCVD), metal organic vapour phase epitaxy (MOVPE) and, most recently, atomic layer deposition (ALD).

**Photonic band gap materials**

- Synthesis of novel particles and their self-assembly into photonic band gap materials, that are similar in structure to natural opals.

# Deposition Equipment

Wide range of ALD and CVD systems available

- small scale lab systems through to 12 inch systems

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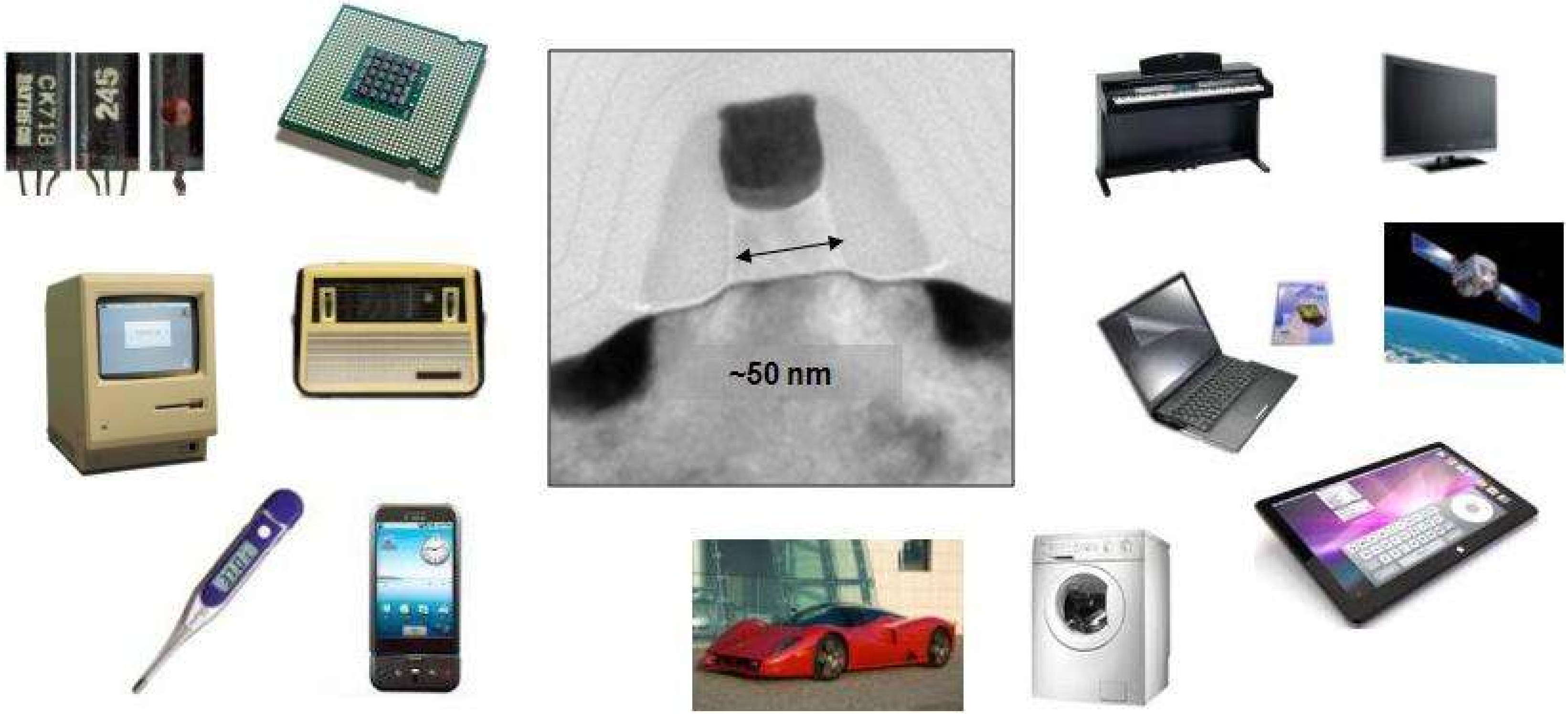
# MOS Technology

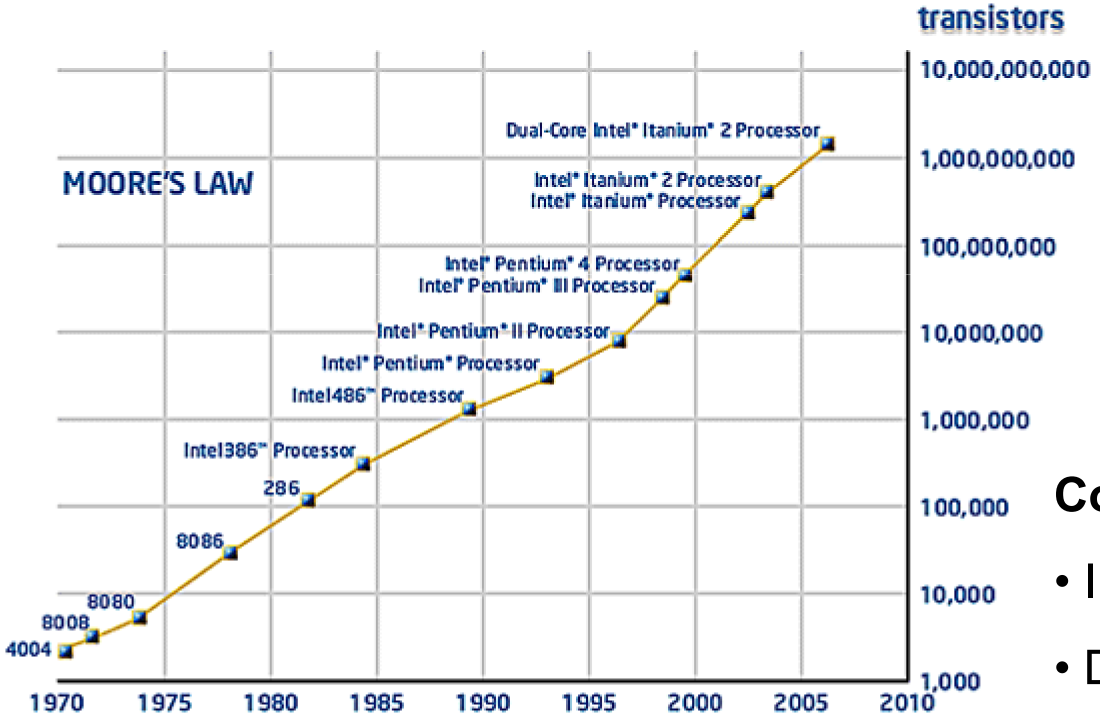
## Metal Oxide Semiconductor Field Effect Transistor
## MOSFET

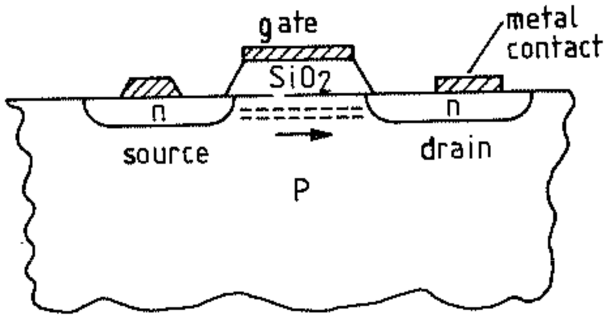


The MOSFET is at the heart of the information and communication age

# MOS Technology

- Industry standard are Si/SiO$_2$ devices; scaling required as predicted by Moore [1]





**Continued scaling of gate oxide:**

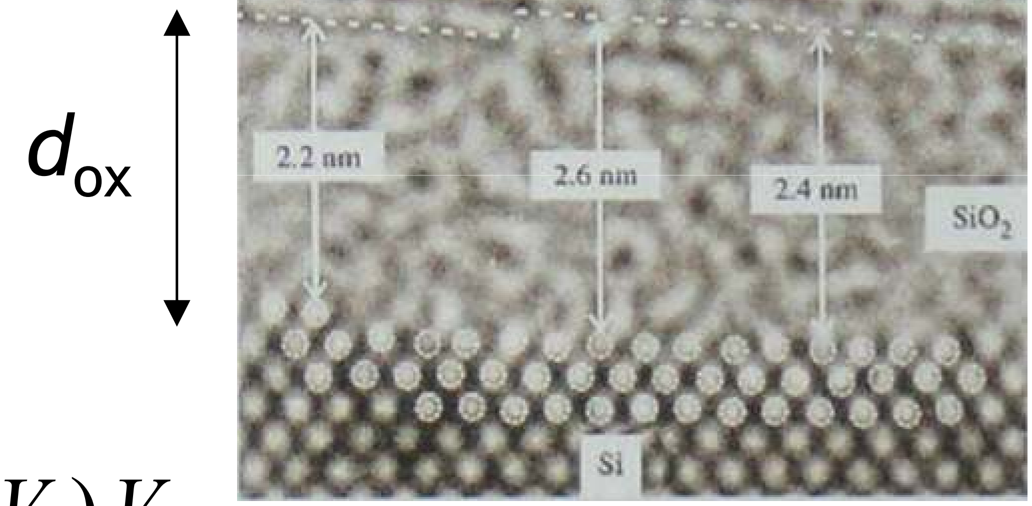
- Increased leakage current
- Device breakdown

[1] Moore, *Electronics*, **38** (8), (1965).

# Si/SiO$_2$ Limit

*Only disadvantages*
*SiO$_2$, k = 3.9*

$$C_{ox} = \frac{\varepsilon_0 \kappa}{d_{ox}} A$$



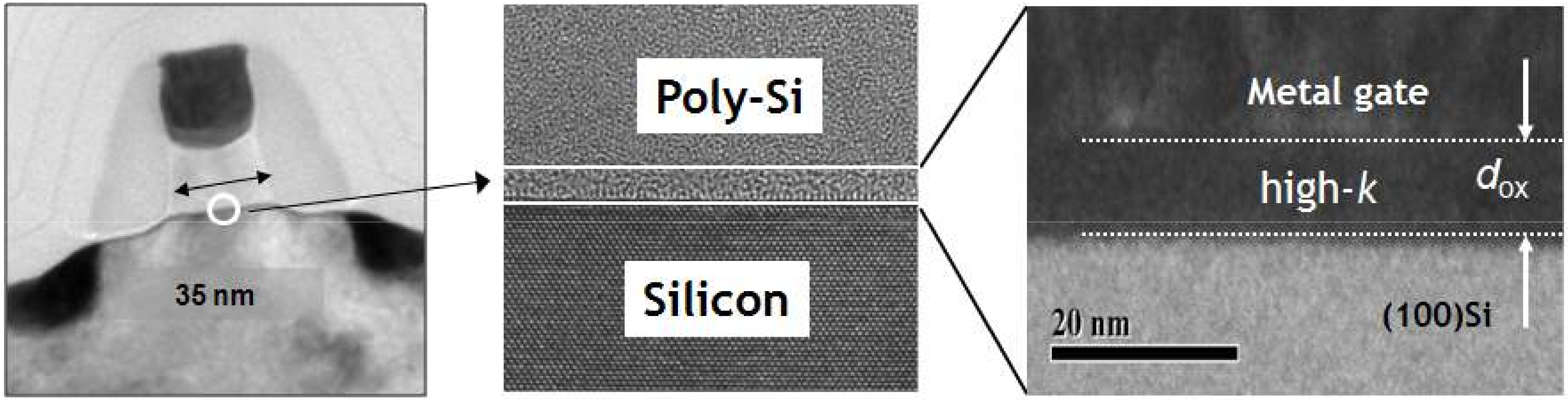
$$I_d = \mu.C_{ox} \frac{W}{L} (V_{gs} - V_t).V_{ds}$$

Running out of atoms in the gate oxide as they cannot be scaled

# Solution: High-*k* Oxide

**65 nm (2006) MOSFET** **$SiO_2$ ~1.1nm**

High-*k* structures fabricated at Tyndall



$$C_{ox} = \frac{A.\varepsilon_0 \kappa}{d_{ox}}$$

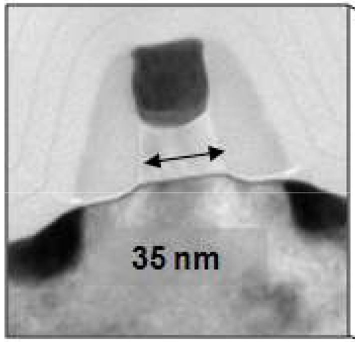
$\kappa$ ($SiO_2$) = 3.9
$\kappa$ ($ZrO_2$) : 20-25

Same Gate Capacitance / Physically Thicker Gate Oxide

# Future: III-V Channels

> 2 billion transistors per chip, Gate length ~ 10nm, $V_{dd}$ ~ 0.5 V, Clock speed>20GHz

65nm



2006

45nm

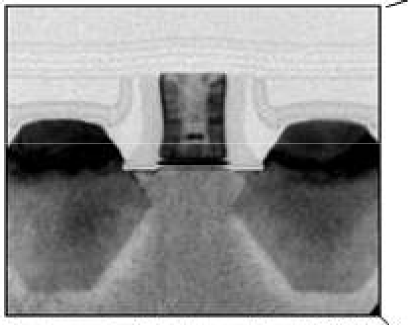
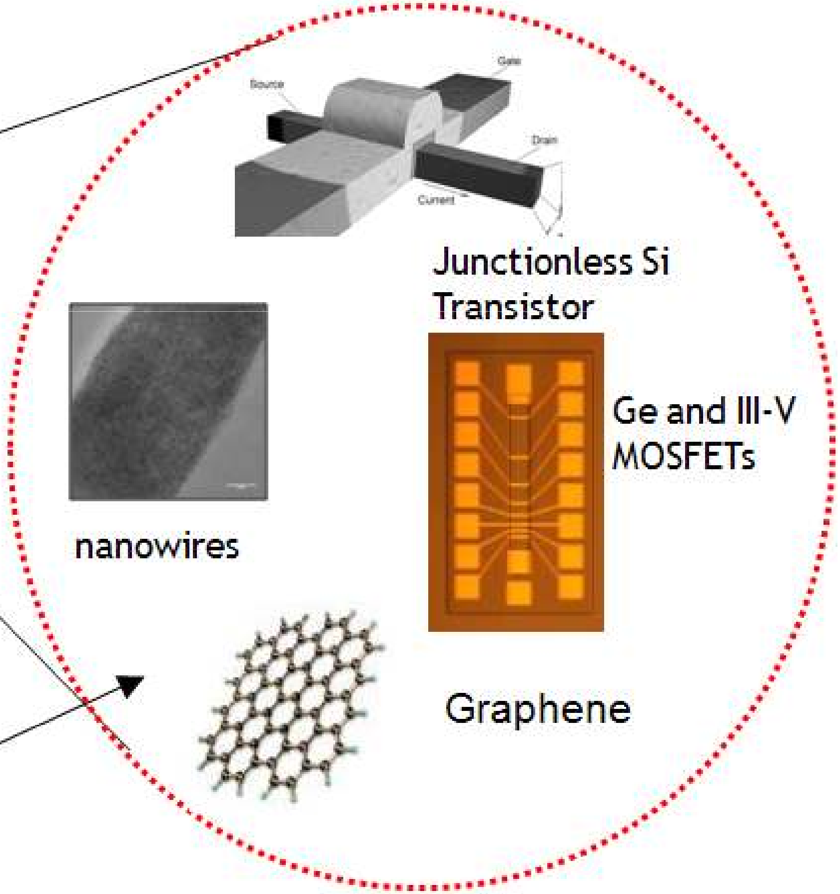


Fig.6 TEM micrograph of high-k + metal gate PMOS transistor.

2010

~10 nm



> 2015

Transistor options beyond 2015

Higher Performance / Same Power

Same Performance / Lower Power

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# FORME Project

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## Strategic Research Cluster: Functional Oxides and Related Materials for Electronics

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University College Cork, Ireland

TRINITY
COLLEGE
DUBLIN

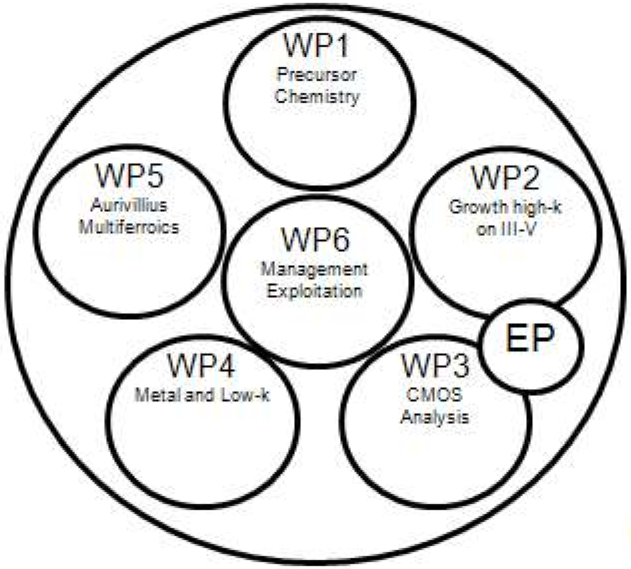
DCU

sfi
Fondúireacht Eolaíochta Éireann
Science Foundation Ireland

UCD
DUBLIN

Queen's University
Belfast

16 Lead Scientists
7 interns
18 graduate students (+2)
6 postdocs
1 Admin
(+18 collaborators)



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APPLIED
MATERIALS.

SAFC Hitech™
Enabling Technology

Seagate

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# FORME Project

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WP1 & 4
Precursor
Chemistry
Oxide/Metal

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# FORME Project

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# WP2
# Deposition

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# WP3 Device Characterisation

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# FORME Project

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WP5
Multiferroics

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MATERIALS.

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# WP6
# Management
# Exploitation

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# FORME Project

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APPLIED MATERIALS.

AFC Hitech™
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EP
Photovoltaics

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# Knowledge Exchange

Knowledge Exchange describes the processes, mechanisms, networks and relationships that enable knowledge derived from research activity to move between organisations. The term is applied to the sharing of knowledge that has potential impact on innovation, and to change, transform, enhance or generate new or improved professional practices, policies, technologies, products, services and public perceptions.

ie Talking to one another to spread the word and advance state of the art

# Commercialisation

Commercialisation describes the process by which the outcomes of research activity are brought to the market place through the development of new products, processes, services or technologies. The process involves the identification of research which has potential commercial interest and the designing of strategies for how to exploit this research. This will include the protecting and managing of the rights to intellectual property. Strategies can include the creation of licensing agreements or joint ventures, partnerships, or spin-out companies.

ie Talking to one another to deliver new products to make money

# Disconnect

The Knowledge Inventor is usually a scientist working in a highly specific area and interested in moving forward state of the art

The Knowledge Exploiter is usually a business man working in a different area and interested in growing the company revenue

These two entities, with different outlooks and desires, require somebody to bring them together. More Universities and Companies are establishing Technology Transfer Offices to address the disconnect

At the onset of the project a collaboration agreement was implemented to establish protocols to try to address this issue

# Knowledge Flow

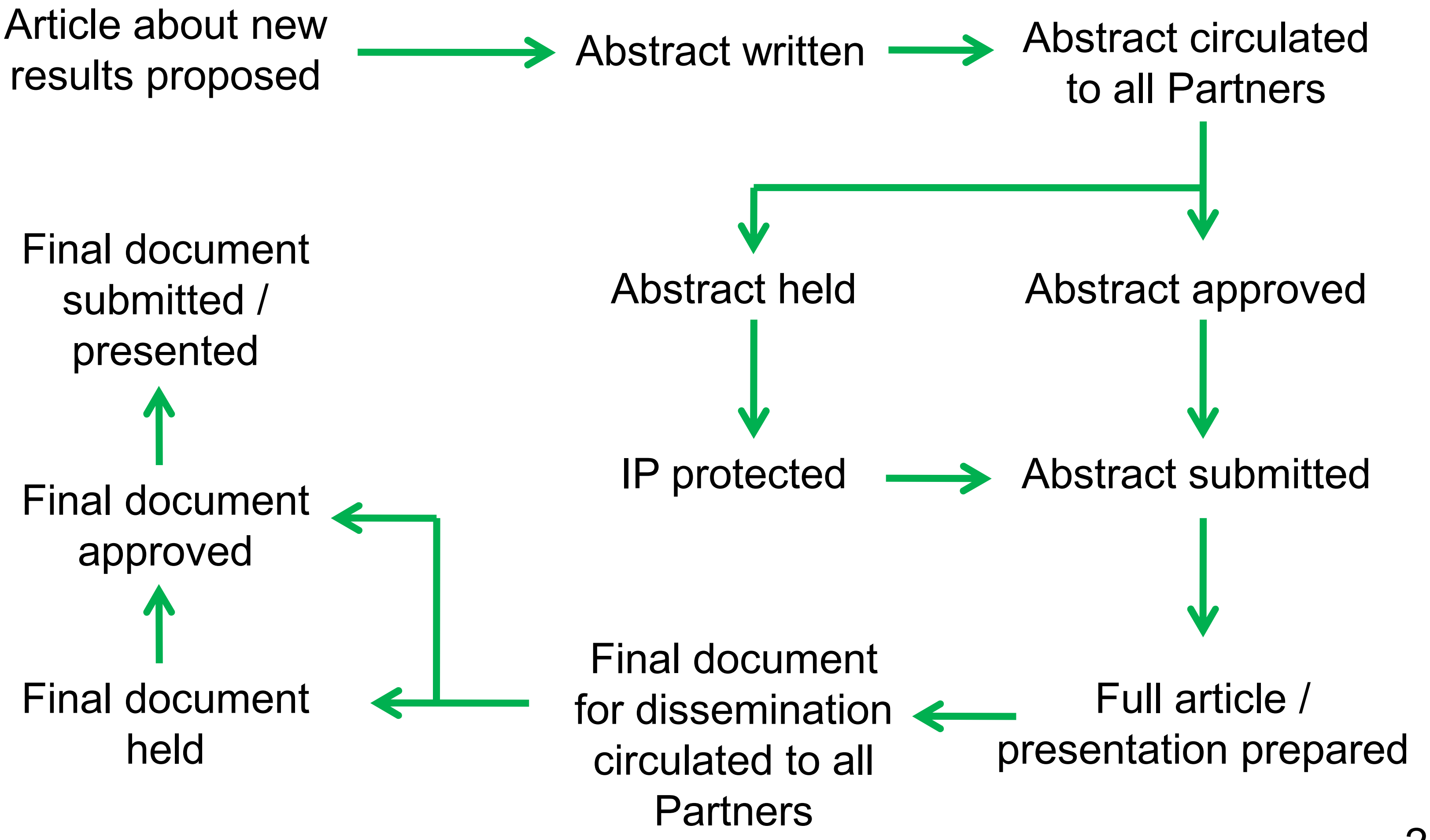
Individual Partners generate Knowledge
Knowledge exchange between Partners to extend Knowledge
Identification of exploitable Knowledge
Protection of exploitable Knowledge
Dissemination of exploitable Knowledge

Industry engagement
Knowledge Transfer
Commercialisation

Consortium Agreement

Problem areas – Secrecy,
– Value of Knowledge

# Dissemination Protocols



Article about new results proposed

Abstract written

Abstract circulated to all Partners

Abstract held

Abstract approved

IP protected

Abstract submitted

Full article / presentation prepared

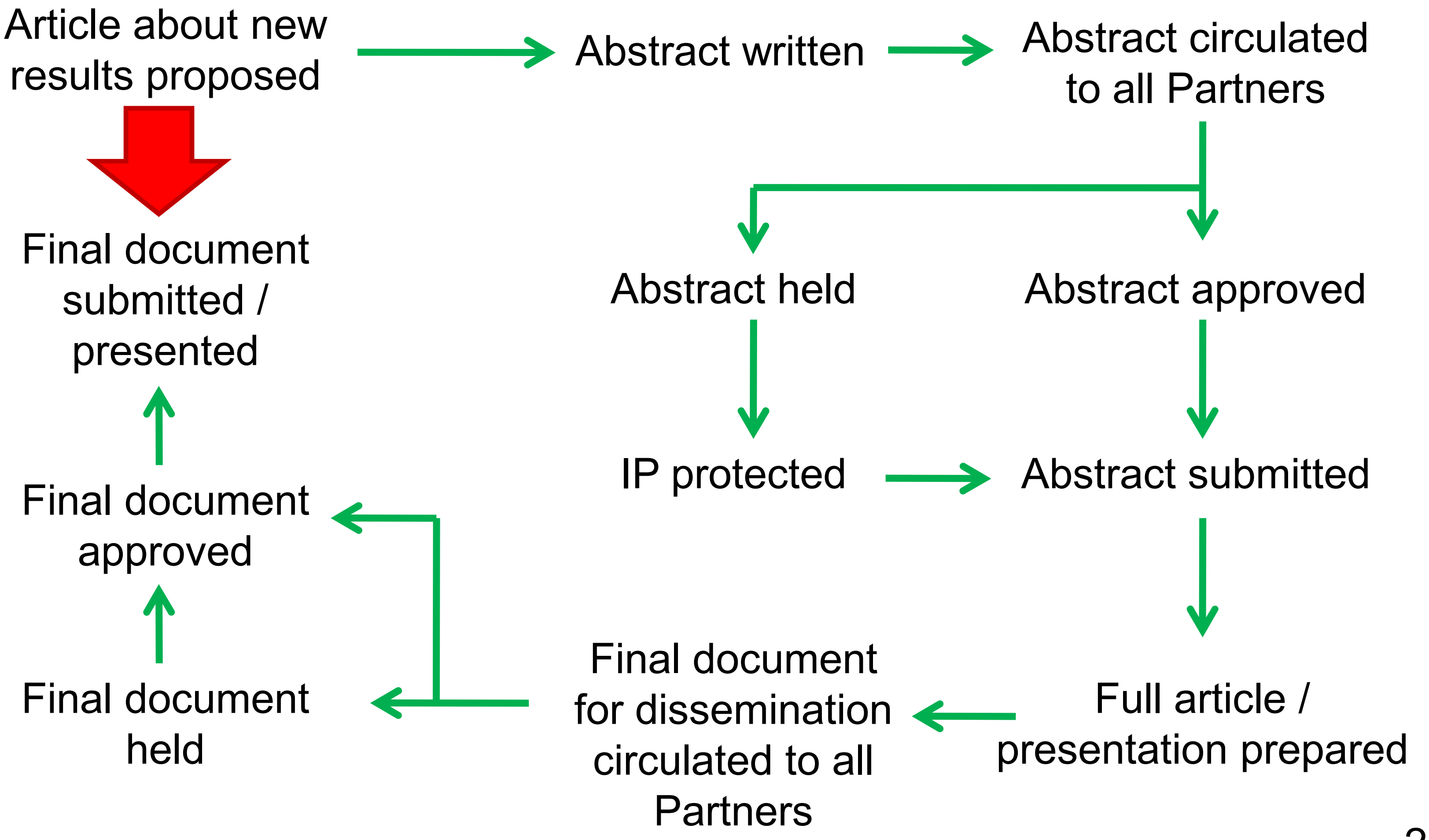
Final document for dissemination circulated to all Partners

Final document held

Final document approved

Final document submitted / presented

# Dissemination Protocols



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# Negotiations

Academic Partners good science hence pressure to publish
Industrial Partners good process hence pressure to keep secret

Industry proposes it will take significant resource to turn Knowledge into a product => low valuation

Academia proposes Knowledge is cutting edge and took significant resource to achieve => high valuation

Industry support of project vital to achieve funding and commercial inputs to focus research => low valuation

Academia support primarily through public funding requiring value for money demonstration => high valuation

# Negotiations

Case by case review to reach a compromise to benefit all

On FORME a specific post of Exploitation Manager was created

Example
The key development was the ability to deposit highly controlled interface control layers using ALD

Compromise articles presented on device performance but process details withheld. In-house Industry research ongoing to develop product.

Further exploitation of technology outside project in different fields where a highly controlled film fabrication process is of benefit

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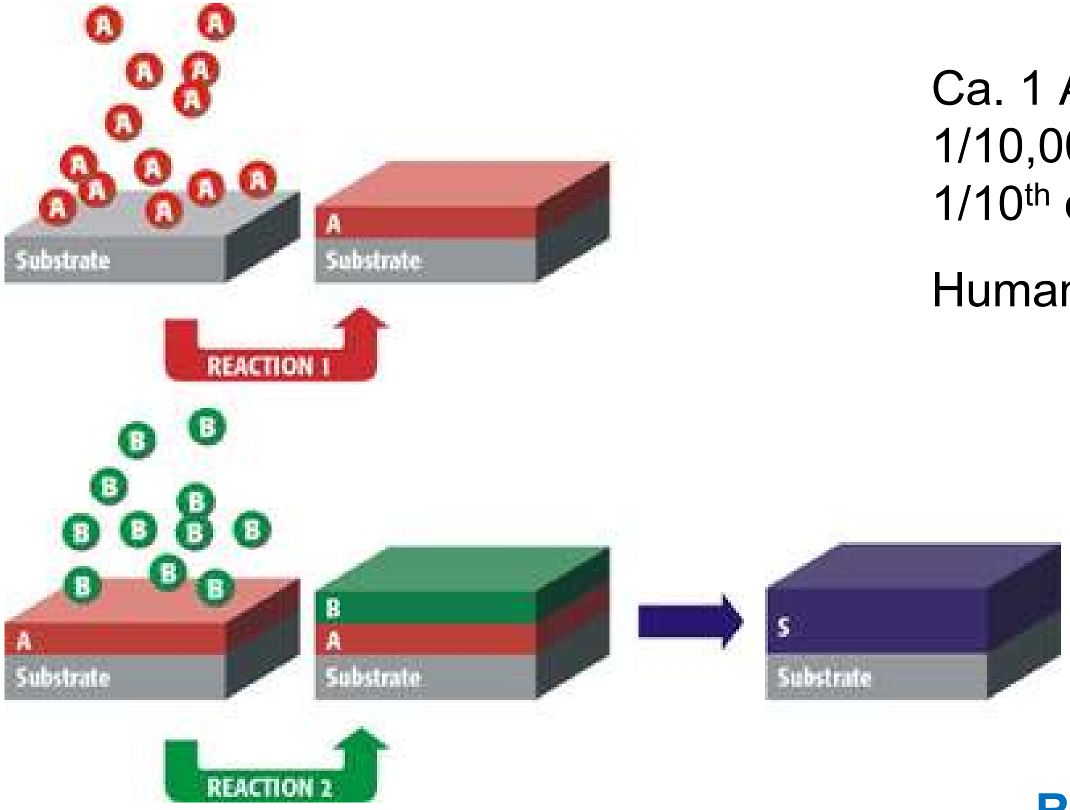
# Atomic Layer Deposition



Ca. 1 Å per cycle, where 1 Å = 1/10,000,000,000th of a metre, or 1/10th of a nanometre

Human hair = ca. 0.00005 metres

H Hoffmann, TU Vienna

**Reaction driven process**

Self-limiting growth, between 0.4 and 0.8 monolayers per cycle,

low temperatures, typically less than 350°C, highly conformal

# Atomic Layer Deposition

Advantages of ALD

Uniform surface coverage

– excellent for coating 3D structures

Low temperature process

– compatible with heat sensitive substrates

Precise growth rate control

– accurate layer thickness on nm scale

Flexible stoichiometry control

– film composition as targeted

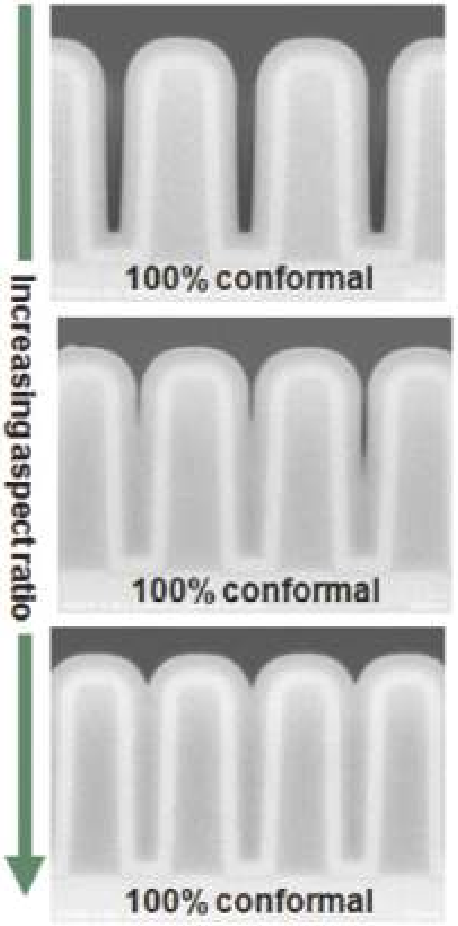
Surface reaction driven process

– more efficient precursor usage

Disadvantage

Slow deposition rate

– not suited to thick film growth



# Material Systems

**Oxides**

$Al_2O_3$, $TiO_2$, ZnO, $ZrO_2$, $HfO_2$, MgO, CaO, $Ga_2O_3$

**Nitrides**

TiN, TaN

**Metals**

Ir, Ru, Co, Cu,others

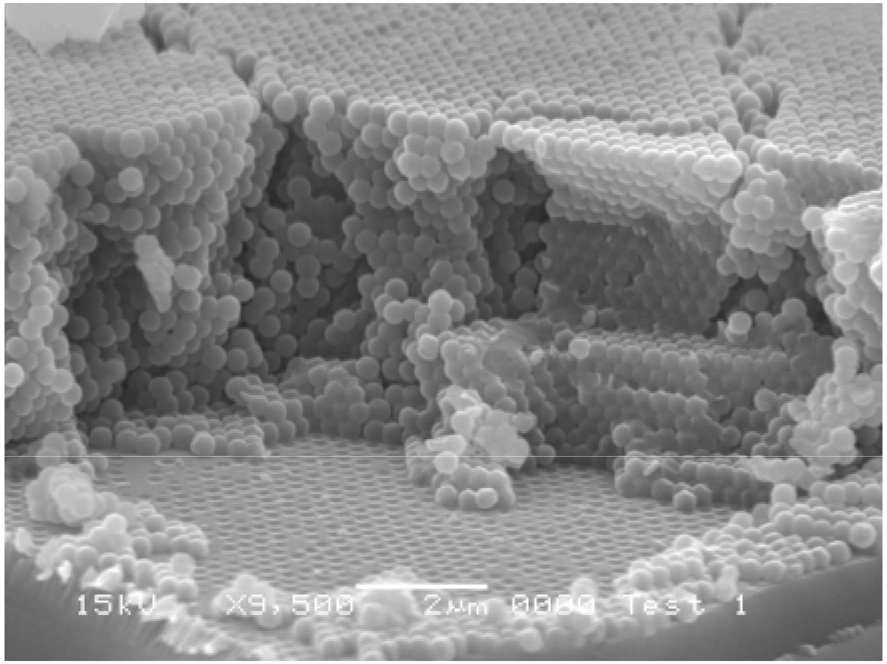
**Current areas of interest**

Interface control and surface modification processes
new chemistries

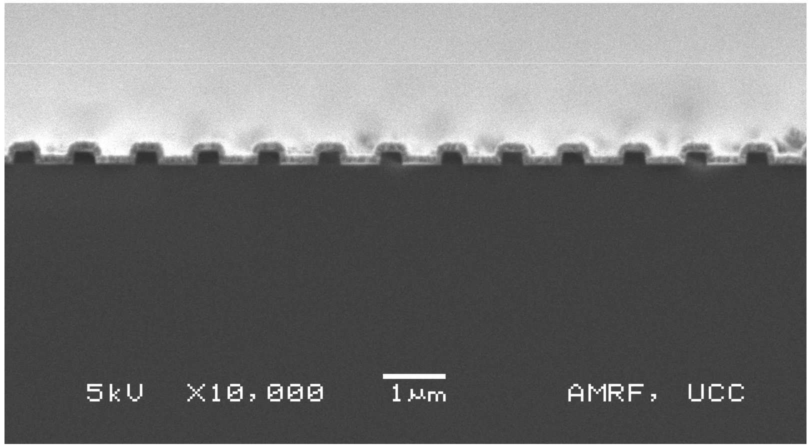
# ALD Capabilities

ALD- highly conformal coating of 2D and 3D objects

Low T (room temp possible)



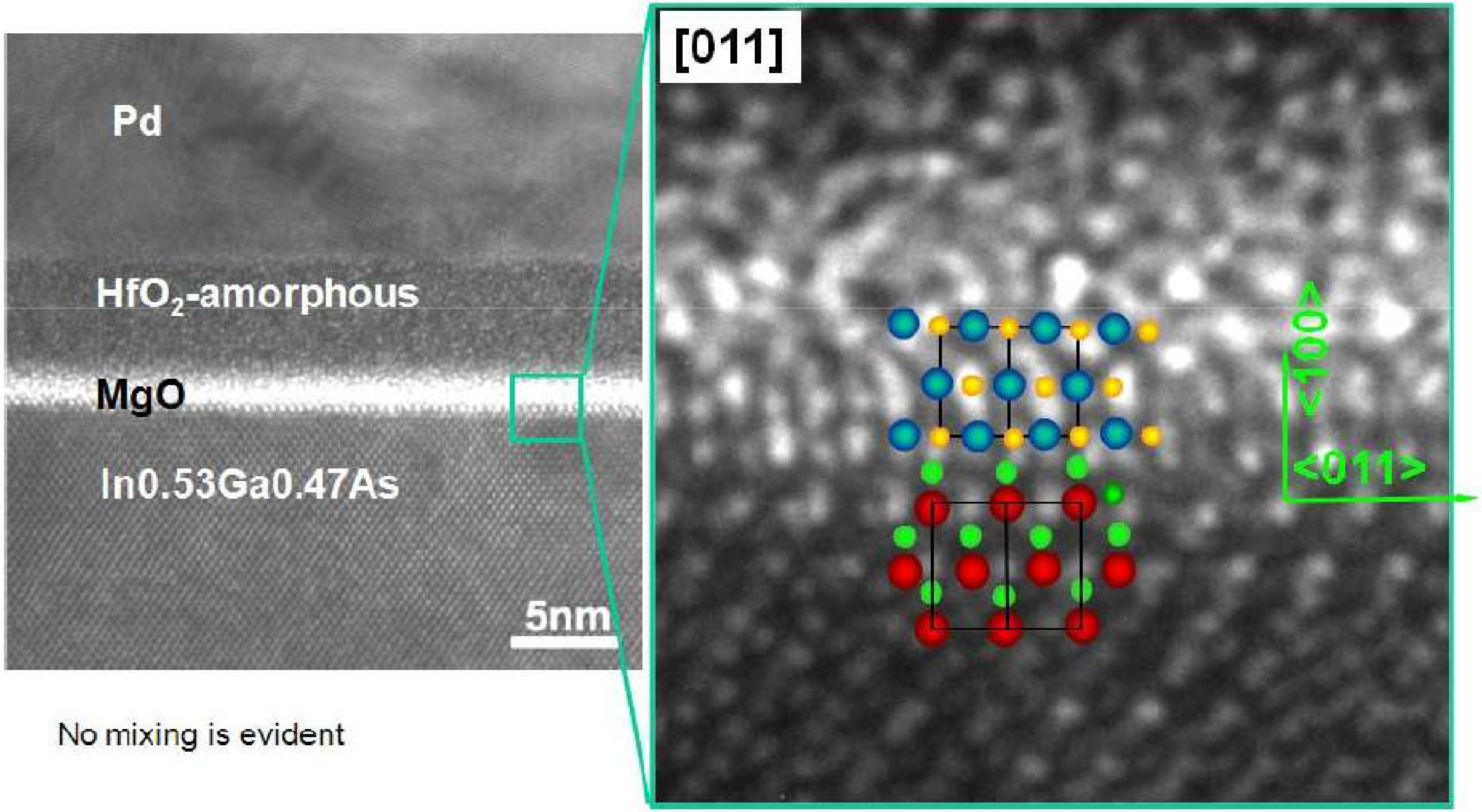
Demonstration of complete, conformal infilling, through a complex 3D structure- $Al_2O_3$ growth by ALD inside an opaline thin film



Demonstration of highly conformal coating of Ru metal over a textured Ta/TaN substrate using ALD

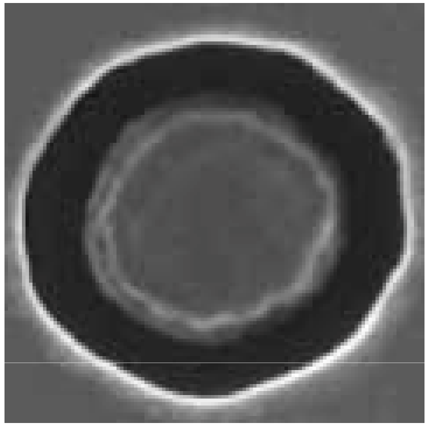
# ALD Capabilities

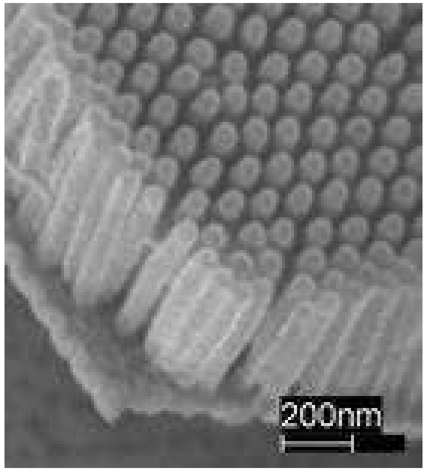
Markus Boese, Yanhui Chen, Colm C. Faulkner,
CRANN, Trinity College Dublin

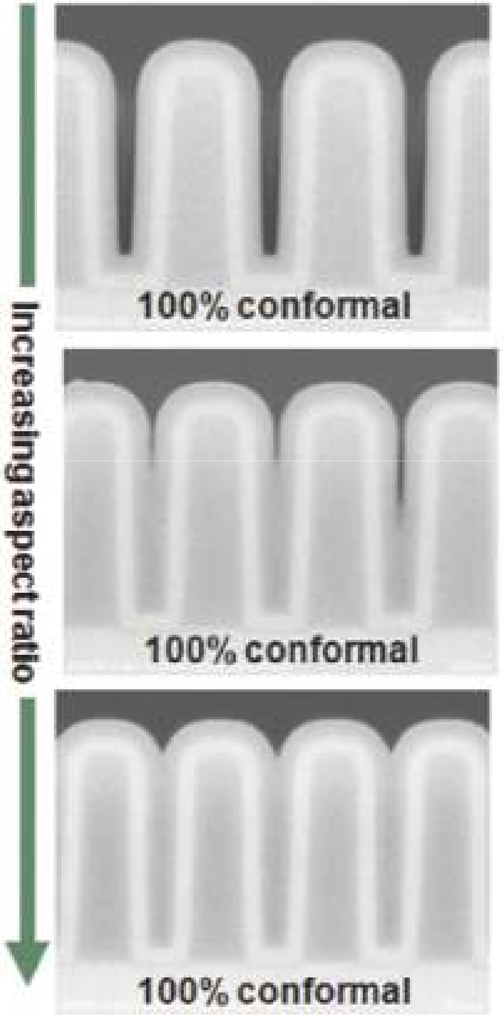


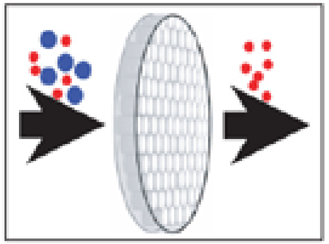
No mixing is evident

# ALD Capabilities



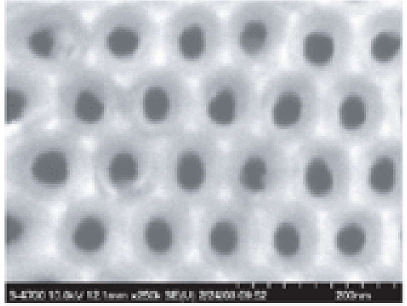






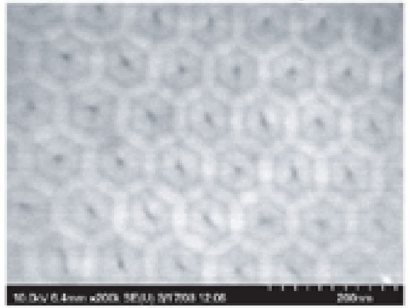
Nanoporous Separation Membrane

Before ALD Coating



40 nm pores

After ALD Coating



10 nm pores

Further examples of structural geometries that can be coated

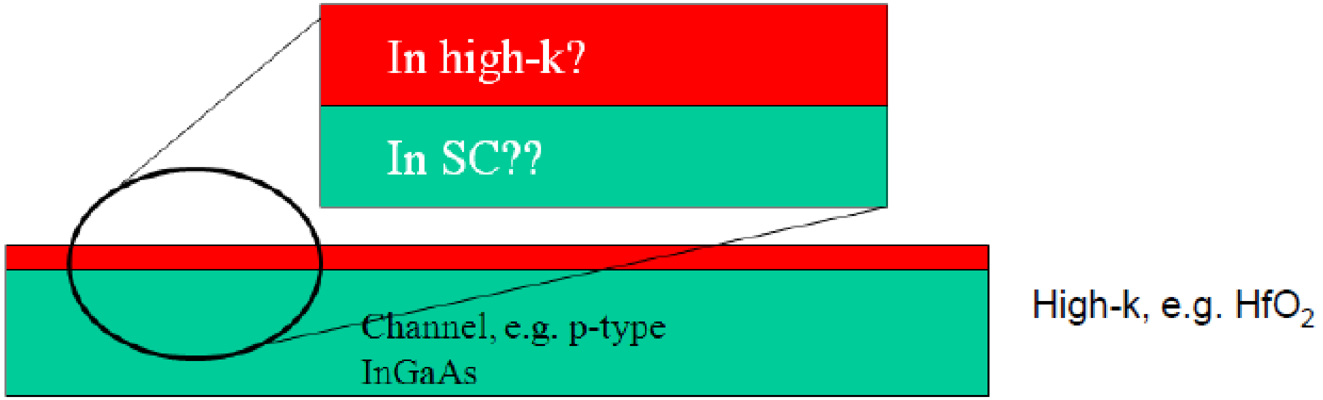
# Target Application

## High-k on III-V MOSFETs

Abrupt 'clean' interfaces- to avoid Fermi level pinning and interface traps

Fermi Level Pinning: imperfections of various nature at semiconductor surfaces may cause pinning of the Fermi energy on the surface preventing changes of the surface potential in response to the changes of the voltage applied to the metal contact of metal-semiconductor and metal-insulator-semiconductor structures

Interface traps: additional capacitance degrading device performance, reduction in mobility- where and what are these?



# Target Application

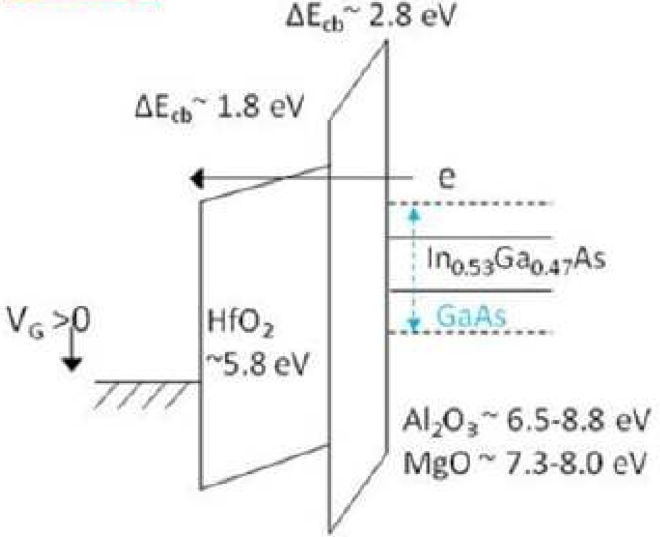
## High-k on III-V MOSFETs

### Interface Control Layers

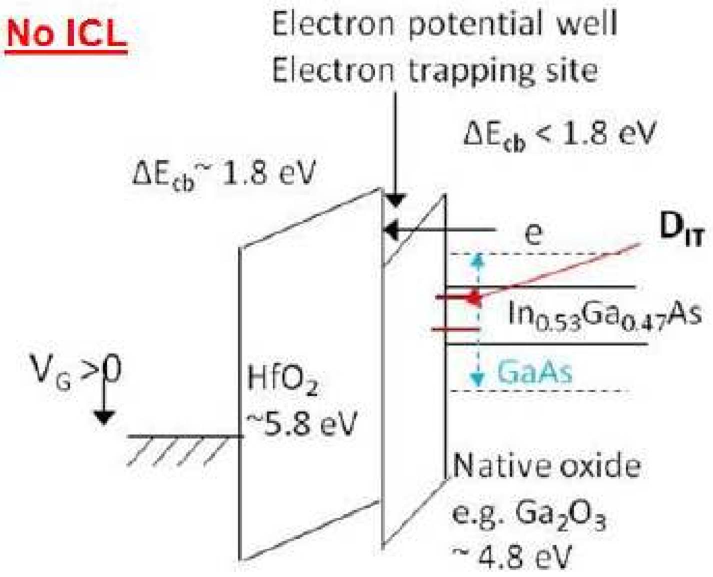
**Use ~1 nm of $Al_2O_3$ or MgO as <u>interface control layers</u> on III-V substrates, to:**

- Minimise leakage current ($E_g$~8 eV)
- Use $HfO_2$ (κ ~20) on ~1 nm $Al_2O_3$/MgO (κ ~8-10) for EOT scaling [1]
- Removal or reduction of native III-V oxides

**With ICL**



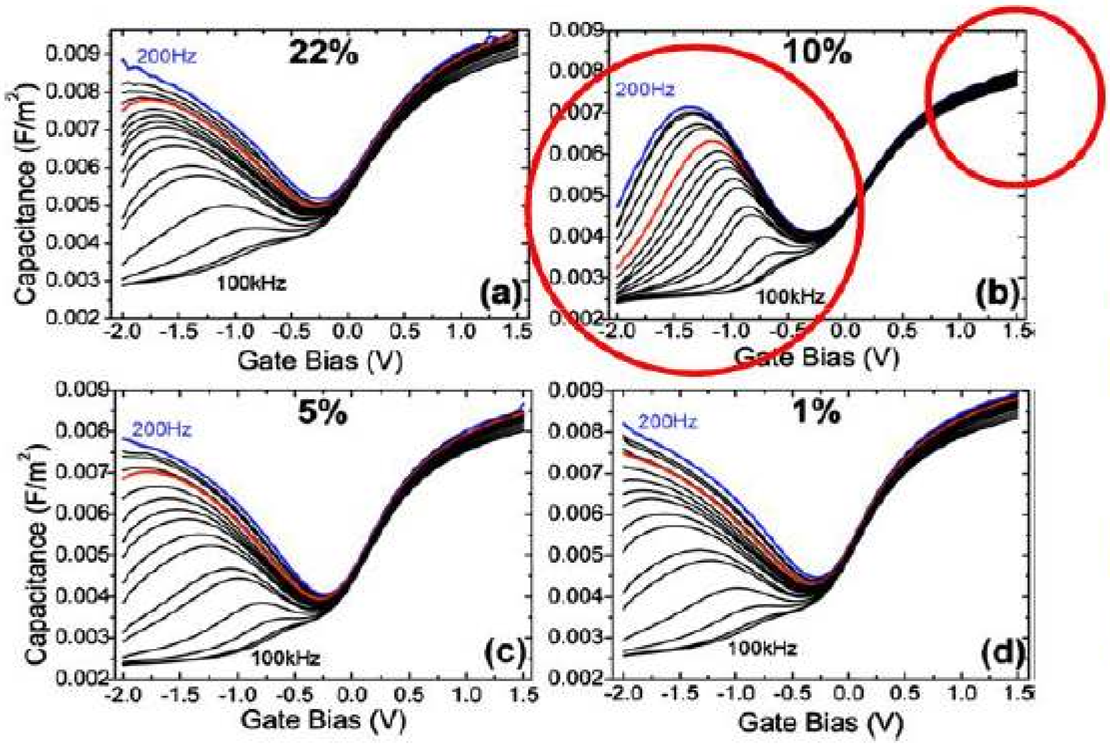
**No ICL**



# Target Application

## High-k on III-V MOSFETs

### Variable Frequency C:V Analysis: n-type



Interface states manifest as additional capacitance on the inversion profile (true inversion is not achieved

(constant capacitance determined by $C_{ox}$ + temp)

For 10% solution, a reduction in peak area and dispersion in accumulation seen

Further improvement? E.g. forming gas anneal

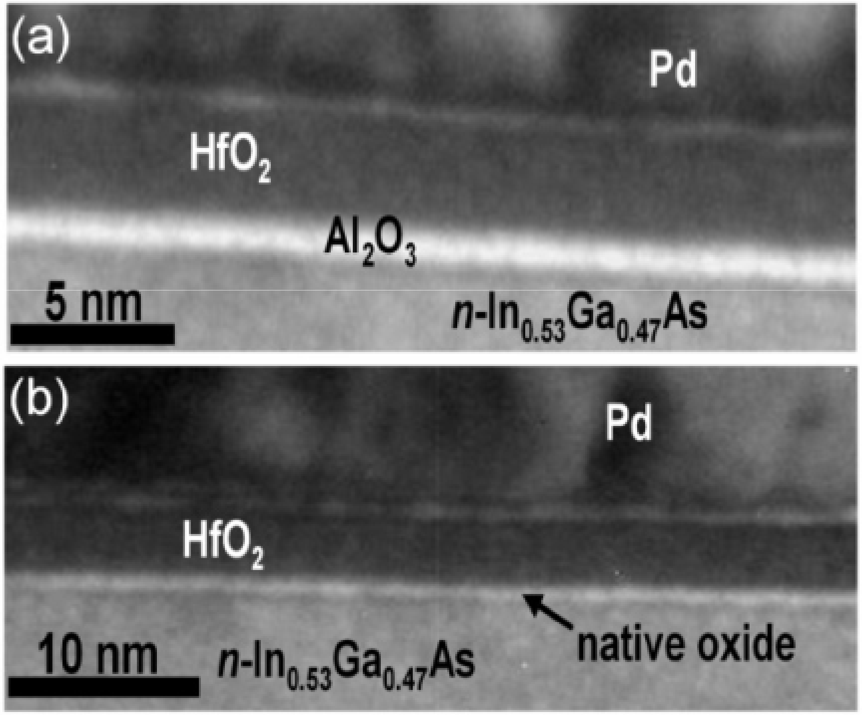
c.f. Kim et al., Appl. Phys. Lett. **96**, 012906 2010.

NH4$_2$S treated, Au/Ni / 8 nm $Al_2O_3$ /*n*-In$_{0.53}$Ga$_{0.47}$As/InP devices. Frequencies: 200 Hz, 400 Hz, 500 Hz, 800 Hz, 1 kHz, 1.5 kHz, 2.0 kHz, 2.5 kHz, 3.0 kHz, 4 kHz, 5 kHz, 8 kHz, 10 kHz, 20 kHz, 40 kHz, 80 kHz, and 100 kHz. The 1 kHz curves have been highlighted in red to illustrate that a more accurate representation of the interface defect response is obtained by measuring down to 200 Hz.

O'Connor *et al.* J. Appl. Phys. **109**, 024101, 2011

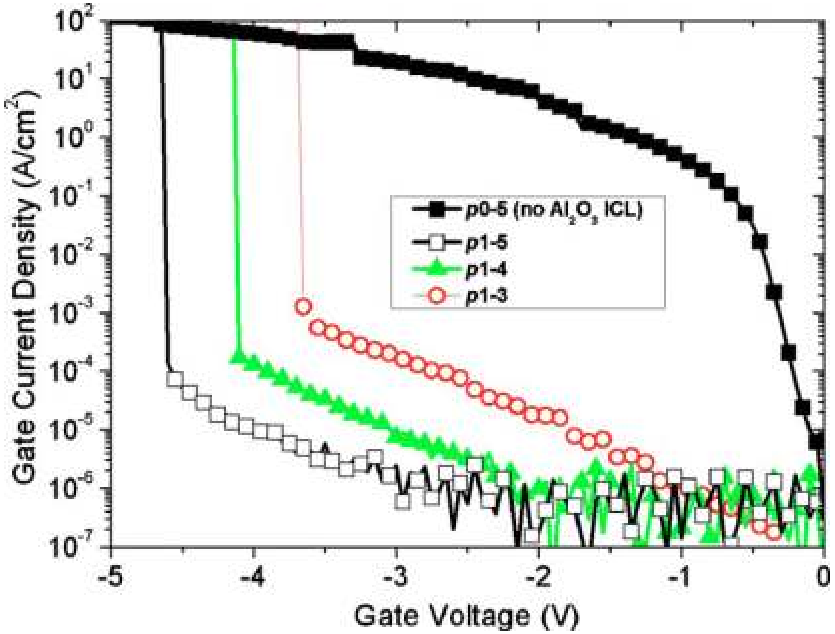
# Target Application

## High-k on III-V MOSFETs



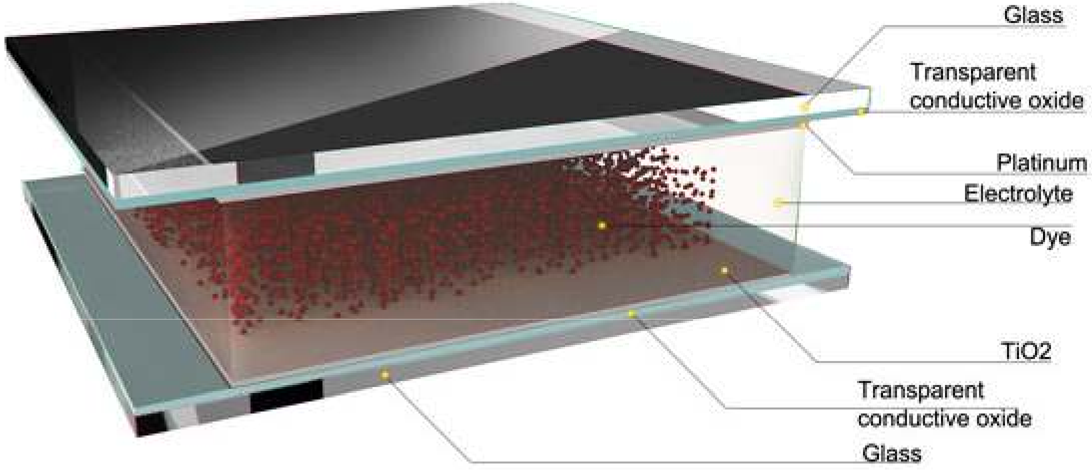
Reduce $D_{it}$ achieved
Low leakage

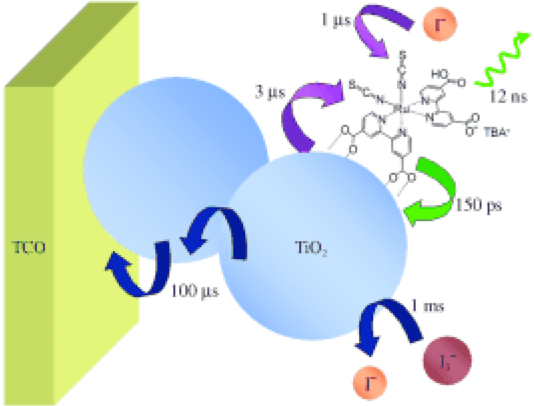
ALD used to apply interface control layer and subsequent High-k layer to improve performance



# Alternative Applications

## Dye sensitised solar cells





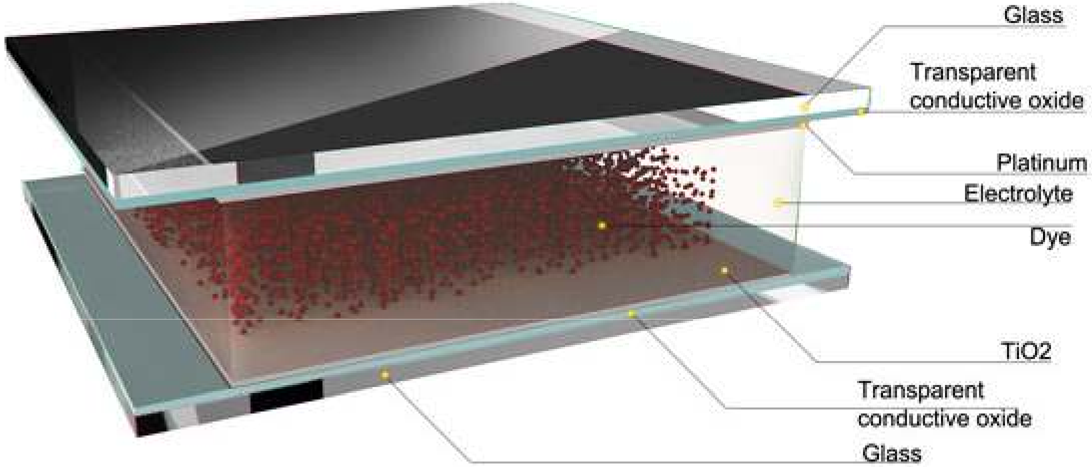
ALD on surfaces/interfaces to enhance properties and improve efficiency of final module

ZnO nanorod arrays increase surface area => better charge transfer

SOLARPRINT

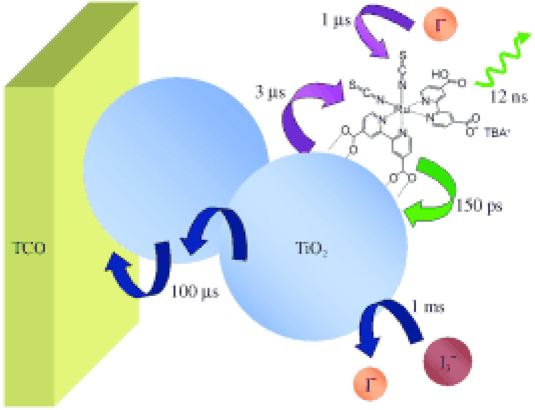
# Alternative Applications

## Dye sensitised solar cells



ALD on surfaces/interfaces to enhance properties and improve efficiency of final module

$TiO_2$ blocking layer improves photocurrent



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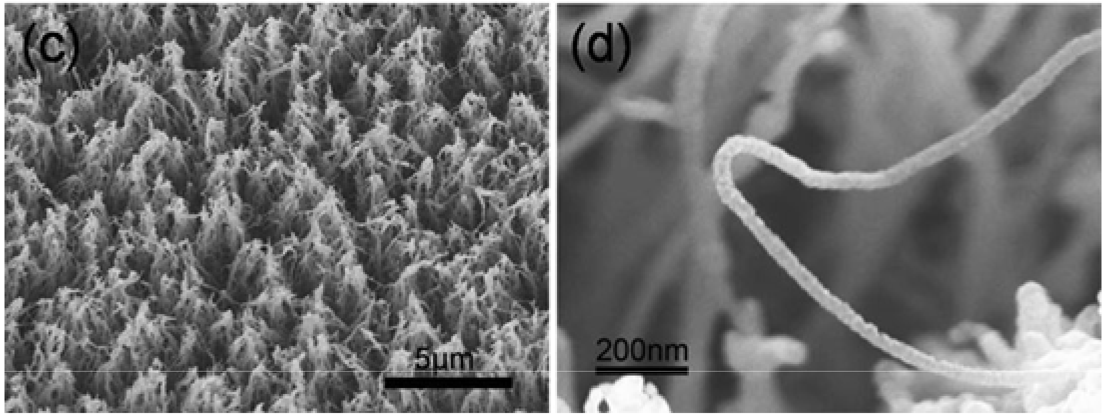
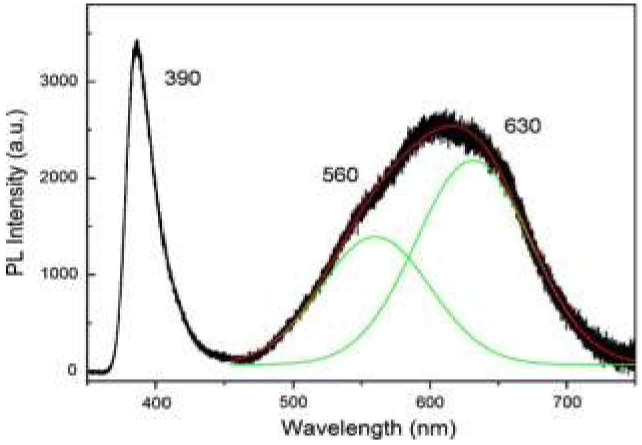
New industry engagement

# Alternative Applications

## UV Photodetectors



SEM of ALD ZnO-coated CNTs

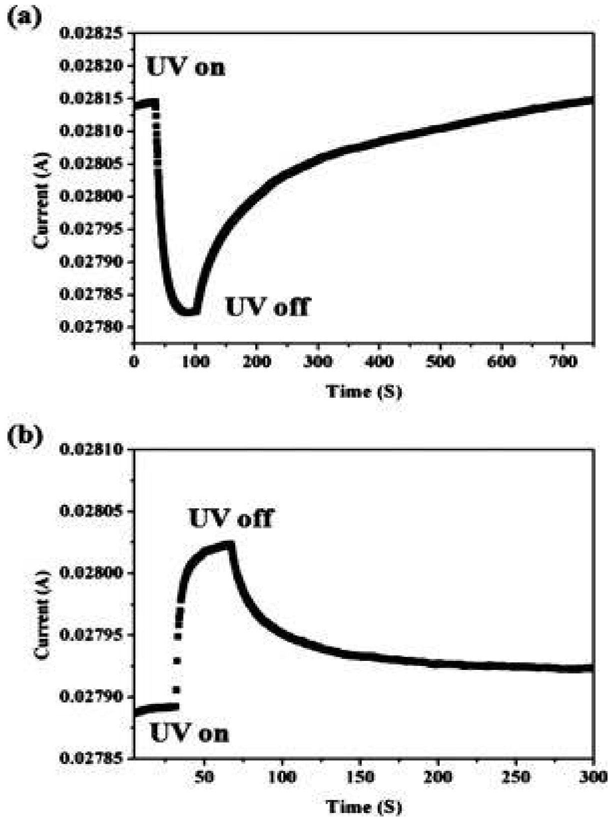


RT PL spectra of ALD ZnO-coated CNTs

XL Li et al, *Nanoscale Res Lett* (2010) 5:1836–1840

Significantly higher response due to improved crystal quality of ALD ZnO

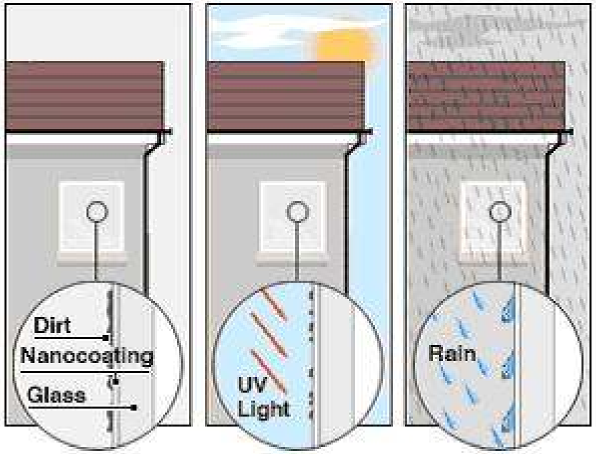
Photoresponse curves for ZnO-CNT-based photodetectors. Wavelength of UV light = 365nm.

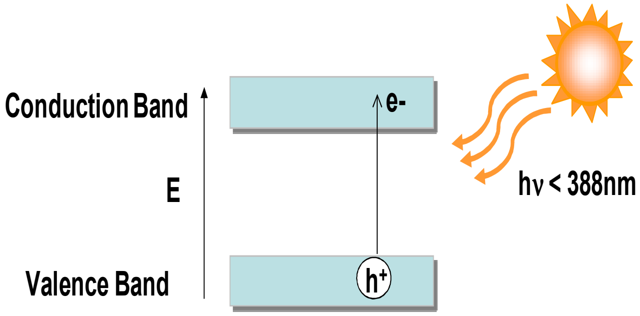


JH Lin et al, *J. Electrochem. Soc.*, 2011, Vol. 158, No. 2, pp. K24–K27

# Alternative Applications

## Photocatalytic, self-cleaning materials*



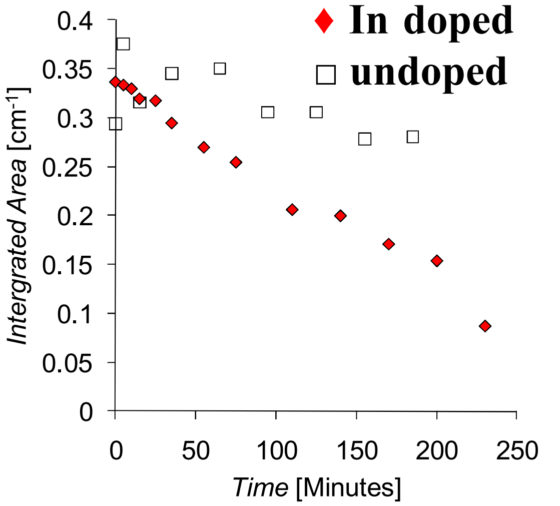


* e.g. Pilkington Activ™ glass, St Gobain Bioclean®

### Alternative coatings investigated/assessed by AMSG

**Stearic Acid Test used to compare performance**

- A thin layer of stearic acid, a long chain organic molecule simulating dirt, is applied to the samples.
- The samples are exposed to UV light.
- The rate of destruction of the stearic acid is monitored using FT-IR spectroscopy.



## Indium doping found to increase destruction rate

M.G. Nolan et al, *Journal of Photochemistry and Photobiology A:* Vol219 (1), 2011, p10-15

# Alternative Applications

## Medical application areas

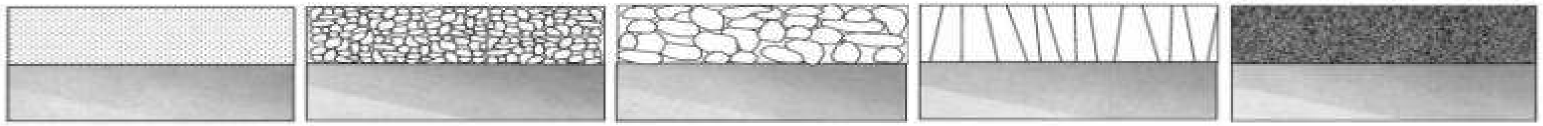
**Anti-bacterial/self-cleaning coatings**

**Protection coatings**

**Growth templates – pore size control**

**Functionalised surfaces**

Crystallinity range – single crystal through polycrystalline to amorphous
– ultra smooth surface to highly textured



# Conclusions

Technically advanced Atomic Layer Deposition processes have been developed to allow the controlled uniform deposition of nm thick metal oxide films capable of enhancing surface functionality

Technology development is a partnership
- effective Knowledge Exchange is critical

Commercialisation is a partnership
- effective Knowledge Exchange and Transfer is critical

Academic and Industry engagement is good for all

# Thank you for your attention

PS. Any parties interested in collaboration please contact me

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