Results from the NA62 Gigatracker prototype: a low mass and sub-ns time resolution silicon pixel detector

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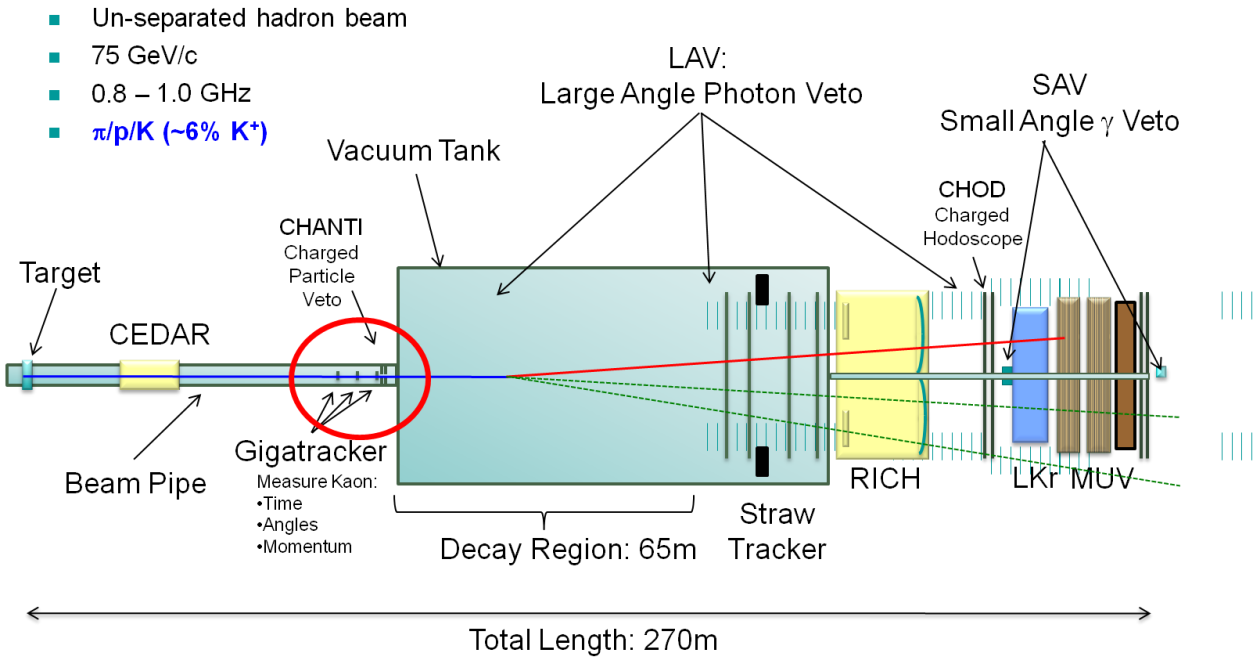
PSD9: 9th International Conference on Position Sensitive Detectors
Wednesday 14 September 2011, Aberystwyth University

Outline

1. Introduction to NA62 and GigaTracker
2. ASIC Demonstator description
    1. Requirements
    2. Architecture: sensor assembly, cooling, electronics
    3. Pixel electronics: On-pixel TDC vs End-of-Column TDC

Conclusions

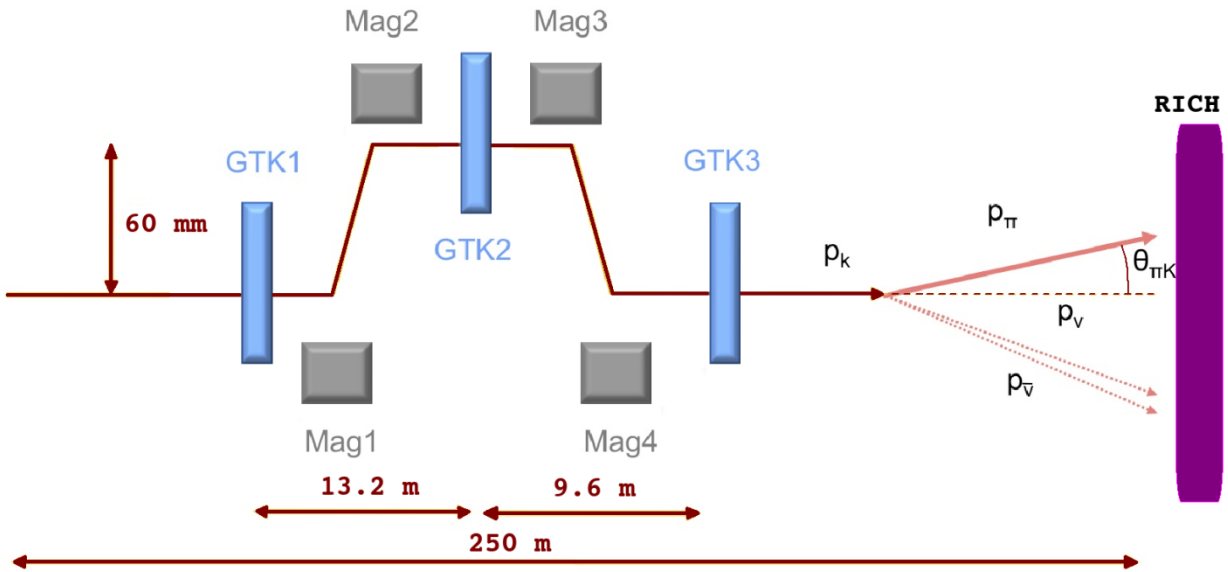
Introduction to NA62 and GigaTracker



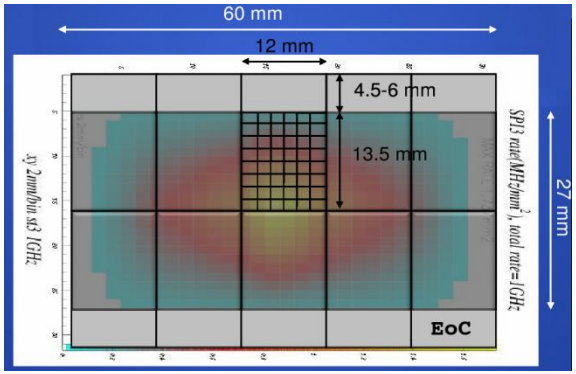
- Fixed target experiment CERN SPS
  - 400 GeV/c p^+ incident on target
  - 75 ±0.8 GeV/c particles selected at entrance to decay line
  - Decay in vacuum tube instrumented with various detectors
- Aims to measure ~80 -100 events over 2 years of run time
- Very rare decay: Branching fraction very small,Massive background rejection required

$$K^+ \rightarrow \pi^+ \nu\bar{\nu}$$

Introduction to NA62 and GigaTracker



- Trajectory
  - Momentum
  - Angle
- Time
  - correlate hits with RICH
  - reduce combinatorics
  - 200 ps per station

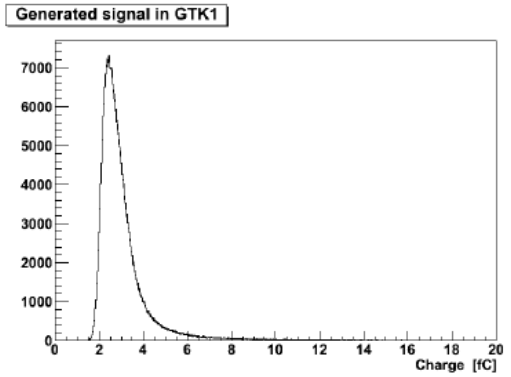


800MHz ≤ Total Rate Seen by GTK ≤ 1GHz

Detector area beam profile
- highly non-uniform intensity distribution
- 2 rows of 5 readout chips

ASIC Demonstator description

Beam Rate	800MHz →1GHz
Mean Hit Rate/Pixel	140kHz (center)
Radiation environment	10^{14}n cm^2 yr^{-1}
Lifetime	~1yr
# stations	3
Detector area	60mm x 27mm
Pixel size	300 μm x 300 μm
Pixels/station	18000
Readout chip/station	10
Sensor technology	p-in-n
Readout	Untriggered
Efficiency	≥99%
Material Budget	≤0.5% Xo (≤500μm Si)
ROC Characteristics	130nm CMOS, Thickness ~100μm
Sensor Characteristics	Thickness ~200μm
Dynamic range	~(6ke$^-$ → 60ke$^-$), ~(1fC → 10fC)
Q_{MP}	2.4fC
Time resolution/station	≤200ps(RMS)



Géant4 Simulation

- charge release mechanism is stochastic
- Landau distr. $Q_{most\ probable}$=2.4 fC

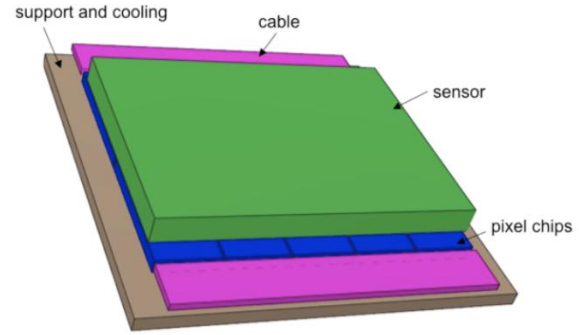
Dissipated power perchip ~2 W/cm²

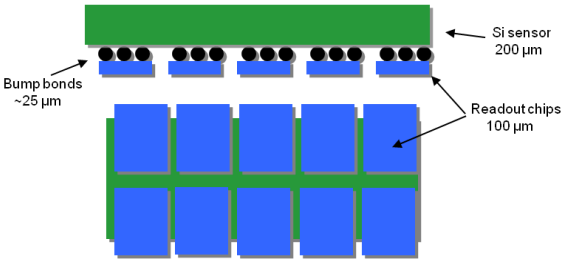
Main challenges:

- Time resolution: 200 ps (rms)/station
- On-pixel fast analog pulse shaping (~4 ns peaking time)
- Max data rate per chip: up to 6 Gbit/s

ASIC Demonstrator description
Architecture: assembly, cooling, electronics

ASSEMBLY	COOLING	ELECTRONICS





standard p-in-n sensors
200 µm sensor wafers thick

ASIC Demonstator description
Architecture: assembly, cooling, electronics

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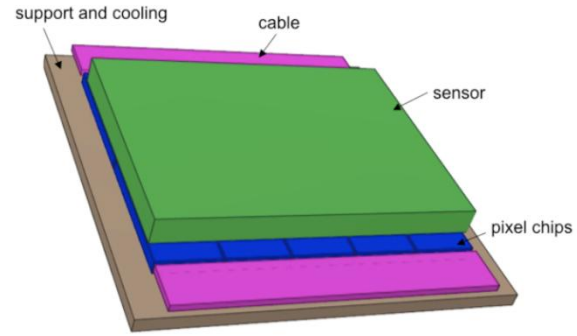
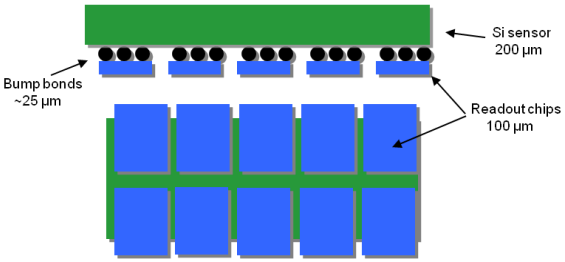




standard p-in-n sensors
200 µm sensor wafers thick

100 running days per year(~2 × 10^{14} (1 MeV n_{eq}/cm^2) ~ expected in inner layers of the LHC trackers during 10 years of operation

Efficient cooling to keep radiation induced leakage current at acceptable value → $T_{operating\ sensor} < 5$ °C

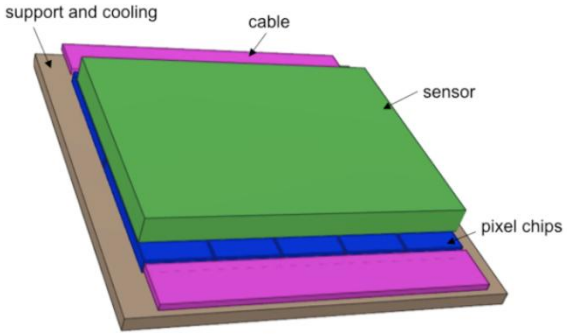
Dissipated power by read-out chips is ~2 W/cm2 (~32 W per station)

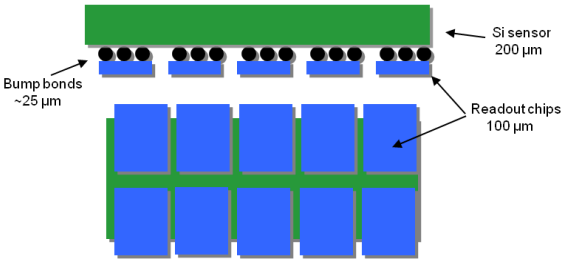
Low material budget (~0.15% X_0) in the beam region

Cooling options under study:
•convective cooling in a vessel
•micro-channel cooling

ASIC Demonstator description
Architecture: assembly, cooling, electronics

ASSEMBLY





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COOLING

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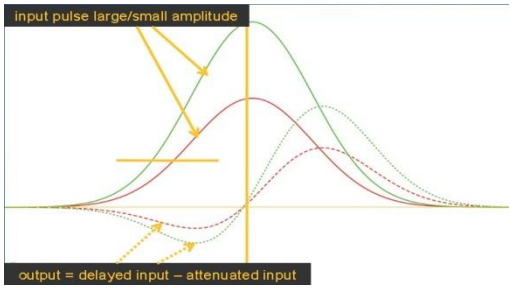
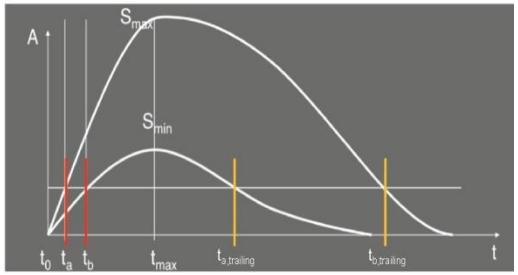
ELECTRONICS

Very high time accuracy, two approaches evaluated



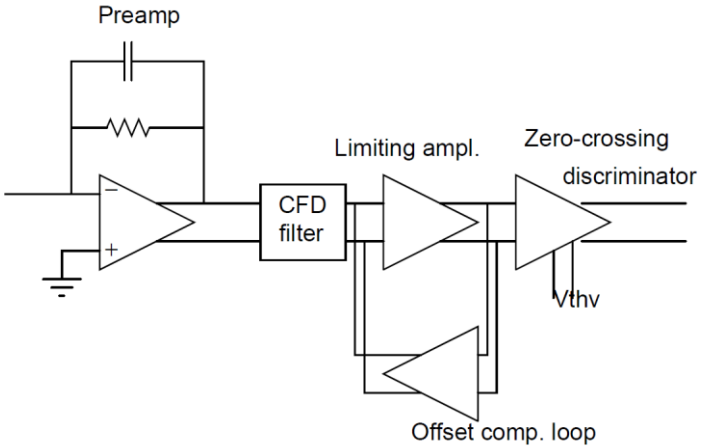
CONSTANT FRACTION DISCRIMINATOR
Single time measurement without time-walk

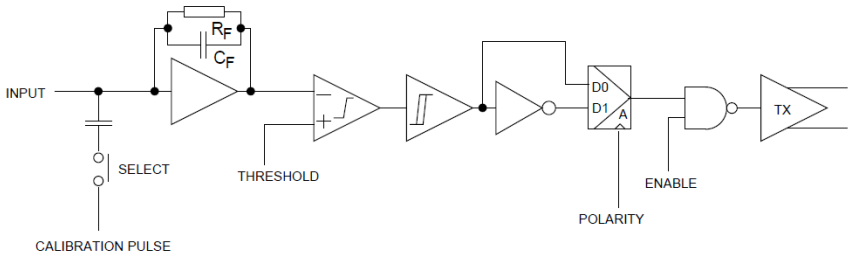


TIME OVER THRESHOLD
time-walk correction algorithm based on the signal time over threshold (pulse width)

ASIC Demonstator description
Pixel electronics

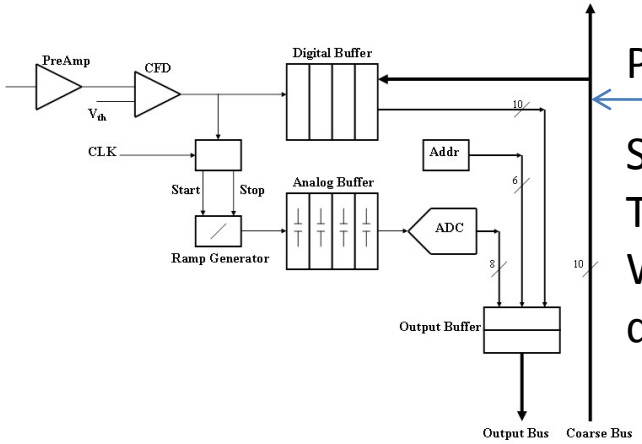
On-pixel TDC	**End-of-Column TDC**
CFD filter + on-pixel TDC based on TAC •maximize signal processing on the pixel cell (including TDC) and distribute clock to the pixel matrix (digital noise) •minimize complexity of end of column logic (no need to propagate the comparator signal outside the pixel) •must be designed to be radiation-tolerant (total dose and SEU aspects), due to the high radiation dose received in the pixel area	ToT + DLL TDC shared among group of pixels •use high precision digital TDC in the end of column, shared by a group of pixels •minimize on-pixel processing for minimum noise •pixel comparator signals should be propagated to the chip periphery (communication of ultra-fast signal in column transmission lines)





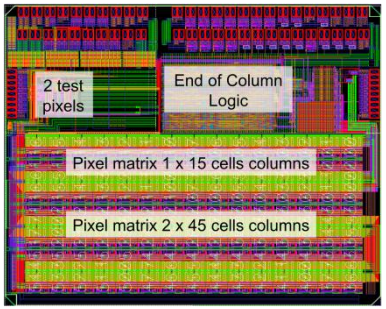
ASIC Demonstator description
Pixel electronics

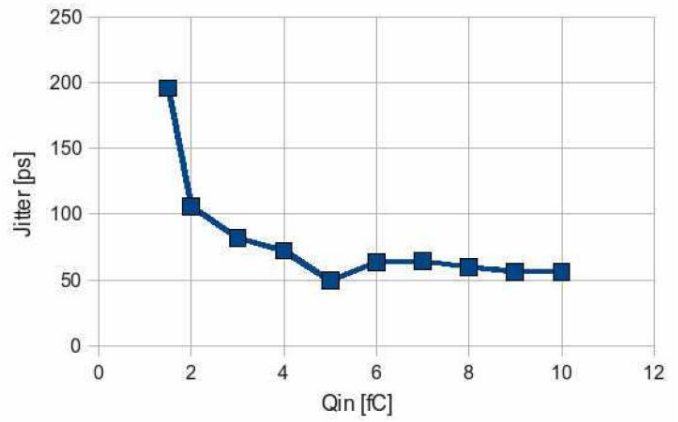
On-pixel TDC: prototype measured with the proposed architecture



Pixel Cell Schematic

Schematic of the pixel TDC based on a Wilkinson time-to-digital-converter





Constant Fraction Discriminator measurements

Dinamic Range	1-10fC
Area	154 um x 74 um
Jitter at 1MIP	90ps rms
Time-Walk resolution	75ps rms
Power consumption	900 uW

ASIC Demonstator description
Pixel electronics

On-pixel TDC: prototype has been re-designed and the CFD improved

On the base of the experience acquired from the CFD on silicon, a second CFD was studied.
Improve the time precision by making the CFD more robust to shape variations.

Smaller area by the delay line of the filter (140*µmx69µm)*

Trigger discriminator to enable the zero-crossing one (Increases the $P_{consumption}$=1.*3mW.*

While this architecture is not yet fabricated, simulations show good performances in correcting both time-walk and fluctuations induced by shape variations.

The simulations were performed using 200 input signals generated with Montecarlo for amplitude variations and shape variations coming from statistical fluctuations in the charge released along the sensor and to non-uniformity in the electrical field at the borders of it.

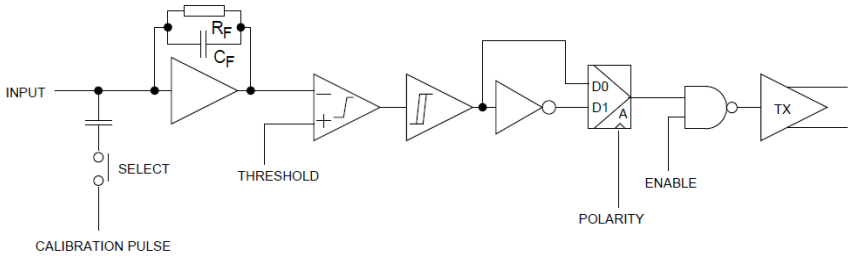
Process corner	RMS jitter @ 1MIP (ps)	Time resolution (ps rms)
Typical mean	65	29
+ 3σ	79	25
- 3σ	68	26

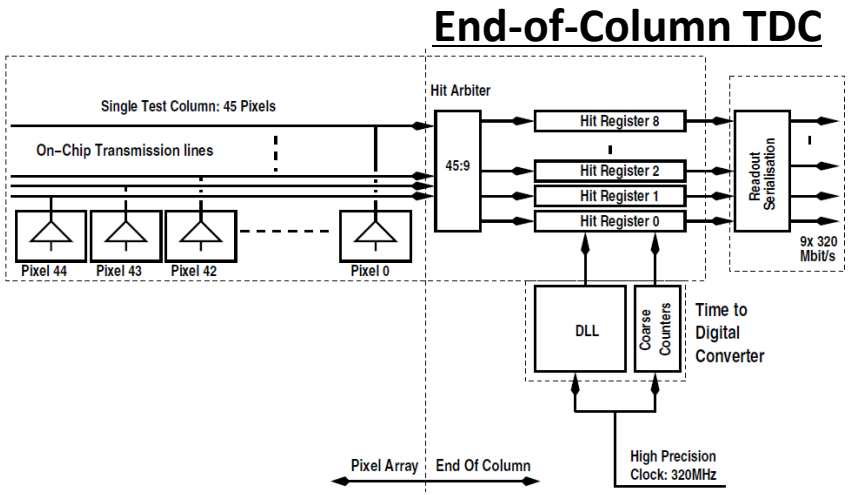
"Implementation of Constant-Fraction-Discriminators (CFD) in Sub-micron CMOS Technology" S. Garbolino et al.

To be presented at IEEE-NSS 2011, Valencia

Jitter is due to parasitc capacitors, reducing slope of the signal

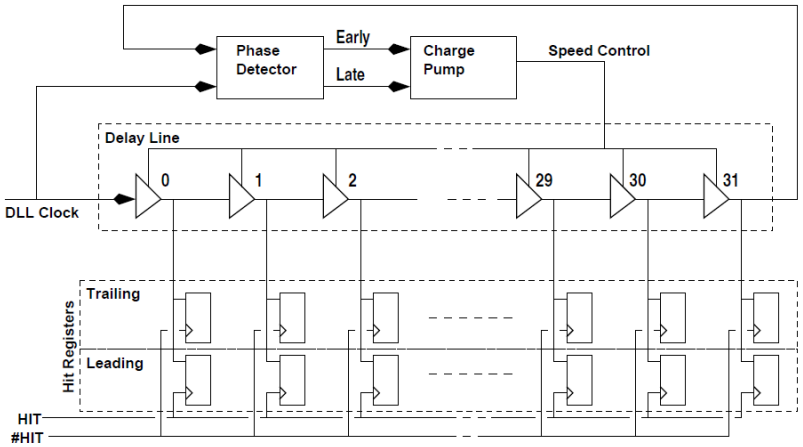
ASIC Demonstator description
Pixel electronics



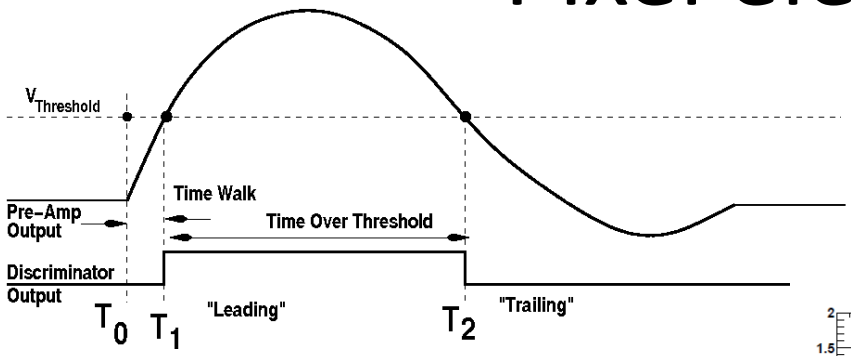


- Power = 120uA/pixel
  - Gain = 70mV/fC
  - 20 fF test charge injection
- Preamp: C_F=14fF and R_F=200kΩ
- TXpre-emphasis, P=100uA

320MHz clock, 32 starved delay cells
→97 ps time bin.

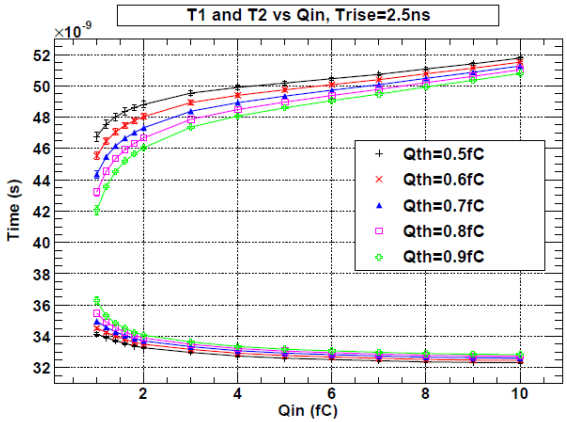


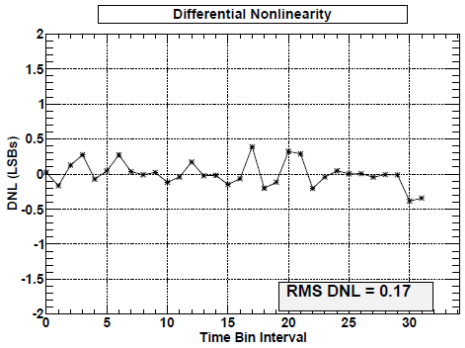
ASIC Demonstator description
Pixel electronics

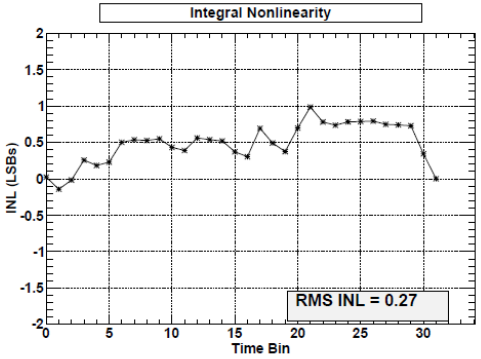


End-of-Column TDC

- TDC





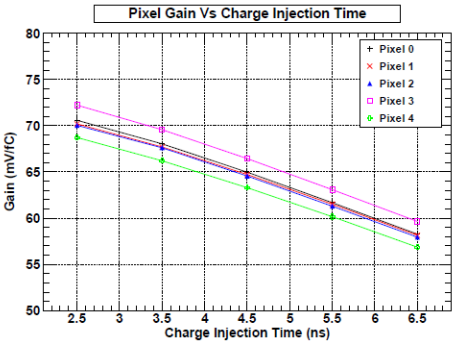


TDC jitter estimated to be better than 10 ps (RMS)

Electrical charge injection. No detector T1=40 ps RMS at 2.4 fC

Laser Charge Injection. Detector biased at 300V. T1=70 ps RMS at 2.4 fC

Good jitter performance over full range of interes

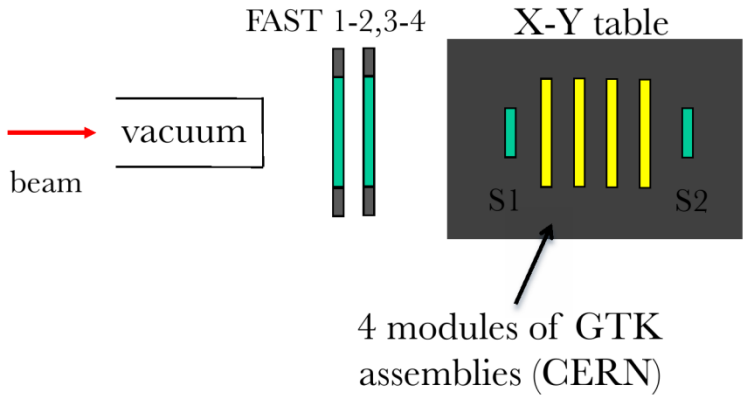


μ_{Gain}=72mV/fC, σ_{Gain}=1.5mv/fC

$noise_{NoSensor}$=130 e

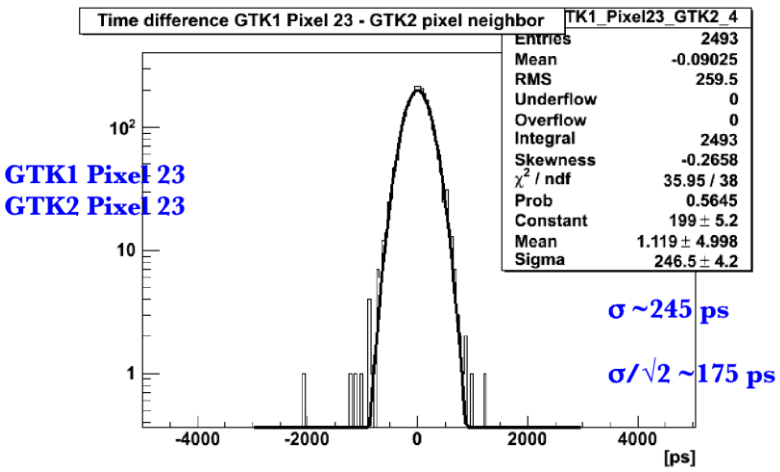
$noise_{Sensor}$=180 e (Consistent with Cdet 250 fF)

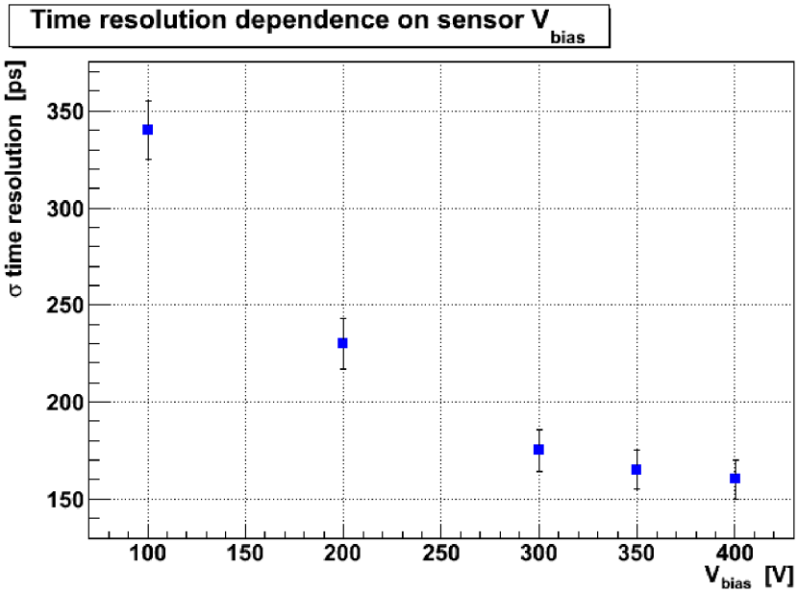
ASIC Demonstator description
Pixel electronics



End-of-Column TDC

- HPTDC used for all external measurements (25 ps time binning)
- Consistently better than 200 ps





Conclusions

- 2 options have been evaluated with 2 different prototypes:
  - CFD simulation shows the possibility of time resolution below 50ps
  - ToT time resolution measured in beam test consistently lower than 200ps
- Another **CFD** prototype is being fabricated to study **lower time resolution architecture**
- ToT architecture has shown a more robust behavour and has been choosen to be included in the GTK system, and a full circuit is being developed