



Recent CMS HGCal activities within CLICdp

Andreas Maier, **Florian Pitters**¹⁾, Eva Sicking

1) florian.pitters@cern.ch

CERN

August 30th, 2016
CLICdp Collaboration Meeting @ CERN

OUTLINE



- The CMS HGCal Upgrade
 - ➔ Overview
 - ➔ Sensors
 - ➔ Modules and Cassettes
- Sensor Testing
 - ➔ Sensor Types
 - ➔ Sensor Probing
 - ➔ Example Results
- Testbeam Plans
 - ➔ Plans
 - ➔ Some first results



Motivation for our participation:

CMS is building a calorimeter based on similar technologies as the CLIC design right now. This is an excellent opportunity to participate and learn!

The purpose of this talk:

Give an overview of recent and planned activities within the LCD group with respect to the CMS high granularity calorimeter upgrade.

The CMS HGCal Upgrade

Summary of the CMS upgrades for Phase-II

Trigger/HLT/DAQ

- Track information at L1-Trigger
- L1-Trigger: 12.5 μ s latency - output 750 kHz
- HLT output \approx 7.5 kHz

Barrel EM calorimeter

- Replace FE/BE electronics
- Lower operating temperature (8 $^{\circ}$)

Muon systems

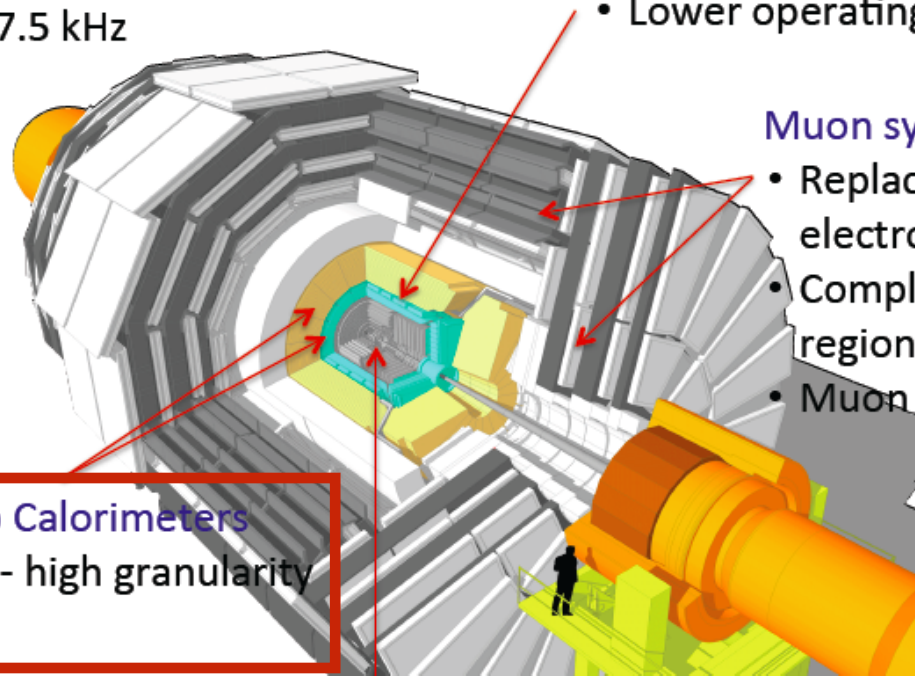
- Replace DT & CSC FE/BE electronics
- Complete RPC coverage in region $1.5 < \eta < 2.4$
- Muon tagging $2.4 < \eta < 3$

Replace Endcap Calorimeters

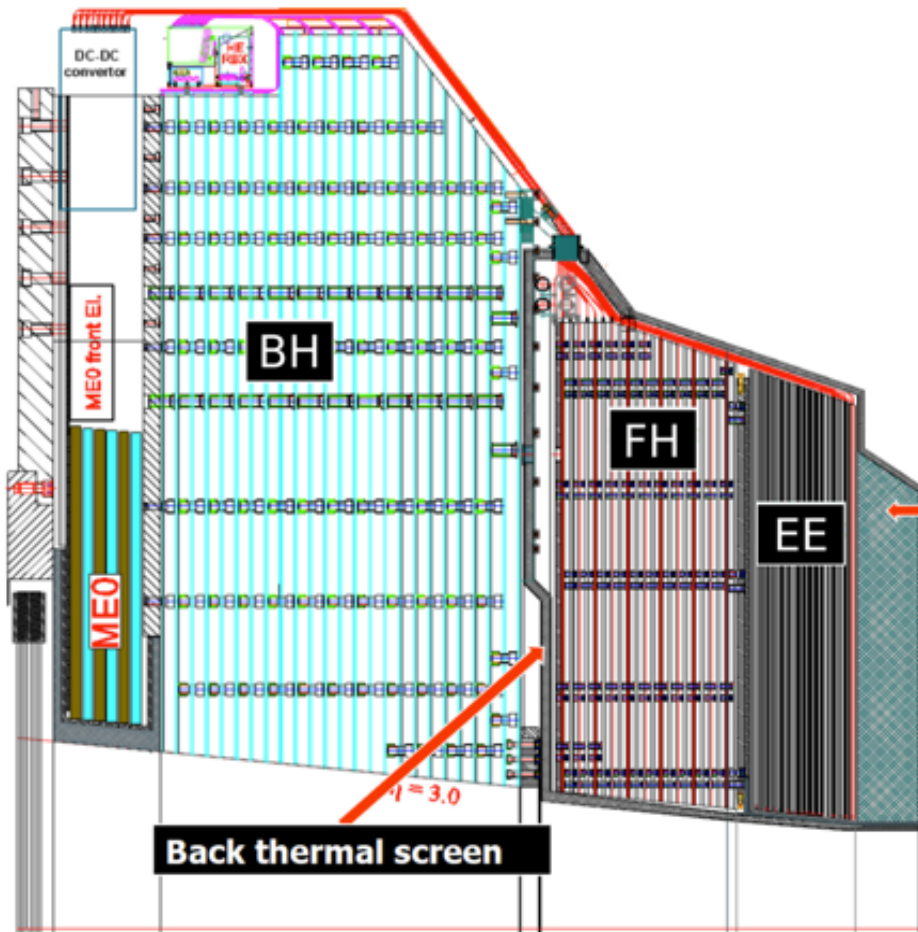
- Rad. tolerant - high granularity
- 3D capability

Replace Tracker

- Rad. tolerant - high granularity - significantly less material
- 40 MHz selective readout ($P_t \geq 2$ GeV) in Outer Tracker for L1-Trigger
- Extend coverage to $\eta = 3.8$



CMS HGCal UPGRADE



- Key facts:
 - ➔ Hexagonal Si sensors with W/Cu backing plate and readout PCB built into modules.
 - ➔ Modules will be mounted on Cu cooling plates to make up cassettes.
 - ➔ Cassettes will be wedge-shaped and inserted into absorber structures.
 - ➔ Goal is ~50 ps timing on cell level for vertex reconstruction/pile-up rejection.
- Key parameters:
 - ➔ 593 m² of silicon
 - ➔ 6M ch, ~0.5 or ~1 cm² cell-size
 - ➔ 21,660 modules (8" or 2x6" sensors)
 - ➔ 92,000 front-end ASICS
 - ➔ Power at end of life 120 kW

System Divided into three separate parts:

EE – Silicon with tungsten absorber – 28 sampling layers – $25 X_0 + \sim 1.3 \lambda$

FH – Silicon with brass absorber – 12 sampling layers – 3.5λ

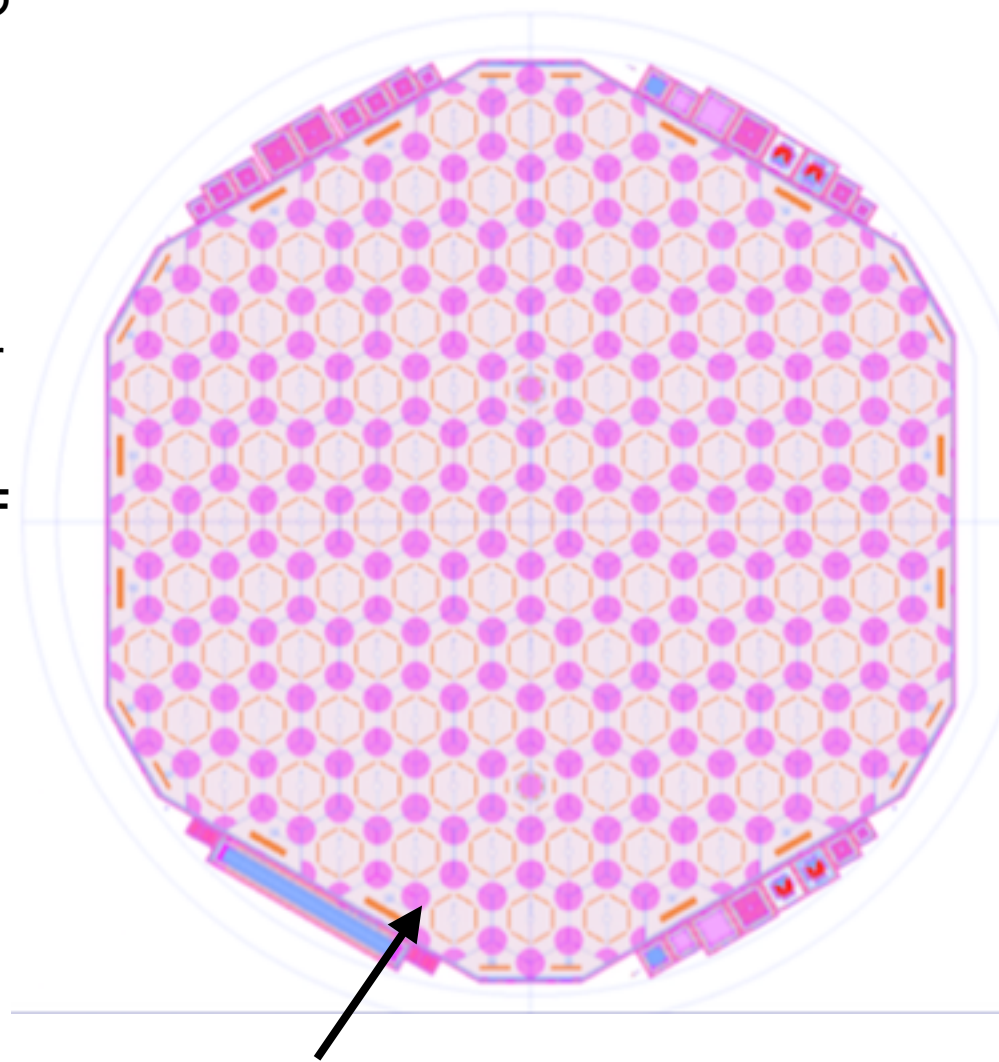
BH – Scintillator with brass absorber – 11 layers – 5.5λ

EE and FH will be operated at -30°C to keep leakage currents at acceptable levels.

SENSOR DESIGN



- **Hexagonal sensor geometry** based on SiD design largest tile-able polygon.
 - ➔ Maximise use of circular wafer.
 - ➔ Minimise ratio of periphery to surface area.
- Truncated tips, so called '**mouse bites**', for module mounting.
- Goal is to have **cell capacitances of $\sim 50\text{pF}$** for all thicknesses.
 - ➔ Smaller cell sizes for thinner sensors.
- A few more details:
 - ➔ Inner **guard ring is grounded**, outer guard ring is floating.
 - ➔ **Calibration cells** of smaller size for single MIP sensitivity at end of life.
 - ➔ Four different **inter-pad gap regions**.

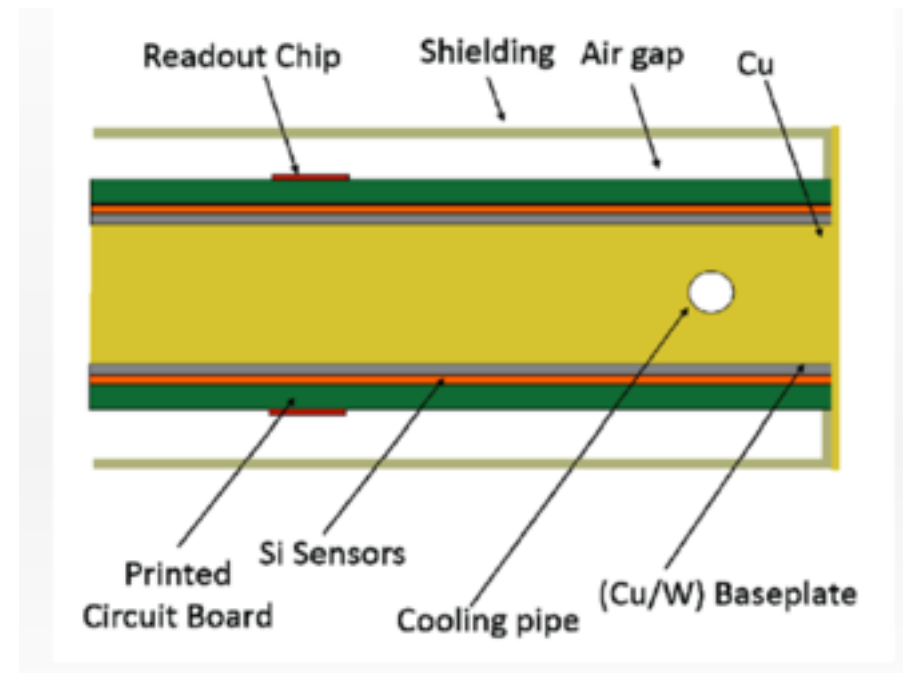
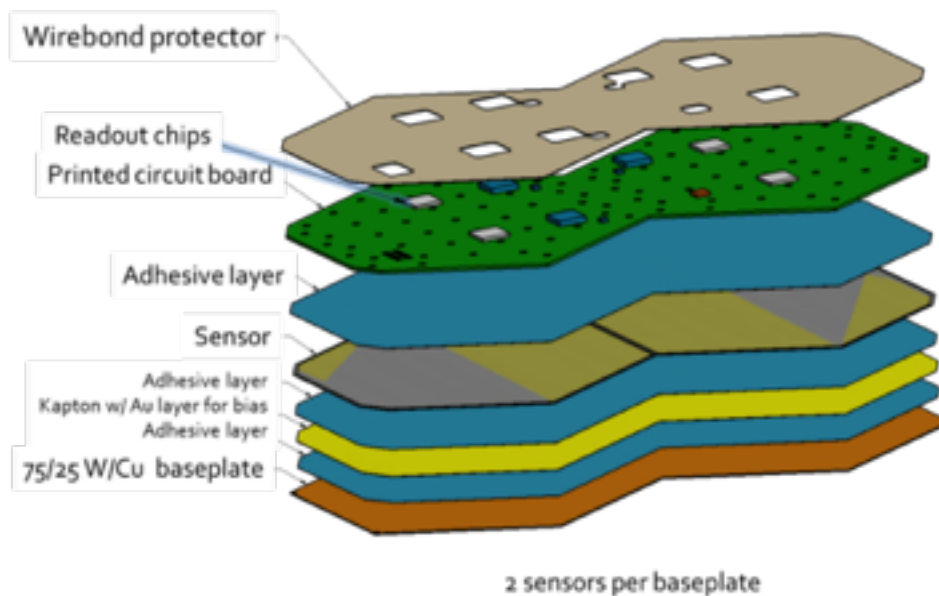


HPK 128ch 6" layout

MODULES & CASSETTES



- Module design is as following:
 - ➔ First, the sensor is glued unto **baseplate covered with Au/Kapton foil**.
 - ➔ Then, the **readout PCB** is glued unto the sensor.
 - ➔ **Deep wire bonds** connect the readout board to sensor cells.
- Cassettes are populated with **modules from both sides**.

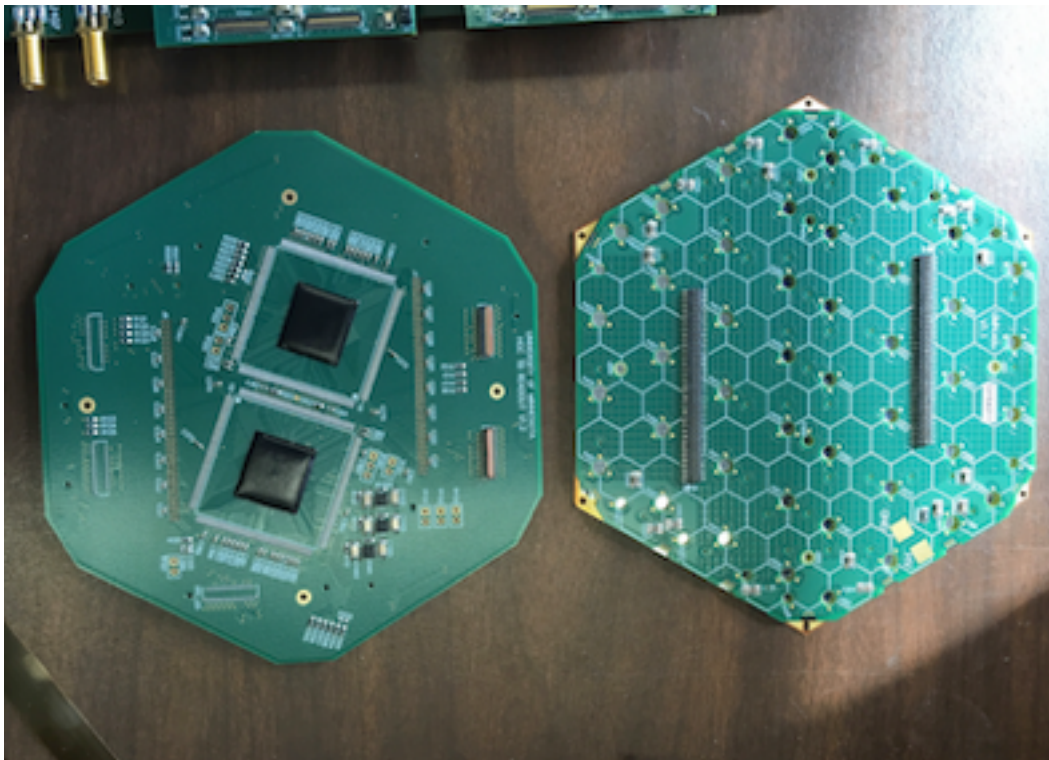


CALICE design adapted to CMS requirements of CO₂ cooling

MODULES & CASSETTES



- For the prototyping phase, a **double layer PCB design** was used for quick exchange of readout board/testing board.
 - ➔ Only sensor PCB with routings to an on-board connector is glued unto the sensor.
 - ➔ Any readout PCB or other testing board plugs in via that connector.



Double layer PCB design and prototype cassette at FNAL

Sensor Testing Activities



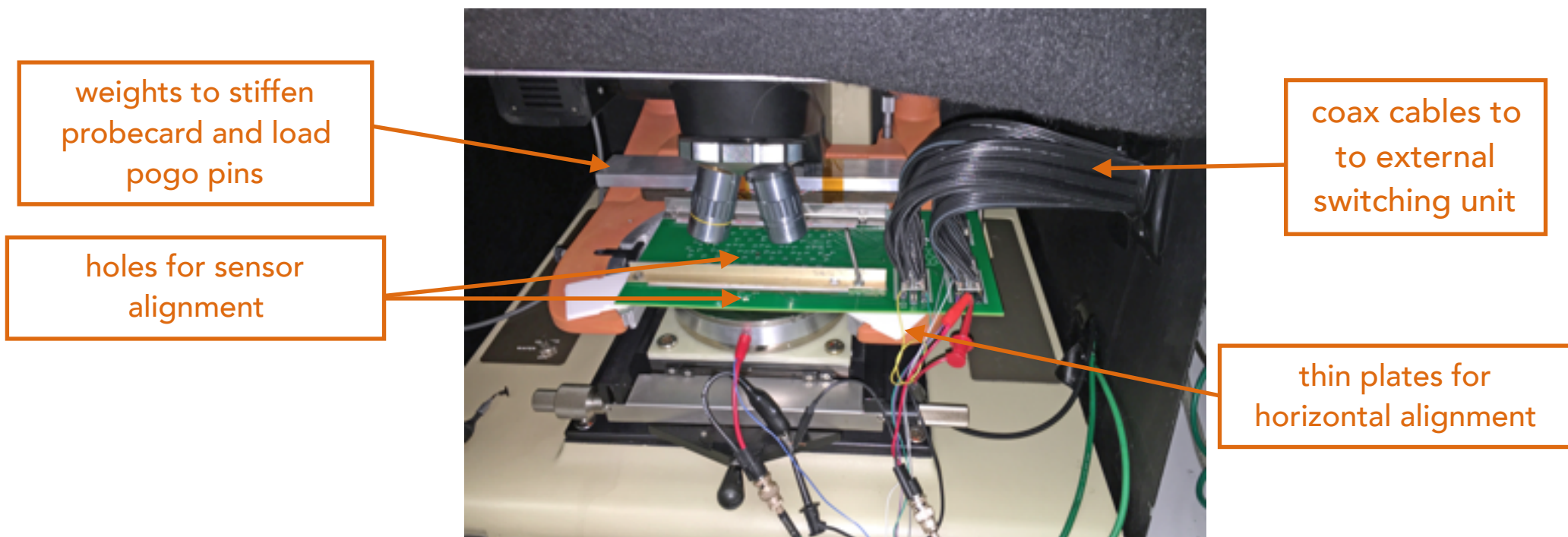
- **Several different sensor types from several different vendors will have to be tested and evaluated.**
 - ➔ Wafer sizes of 6" and 8".
 - ➔ Cell sizes of $\sim 5 \text{ mm}^2$ and $\sim 10 \text{ mm}^2$.

- **For this purpose, we are setting up a laboratory here at CERN.**
 - ➔ Probestation was bought and is awaiting service plus a new location.
 - ➔ An existing probecard will be redesigned, most likely with switching system onboard.
 - ➔ Rest of the setup is either ready or can become available very quickly.

SETUP AT FNAL



- There is an existing sensor testing setup at FNAL to test the HPK 128ch 6" wafers.
 - ➔ It is difficult to contact such a large area uniformly and without damaging the sensor.
 - ➔ Use pogo pins to contact sensor cells. Basically, these are broad needles on little springs.



- The goal is to build on their experience and create a more versatile setup here at CERN that is able to test and evaluate all of the coming sensor types.

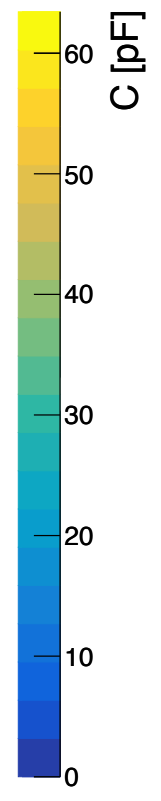
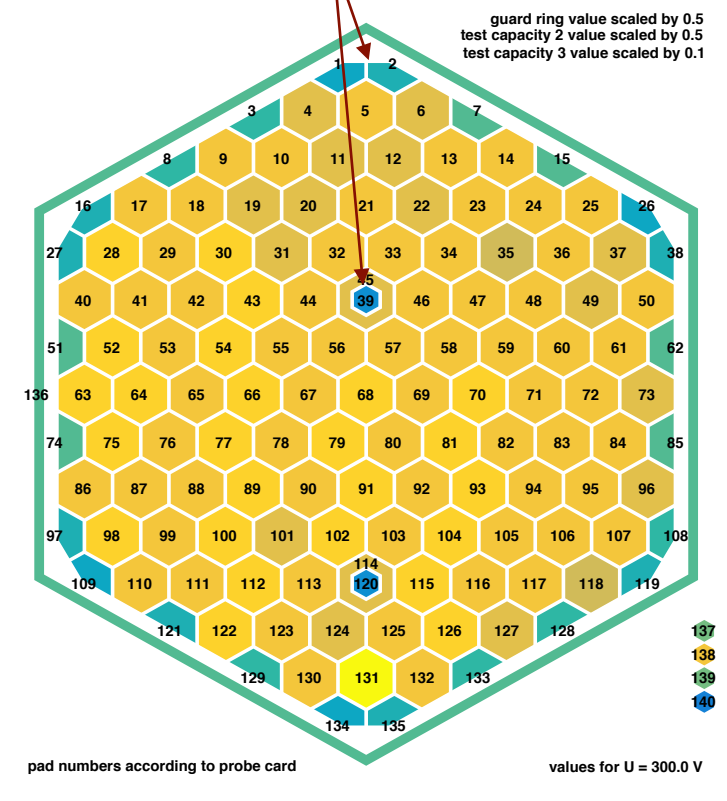
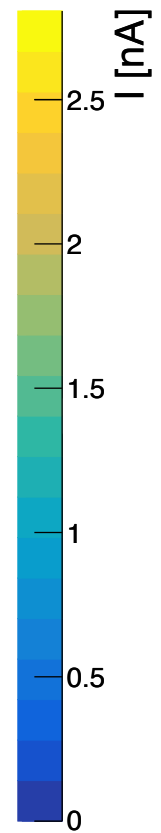
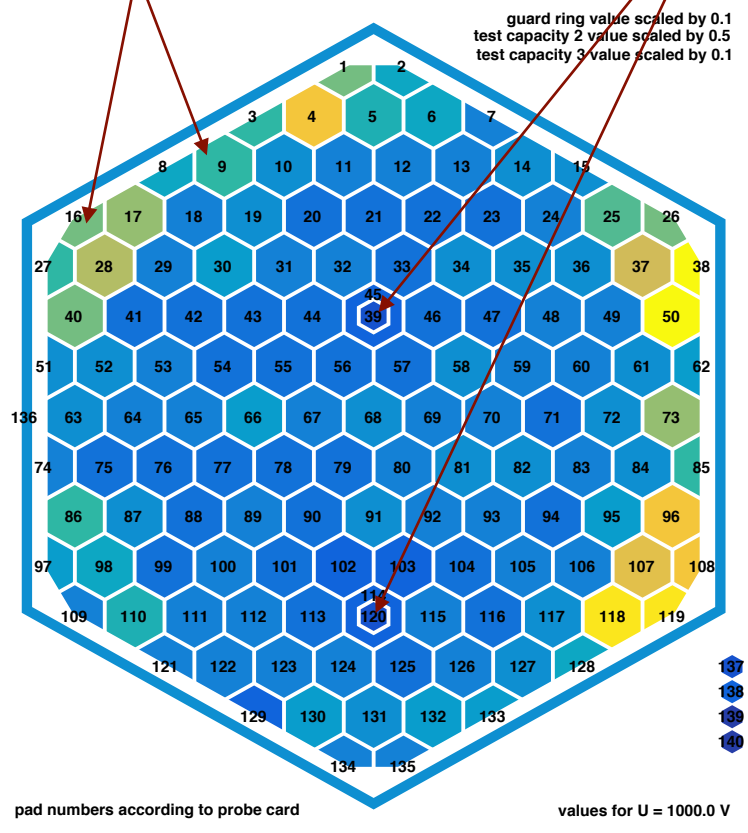
EXAMPLE RESULTS



higher leakage currents at the edge region

lower leakage currents in the calibration cells

mouse bites & calibration cells show lower capacitances than full cells (smaller size)



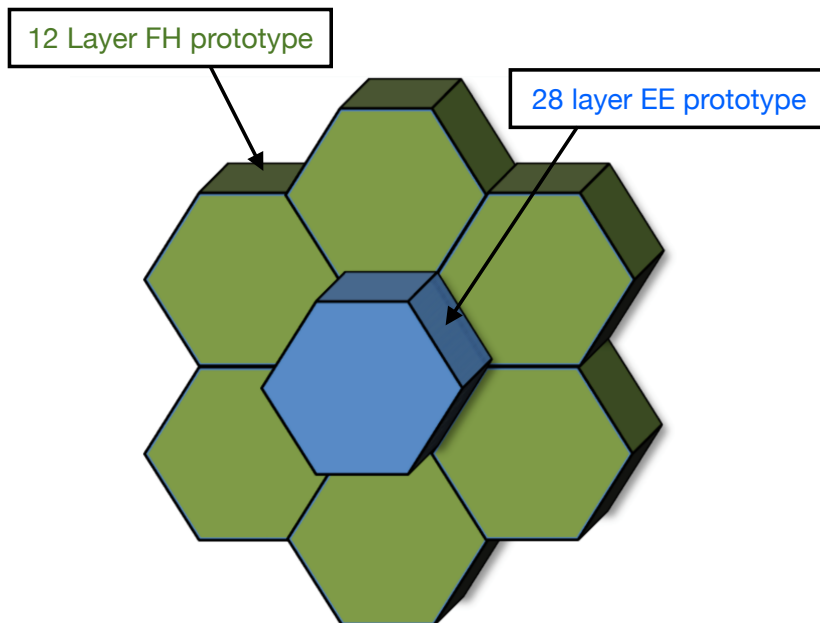
IV and CV example measurements

Testbeam Activities

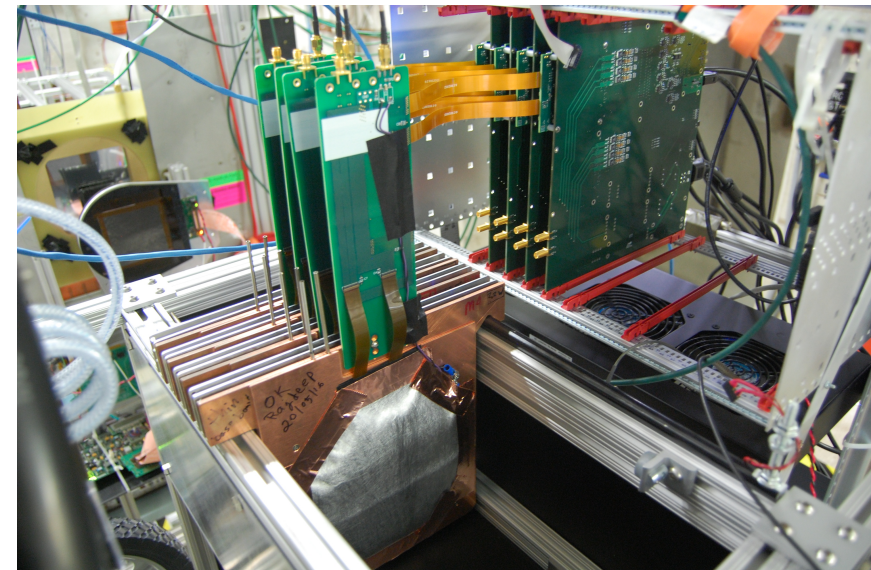
A HGC PROTOTYPE



- In order to validate the HGC concept, a **28 layer ECAL** and **12 layer HCAL prototype** will be build and tested here at CERN.
 - ➔ Readout via **Skiroc2CMS** as soon as it is available, Skiroc2 until then.
 - ➔ Both chips are pin-to-pin compatible and **double board design** allows for uncomplicated exchange of readout board.
 - ➔ Skiroc2CMS has a **faster shaper** (25 ns vs. 180 ns in Skiroc2) and a **TDC for ToA measurement with ~50 ps**. It can also deal with both polarities.



planned prototype



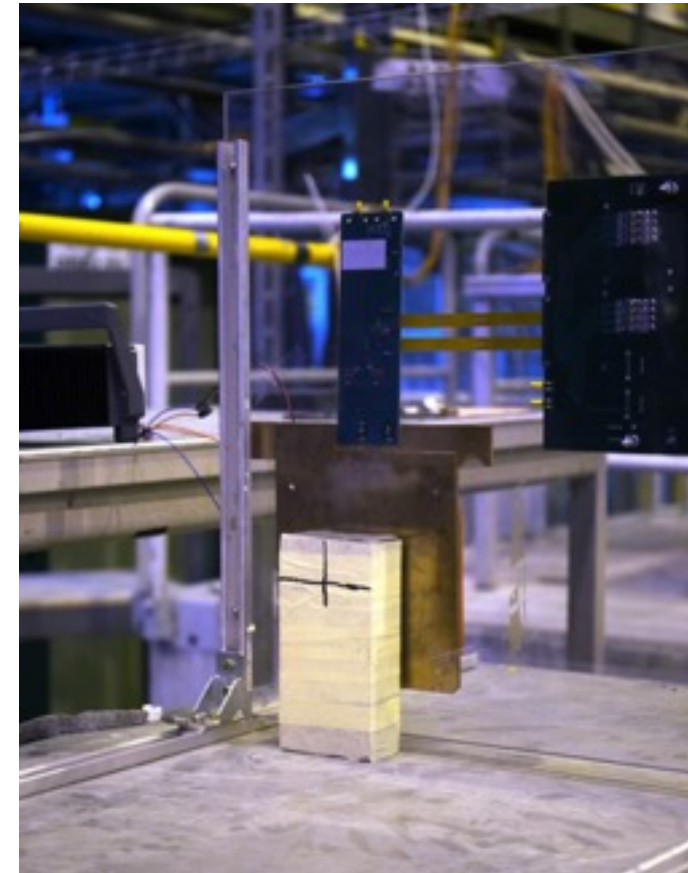
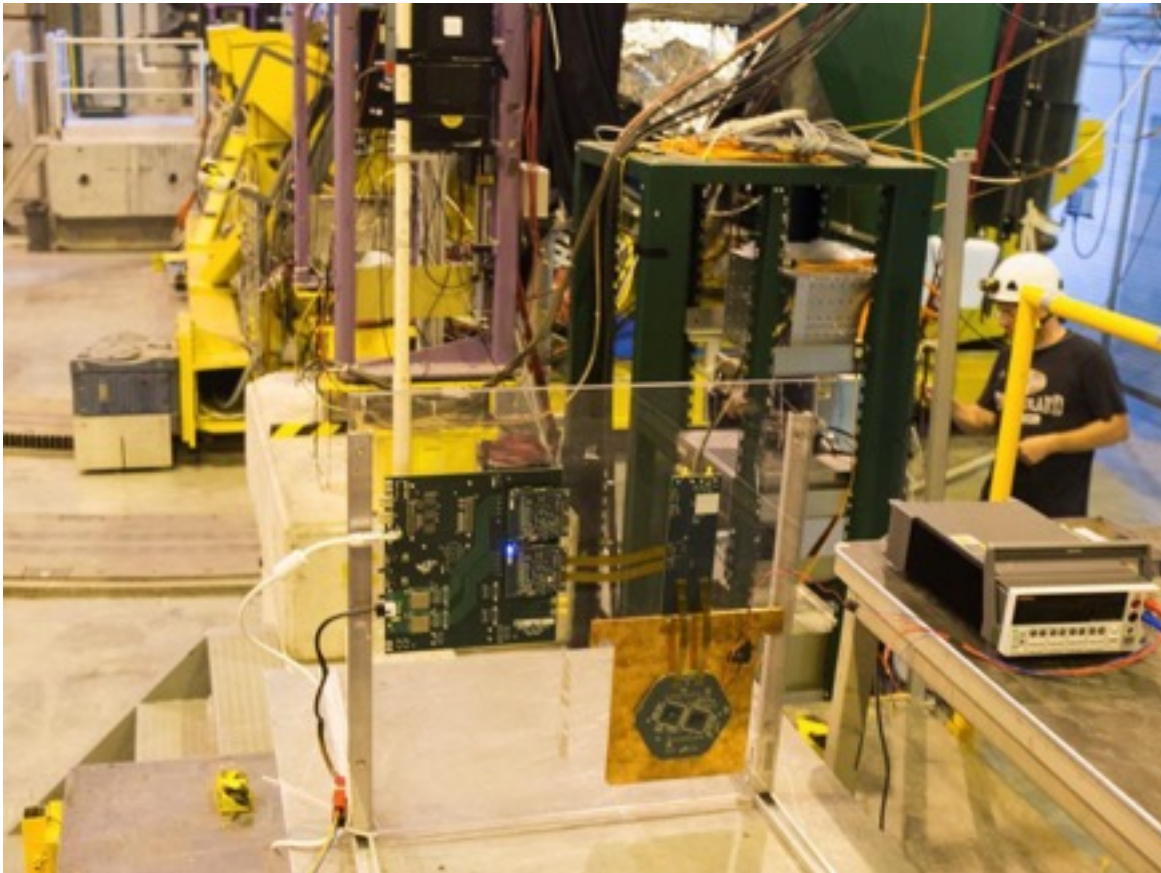
hanging file system



- **Several testbeam periods** are planned in the coming months with the aim to eventually operate the full 28-layer EE + 12-layer FH prototype.
 - 17.8. - 24.8.: Get DAQ running, take data with a single module
 - 31.8. - 7.9.: Operate a multilayer system, performance tests and characterisation
 - 2.11. - 7.11.: Operate a near 28 layer system with Skiroc2CMS
 - Sometime early next year: Full 28-layer EE + 12-layer FH system

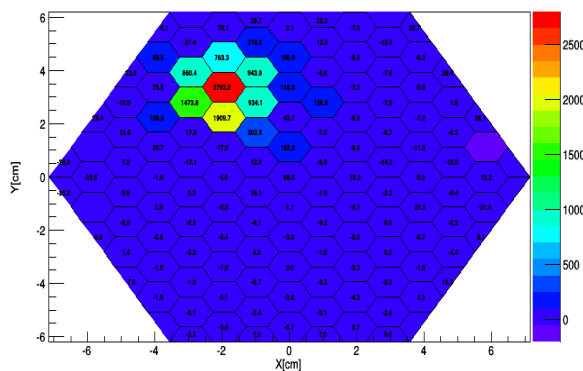
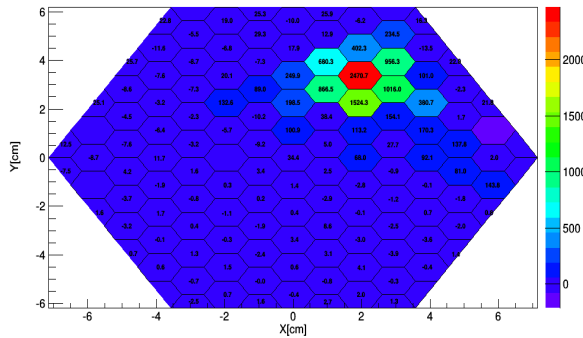
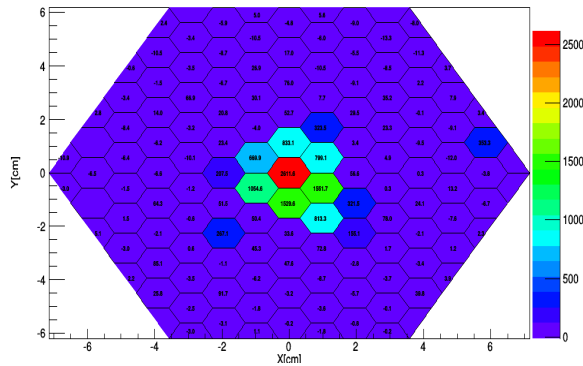
- LCD group participates in **cassette preparation, data taking and data analysis.**

TESTBEAM SETUP AT H2



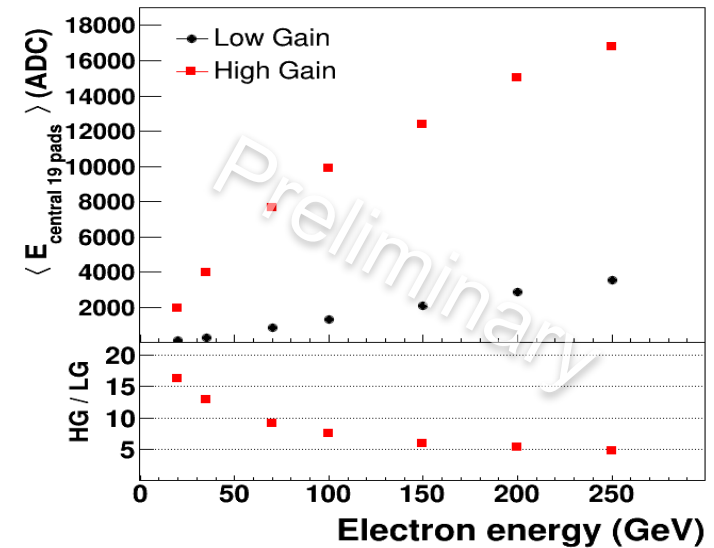
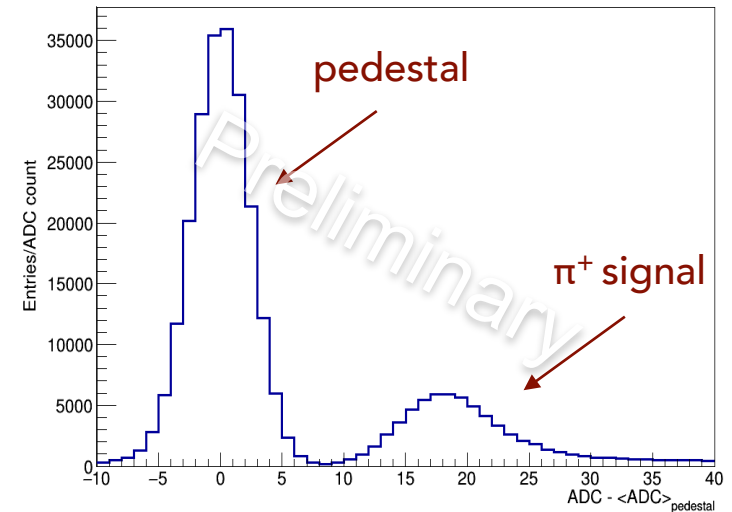
- One sensor only (status 17.8.)
- Lead block of 5 cm thickness used for most runs ($\sim 9X_0$)
- Took mostly e^+ and some π^+/μ^+ data (and noise data)

A FEW FIRST IMPRESSIONS



Studies done:

- Pedestal and CM noise runs
- Energy scans
- Region scans
- MIP uniformity



150 GeV electrons with 5cm lead absorber

MIP signal and electron energy scan

Thank you!

Backup

- Key specs

- Low noise of 0.4 fC (~2.5k e-)
- High dynamic range of 2 fC to 10 pC (~12k e- to ~6M e-)
- Slow shaper for charge measurement of 180ns
- Adjustable fast shaper of 50 to 100 ns
- 10-bit DAC for discriminator threshold, 4-bit trim DAC for each channel
- Power pulsing possibilities

