Test-beam studies on the ALICE investigator chip

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Outline



- Motivation of study on ALICE investigator chip
- Introduction of the ALICE investigator chip
- Test-beam data taking & analysed data
- · Results
- Summary & outlook

Motivation of studies on ALICE investigator chip



Large surface silicon tracker planned for CLIC (~ 90m²):

→ Need of large scale production

Benefit from integrated technologies:

- → Monolithic technologies
- No need of bump bonding
- → Reduced material budget

Benefit from synergies with ALICE collaboration:

- → Test-chip developed within ALICE collaboration to investigate full analogue performance of monolithic technology chosen by ALICE
- Interesting to study feasibility of monolithic technology with respect to CLIC tracker requirements (time slicing of 10 ns, single point resolution of ~ 7 μm)

CLIC tracker layout:



The ALICE investigator chip



ALICE INVESTIGATOR, monolithic HR-CMOS test-chip (W. Snoeys, J. W. Van Hoorne et. al.):

- Developed by the ALICE collaboration to test
 analogue performance
- 180 nm High Resistivity (HR) CMOS process
- 15-40 μ m thick epitaxial layer (1-8 k Ω cm)
- 134 mini-matrices with different pixel layouts
- 8x8 pixel matrix per mini-matrix
- Optimisation of collection-diode geometry
- → Minimise capacitance (~ 2 fF) → fast timing (~ ns)

External readout (designed by K. M. Sielewicz):

- Selectable mini-matrix
 - → Connected to readout
 - → 64 ADCs to read out full waveform of each pixel
- 65 MHz sampling clock
 - → Limits achievable accuracy of timing resolution





Test-beam data taking



ALICE INVESTIGATOR integrated in CLICdp Timepix3 telescope at SPS beam-line:

Mechanical integration of investigator in Timepix3 telescope setup:



Integration of investigator data in telescope software:



Time

- If a hit gets recorded in the investigator:
 - → Read out of waveform of all pixels
 - → Sent trigger package to telescope planes
 - Used for offline synchronisation
- → Benefit from good single point (~ 2 μ m) and timing (~ ns) resolution of Timepixe3 telescope

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Event reconstruction

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Basic reconstruction and definition of observables: Example of pixel waveform: Amplitude / ADC Signal defined as magnitude of amplitude drop -20 Hit time Pedestal Noise defined as RMS of fluctuation -40 Signal around baseline **Rise time** -60 defines slope Cut on S/N > 8of exponential -80 decay Fit exponential function f(t) to waveform -100 Work in of each pixel to extract timing: progress -120 40 45 50 60 65 55 70 Time sample / 65 MHz $f(t) = \begin{cases} Pedestal \\ Pedestal + Signal * (e [t-t(hit)] / t(rise) - 1) \end{cases}$ $t \leq t(hit)$ t > t(hit)Example of χ^2 / ndof distribution: Arbirtrary units 1400 1200 Work in progress **Further quality cuts:** 1000 800 Cut on χ^2 / ndof of waveform fit \rightarrow only for timing observables 600 Track-cluster distance < 100 μm 400 200 Masking of edge pixels 0 2.5 2 3 0.5 1.5 3.5 4 χ^2 / ndof p. 5

Cluster size and spatial resolution for V_{bias} = 6 V

Results for pitch of 28 µm and bias voltage of 6 V:



- Significant charge sharing for small pitch:
- → Cluster size of ~ 1.5
- Position reconstruction improves with respect to binary expectation of ~ 8 μm (η-correction applied):
- → Single point resolution ~ 4.6 μ m (telescope track resolution of ~ 2 μ m unfolded)

Hit time resolution and rise time for $V_{bias} = 6 V$

Definition of timing observables:

- Use first pixel in cluster associated to telescope track to extract timing
- → Minimise impact from charge sharing

Results for pitch of 28 μm and bias voltage of 6 V:



- Hit time relevant for CLIC to achieve time slicing of 10 ns:
- → Hit time resolution of ~ 7 ns
- Rise time interesting to study technology:
- → Expect slower contributions from charge sharing and / or non depleted regions

In-pixel studies at $V_{bias} = 6 V$

clc

Results for pitch of 28 μ m and bias voltage of 6 V:



Work in progress

- Seed signal drops at pixel edges and pixel corners due to charge sharing:
- → Lowest cluster sizes in pixel center
- → Intermediate cluster sizes at pixel edges
- → Highest cluster size in pixel corners

In-pixel studies at $V_{bias} = 6 V$



Results for pitch of 28 μ m and bias voltage of 6 V:



- Mean hit time of all pixels in cluster interesting to study dependency of timing in pixel cell on charge sharing:
- → Large variations according to charge sharing at pixel edges and pixel corners
- Hit time of first pixel in cluster interesting to study in pixel performance of time slicing:
- → Small variations in pixel cell → no significant dependency on charge sharing
- → Good timing resolution

In-pixel studies for different bias voltage



Mean cluster size in pixel cell for a pitch of 28 µm and different bias voltages:



Work in progress

- More charge sharing for higher bias voltages due to:
 - → Larger depleted region for higher bias voltages
 - → Larger signal for higher bias voltages
- → Higher cluster size in pixel corners for higher bias voltage



Summary & outlook



- ALICE investigator chip interesting to study full analogue performance of monolithic technology chosen by ALICE with respect to CLIC requirements
- Integration of ALICE investigator chip in CLICdp Timepix3 telescope
- Single point resolution of \sim 5 μ m
- Hit time resolution of ~ 7 ns
 (*Test-chip with external readout*)
- Charge sharing and timing investigated on sub-pixel level
- Efficiency measurement and study of different pixel layouts currently ongoing

BACKUP

In-pixel timing at $V_{bias} = 6 V$





Observe behavior expected from charge sharing with in-pixel accuracy:

- Seed signal
- Cluster size
- Resolution
- Timing

Analysis performs on great level of detail for observables we want to study





- Select pixels with S/N > 8
- Note cut on DAQ level frames are only readout if at least one pixel has S/N > 10

Common mode correction





- Common mode visible in all pixels, different for different events
- → Correct on event basis:
 - Use all pixels with no hit to calculate common mode
 - Use all pixels with a hit \rightarrow subtract common mode \rightarrow use for further analysis

In-pixel studies at $V_{bias} = 6 V$



Hit map in pixel cell for different cluster sizes:

1-pixel hit:



Analysed data set





Pixel layout of studied mini-matrix:

Aim for analysed data presented in this talk:

→ Study spatial and timing resolution

- Study mini-matrix with pitch of 28 μ m
- CMOS transistors outside p-ring
- → Shielded by deep n-wells
- Data recorded during June test-beam period
- → Investigator running in self triggering mode
- Add busy signal from investigator to telescope planes in current test-beam (ongoing) to perform efficiency measurements

Pixel schematic



