Characterization of the C3PD HV-CMOS Sensor

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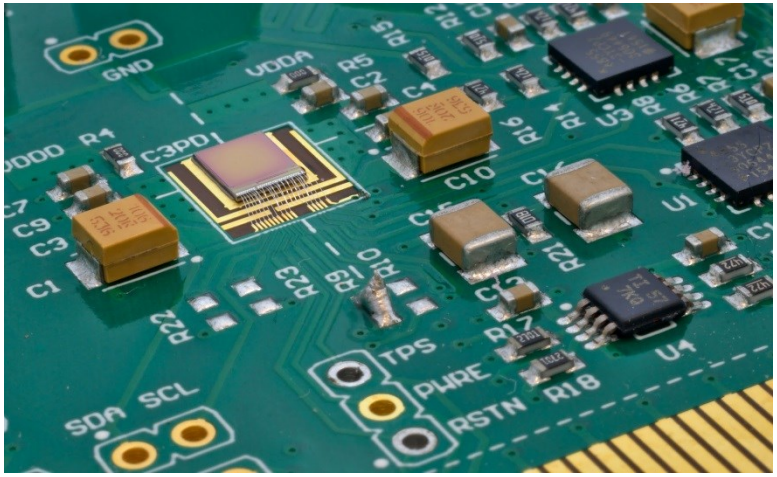
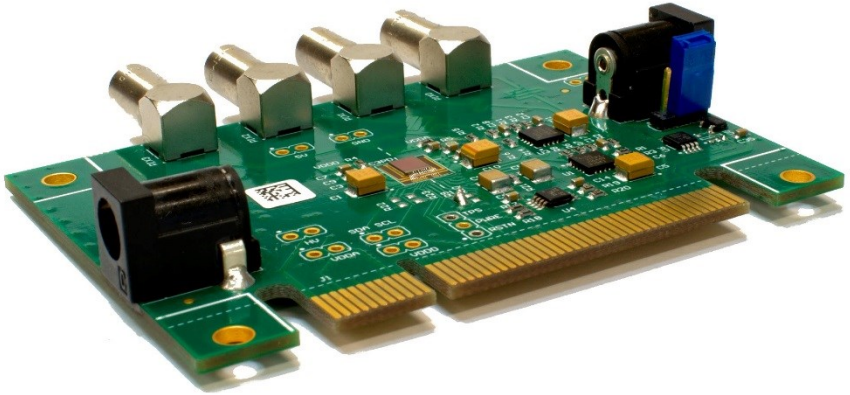
Overview

- The C3PD chip
  - Basic blocks and testability
  - Monitoring output configurations
- Chip calibration and optimum operating settings
- Measurements with sources:
  - ^{55}Fe and
  - ^{90}Sr spectrum
- Feedback and test capacitance calculation
- Sensor's leakage current and breakdown voltage



Photos: S. Kulis



The CLICpix Capacitively Coupled Pixel Detector (C3PD)

- HV-CMOS sensor that will be capacitively coupled to the CLICpix2 read-out chip
  - 128x128 pixels
  - 25 µm pitch
  - 3 different flavours of pixels:
    - 62 double columns with regular pixel (CMOS coupling, original sensor bias)
    - 1 double column with modified biasing for the sensor (single PMOS transistor)
    - 1 double column with modified coupling capacitance (Metal-to-metal coupling)
  - Cluster of pixels buffered directly to the IOs
  - Alignment marks for precise alignment with CLICpix2

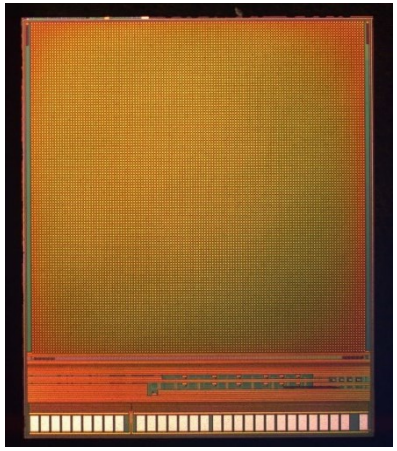
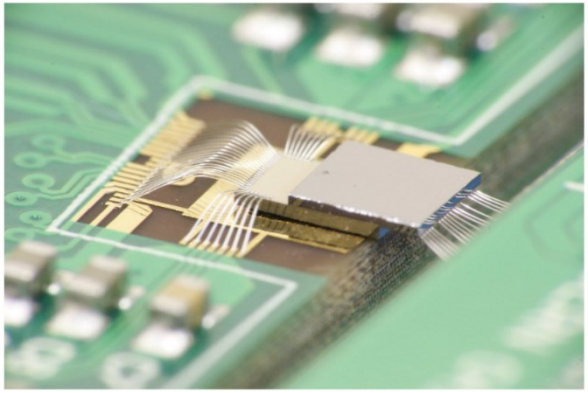


Photo: J. Alozy

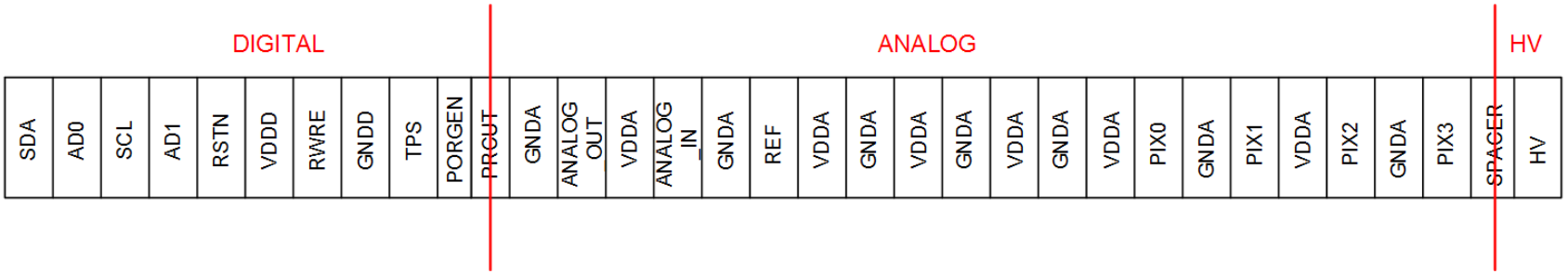
- Technology: AMS 180nm HV-CMOS
- First experience using technology: CCPDv3 chip (I. Peric)
- Important architectural changes to minimize power consumption and to improve speed



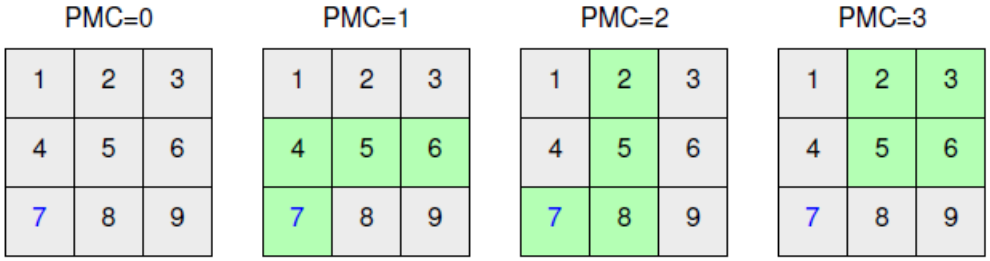
CLICpix/CCPDv3 assembly

Chip Interface - Monitoring Outputs

- 30 IO pins, separated analog and digital power domains:



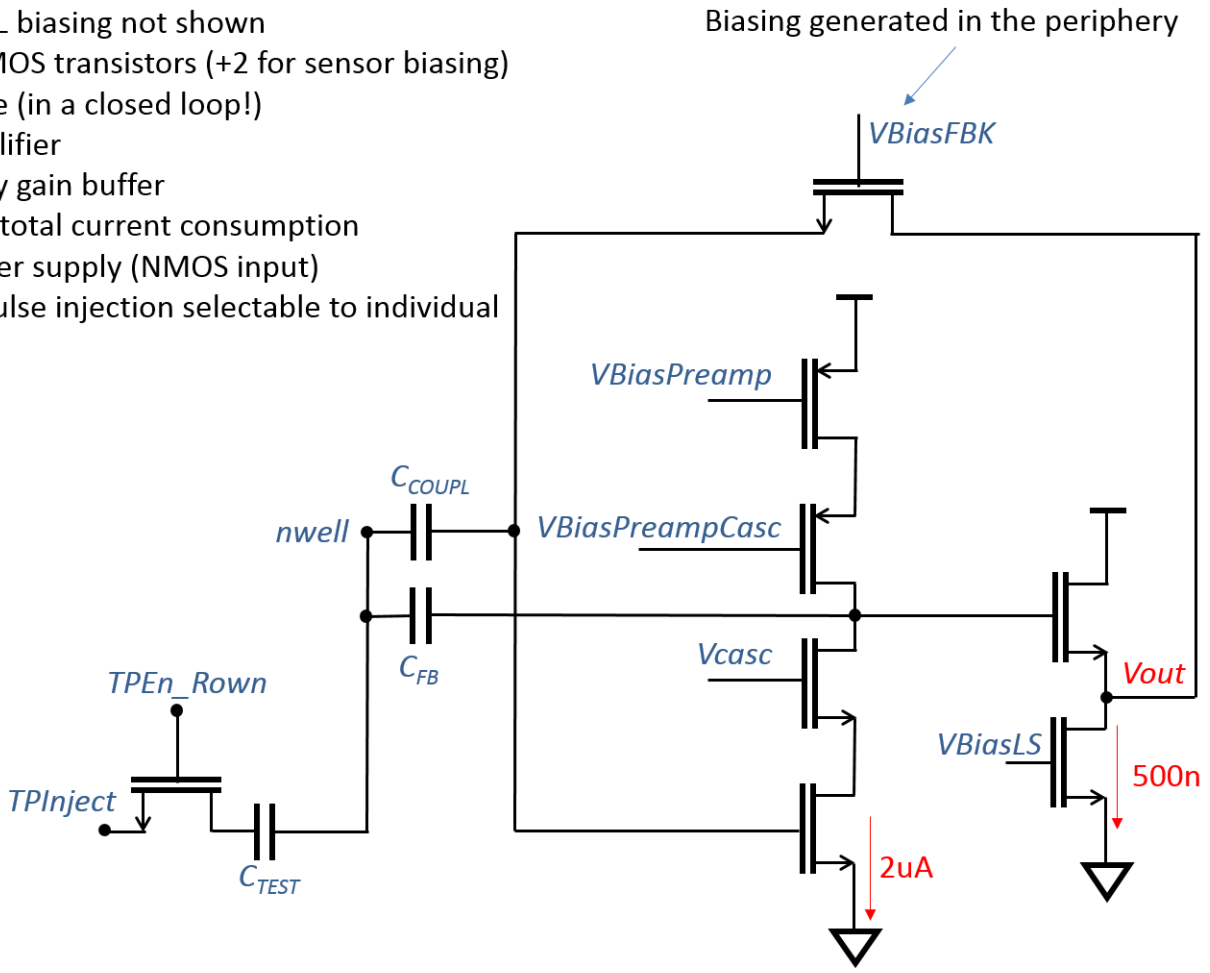
- A 3x3 pixel cluster is implemented in order to monitor different combinations of pixel outputs:
  - Horizontal / Vertical / Square
  - Output of pixel 7 is directly connected to the injected test pulse so that we can monitor test pulse amplitude



*) Pixel 7 is used to monitor actual test pulse amplitude

C3PD Pixel Schematic

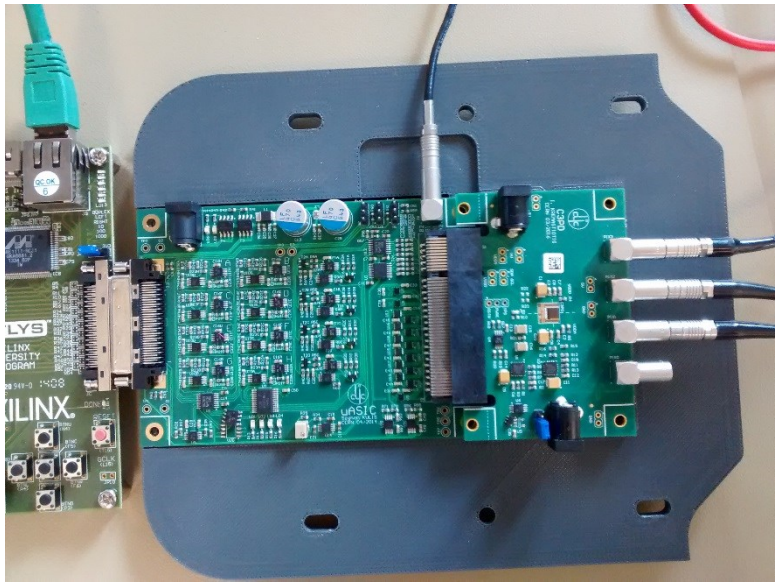
NWELL biasing not shown
1.5 PMOS transistors (+2 for sensor biasing)
2 stage (in a closed loop!)
  Amplifier
  Unity gain buffer
2.5uA total current consumption
1 power supply (NMOS input)
Test pulse injection selectable to individual pixels

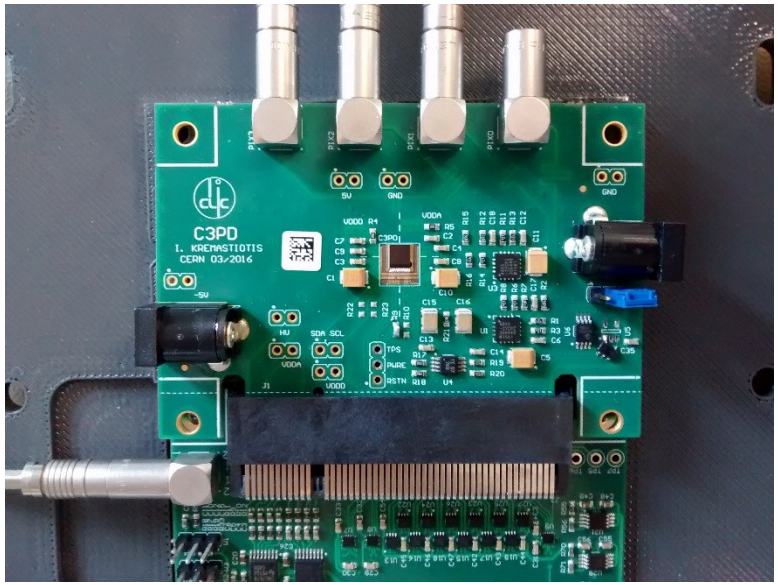


R. Ballabriga

Stand-alone test setup

- C3PD was wire-bonded on a custom designed chipboard connected to uASIC
- Power supplies, external voltage supplies and digital signals are provided from uASIC
- Analog voltages can be monitored using 12-bit ADC on uASIC
- Rail-to-rail operational amplifiers used to monitor pixel outputs

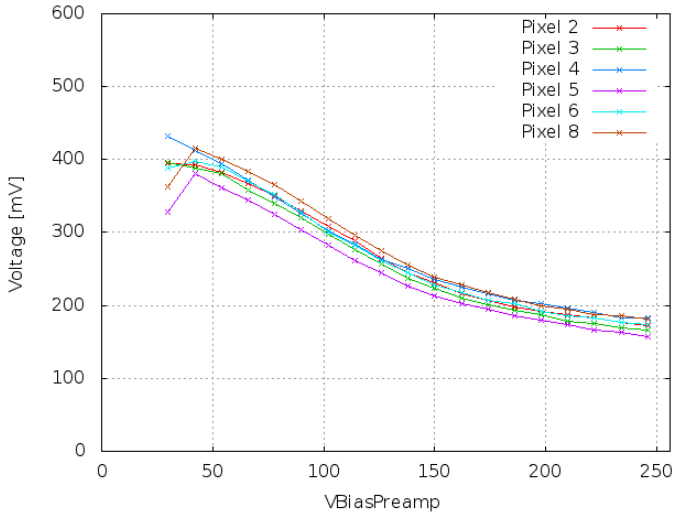


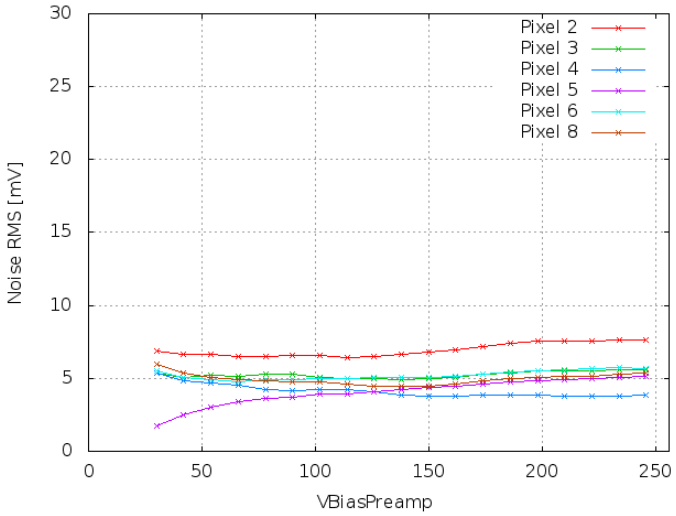


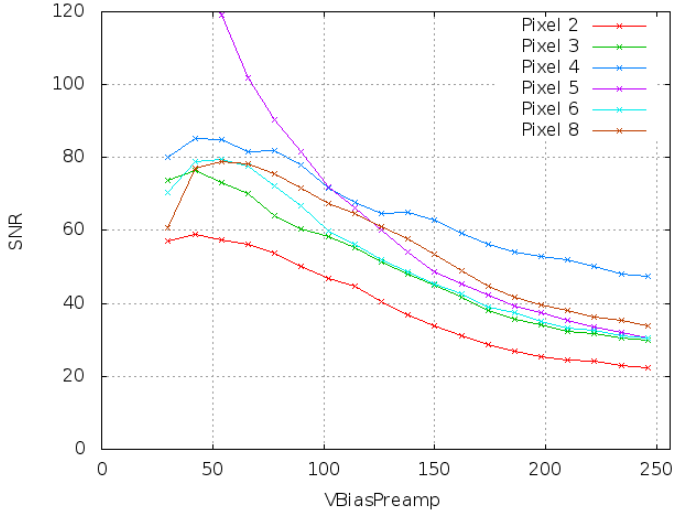
DAC calibration

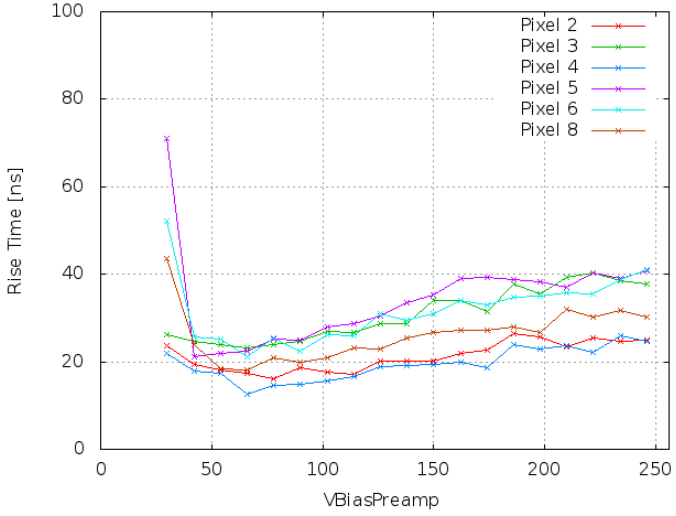
- Digital-to-Analog Converters used to bias the different nodes of the front-end were scanned in order to understand the impact of each setting on the chip's performance.
- Scans were performed for each DAC individually and, in some cases, for pairs of DACs that were scanned simultaneously.
- The results of these scans were used in order to determine the optimum biasing settings with respect to the main performance parameters of the chip:
  - Amplitude
  - Noise
  - SNR
  - Rise time (from 10% to 90% of the pulse height)
  - Power consumption
- A test pulse of 1750 e^- was injected to each pixel individually during these measurements

VBiasPreamp



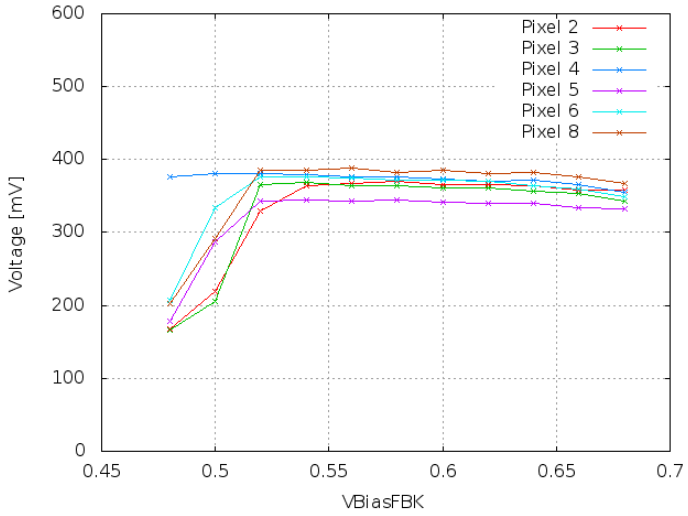


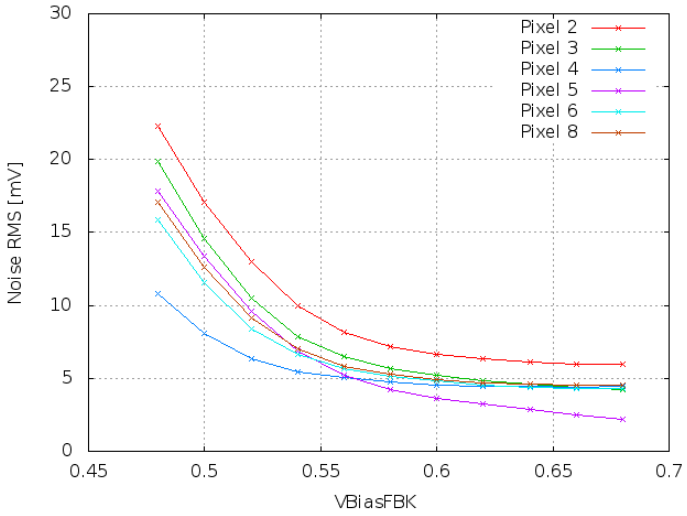


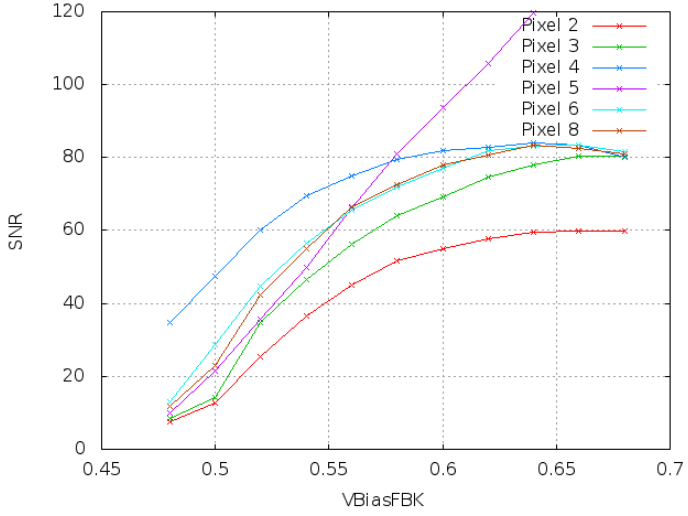


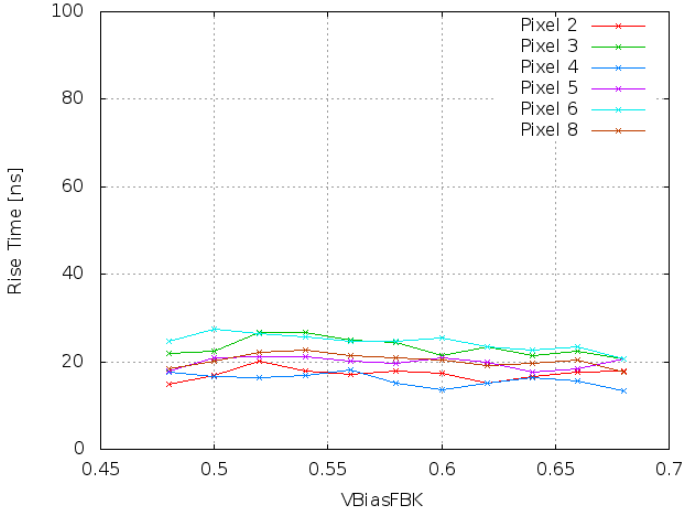
SNR calculated for 1750 e^-

VBiasFBK-external



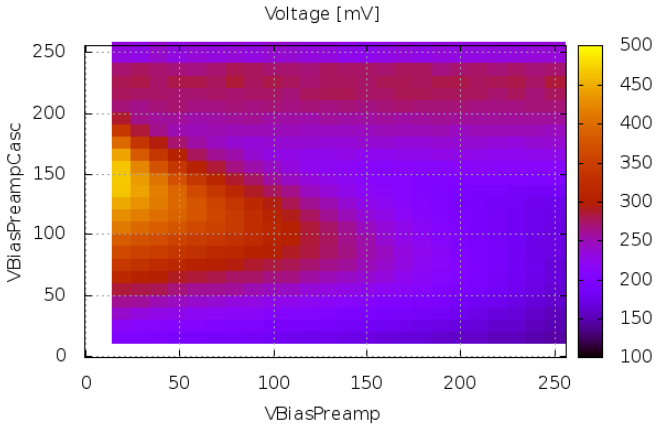


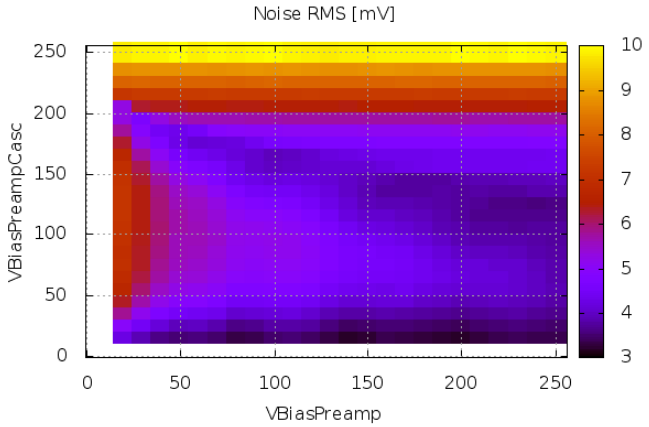


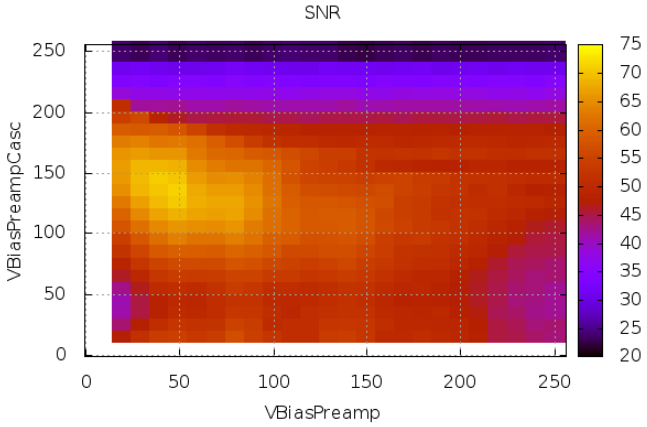


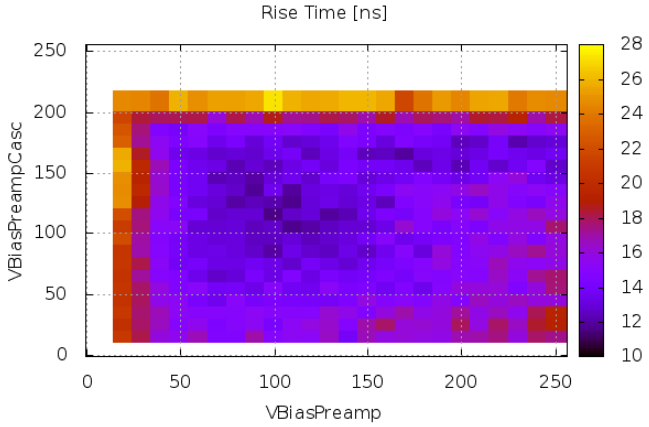
VBiasPreamp vs VBiasPreampCasc

Pixel 4



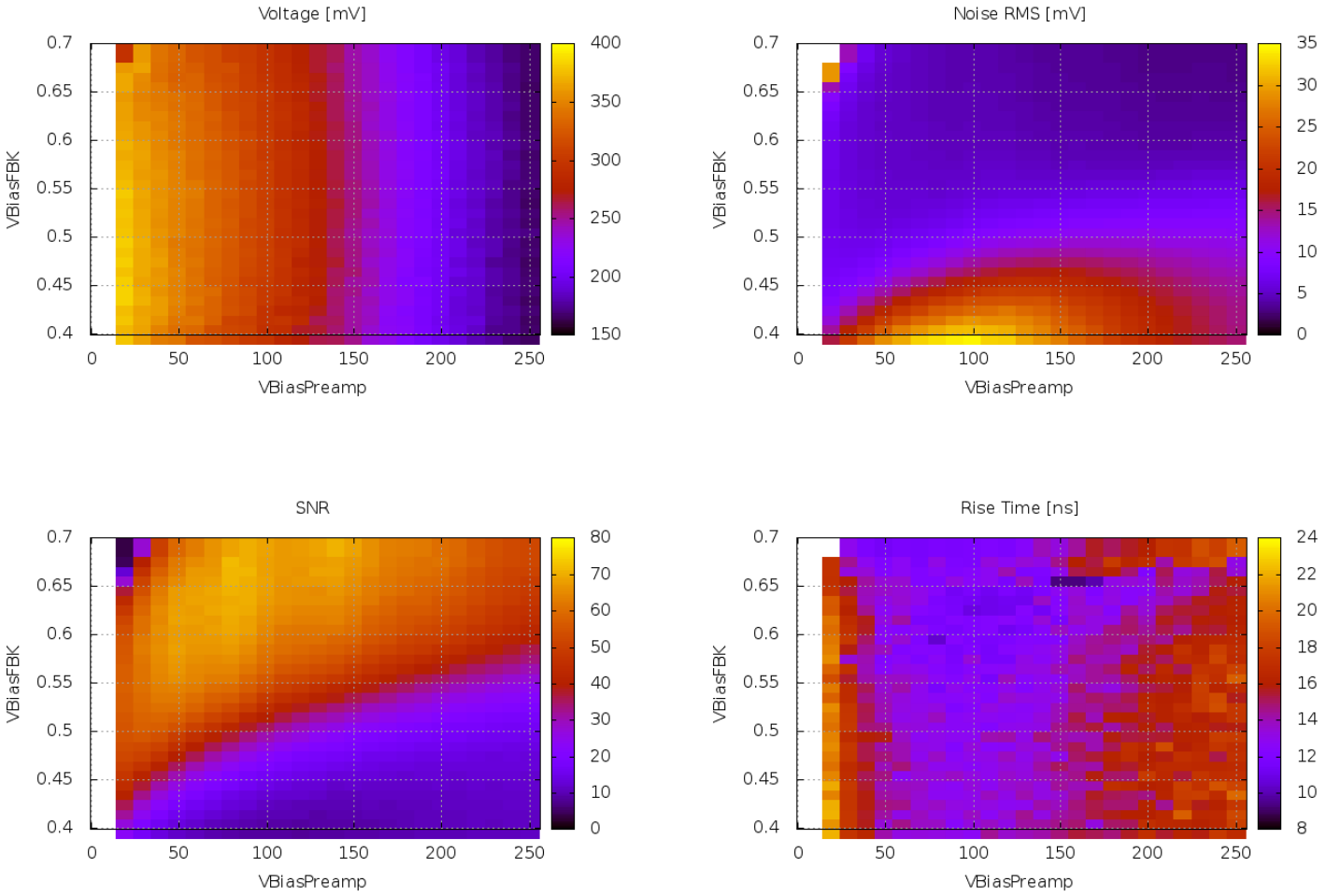






VBiasPreamp vs VBiasFBK-external

Pixel 4

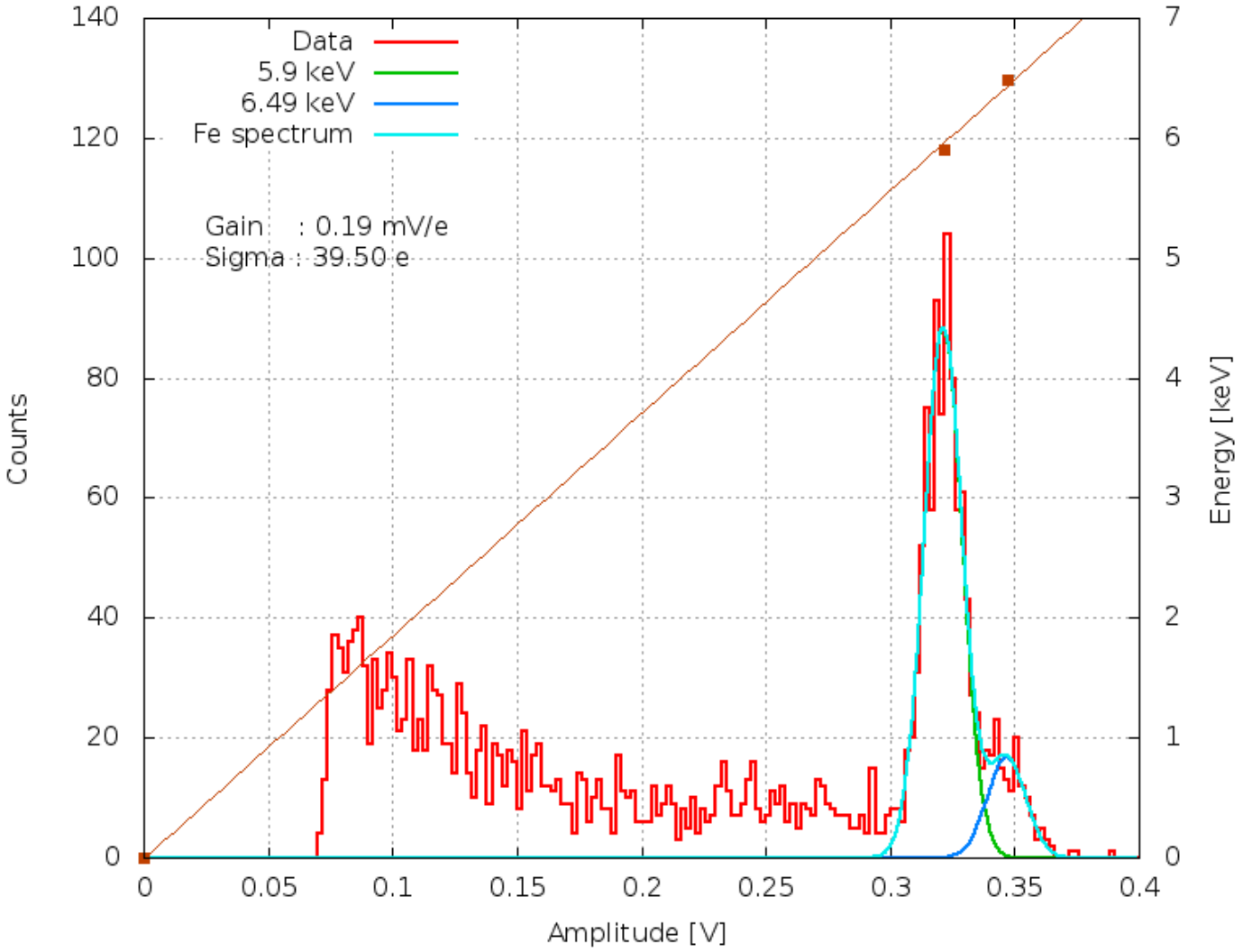


DAC settings

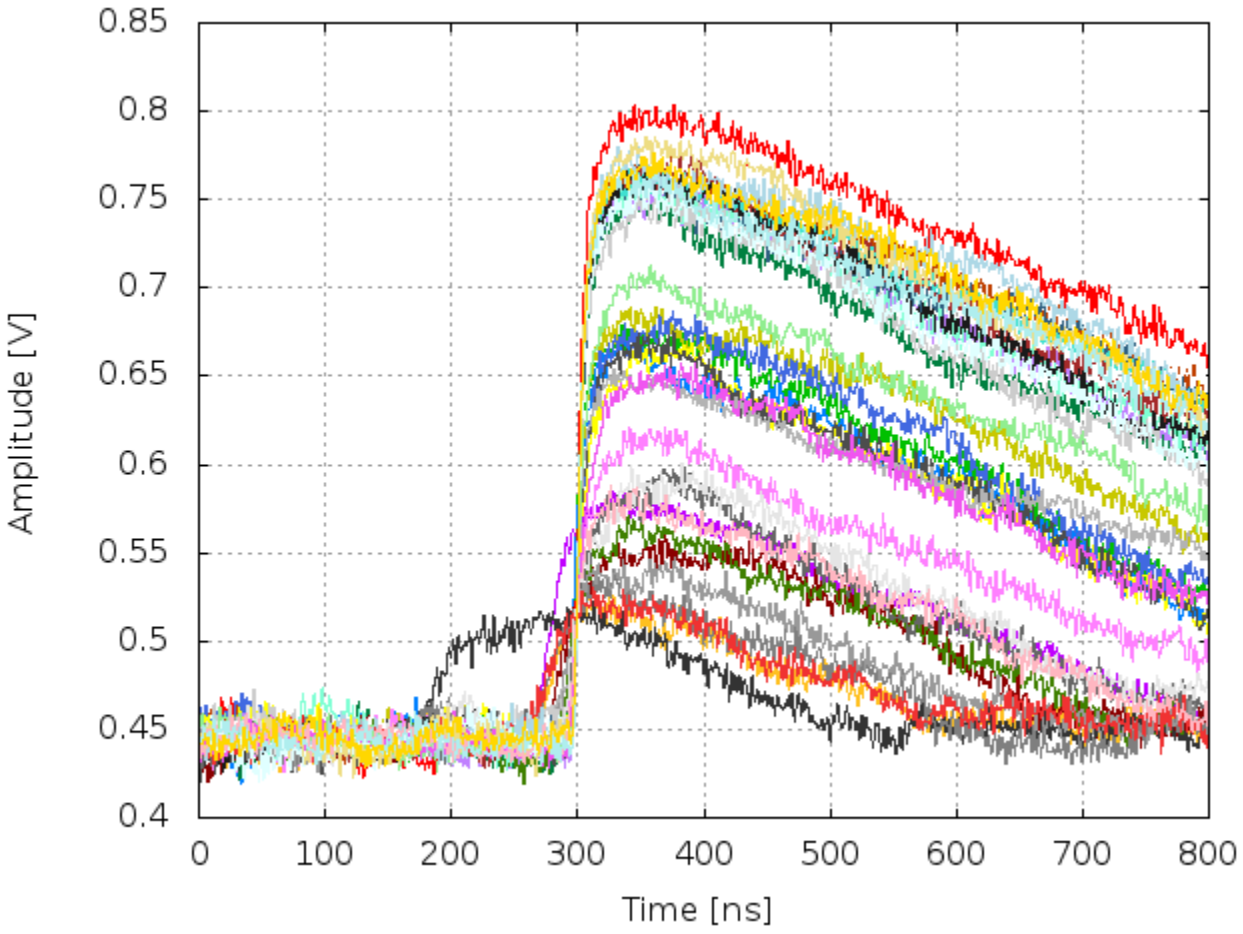
- The optimum DAC settings as extracted from the calibration results are presented in table (in hexadecimal format):
- Feedback biasing (VBiasFBK) is set externally for stand-alone measurements
- These values were extracted as the operating point where we can have:
  - Fast rise time
  - Low noise
  - High output amplitude (and Signal-to-Noise ratio)
  - Low power consumption
  - Without compromising other parameters
- Measurements were run with the above settings using an ^{55}Fe and a ^{90}Sr source.
  - Feedback biasing was set externally to 0.65 V

DAC	Power-on value
VBiasPreamp	0x40
VBiasPreampCasc	0x80
VBiasOA_LF	0x48
VBiasOA_HF	0xFF
VBiasLS	0x10
VBiasFBK	0xFF
VBiasSensor	0x0A
VBiasSensorPMOS	0x0A
VBiasPreampOFF	0x02
VBiasLSOFF	0x02
VBiasTestPulse	0x00

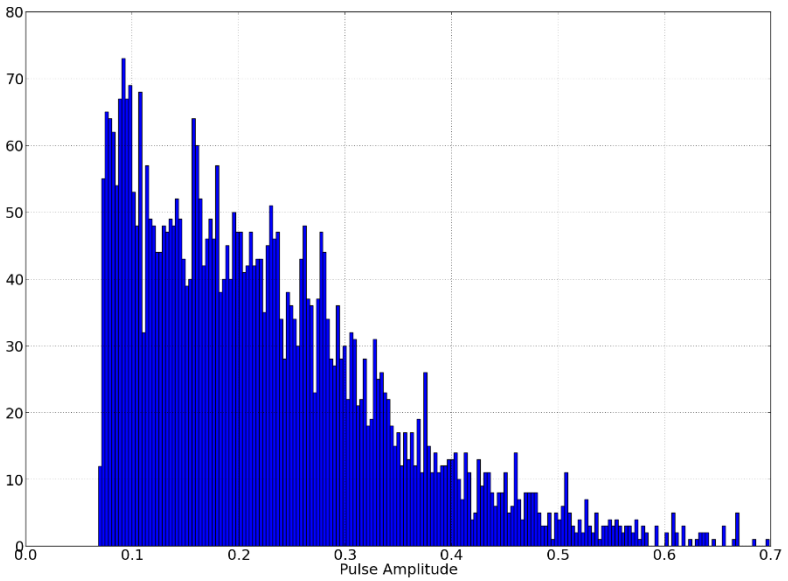
Spectrum from ^{55}Fe source

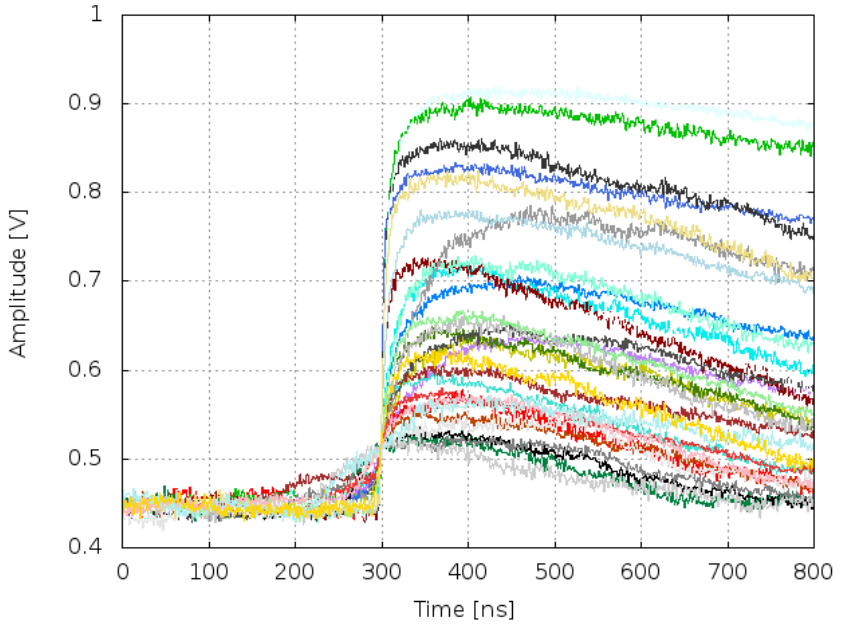


Pulses from ^{55}Fe source



Spectrum and pulses from ^{90}Sr source





Feedback capacitance calculation

- From the spectrum extracted from measurements using an ^{55}Fe source, we can estimate the feedback capacitance:
  - With a known ^{55}Fe energy of 5.89 KeV and Silicon conversion factor of 3.62 we can expect a deposited charge in the sensor volume equal to:

$$\frac{5.89KeV}{3.62} = 1.63\ Ke\ or\ 0.26fC$$

  - The voltage peak corresponding to this energy is at 321 mV, as taken from the mean value of the first Gaussian in the histogram, which gives a charge gain of:

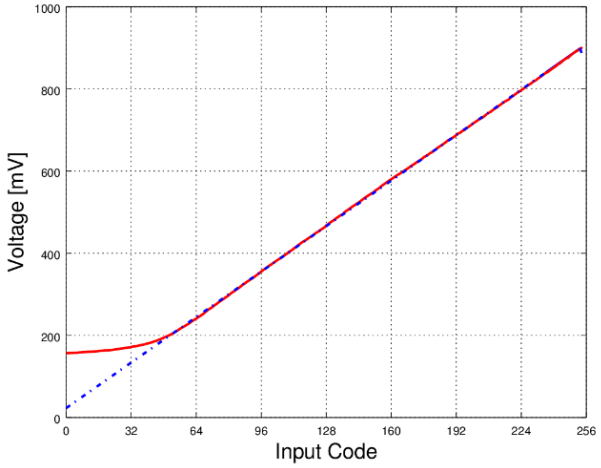
$$A_{charge} = \frac{321\ mV}{1.63\ Ke} \cong 0.19\ mV/e$$

  - From the voltage peak at ~321mV, we can get an estimation on the feedback capacitance:

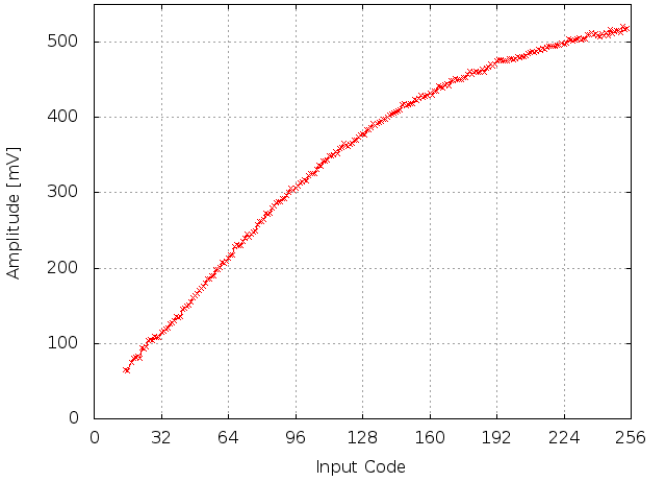
$$C_{fb} = \frac{0.26fC}{0.321V} \cong 0.81fF$$

Test capacitance calculation

Test pulse amplitude



Amplifier's output amplitude
(as function of test pulse DAC code)



- Non-linearity for low Test pulse DAC codes results from HF output buffer's performance
- As shown in the plot in the right, a test pulse DAC code of 102 is needed in order to achieve an output amplitude close to 321 mV.
- This pulse should then inject a charge equal to 1.63 Ke^- at the input of the preamplifier.
- A DAC code equal to 102 gives an injected pulse amplitude of ~370 mV. Since we know the test pulse amplitude and the injected charge, we can then calculate the test pulse capacitance as following:

$$C_{test} = \frac{0.26fC}{0.37\ V} \cong 0.7\ fF$$

- The value for the test pulse capacitance, as extracted from the design is 0.64 fF

Feedback and test capacitance calculation

- The same procedure was followed for the other samples in order to characterize their performance with the ^{55}Fe source and estimate their feedback and test capacitance.
- In addition to the assemblies with the standard 250 µm thick sensor (labelled 1-4 in the plots), 2 more assemblies with sensors thinned-down to 50 µm were tested (labelled t1 and t2)

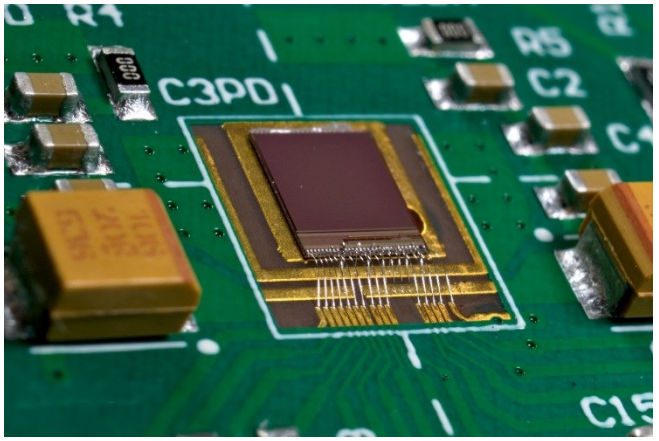


Photo: S. Kulis

Sample	Thickness (µm)	Peak (mV)	C_{FBK} (fF)	C_{Test} (fF)
1	250	321	0.81	0.7
2	250	266	0.97	0.7
3	250	301	0.86	0.68
4	250	348	0.75	0.71
t1	50	327	0.79	0.71
t2	50	322	0.81	0.71

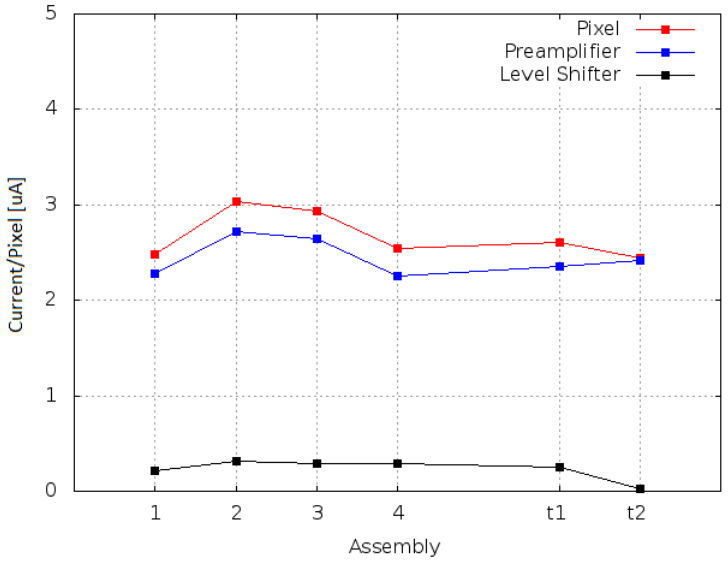
- Average C_{FBK}: ~0.83 fF ± 15%
- Average C_{Test}: ~0.7 fF ± 2%

Test Pulsing

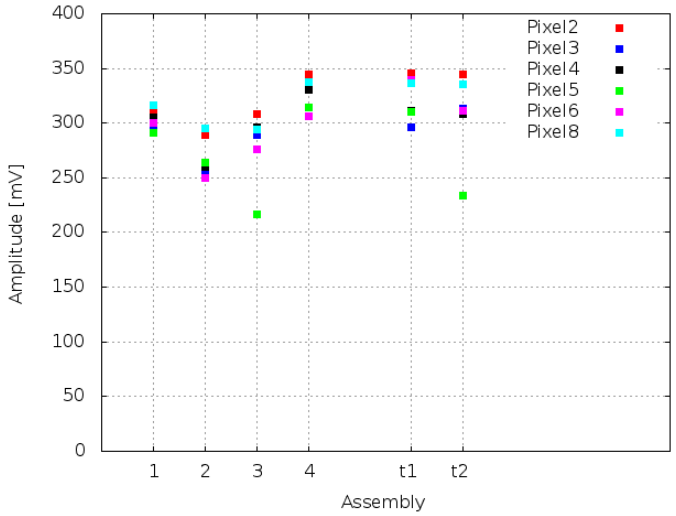
- Measurements were run using the DAC settings, as extracted from the calibration, while keeping the Feedback biasing (VBiasFBK) externally to 0.65 V.

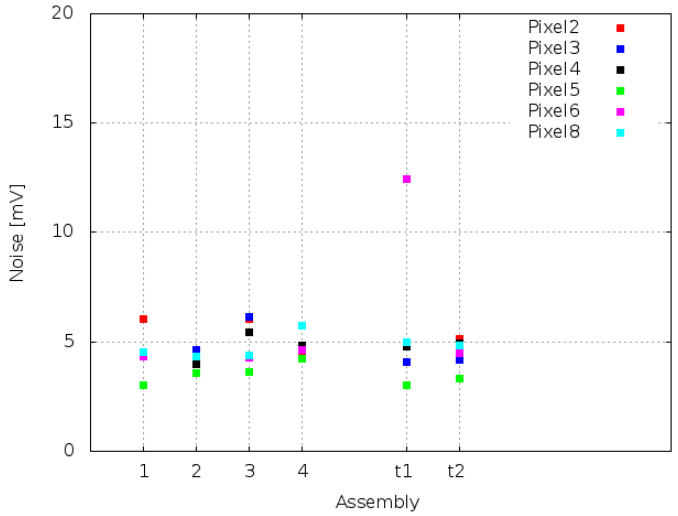
- A test pulse of 1.63 Ke^- (equal to the charge deposited by the ^{55}Fe source) was injected to each pixel individually.
  - The test pulse DAC code needed in order to inject this charge was extracted from the ^{55}Fe source results of each assembly (similarly to sl. 17)

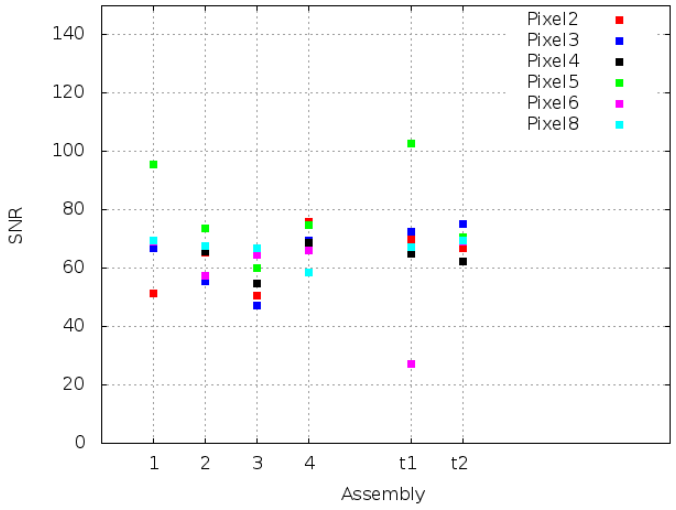
- As shown in the next slide, these settings result to the following average values (as extracted by the 6 monitored pixels of 6 assemblies):
  - Amplitude: 302 mV
  - Noise RMS: 5 mV
  - SNR: 60
  - Rise time: 20.8 ns
  - Current/Pixel: 2.67 μA
    (2.44 μA for Preamplifier and
    0.23 μA for Level Shifter)

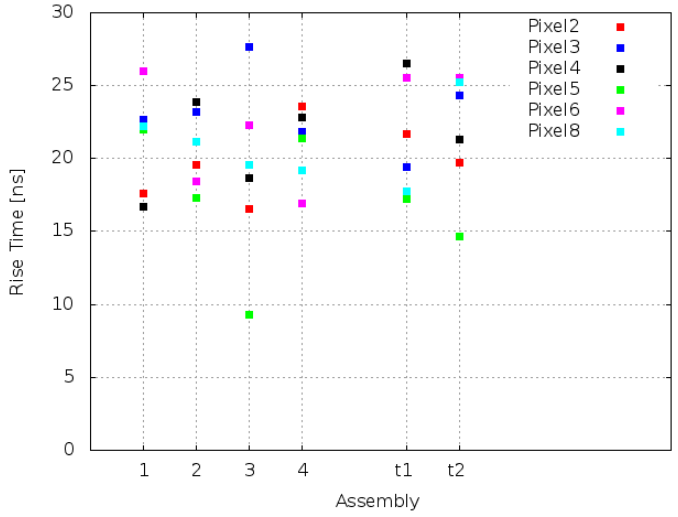


Test Pulsing



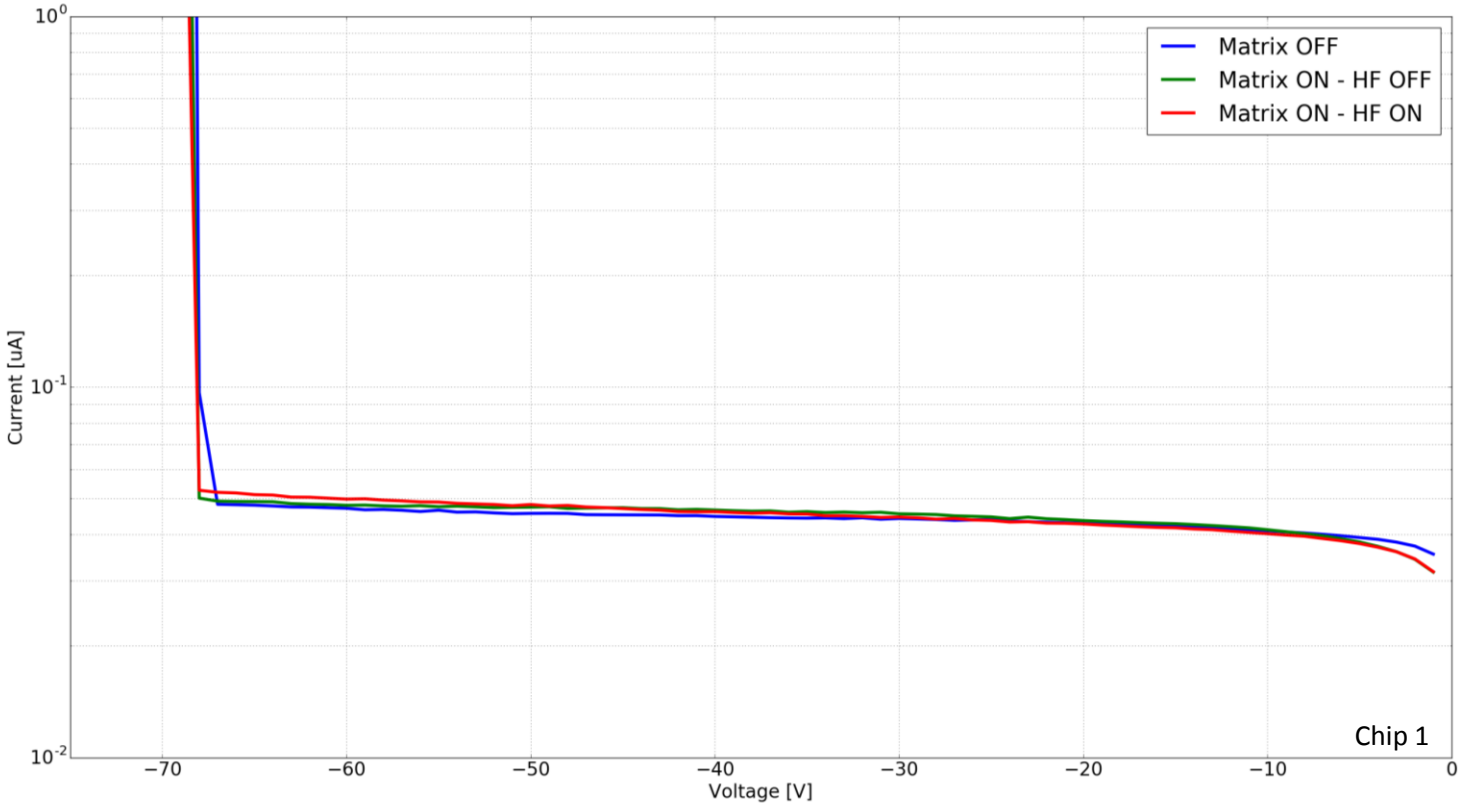






I-V curve for sensor leakage current

- Leakage current: ~50 nA
- Breakdown voltage: -68 V



Summary

- C3PD (CLICpix Capacitively Coupled Pixel Detector):
  - Submitted in February 2016
  - First assemblies received in May 2016
  - Measurements on-going since June 2016
  - 4 standard thickness (250 µm) and 2 thin (50 µm) assemblies were successfully tested so far.

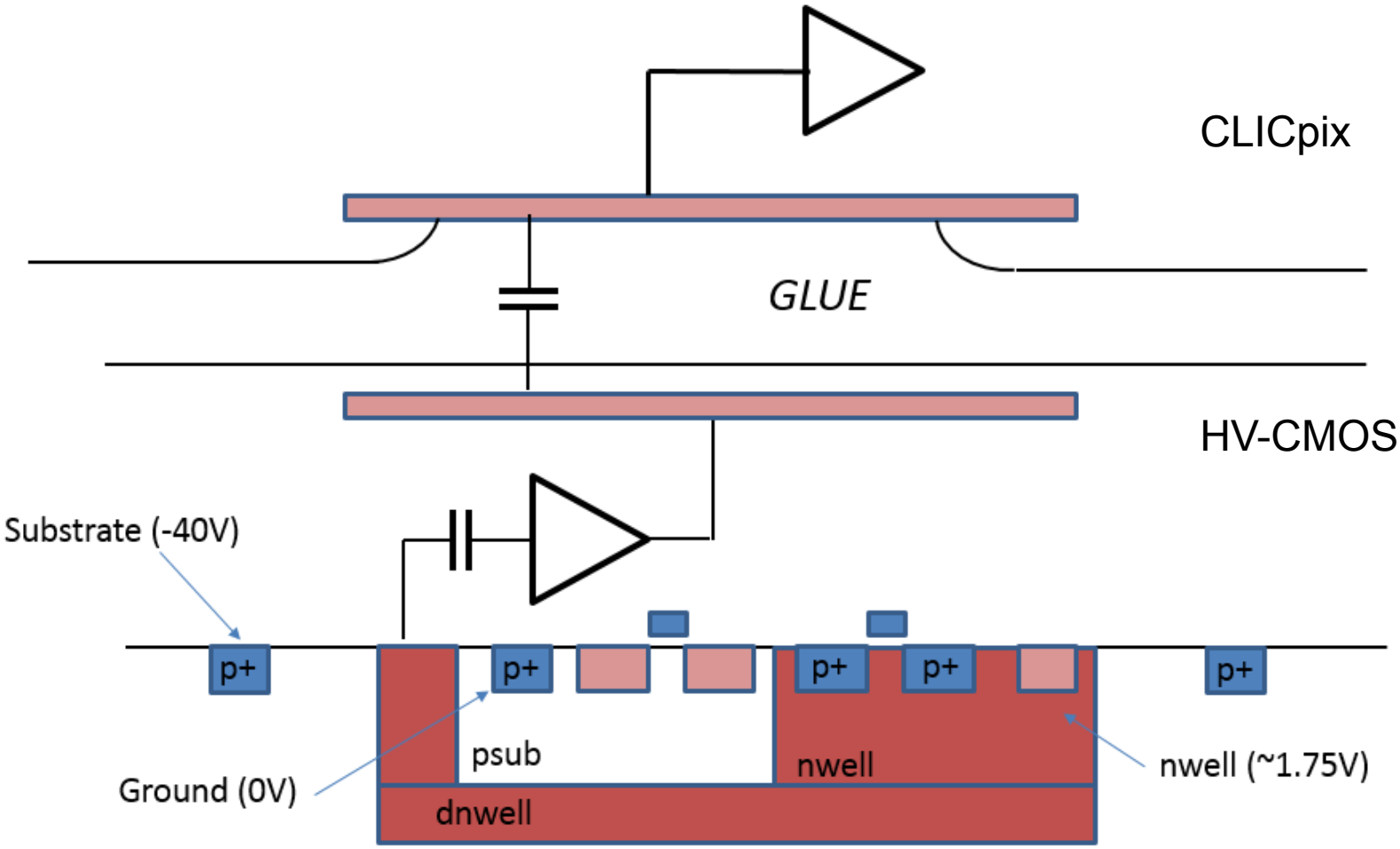
- New chip designed has improved performance in terms of rise time and power consumption compared to the previous CCPDv3 design:
  - Rise time: ~20 ns
  - Consumption: 2.7 µA/pixel
  - Noise: 40 e^-
  - Charge gain: 190 mV/Ke^-

- Feedback and test capacitance calculation
  - Good channel to channel uniformity
  - Average C_{FBK}: ~0.83 fF ± 15%
  - Average C_{Test}: ~0.7 fF ± 2%

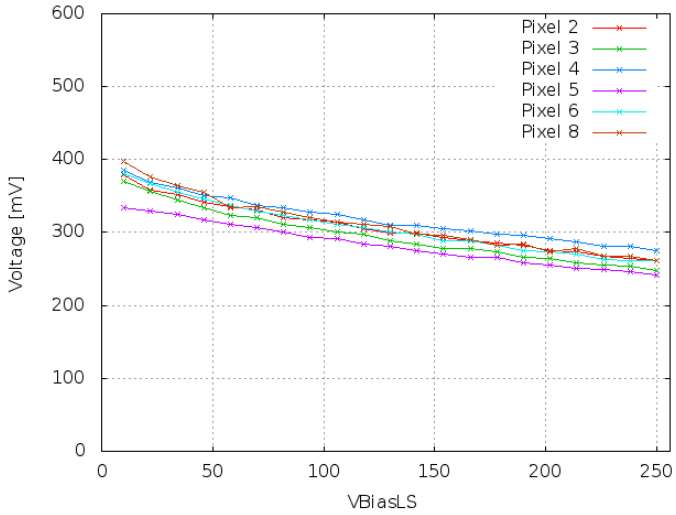
- Further testing:
  - External digital signals to be tested:
    - Power pulsing test with precise timing
    - External test pulse injection

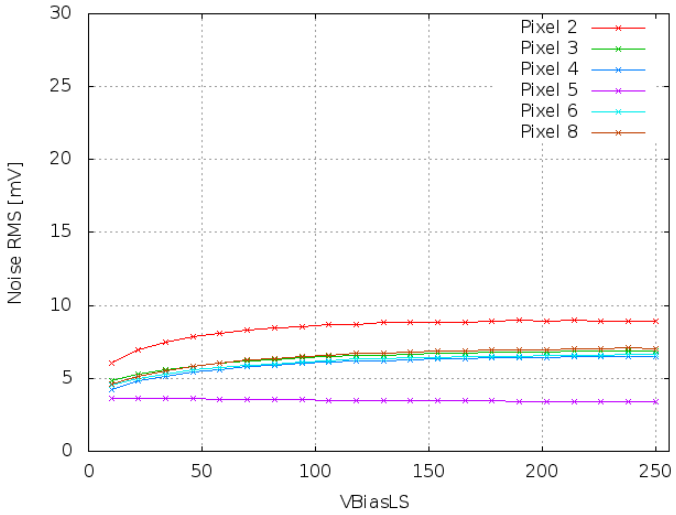
Back-up Slides

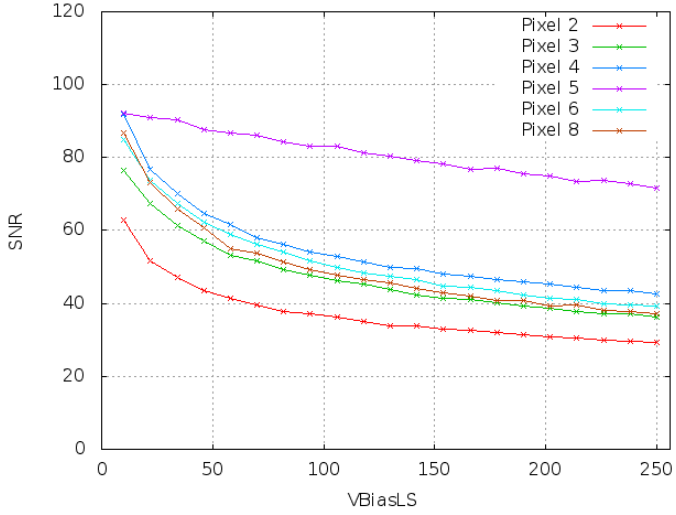
Assembly Cross-Section

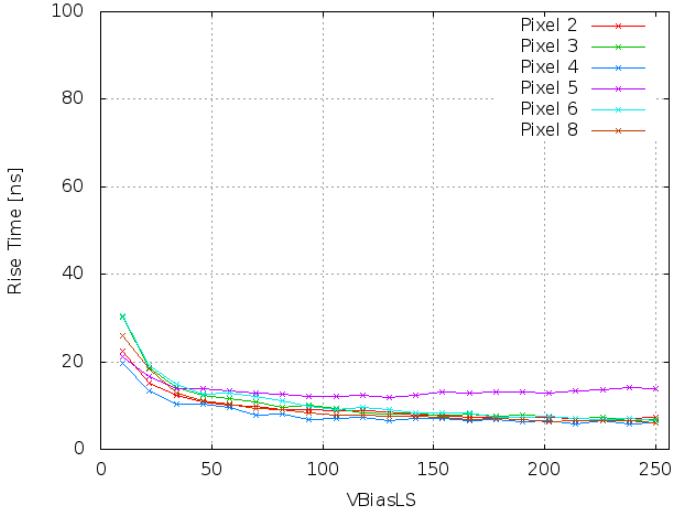


VBiasLS


Voltage [mV]
VBiasLS
Pixel 2
Pixel 3
Pixel 4
Pixel 5
Pixel 6
Pixel 8


Noise RMS [mV]
VBiasLS
Pixel 2
Pixel 3
Pixel 4
Pixel 5
Pixel 6
Pixel 8


SNR
VBiasLS
Pixel 2
Pixel 3
Pixel 4
Pixel 5
Pixel 6
Pixel 8


Rise Time [ns]
VBiasLS
Pixel 2
Pixel 3
Pixel 4
Pixel 5
Pixel 6
Pixel 8