Irradiated and non-irradiated CCPD manufacturing, lab and testbeam characterization

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Outline

- The CCPDv4-5-6 concept, capacitive coupling
- The FEI4 Telescope at SPS
- Test beam characterization of CCPDv4
  - Comparison of AMS and IBM processed chips
  - Results with CCPDv4, irradiated to 1e15,5e15 n_{eq}/cm^2
- Next steps: H35DEMO, Glueing process qualification etc..

The CCPDv4/v5/v6 Concepts

- Capacitively-Coupled Pixel Detectors (CCPD)
  - Based on HV-CMOS Commercial process
  - Possibility to implement amplifier and discriminator in-pixels (in pixel threshold ~600e)
  - High-Voltage swing allows for Capacitive-coupling

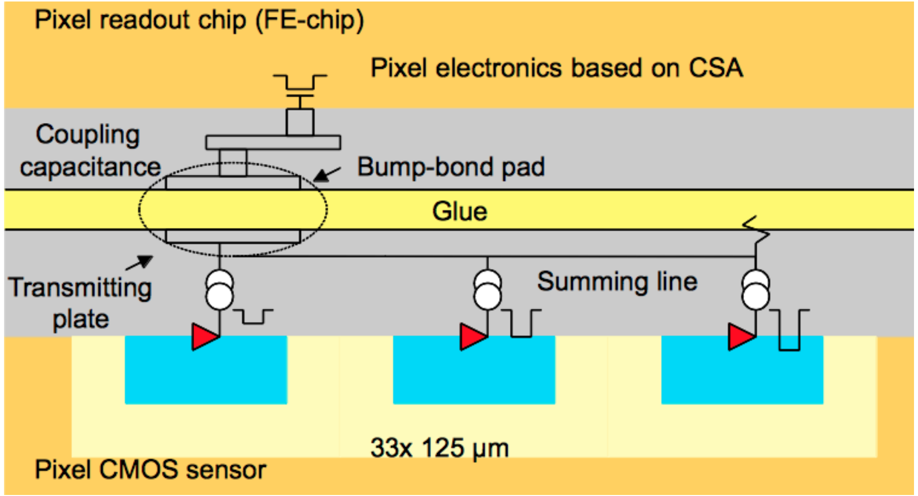
In CCPD pixel

Depletion (d)= 20um
Q = d*80e/um = 1600e
Noise = 120e -> 14mV
Threshold = 600e -> 70mV

In FEI4 pixel

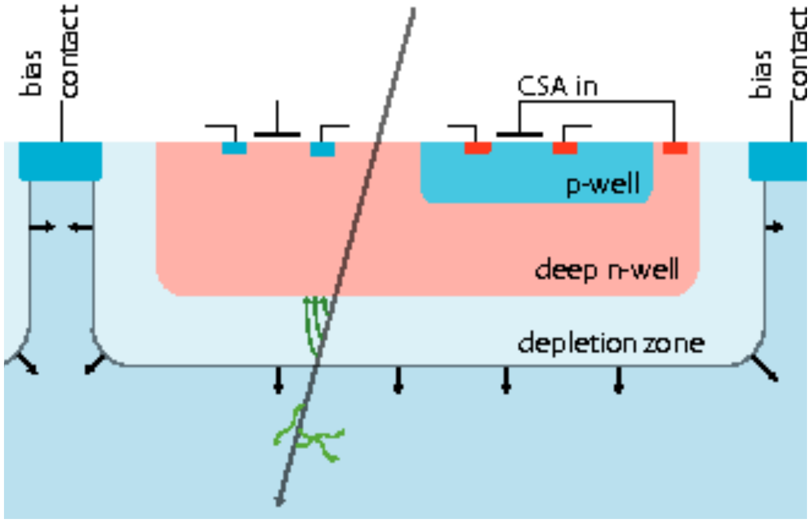
dQ = C dV/dt
For C = 4.5fF, dV=300 mV
dQ = 8500e

dV is programmable by DAC

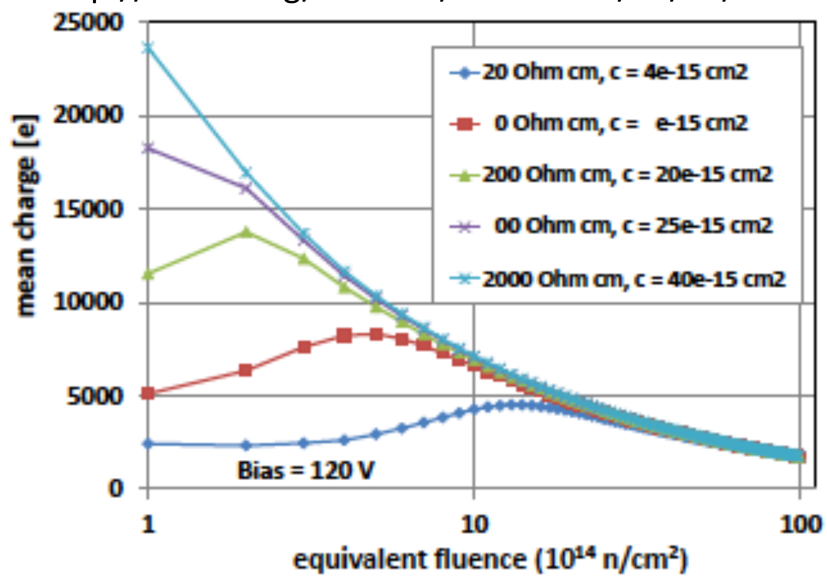


The CCPDv4/v5/v6 Concepts

- In standard AMS HV-CMOS process, High Voltage is applied from top-side , up to 120V
- Resistivity is 20Ohmcm, but higher resistivity are available with AMS fab (H35DEMO, aH18)
- Experimental data show increase in depletion area with fluence



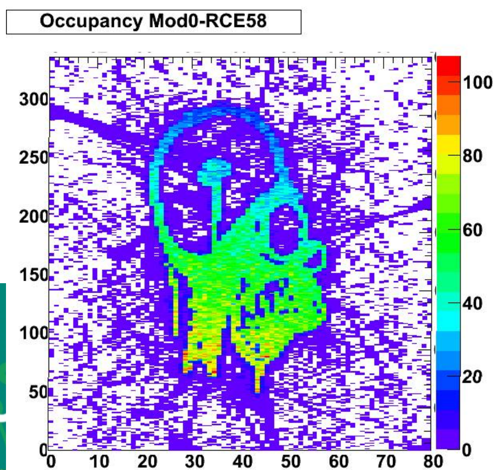
http://dx.doi.org/10.1088/1748-0221/11/04/P04007

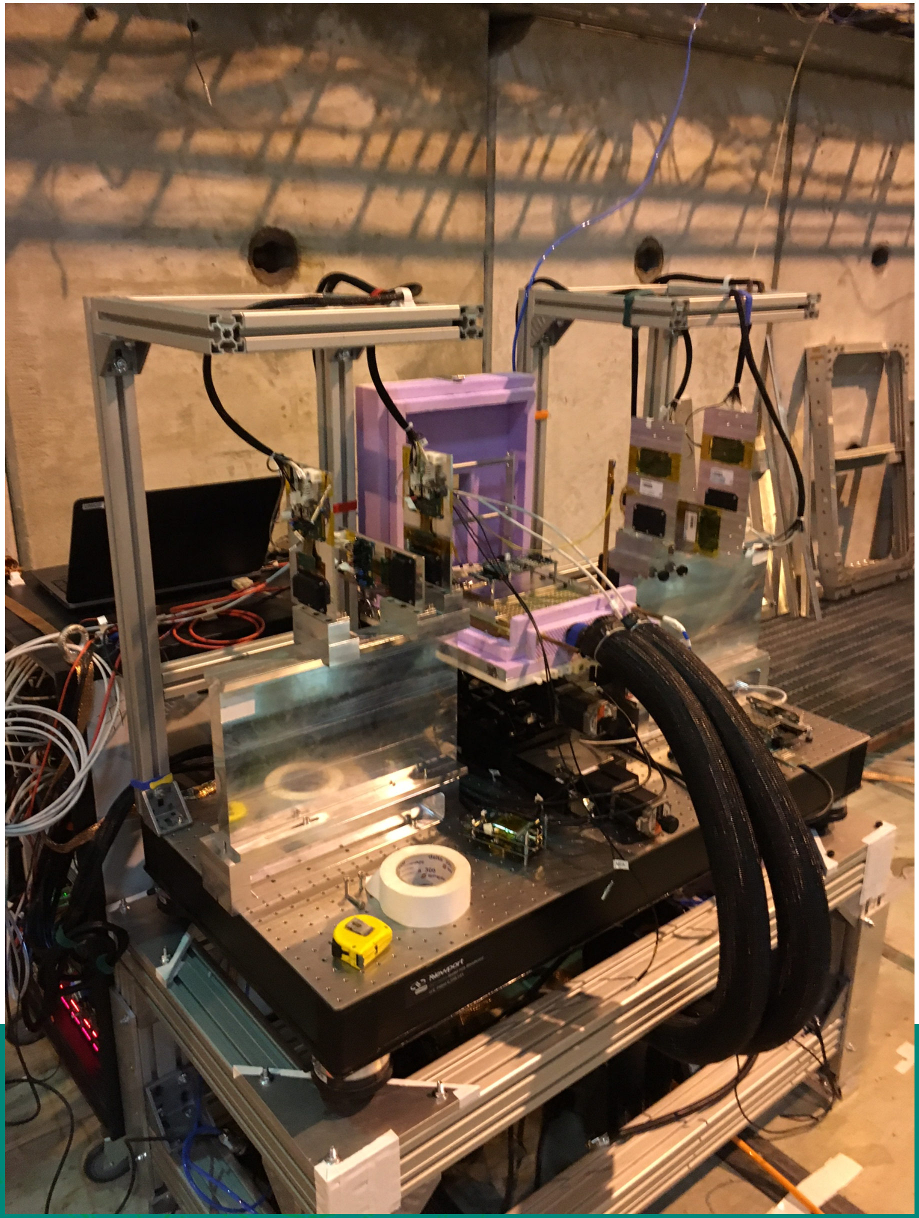


The FEI4 Telescope at SPS

- Telescope:
- - 6 planes of silicon pixel sensors
- - ~27000 pixels (250x50µm,) per plane
- - Spatial resolution: 12 x 8µm,
- - Trigger rate: 6 - 18kHz
- - Custom Data Acquisition System
- - Custom C++ Analysis framework
- Customizable ROI !
- Services:
  - Low and High Voltage
  - Power supplies
  - Cooling and environmental monitoring
  - Scanning stages
  - Remote control and monitoring

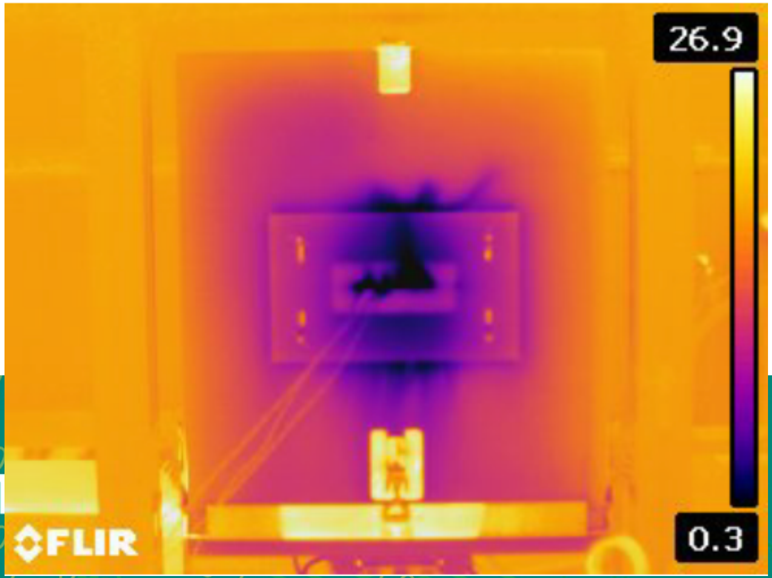
https://arxiv.org/abs/1603.07776





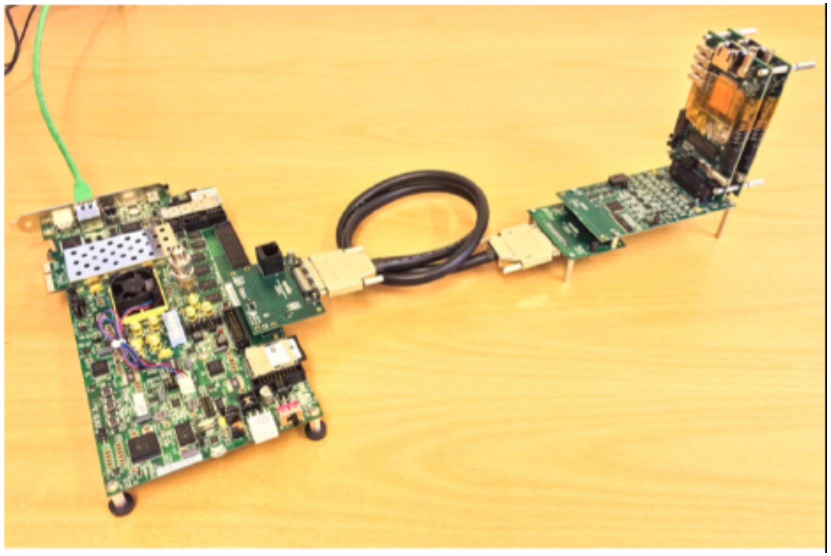
The FEI4 Telescope at SPS (cooling)

Sensor	Copper tape	No copper tape	No sensor
Baseplate [°C]	-46.10	-37.00	-37.08
Box air [°C]	-28.71	-28.00	-28.20
FEI4 [°C]	-26.93	-21.00	N/A
HVCMOS [°C]	-26.60	-21.00	N/A



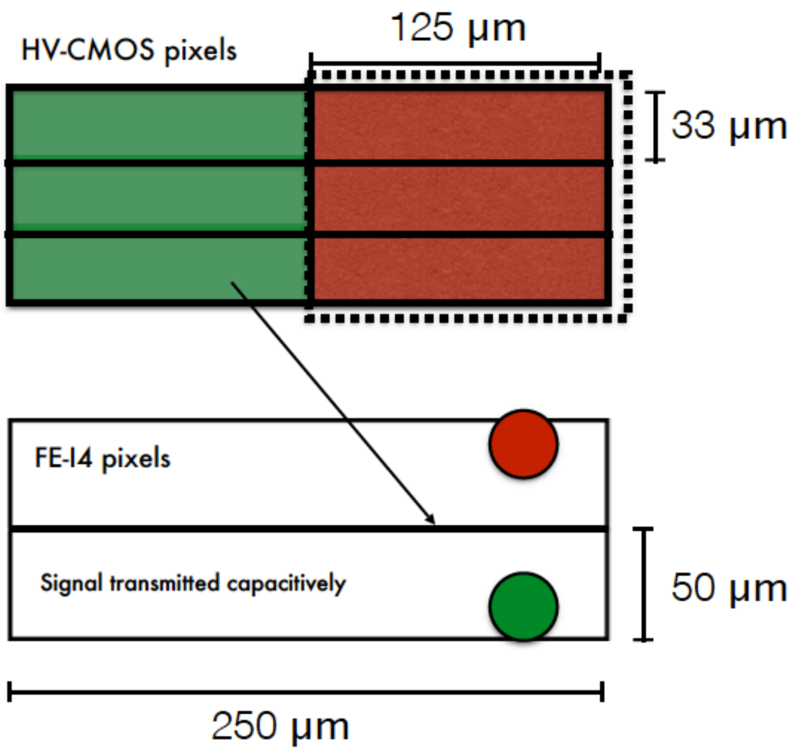
CCPDv4 AMS vs IBM Foundry

- AMS is transferring their HVCMOS process to their in-house fab in Graz
  - Allow for more customization of the process
    - Quad wells
    - Hi resistivity substrate
- The new process, labelled aH18, must be qualified with regard to the Chip produced by IBM

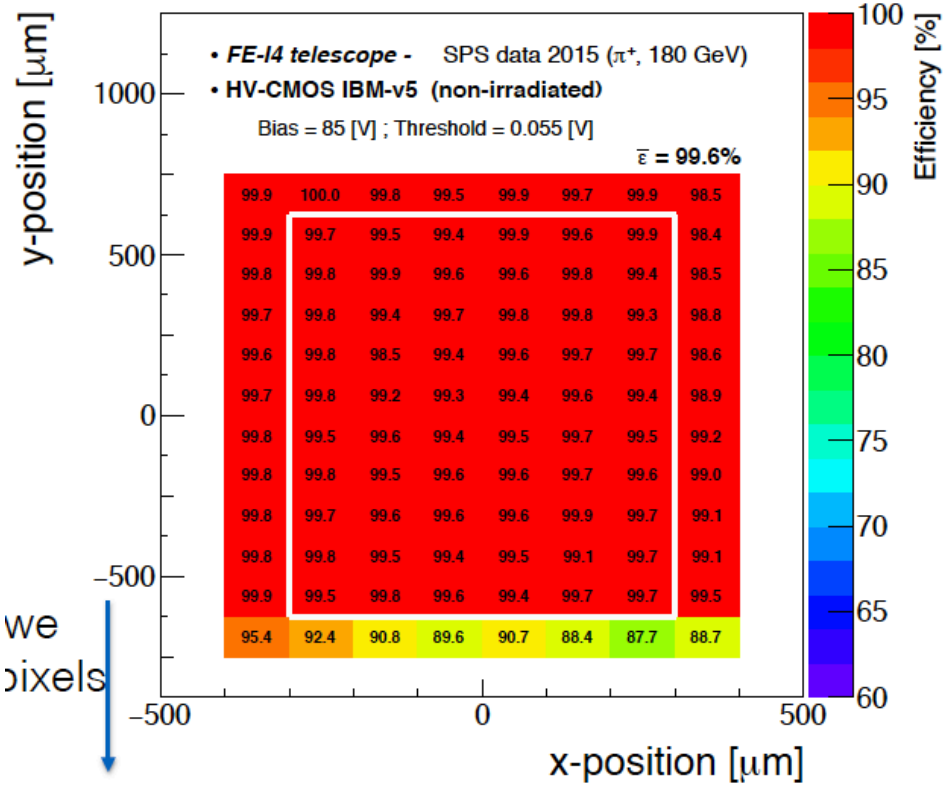


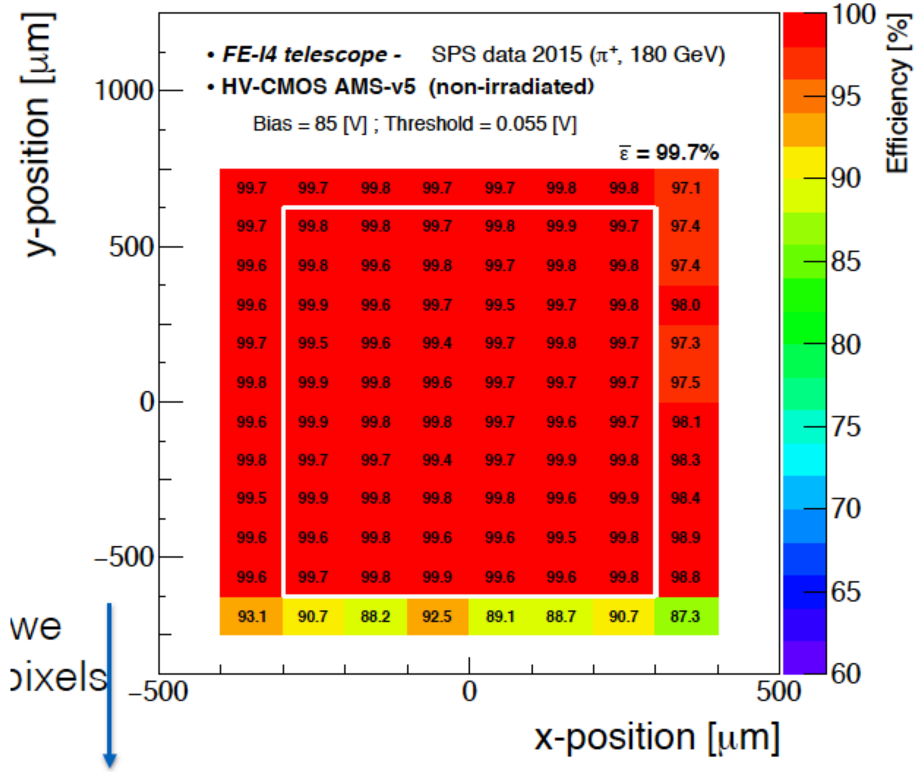
HV-CMOS pixels connection to FE-I4

- HV-CMOS pixel size: 125 x 33 μm
- FE-I4 pixel size: 250x 50 μm
- 3 HV-CMOS sub-pixels connected to 1 FE-I4 pixel
- In reconstruction we define a virtual pixel of 100 x 125 μm containing 3 HV-CMOS sub-pixels

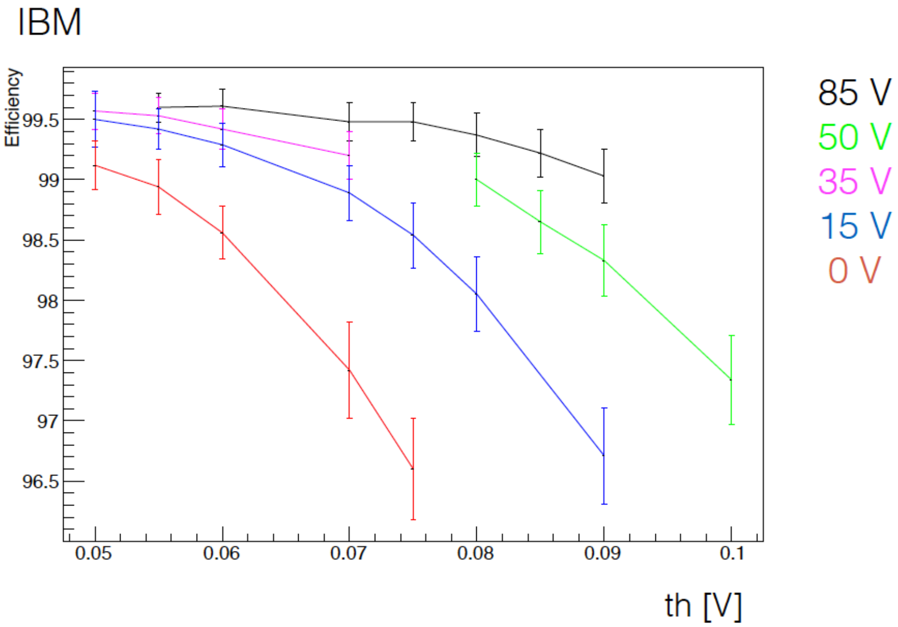


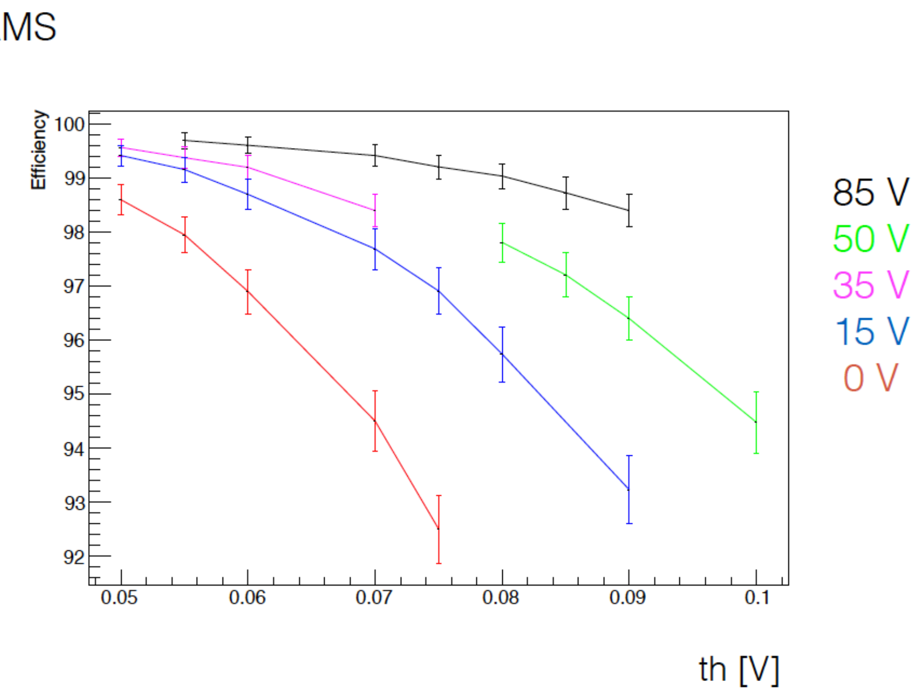
CCPDv4 AMS vs IBM Foundry (Global efficiency)



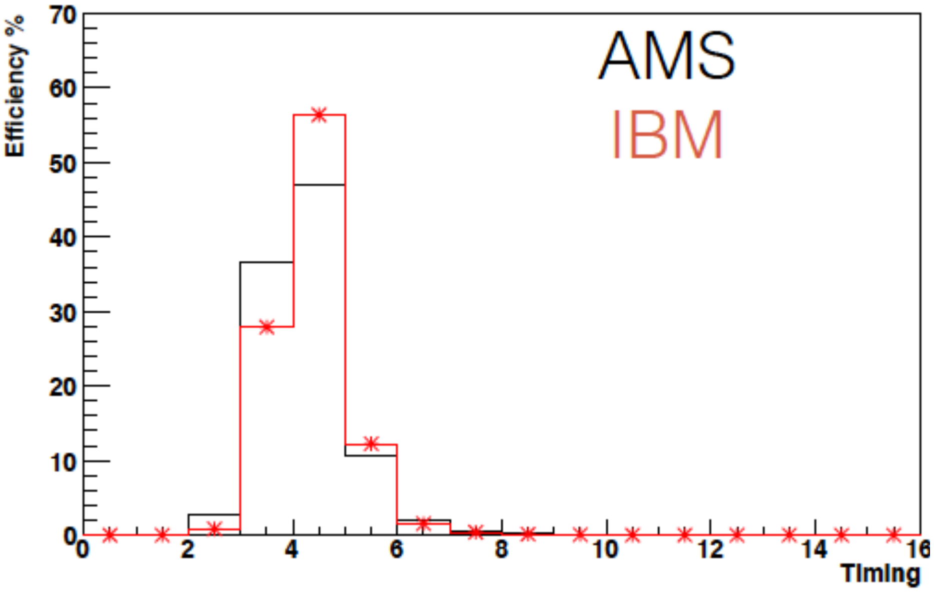


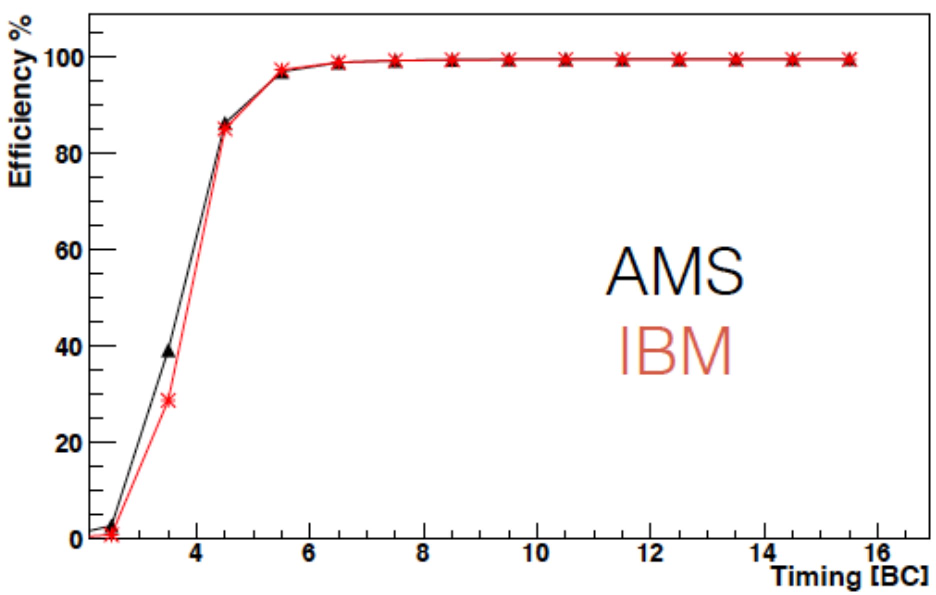
CCPDv4 AMS vs IBM Foundry (Threshold scans)





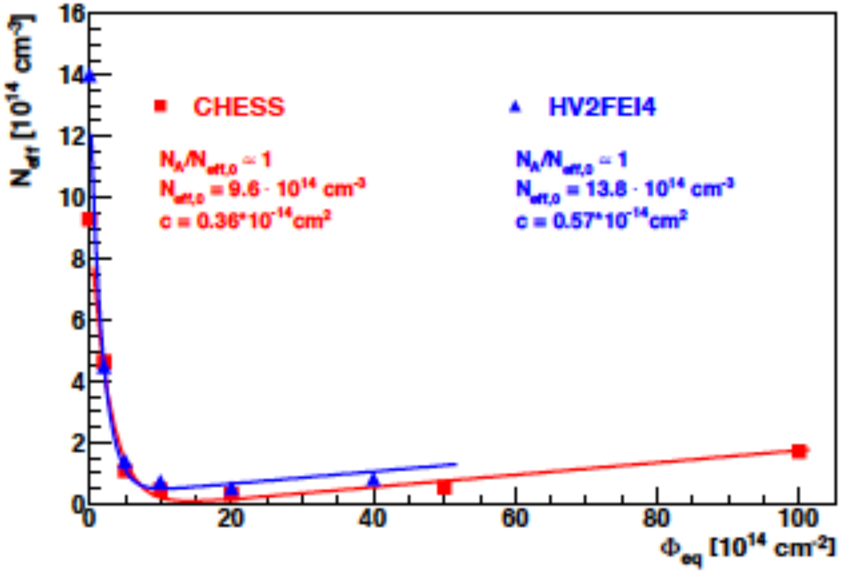
CCPDv4 AMS vs IBM Foundry (Timing performances)





Irradiated CCPDv4 Characterization

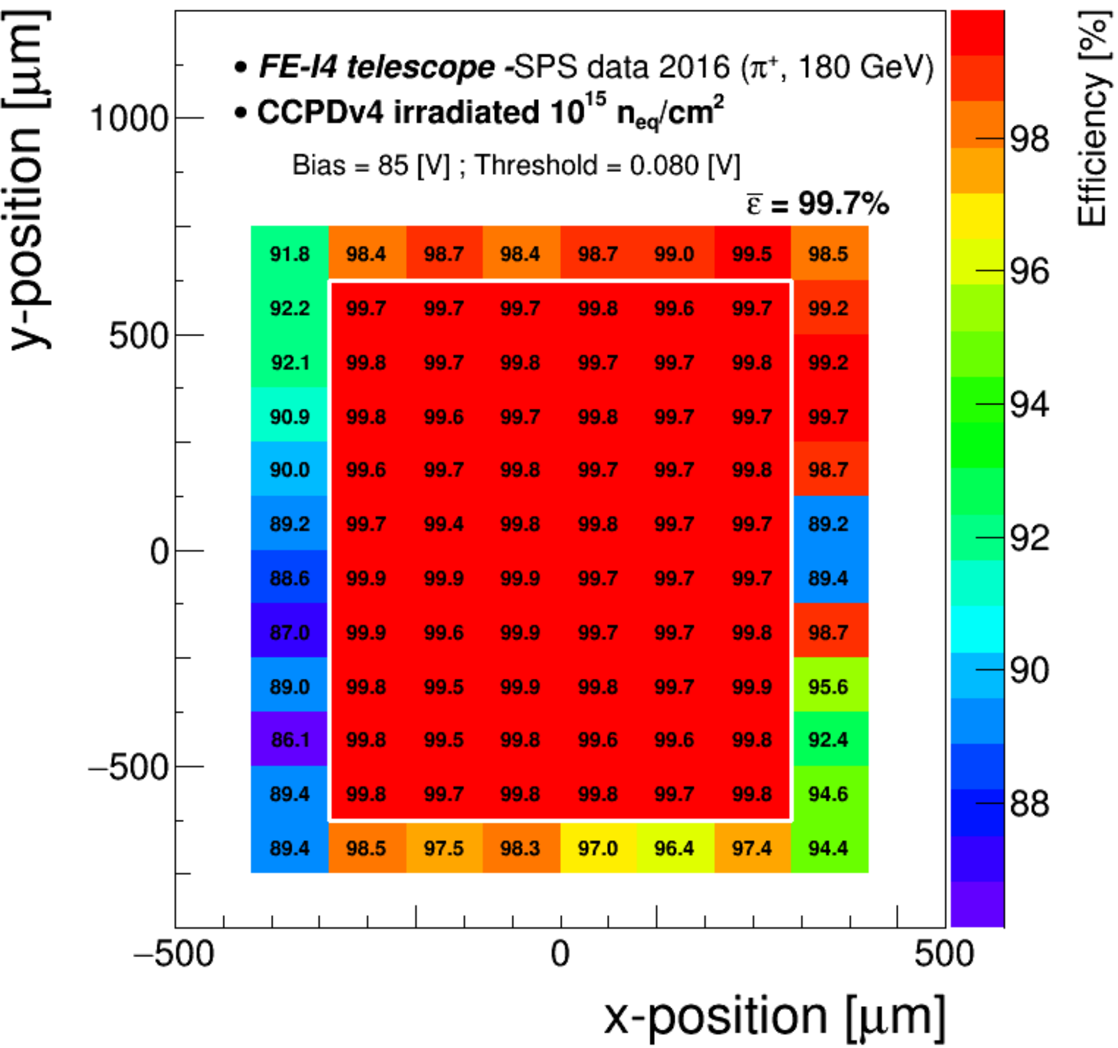
- Focus of the following study is on two CCPDv4 irradiated samples
  - **Caribou04** 1e15n_{eq}/cm^2
  - **Caribou06** 5e15n_{eq}/cm^2
- Sample cooled down to -20 C (die temperature)
- Leakage current <1uA
- Bias voltage up to 85V

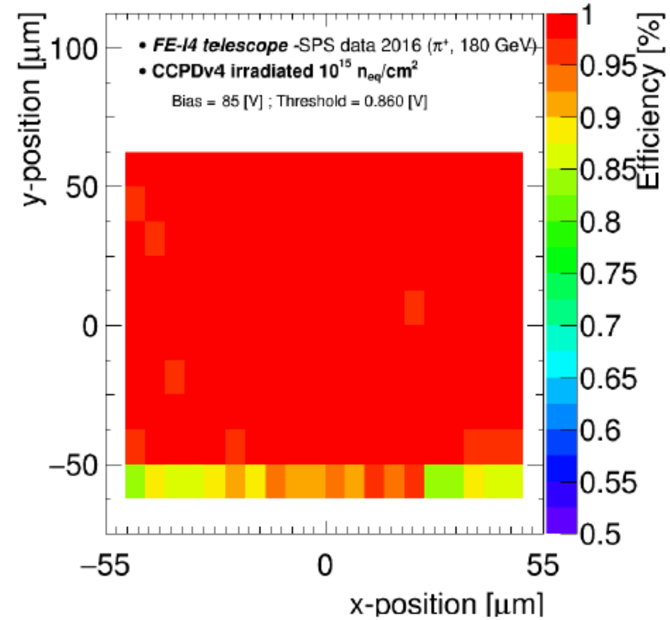


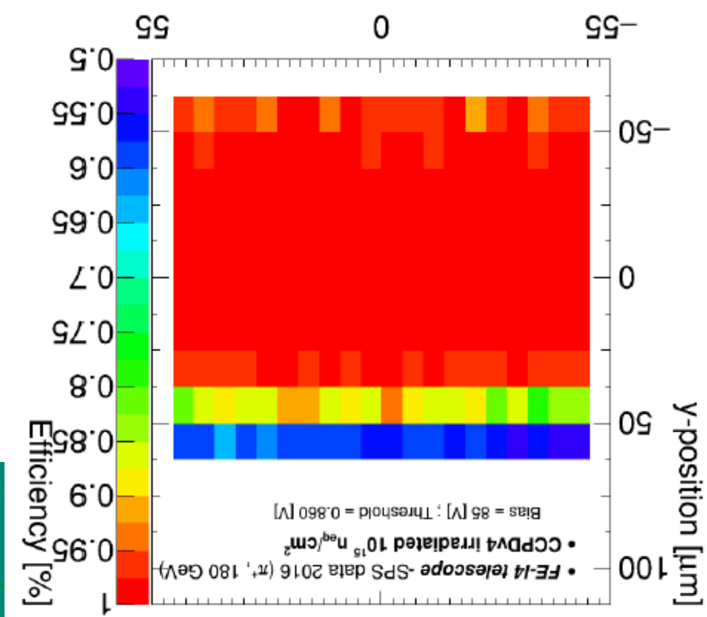
http://dx.doi.org/10.1088/1748-0221/11/04/P04007

Non-irradiated sensors results published in JINST http://arxiv.org/abs/1603.07798

1e15 Irradiated CCPDv4 (efficiency)







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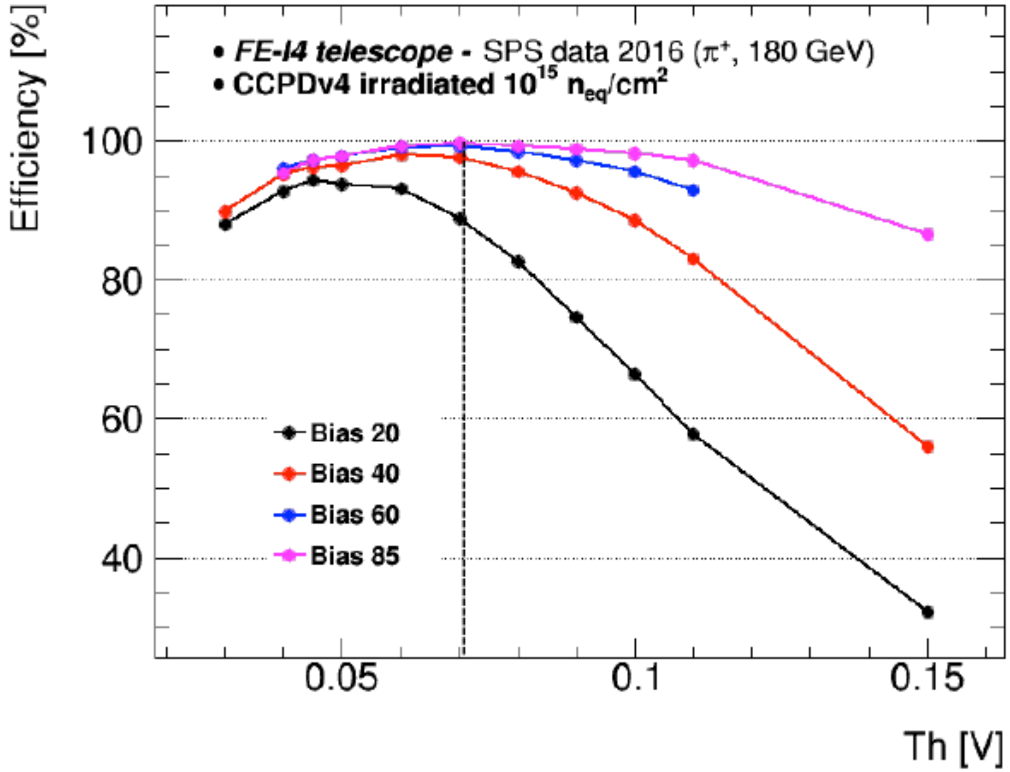
1e15 Irradiated CCPDv4 (Threshold Scans)

- Pixel discriminator threshold scan for different bias voltages
- Effective Threshold= Threshold-Baseline (0.8 V)
- At low threshold, a lot of pixels become noiser and need to be masked
- At high threshold the small signal are killed, especially for lower HV → trapping



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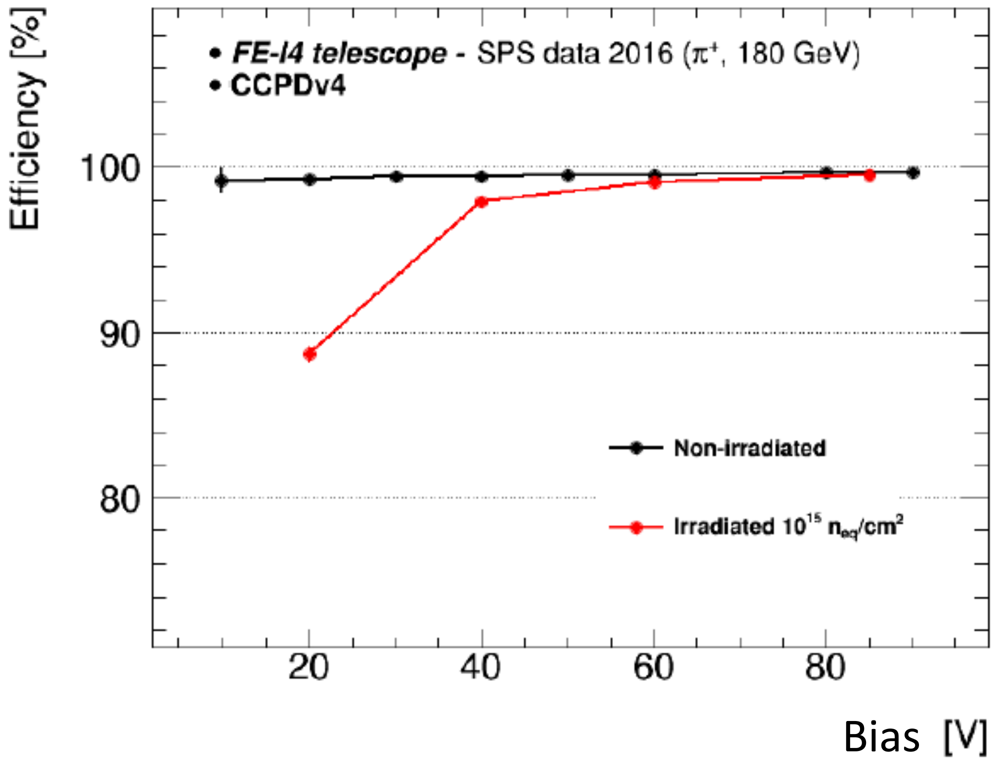
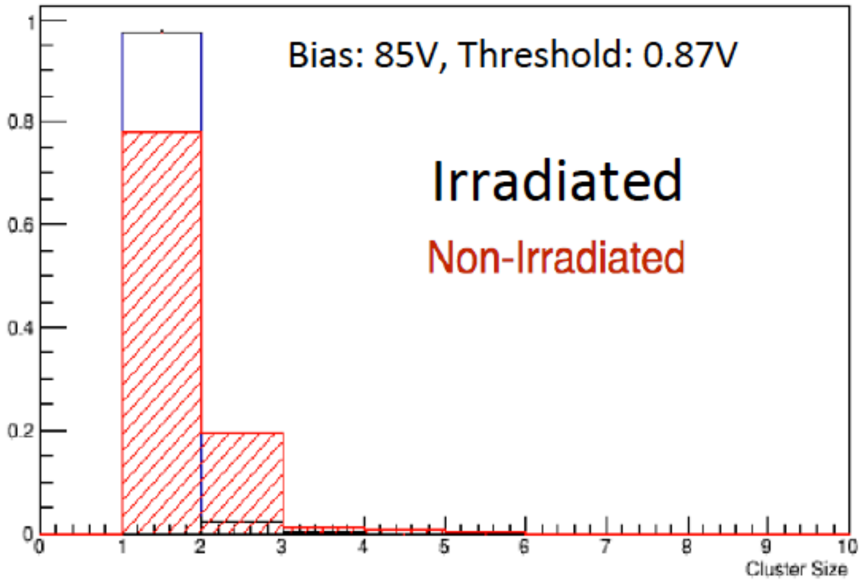
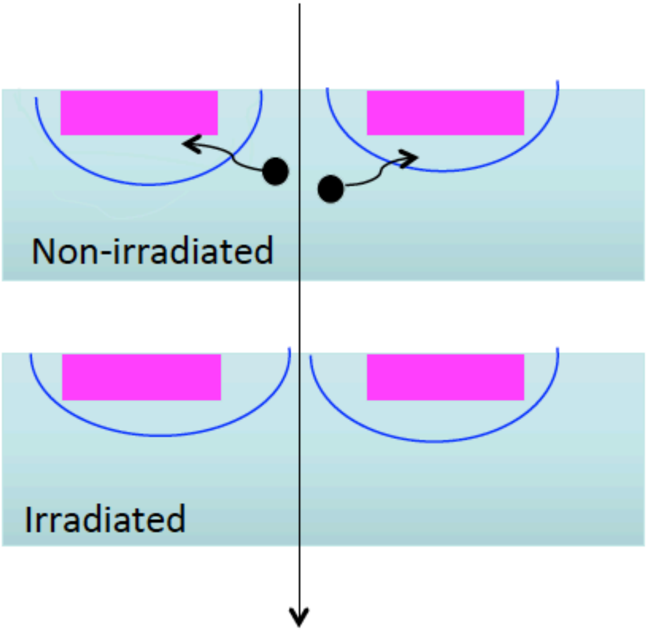


1e15 Irradiated CCPDv4 (Cluster size)

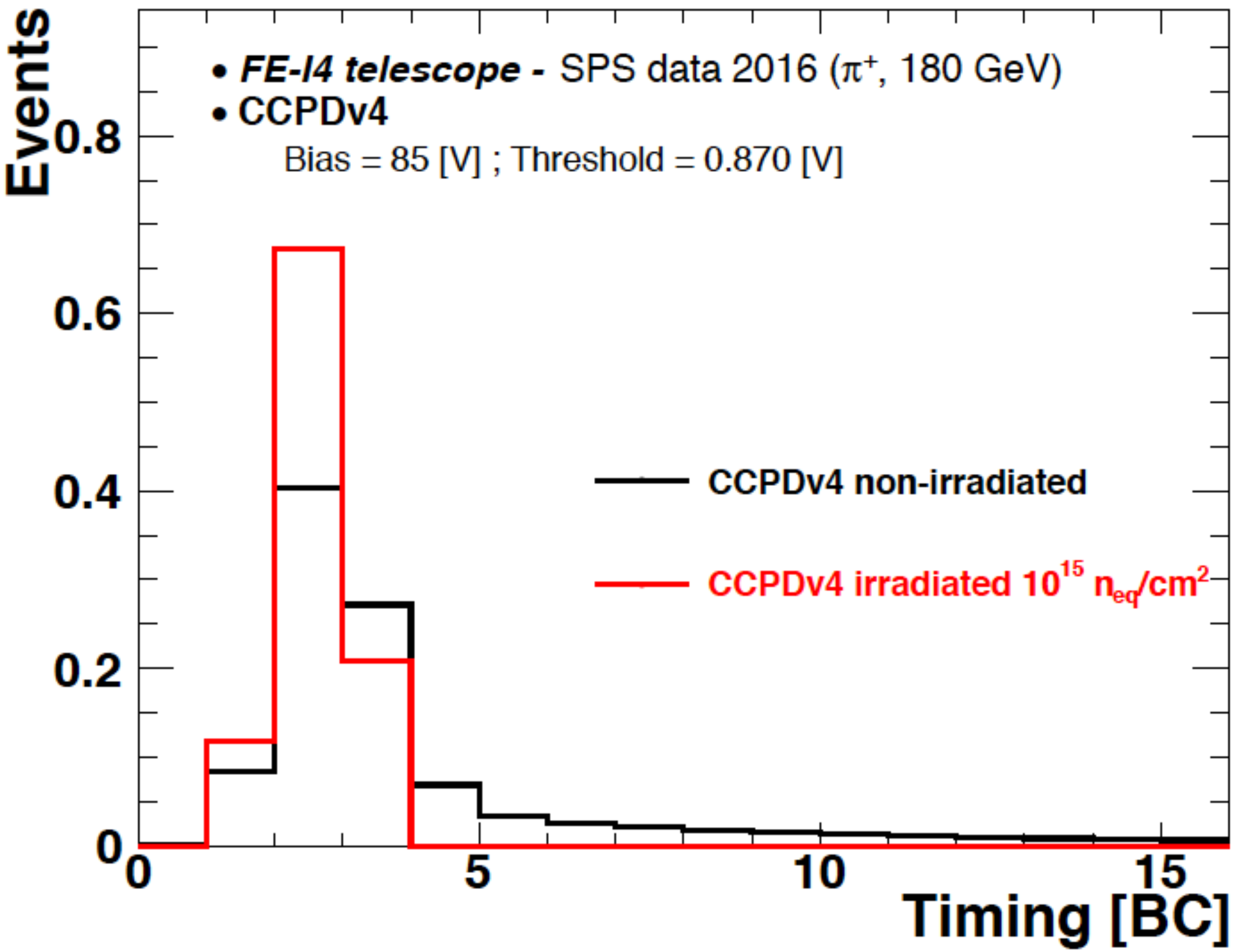
- Cluster size comparison
- Most pixels have cluster size of 1
- CS > 1 is strongly reduced compared with the non-irradiated sample
  → Acceptor removal mechanism



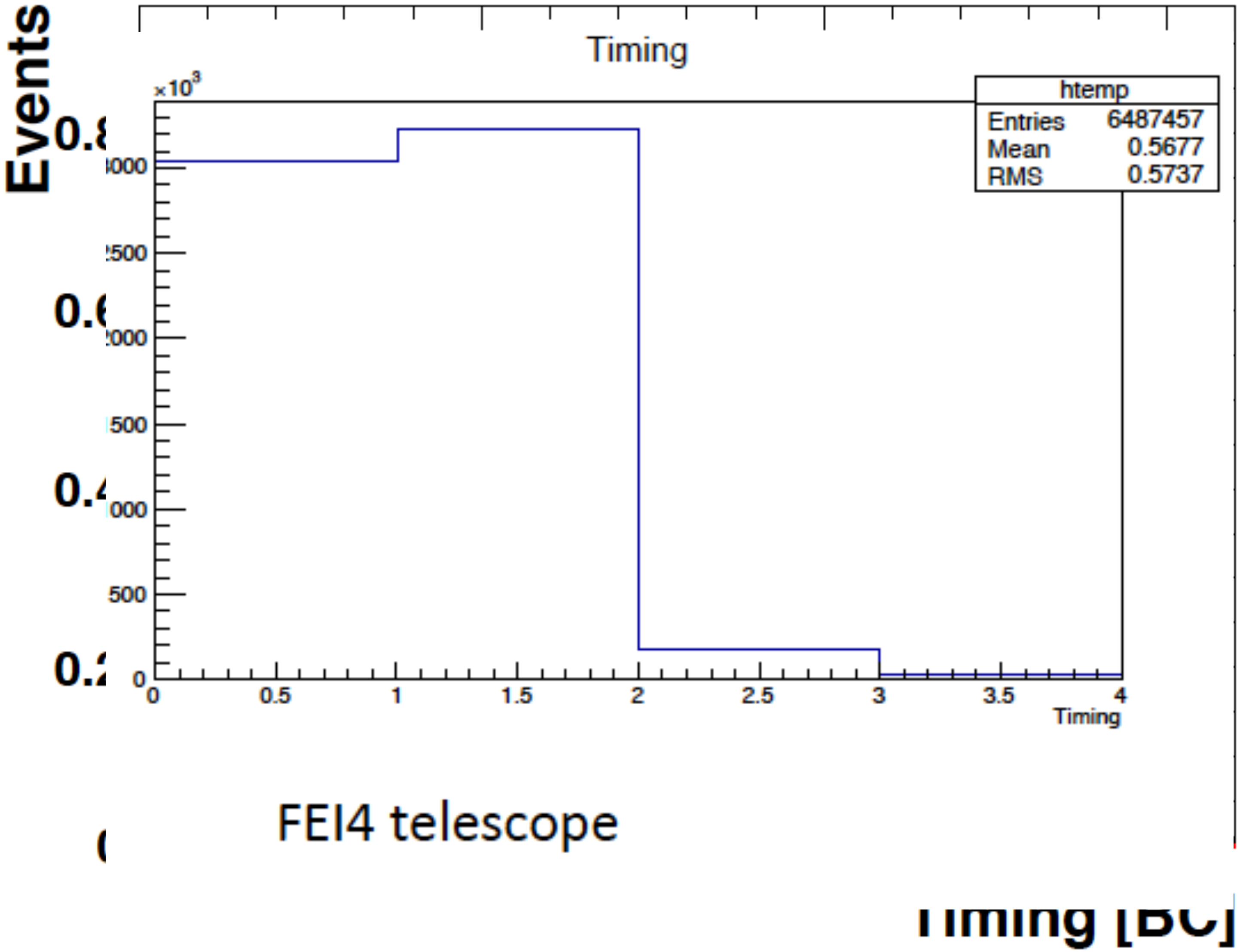


After irradiation, the depletion zone expanded → lower chance of diffusion

1e15 Irradiated CCPDv4 (Cluster size)



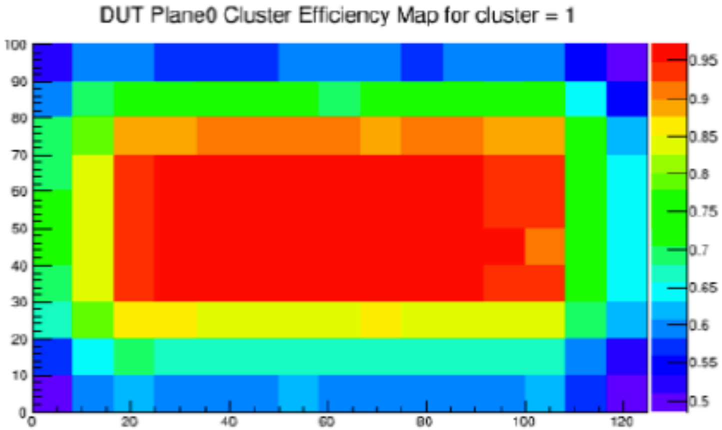
1e15 Irradiated CCPDv4 (Cluster size)



1e15 Irradiated CCPDv4 (In pixel efficiency)

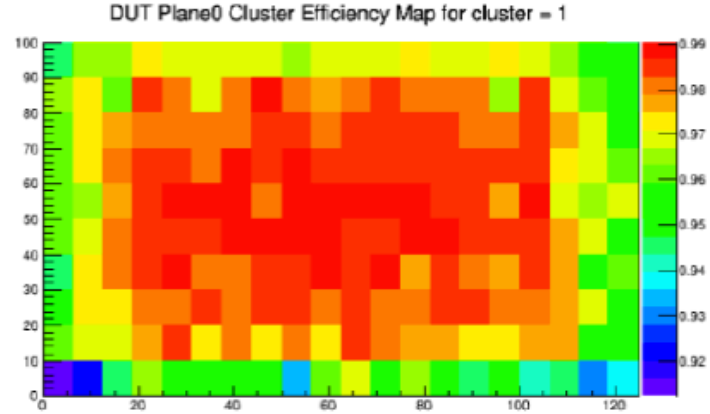
C.S.=1

Non-Irradiated



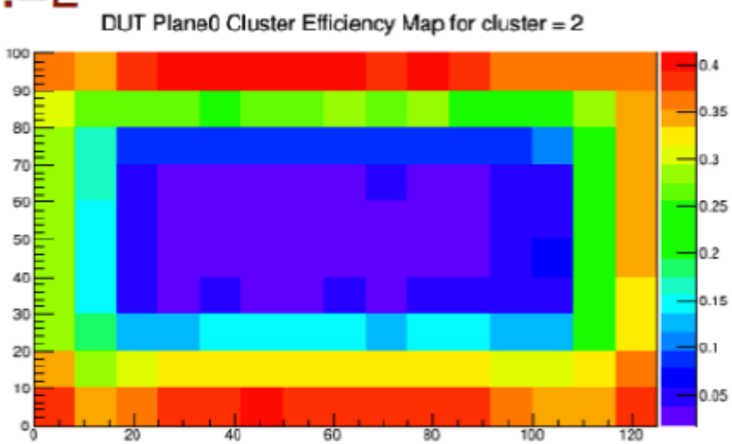
C.S.=1

Irradiated



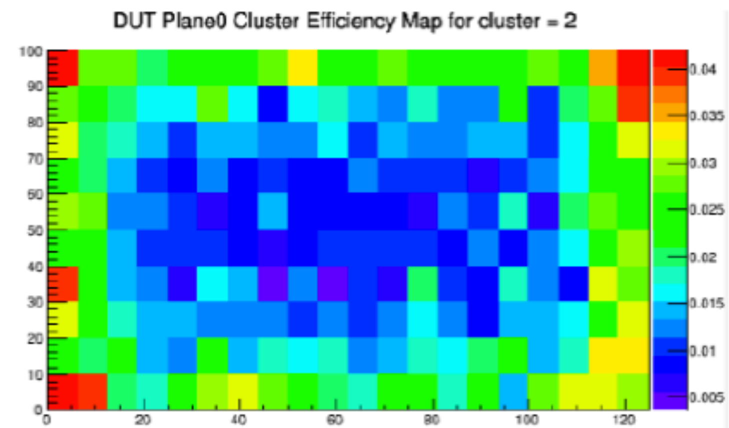
C.S.=2

Non-Irradiated



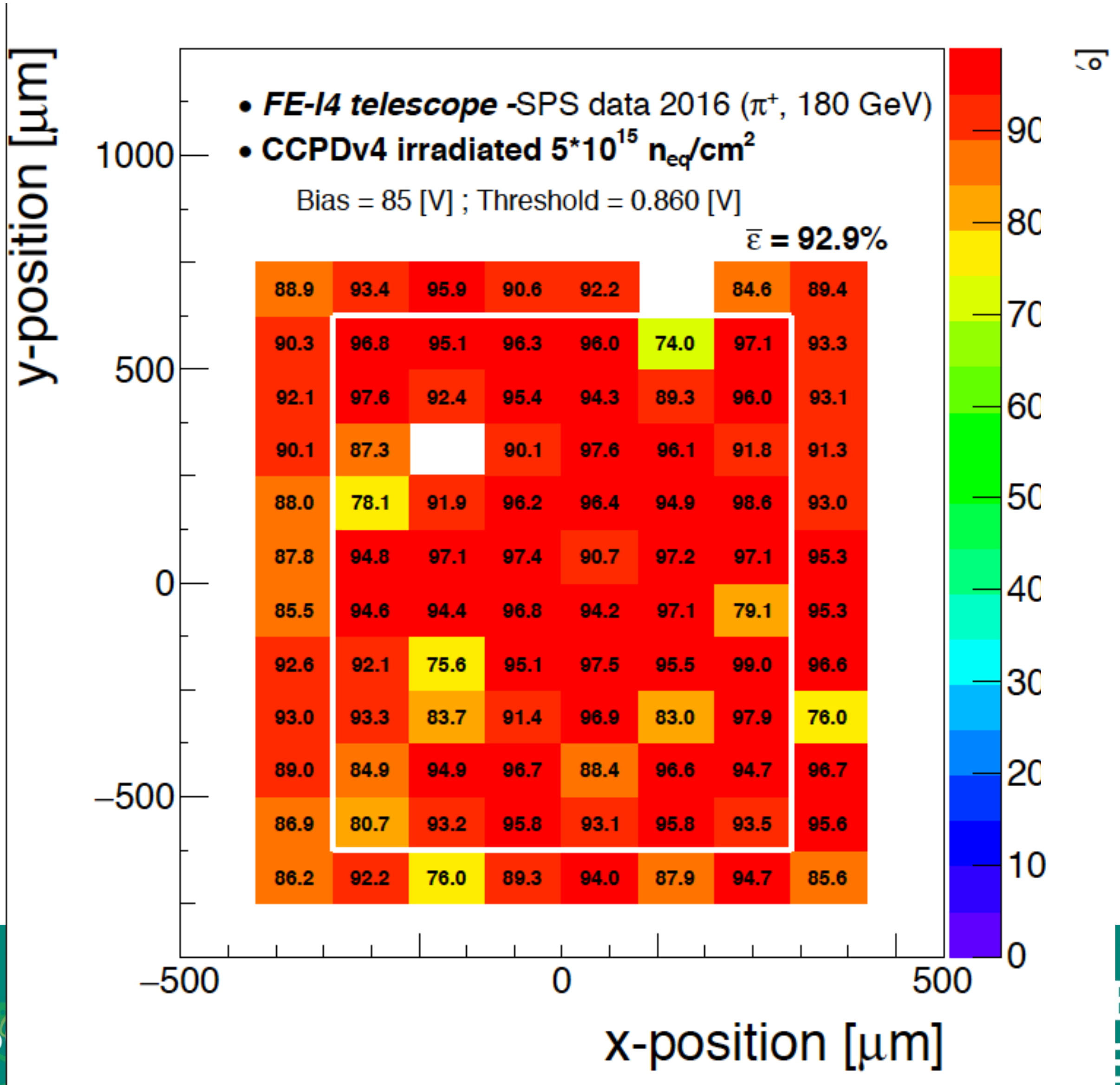
C.S.=2

Irradiated

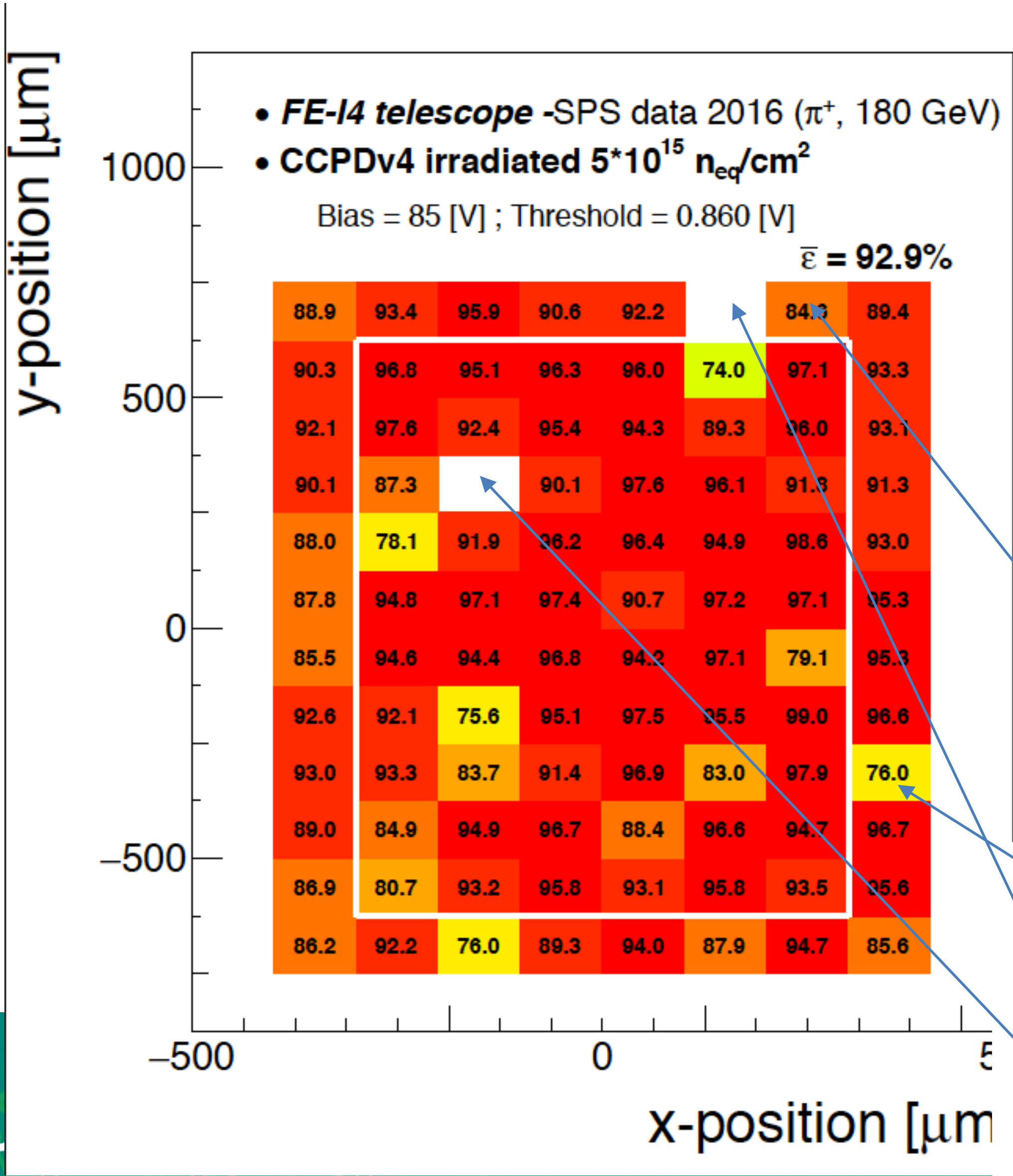


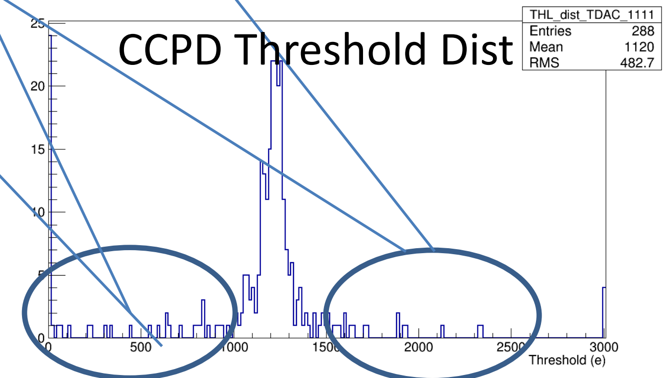
5E15 IRRADIATED CCPDV4

5e15 Irradiated CCPDv4 (Efficiency)

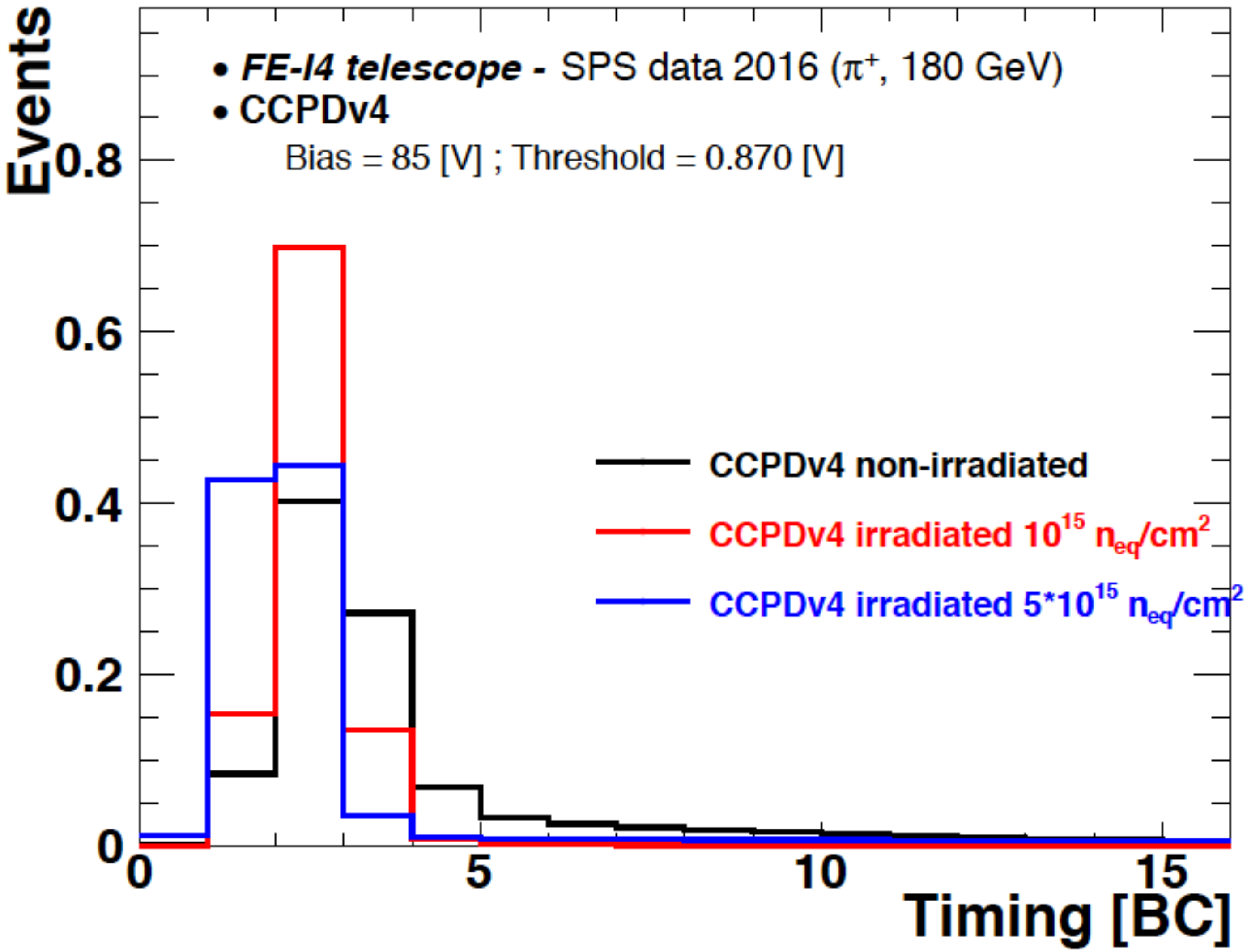


5e15 Irradiated CCPDv4 (Efficiency)





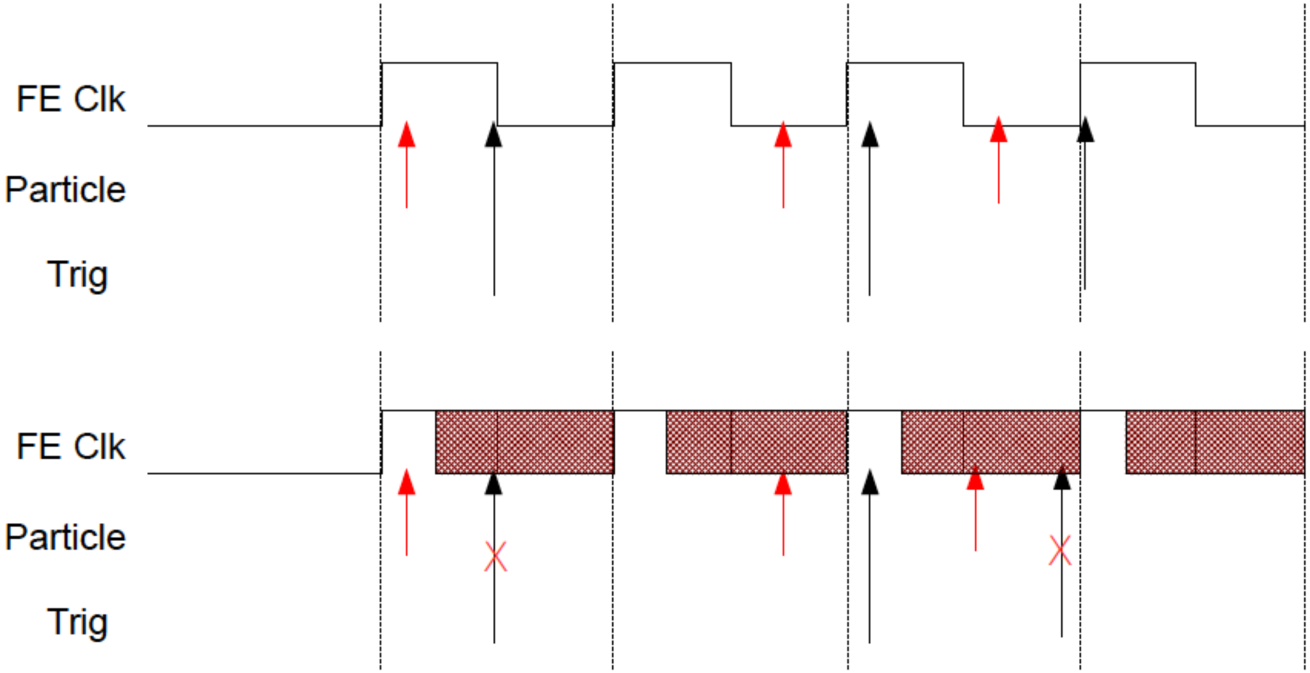
5e15 Irradiated CCPDv4 (Timing)



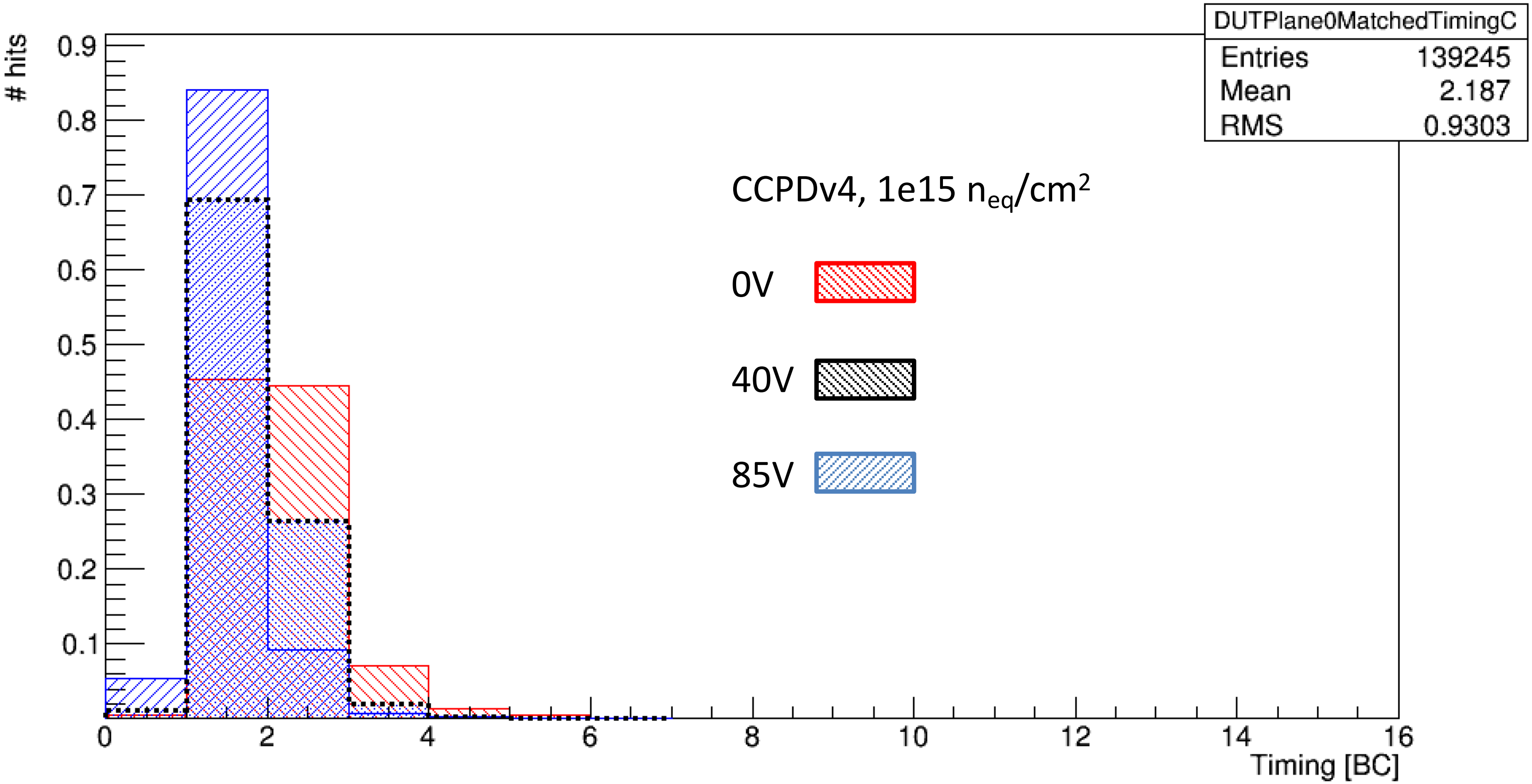
Telescope Jitter

- Idea: Introduce artificial dead time based on FE clock phase

LHC, CLIC beam is synchronous to the clock, while SPS beam is Poissonian. To operate close to the real condition, we take only particles in synch with the clock



CCPDv4 Timing distribution, jitter corrected



Conclusion

- **CCPD represent a possible cost reduction for larger radius of the ITk**
  - Large scale production
  - Single-sided process
  - Possibility to deal with small signal with CMOS electronics
  - Good test vehicle for possible monolithic integration

- **CCPD show good performances in terms of efficiency up to 5e15n_{eq}/cm^2**
  - Timing before irradiation still to be improved to have 99% in 1 B.C.
  - After irradiation , very close to meeting specifications (95% in 1 B.C.)
  - Improvement of the Telescope Trigger jitter should fix this
- Next steps : H35DEMO (2x2cm), multiple substrate resisitivities, BS Biasing etc…