Challenges for the design of radiation hard ASICs

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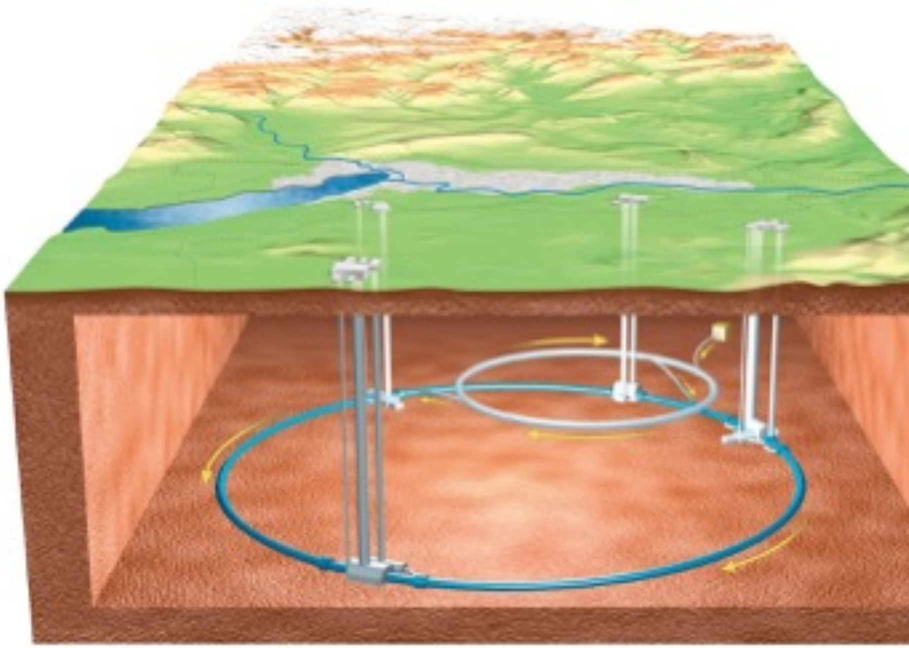
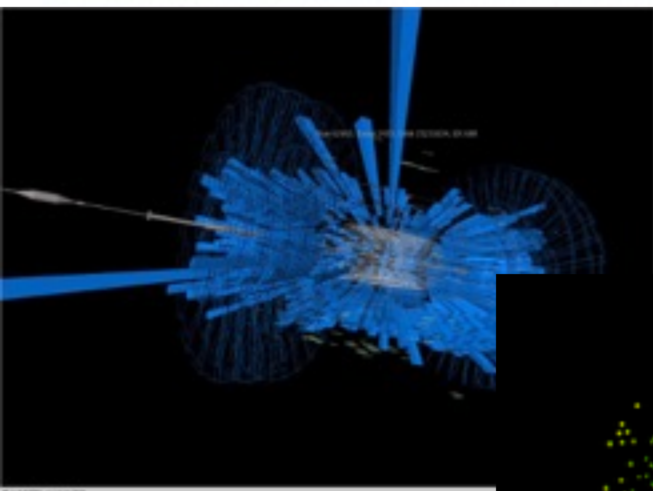
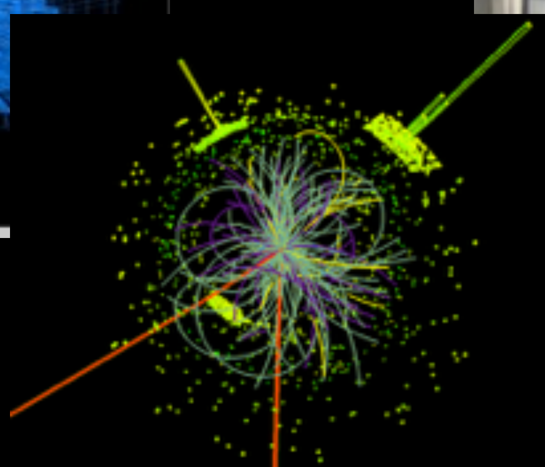
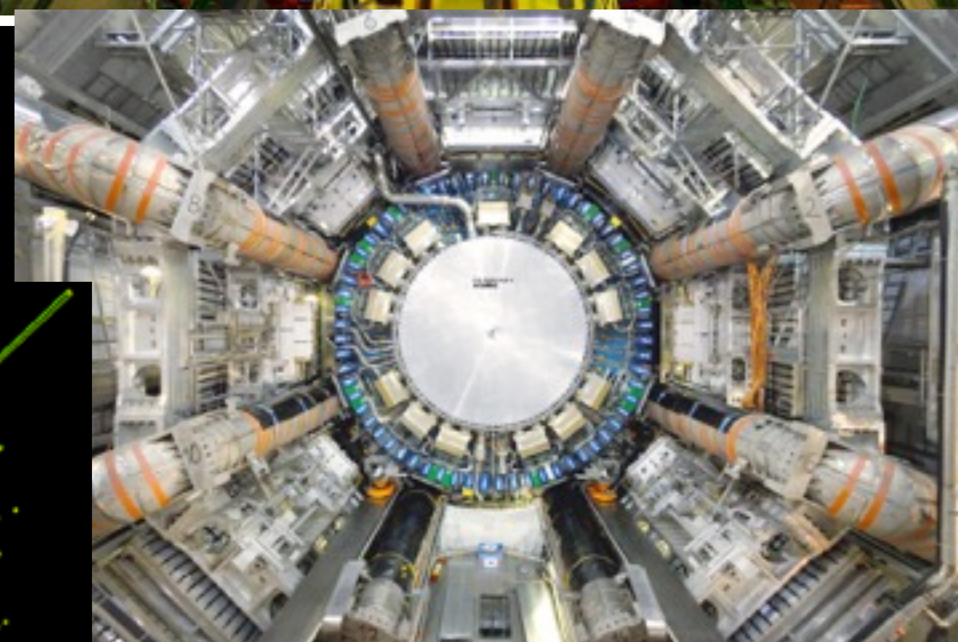
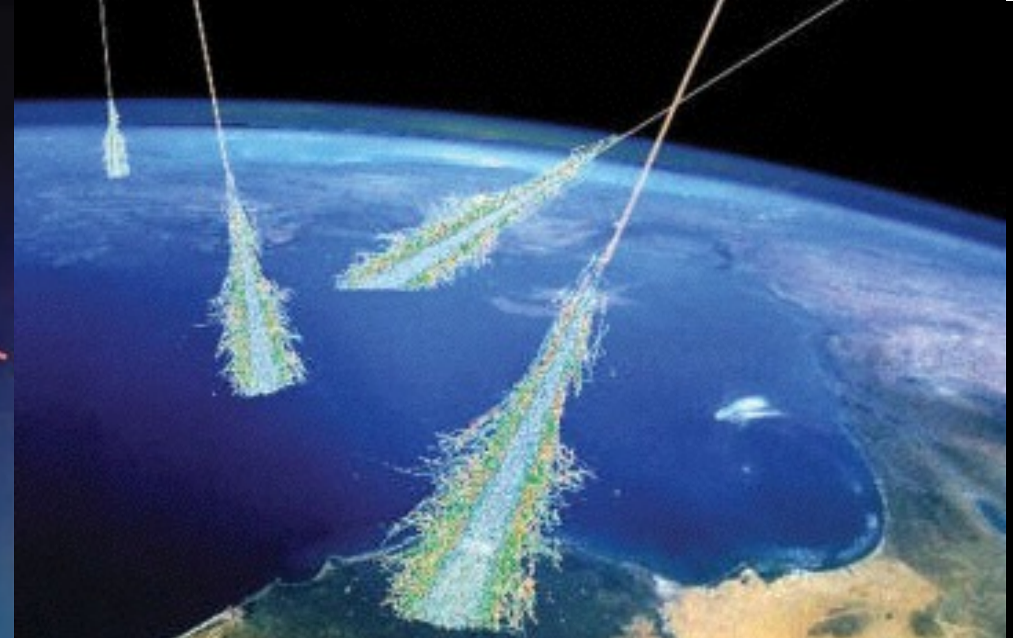




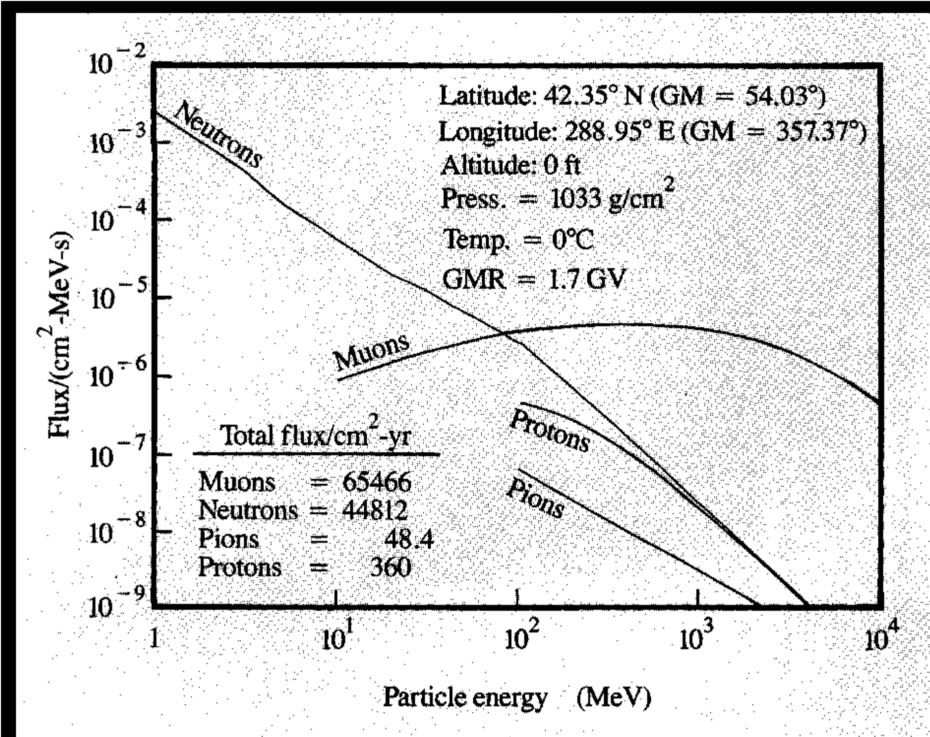






On October 7, 2008, an Airbus A330-303 operated by Qantas Airways was en route from Perth to Singapore. At 37,000 feet, one of the plane's three air data inertial reference units had a failure, causing incorrect data to be sent to the plane's flight control systems. This caused the plane to suddenly and severely pitch down, throwing unrestrained occupants to the plane's ceiling. At least 110 of the 303 passengers and 9 of the 12 crew members were injured. The injuries of 12 of the occupants were serious, and another 39 occupants required treatment at a hospital. An SEU was the only potential cause for the malfunctions not ruled out. All potential causes were found to be "unlikely," or "very unlikely," except for an SEU. However, the Australian Transport Safety Board (ATSB) found it had "insufficient evidence to estimate the likelihood" that an SEU was the cause. –ATSB Transport Safety Report Aviation Occurance Investigation AO-2008-070 Final

Terrestrial



J.Ziegler, IBM J.Res.Develop., Vol.40, Jan1996

IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 43, NO. 6, DECEMBER 1996

Single Event Upset at Ground Level

Eugene Normand, *Member, IEEE*
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Abstract
Ground level upsets have been observed in computer systems containing large amounts of random access memory (RAM). Atmospheric neutrons are most likely the major cause of the upsets based on measured data using the Weapons Neutron Research (WNR) neutron beam.

a sophisticated ground-based detector system made at 100, 5000 and 10,000 feet above sea level indicate that the 10-100 MeV flux falls off approximately linearly with altitude [8]. Very few measurements of the neutron spectrum at ground level have been made, especially over the entire energy range. One set of the most recent terrestrial spectral measurements,

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Single Event Upsets in Implantable Cardioverter Defibrillators

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[2] Boeing Defense and Space Group, Seattle, WA 98124-2499 USA

Nuclear power

Military

Origin of radiation effects

- ✓ Very simplified summary
- ✓ Effects traceable to energy loss from incoming radiation in the devices

	Particles	Radiation effect
Ionizing energy loss		
Small charge density	All (photons, electrons, protons and other charged hadrons, Heavy Ions, …)	Total Ionizing Dose (TID)
Large charge density	Heavy Ions (maybe from hadron nuclear interaction in Si)	Single Event Effects
Non ionizing energy loss	Hadrons (neutrons, protons, ….)	Displacement damage

Radiation effects in CMOS

Cumulative effects

Total Ionizing Dose (TID)

TID measured in Gy (rad)

Single Event Effects (SEE)

Permanent SEEs

SEL

SEGR, SEB

Static SEEs

SEU, SEFI

Digital ICs

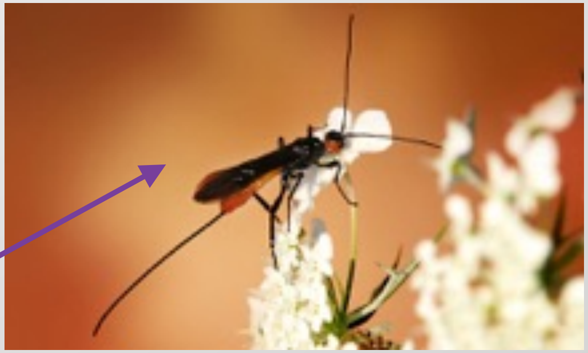
Transient SEEs

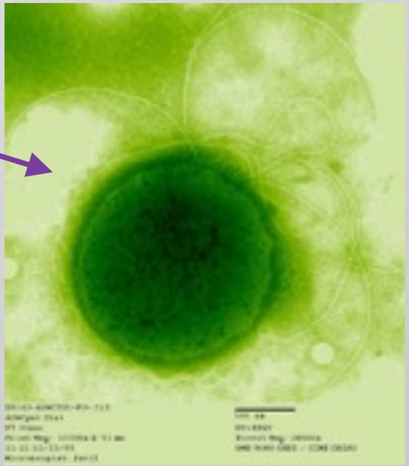
Combinational logic
Operational amplifiers

SEEs are stochastic, sensitivity is measured in cross-section
Environment characterized by flux/fluence (particles/cm^2 s)

Lethal radiation doses (Gray)

Organism	Lethal dose	LD_{50}	LD_{100}	Class/Kingdom
Dog		3.5 ($LD_{50/30\ days}$)[7]		Mammals
Human	4-10[8]	4.5[9]	10[10]	Mammals
Rat		7.5		Mammals
Mouse	4.5-12	8.6-9		Mammals
Rabbit		8 ($LD_{50/30\ days}$)[7]		Mammals
Tortoise		15 ($LD_{50/30\ days}$)[7]		Reptile
Goldfish		20 ($LD_{50/30\ days}$)[7]		Fish
Escherichia coli	60		60	Bacteria
German cockroach		64[8]		Insects
Shellfish		200 ($LD_{50/30\ days}$)[7]		-
Fruit fly	640[8]			Insects
*C. elegans**		160-200 [11]	> 500-800[12][13]	Nematode
Amoeba		1,000 ($LD_{50/30\ days}$)[7]		-
Braconidae	1,800[8]			Insects
Milnesium tardigradum	5,000[14]			Eutardigrade
Deinococcus radiodurans	15,000[8]			Bacteria
Thermococcus gammatolerans	30,000[8]			Archaea



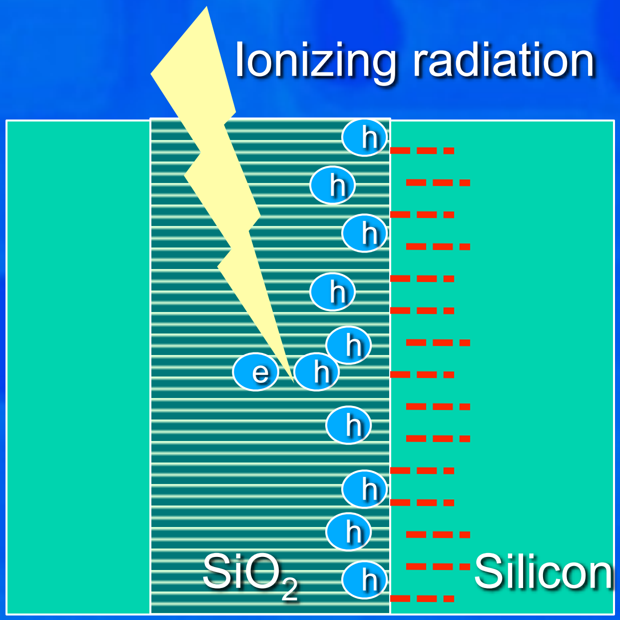


can be killed in 20minutes in our X-ray facility

Typical doses for electronics in different applications:
- Satellites: 1000 Gray
- Deep Space missions: 10 kGray
- HEP (LHC): >100 kGray
- HEP (SLHC): >1 MGray

TID: trapped holes in SiO_2

- ✓ Total Ionizing Dose effects are traceable to ionization from radiation in SiO_2

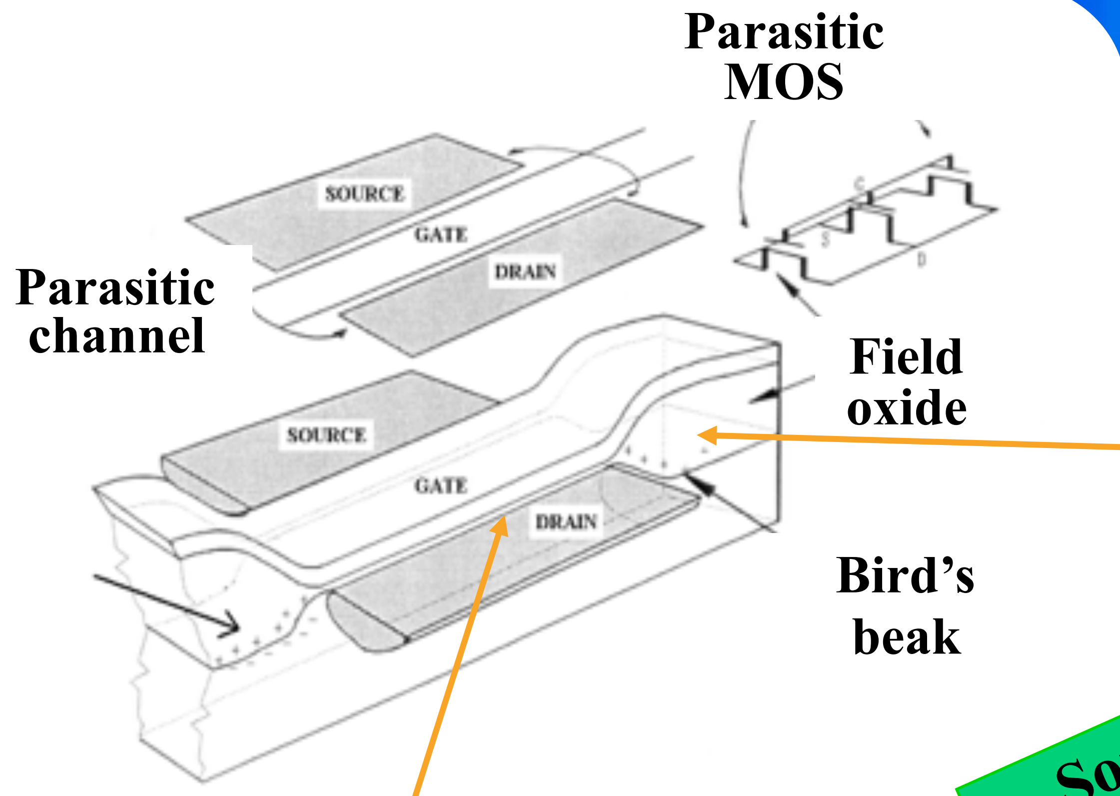


Ionization produces e-h pairs

- Holes have low mobility in the oxide, and can be trapped
- Migration of holes (and other positive ions) to the interface can activate trapping centers

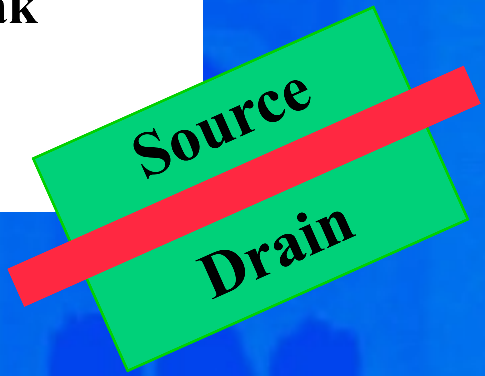
Charge accumulates in the oxide or at its interface with Silicon

TID effects in CMOS



2. Effects in the thick lateral isolation oxide (STI) between source and drain of a transistor

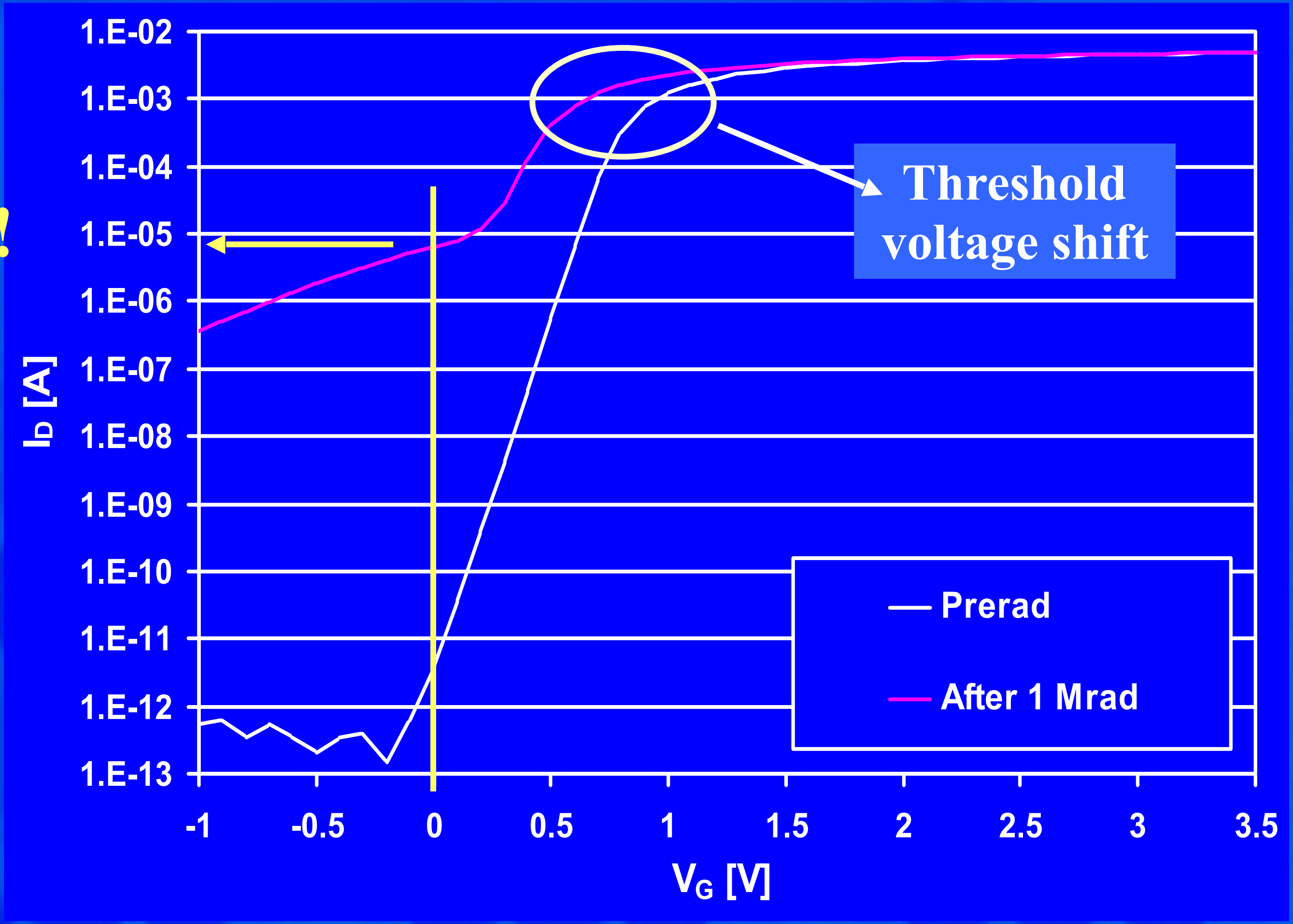
1. Effects in the thin gate oxide

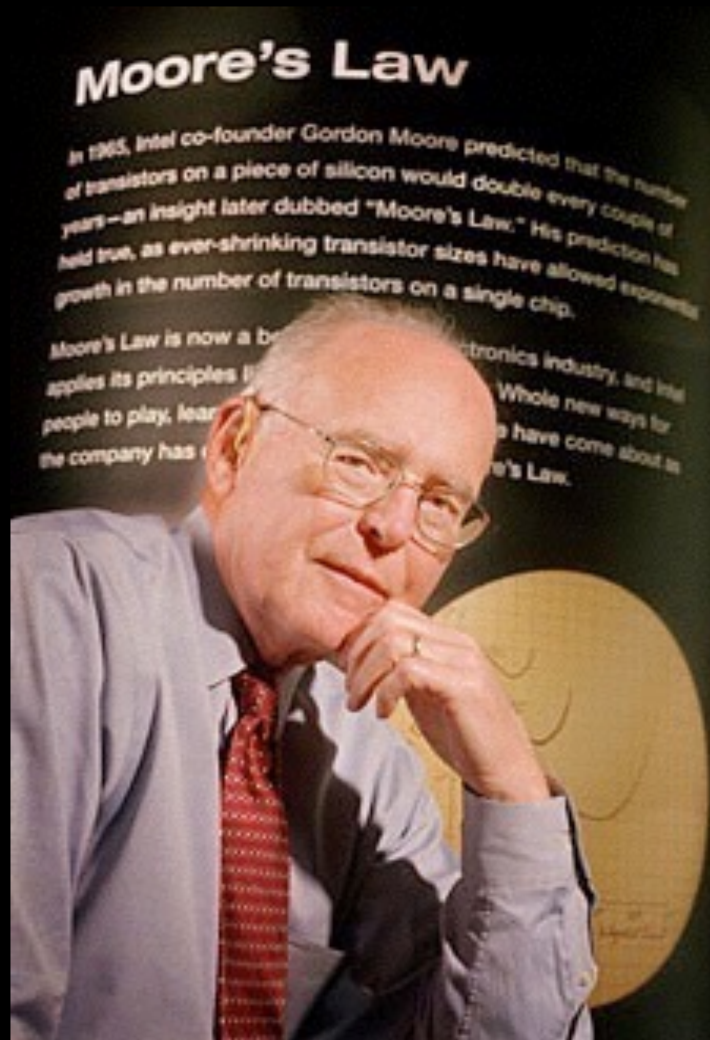


Example

NMOS - 0.7 μm technology - t_{ox} = 17 nm

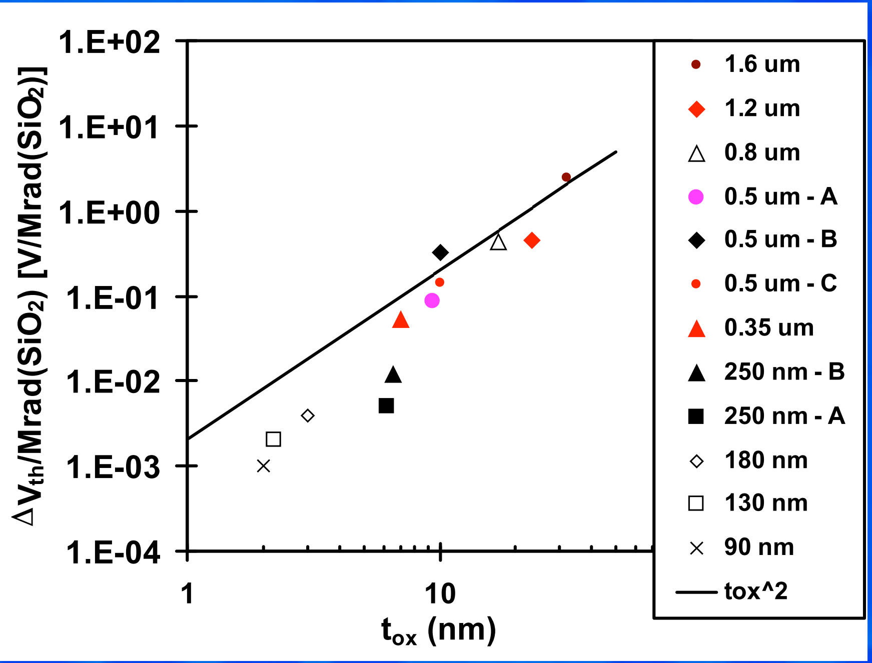
μA!




Moore's Law
In 1965, Intel co-founder Gordon Moore predicted that the number
of transistors on a piece of silicon would double every couple of
years—an insight later dubbed "Moore's Law." His prediction has
held true, as ever-shrinking transistor sizes have allowed exponential
growth in the number of transistors on a single chip.
Moore's Law is now a
industry, and Intel
applies its principles
Whole new ways for
people to play,
have come about as
the company has
Law.

Consequences of thin gate oxide

- ✓ Hole trapping and activation of interface states depend on oxide thickness (this has been known since the ’80s)
- ✓ Remaining problem for TID effects is related to ionization in the thick STI oxide

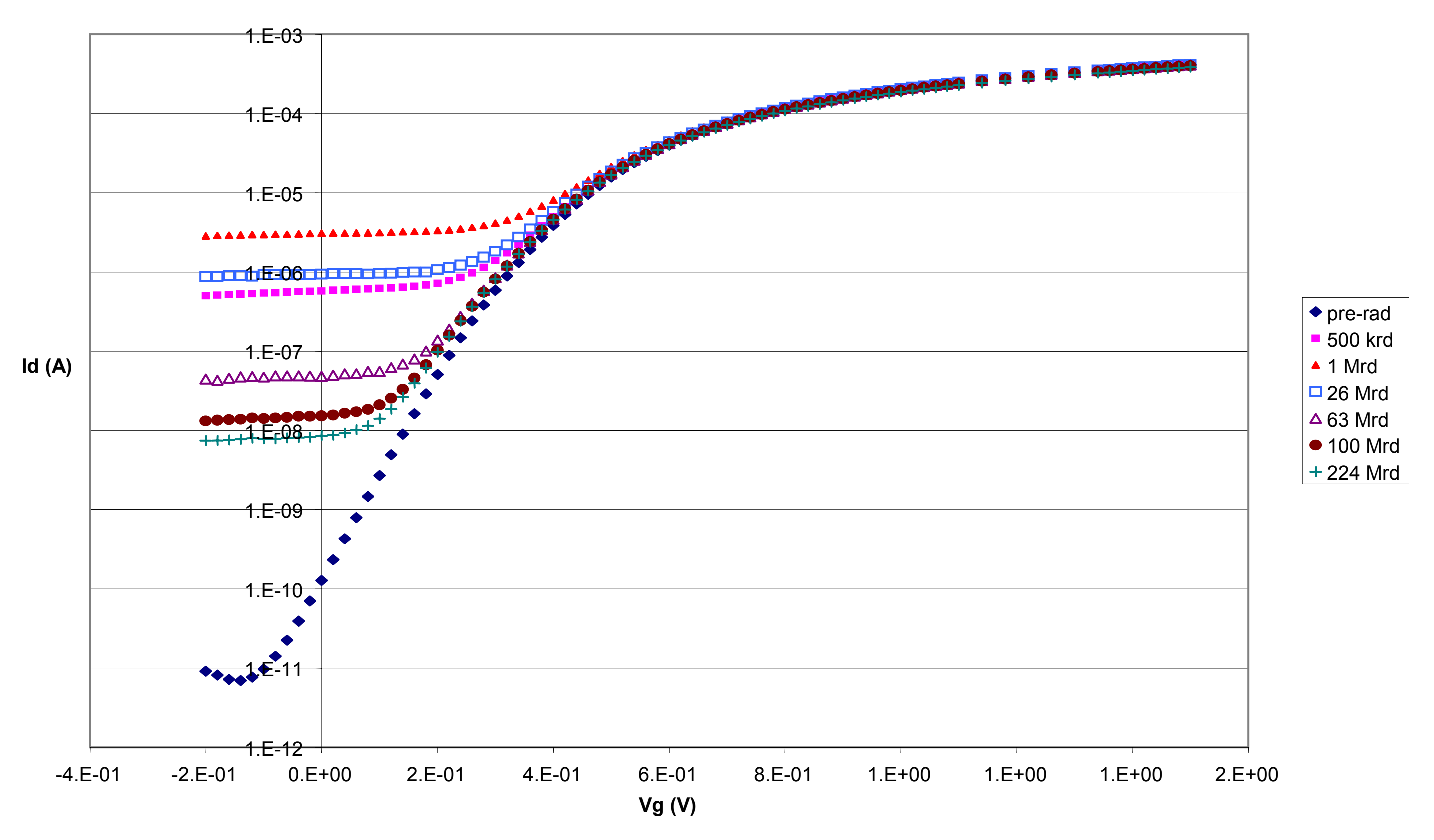


TID-induced threshold voltage shift vs gate oxide thickness.

- Data for commercial technologies from different manufacturers

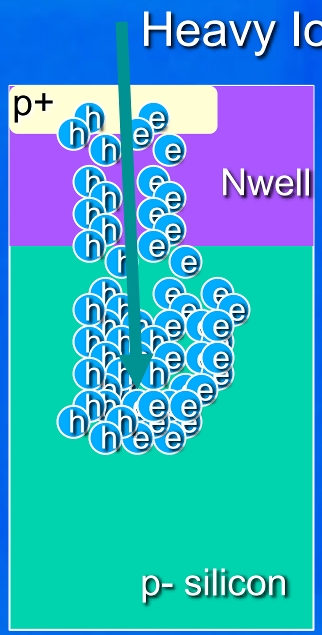
Example leakage currents

Source-Drain leakage (transistor's edge)

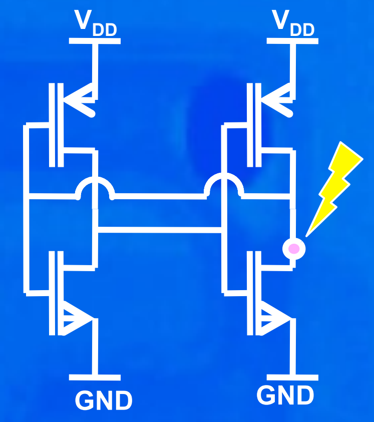


Single Event Effects (SEEs)

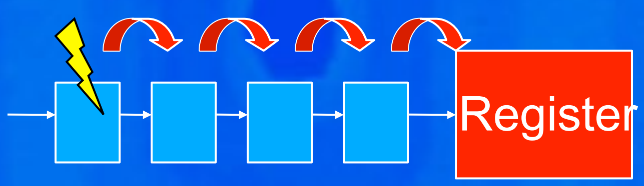
- ✓ SEEs can be traced to the **local and instantaneous** deposition of ionization energy in the semiconductor
- ✓ Only charge in a **given volume**, where it can be collected in the relevant amount of time by the appropriate circuit node, matters
- ✓ An error occurs only when the collected charge is above a given value – called "**critical charge**"



In memory => SEU
(this can lead to SEFI)



In combinatorial logic
=> propagation of hit
can be latched (DSET)



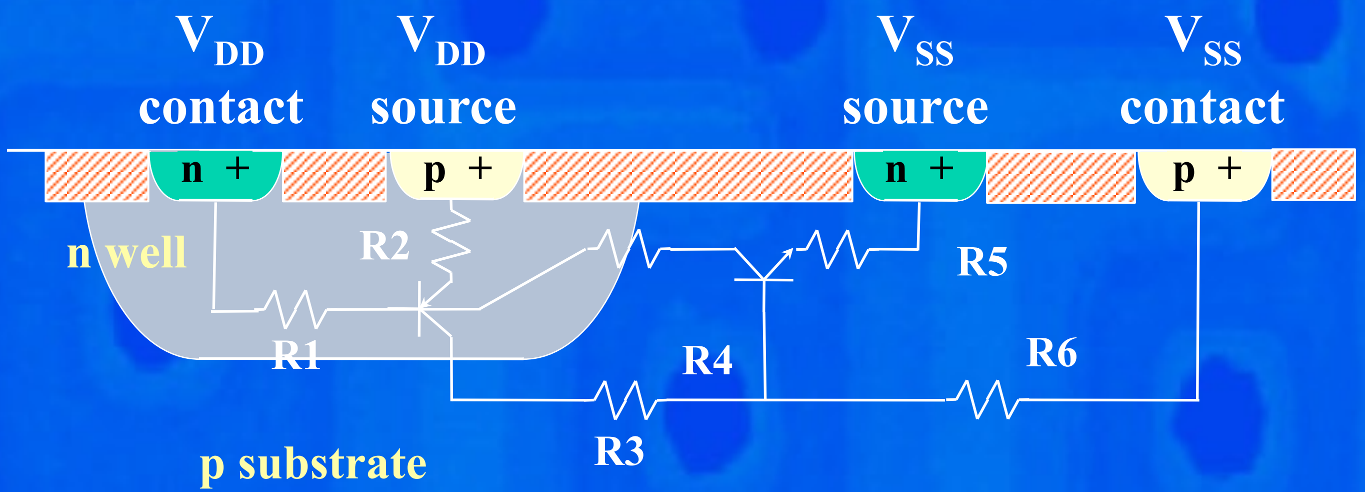
Combinatorial logic

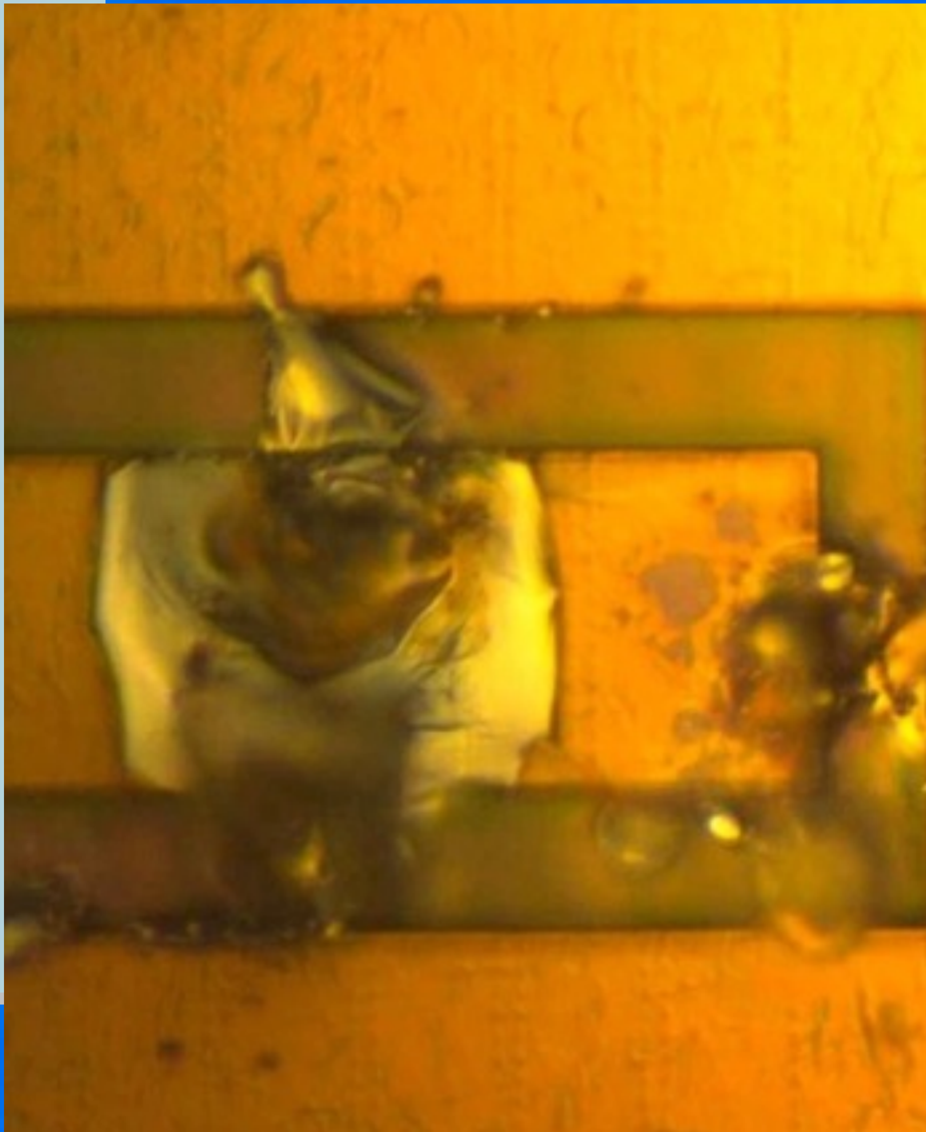
Destructive SEEs (Hard errors)

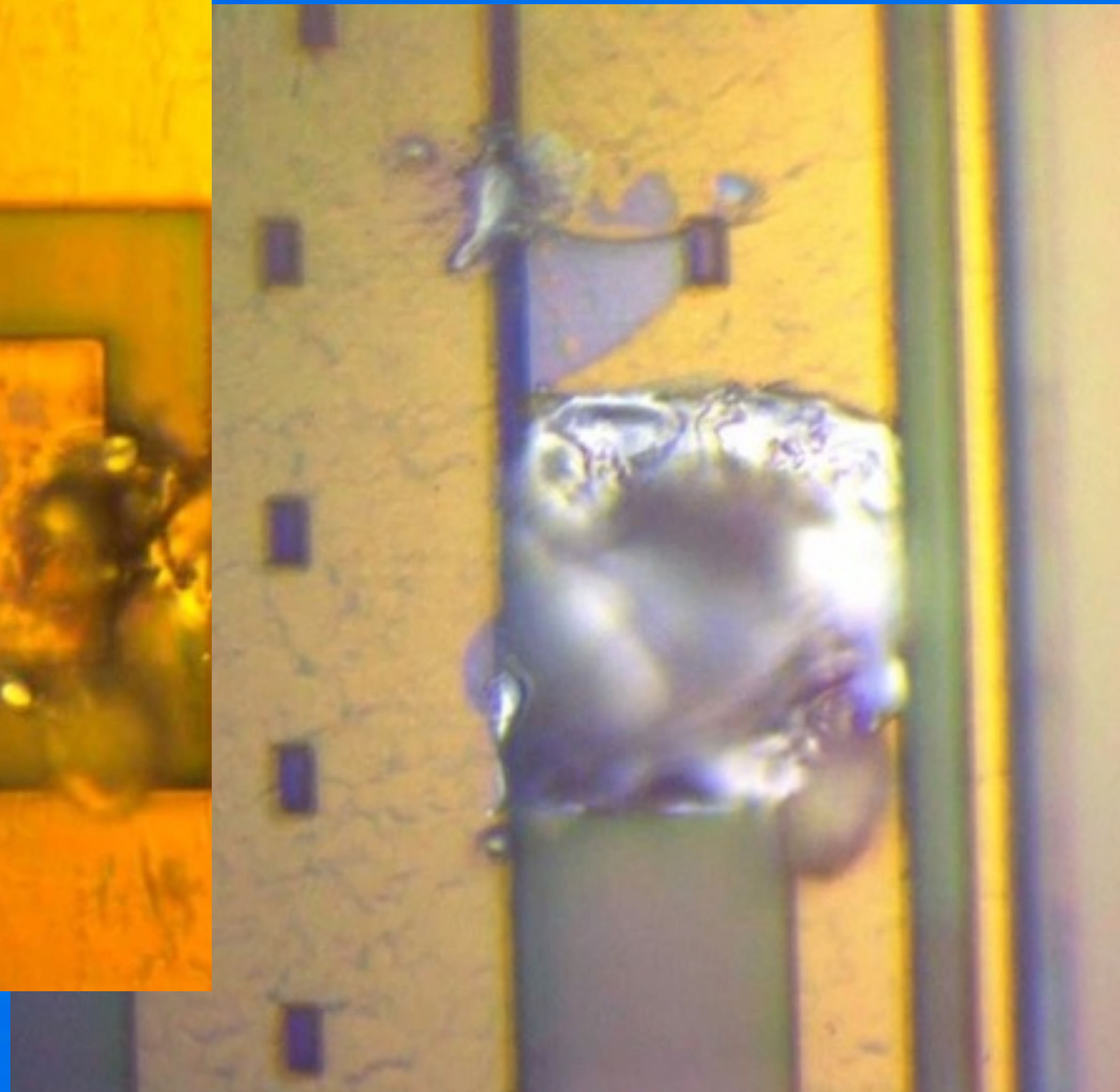
- SEBO => Single Event Burnout occurring in power MOSFET, BJT (IGBT) and power diodes
- SEGR => Single Event Gate Rupture occurring in power MOSFET
- SEL => Single Event Latchup occurring in CMOS ICs
- They can be triggered by the nuclear interaction of charged hadrons and neutrons

Single Event Latchup (SEL)

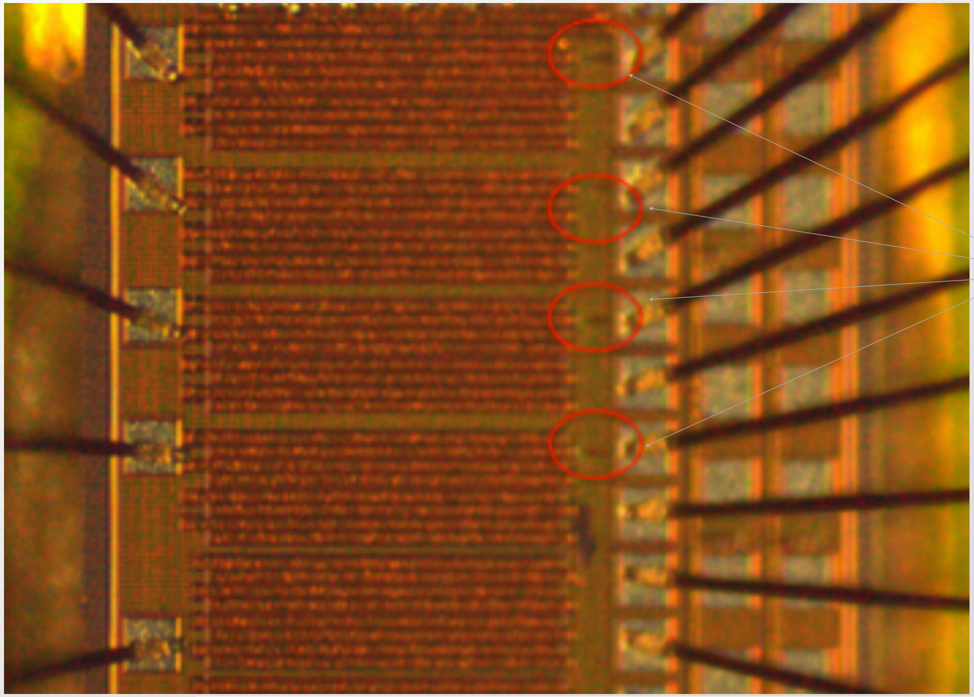
- ✓ Electrical latchup might be initiated by electrical transients on input/output lines, elevated T or improper sequencing of power supply biases. These modes are normally addressed by the manufacturer.Only charge in a given volume, where it can be collected in the relevant amount of time by the appropriate circuit node, matters
- ✓ Latchup can be initiated by ionizing particles (SEL) in any circuit node – not only in IOs







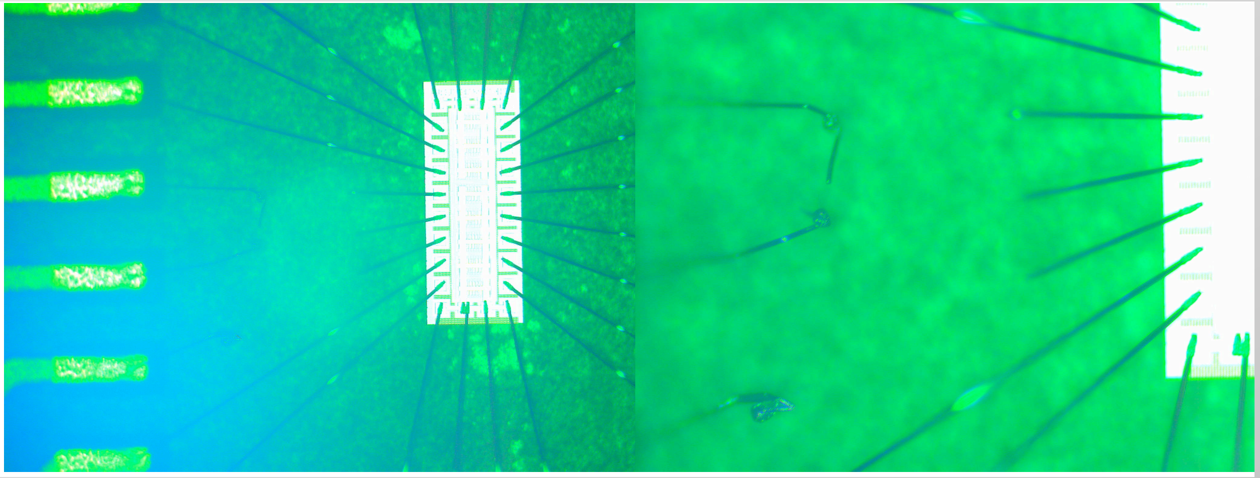
Single Event Burnout (SEB)



Evidence of SEB on test chips with LDMOS

On-chip metal line burnt (encircled dark shadows)

Molten wirebonds



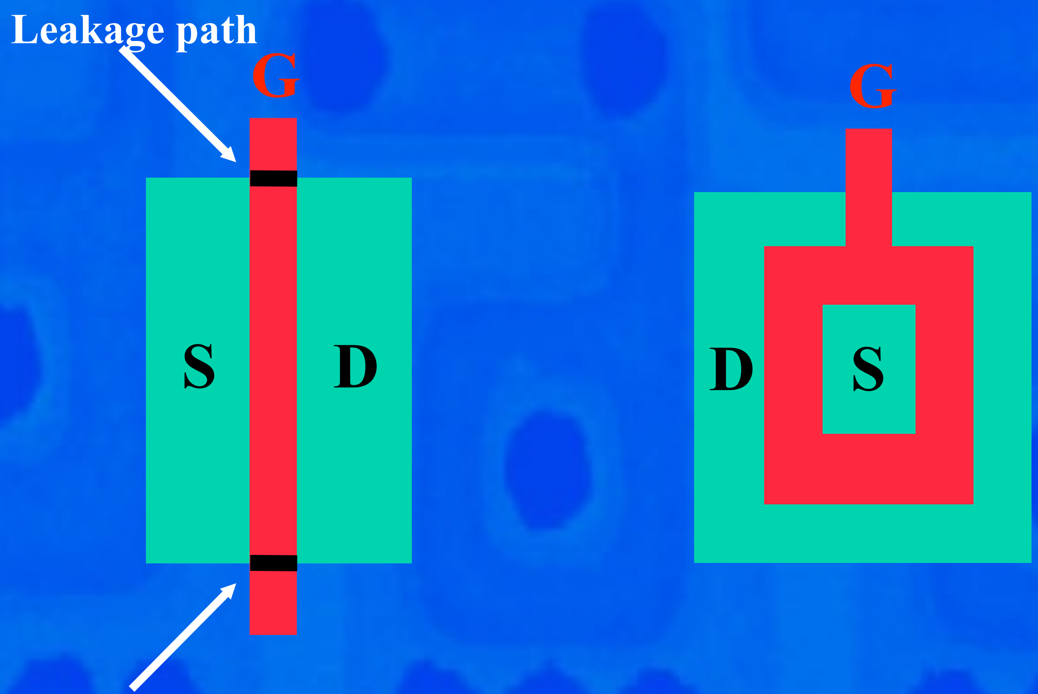
How to design radiation tolerant ASICS

Hardness By Design (HBD)

- ✓ Concept to design ASICs robust to radiation without the use of special rad-tolerant technologies
  - Radiation requirements moved to the design level
    - Modified layout
    - Modified architectures
  - Techniques can be devoted to either TID or SEEs

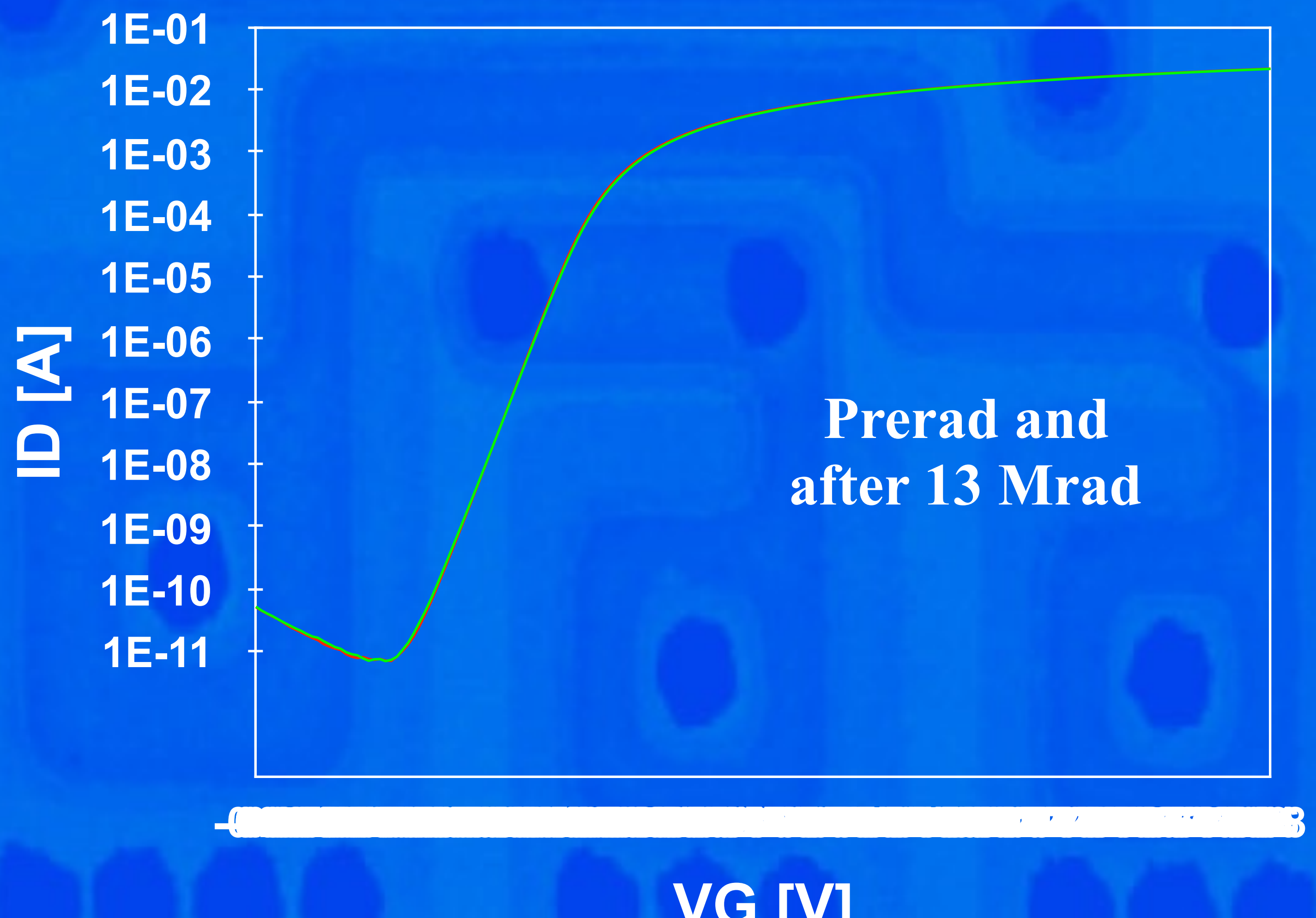
Radiation-tolerant layout (ELT)

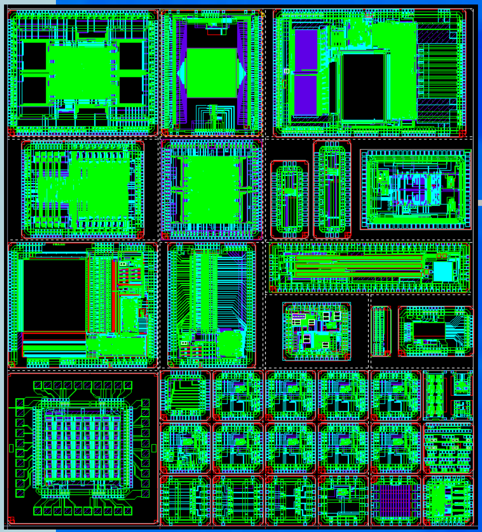
- ✓ Layout techniques enable the elimination of all radiation-induced leakage paths
  - ELT shape eliminates source-drain leakage – needed only for NMOS

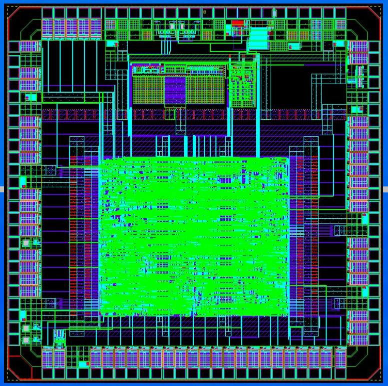


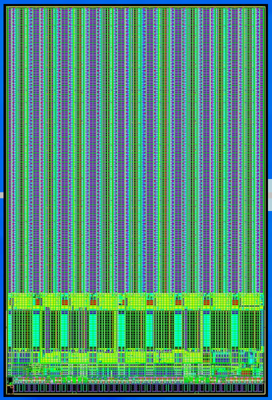
Effectiveness of ELTs

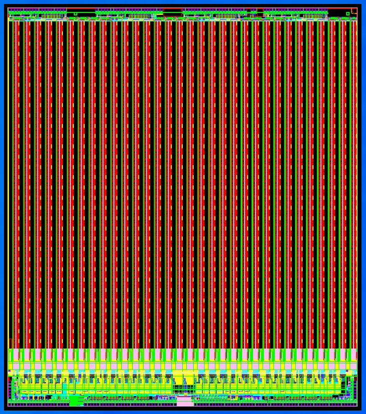
0.25 μm technology - W/L = 30/0.4 - ELT

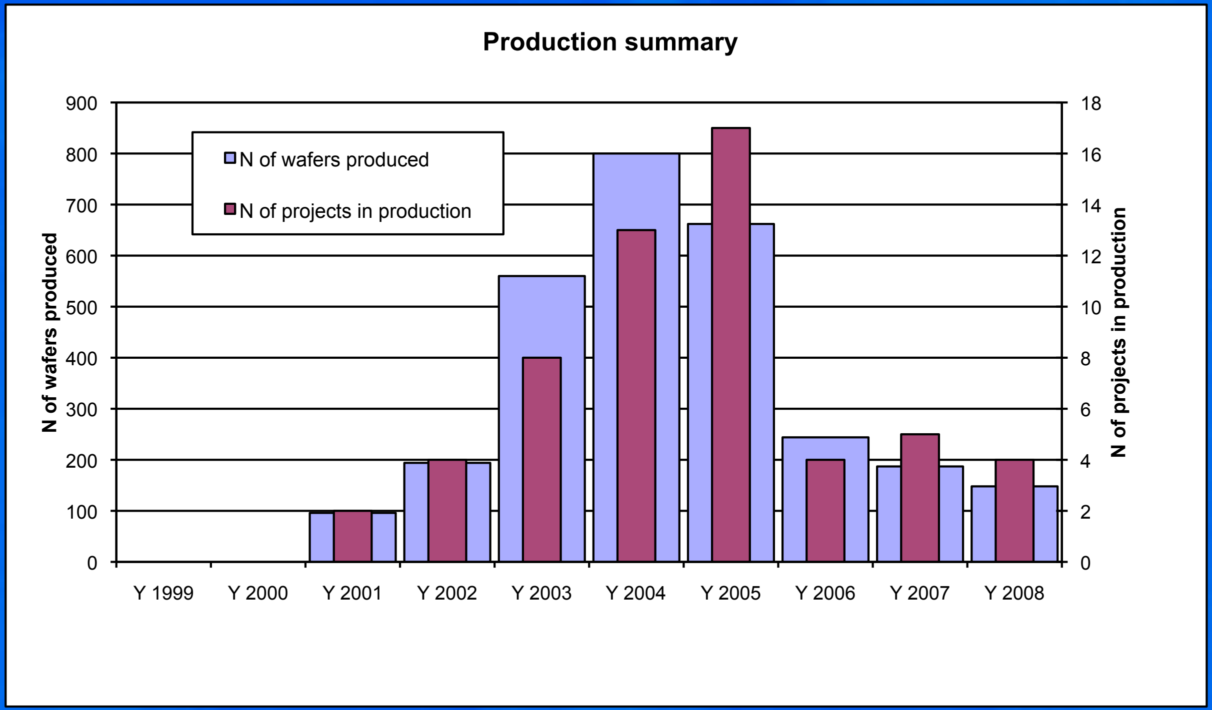












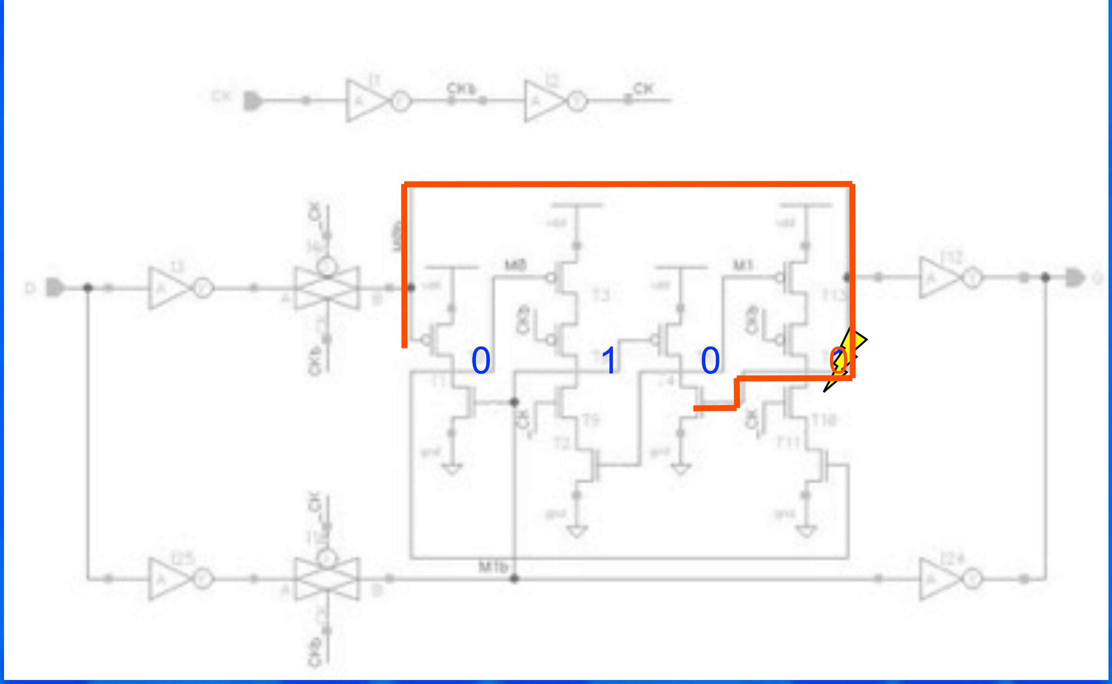
LHC experiments widely used commercial 0.25um CMOS for their detector systems

HBD for SEEs

- ✓ Memory and registers are often the most vulnerable elements to SEUs. HBD techniques concentrate on these cells
- ✓ Hardening can be achieved by
  - Custom modification of the basic memory or register cell
  - Redundancy (triplication and voting)
  - Encoding

Cell design

- ✓ Use of radically different cell design, customized to be insensitive to charge deposition in one single node
  - Example of one of the most popular designs: DICE (Dual Interlock Cell)
    - Dual Interlock ensures SEU protection against hit on one node
    - Writing in the cell requires access to 2 nodes
    - Protection from SEU less efficient in modern technologies – high integration
    - Possible to use the 2 data paths to duplicate combinatorial logic and harden circuit against DSET

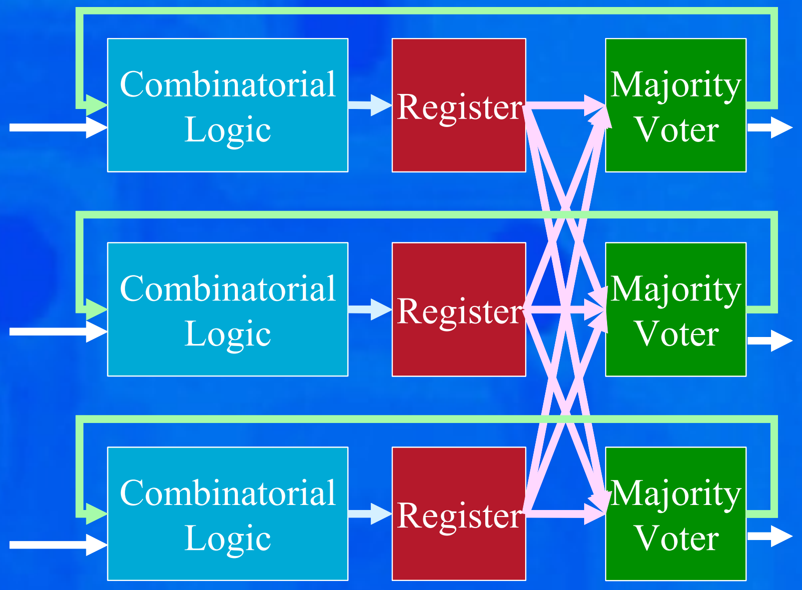


REDUNDANCY

Just in case you're totally oblivious.

Redundancy: TMR

- ✓ Triplication with 3 voters – to protect from errors in the voter itself

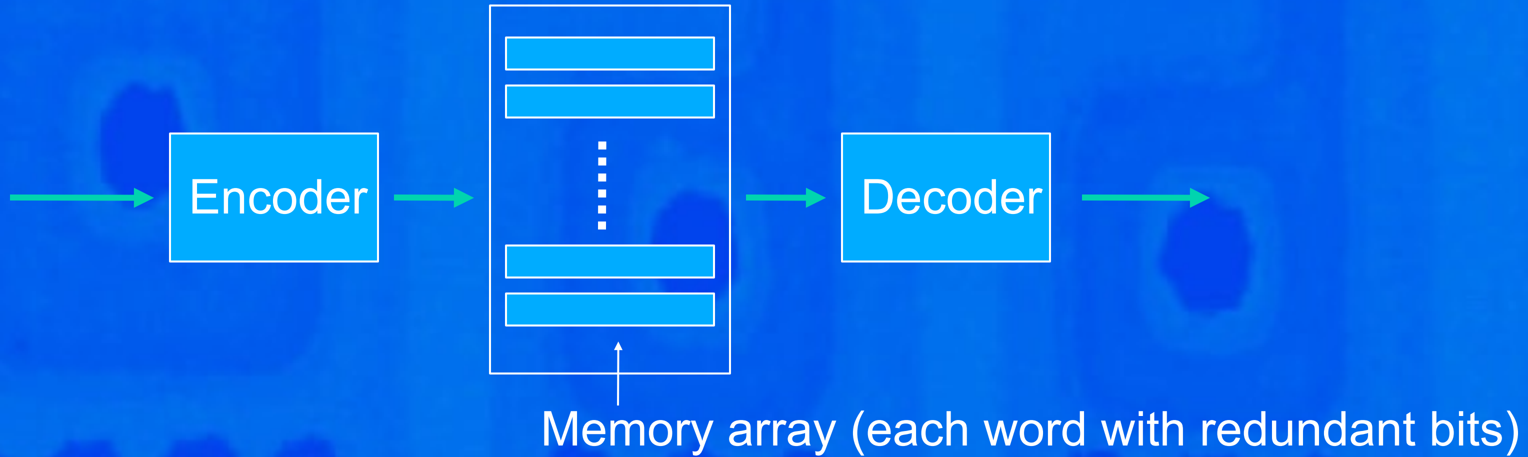


- ✓ The state machine is instantiated 3 times, with 3 voters
- ✓ An SEU can corrupt the output of one of the blocks, but majority voting restores the correct state
- ✓ An error in one of the voters is also restored

Redundancy: encoding

✓ Adding redundant information (bits) and encoding-decoding

- Used for data transmission and for memories
- Requires complex encoding-decoding logic
- Several different codes can be used (Hamming, Reed-Solomon, BCH, etc.)



Conclusion

This was a very quick and incomplete overview

"… even after 25 years of work in the domain, when I irradiate a device I often fall on something I do not understand…"

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This was a very quick and incomplete overview

"… even after 25 years of work in the domain, when I irradiate a device I often fall on something I do not understand…"

The field will require bright, methodic and patient young engineers for a long while…