Development of Superconducting TDC/ADC/ALU and Neutron Detectors

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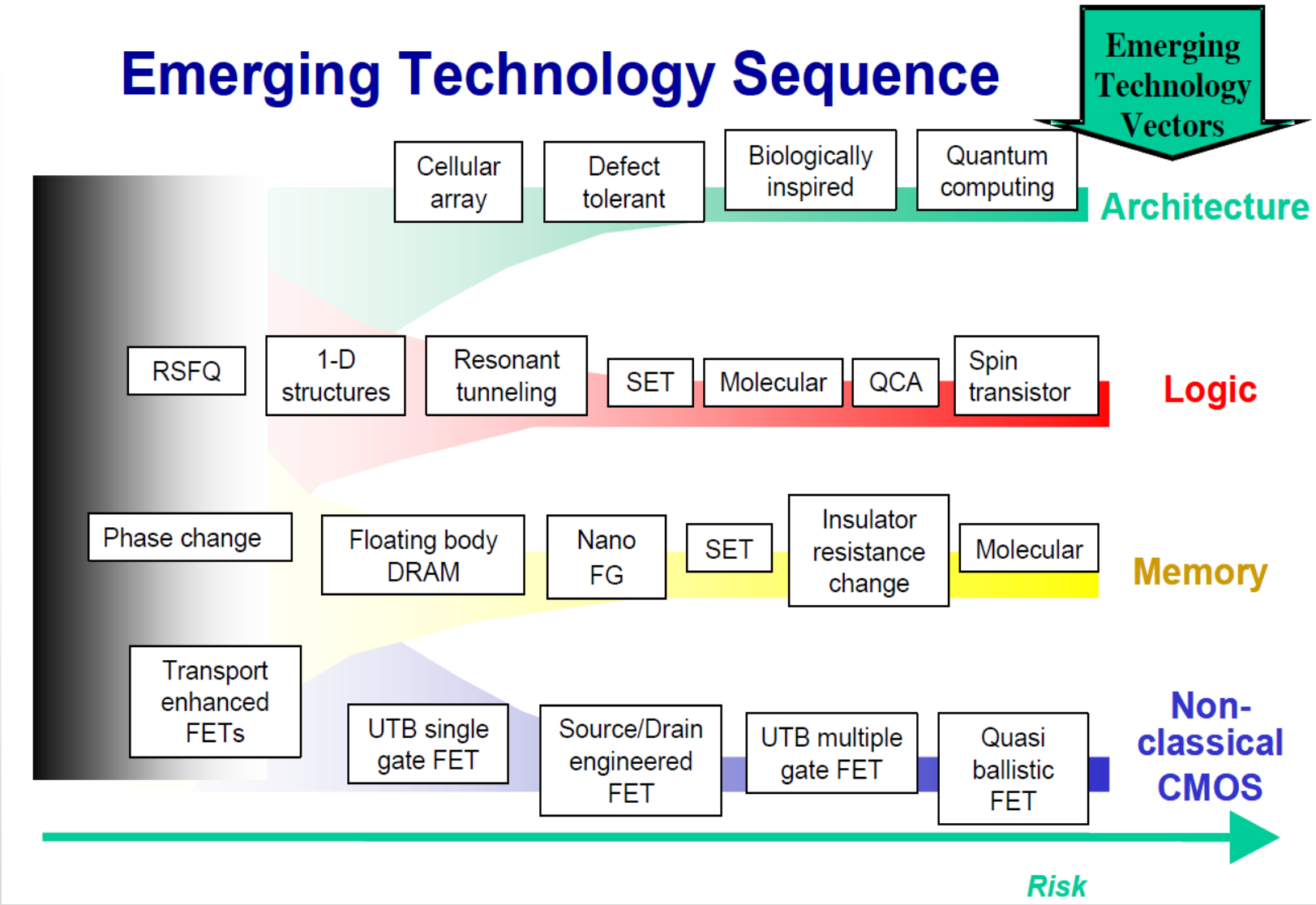
Outline

- Introduction to Superconducting Logic
- Time to Digital Converter
- Analog to Digital Converter
- Superconducting Stripline Detectors Towards Megapixel Neutron Imaging
- Arithmetic Logic Unit

Single Flux Quantum (SFQ) Logic

- Based on switching of the Josephson Junctions
- They can switch up to THz frequencies.
- They have very low power consumption (~mW).
- Compatible with the standard design and fabrication tools.
- It is possible to integrate with semiconductor and/or optical devices.
- Circuit complexities of close to 100 000 Josephson junctions have been reported.
- Gates working about 750 GHz clock frequency has been reported.

ITRS Report



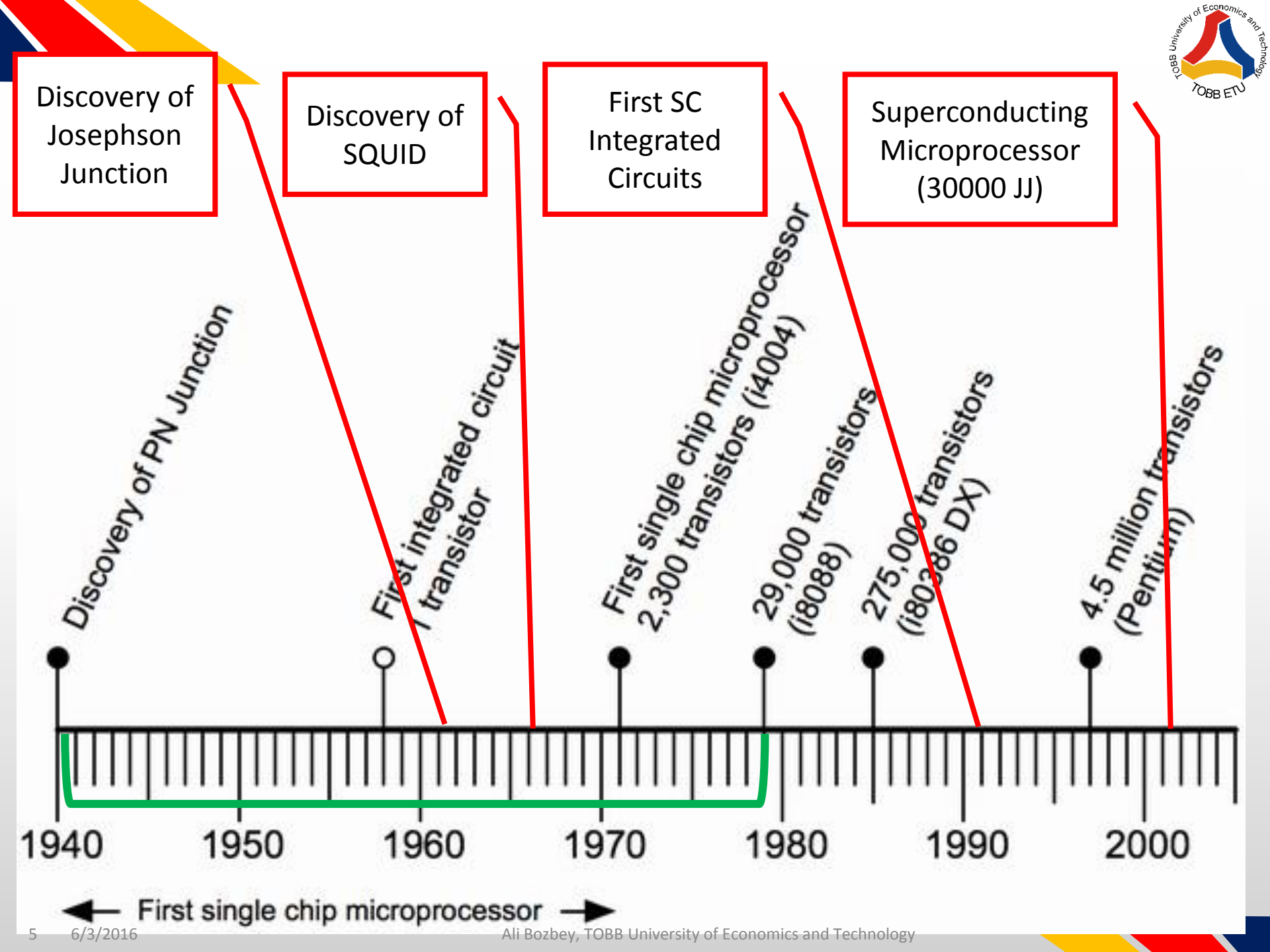
ITRS: The International Technology Roadmap for Semiconductors

Discovery of Josephson Junction

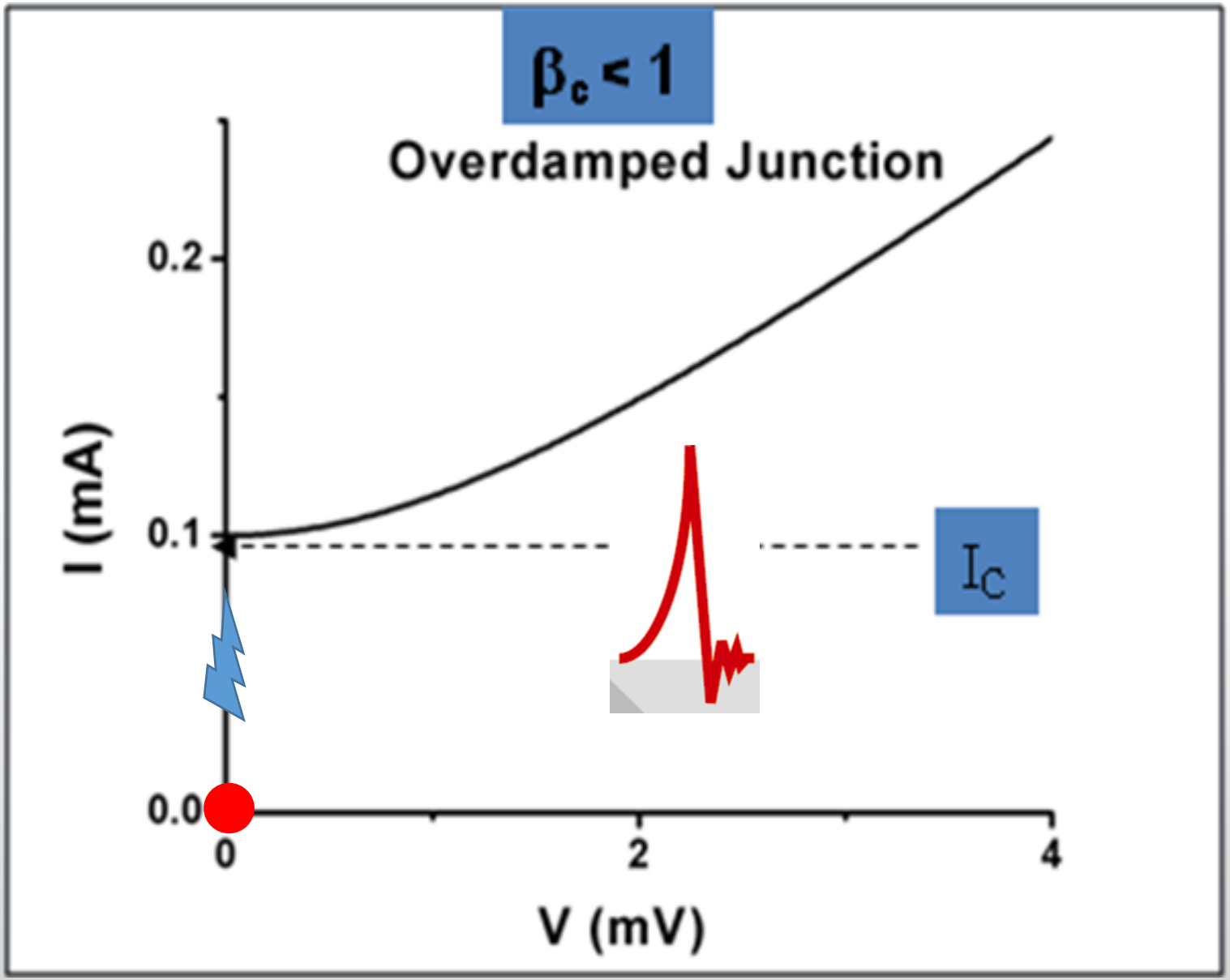
Discovery of SQUID

First SC Integrated Circuits

Superconducting Microprocessor (30000 JJ)



Generation of the SFQ Pulse

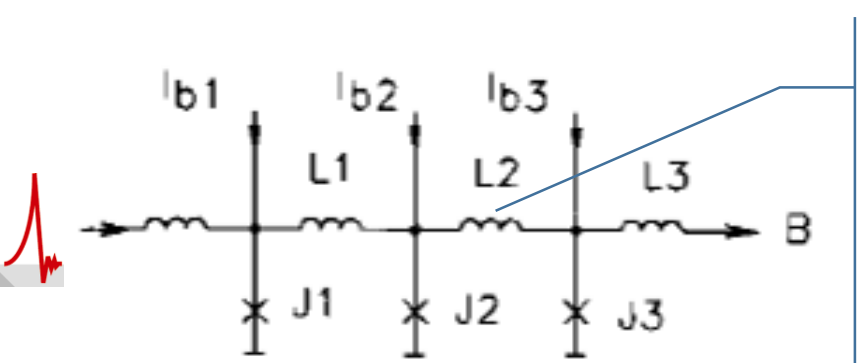


RSFQ Circuit Samples

- Josephson Transmission Lines (JTL)
- SFQ Splitters
- SFQ Mergers
- Gates: AND, OR, NOT …
- Flip-Flops
- DC/SFQ and SFQ/DC converters

- Passive Transmission Lines (PTL)

Josephson Transmission Lines (JTL)

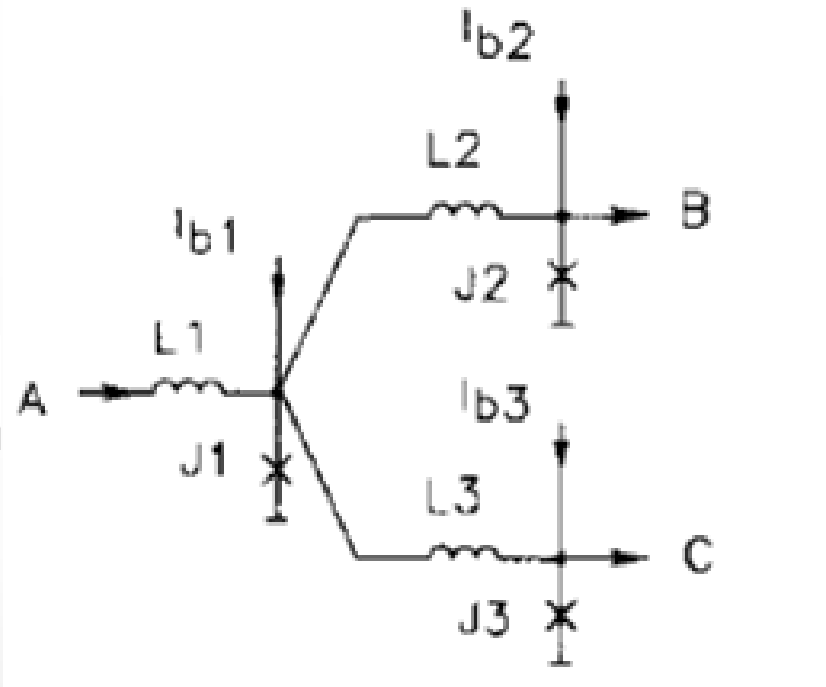


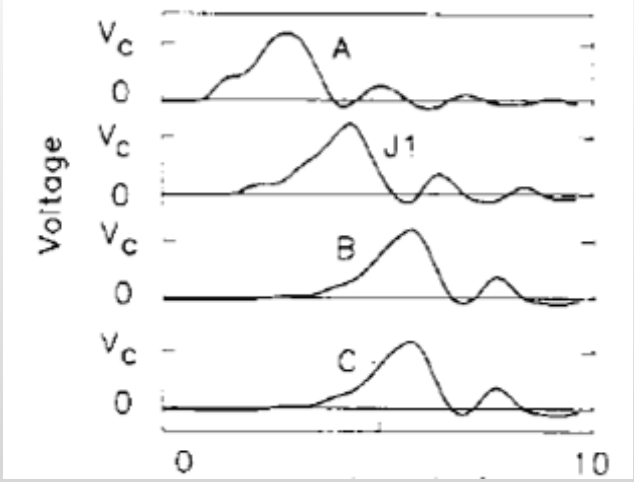
L1, L2, L3; should be small enough in order not to allow magnetic flux storage.
(Ic.L~0.5 Φ0)

- Interconnection of the logic gates and adjusting the timing of the circuits.
- Ib = 0.75 Ic
- SFQ pulse from input A propagates by swithing the junctions J1, J2, J3 respectively and escapes from output B.
- Advantages: recovery of SFQ pulse during propagation
- Disadvantages: time delay, jitter, number of josephson junctions

Likharev

SFQ Splitter

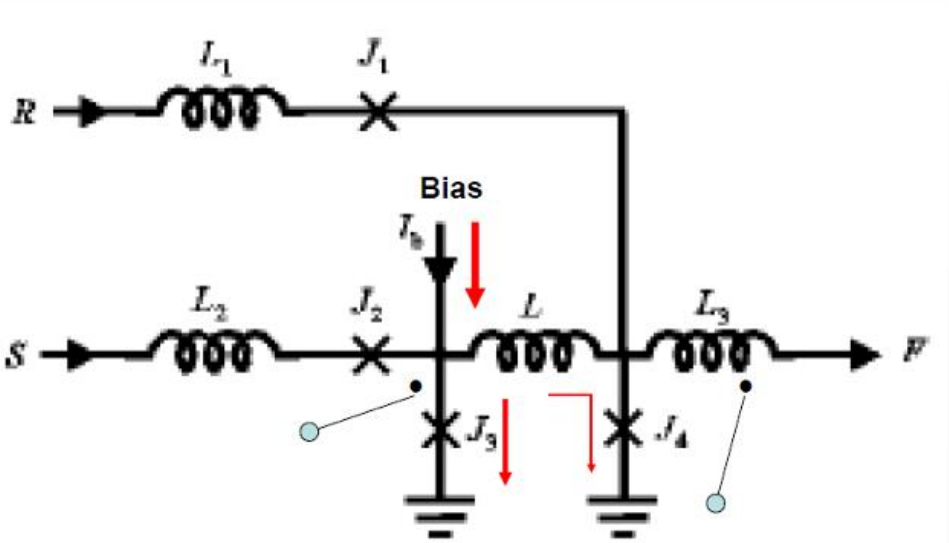


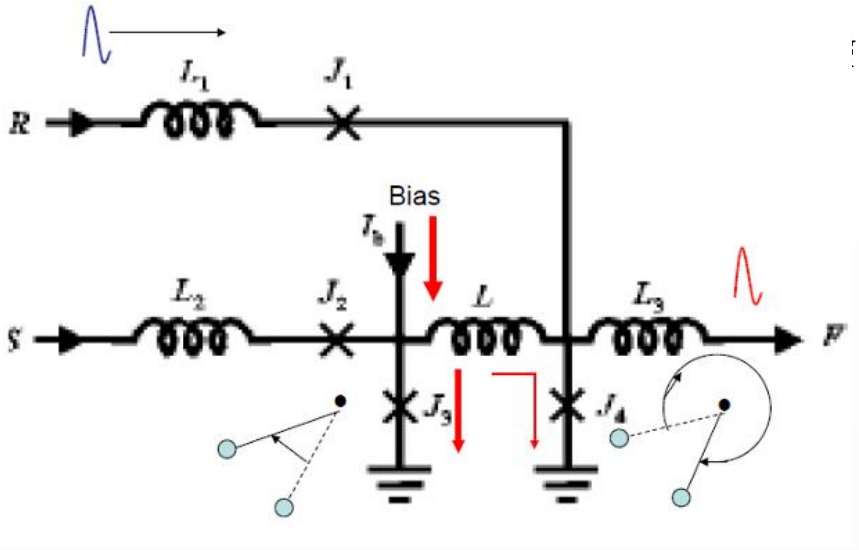


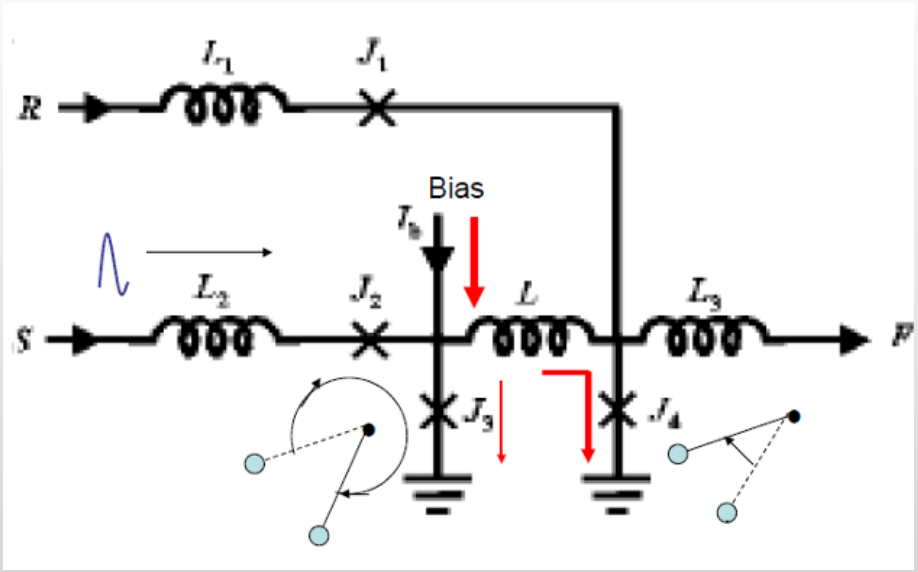
- Splitters are used to increase the fan-out of the logic circuits.
- Similar principle of operation with JTL. Critical currents of the junctions should be chosen properly. ($I_{c1}=1.4I_{c2}=1.4I_{c3}$)
- Hence, the SFQ pulse arriving from J1 can have enough power to move the J2 and J3 to voltage state.

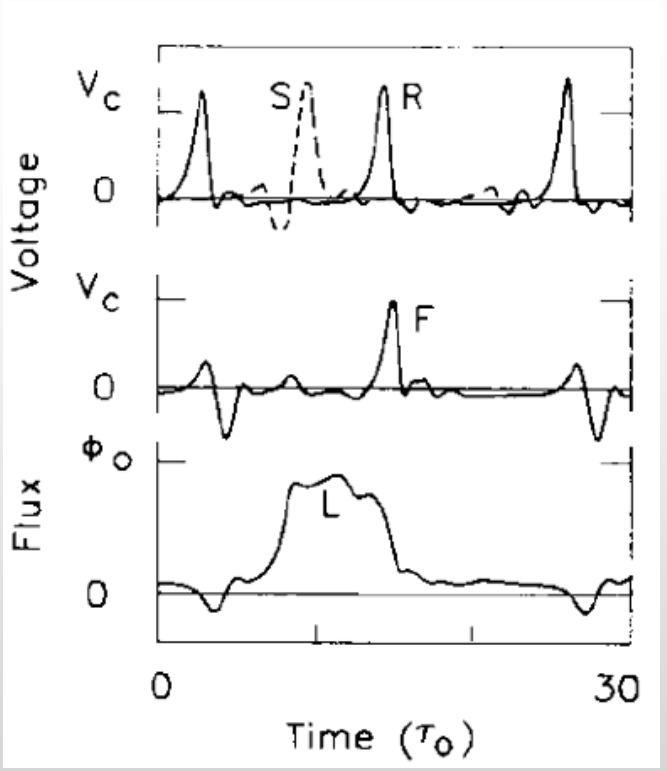
Likharev

RS Flip-Flop



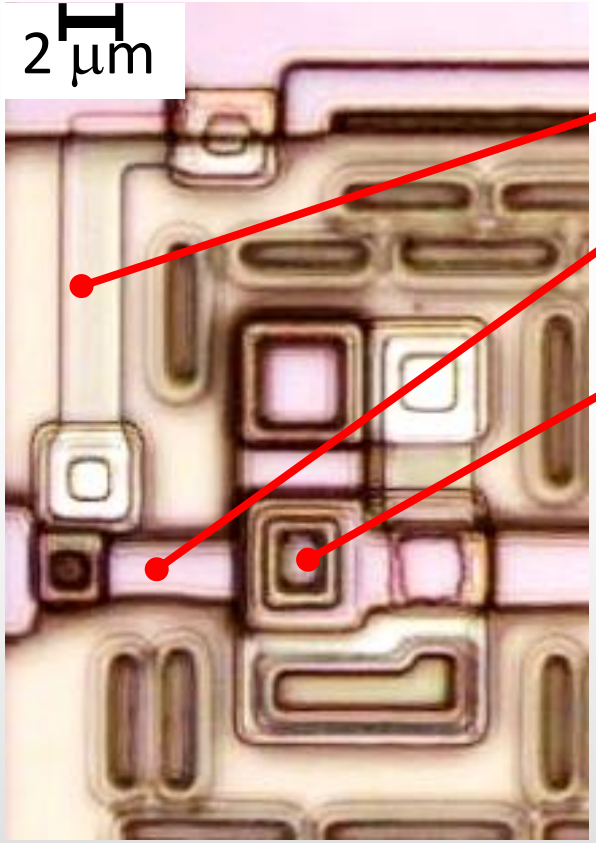


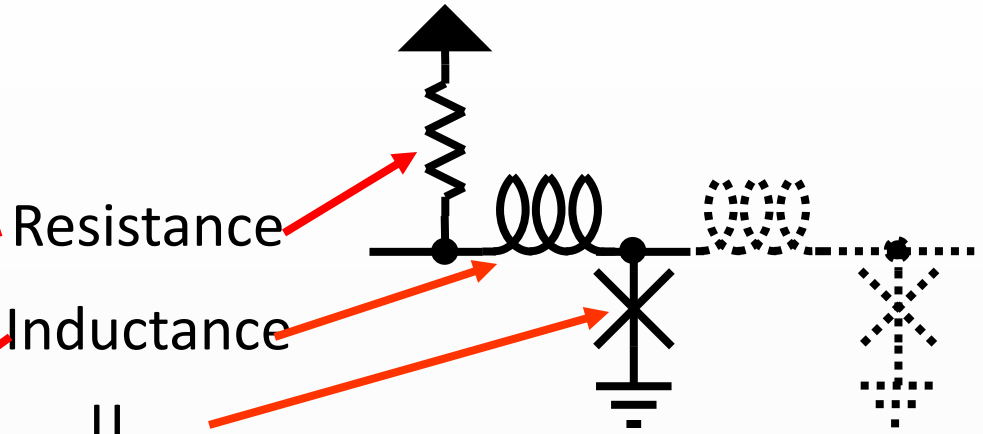


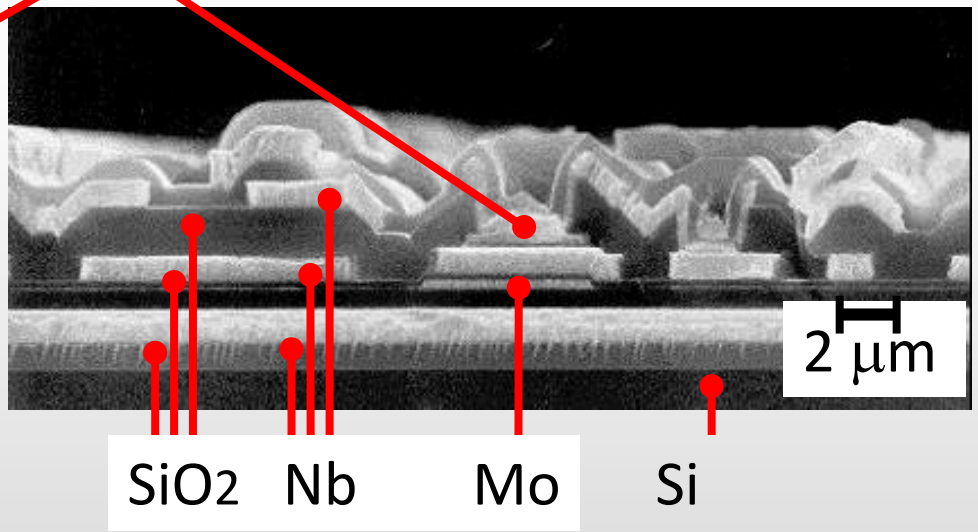


Likharev, Van Duzer

Circuit Fabrication (STP)

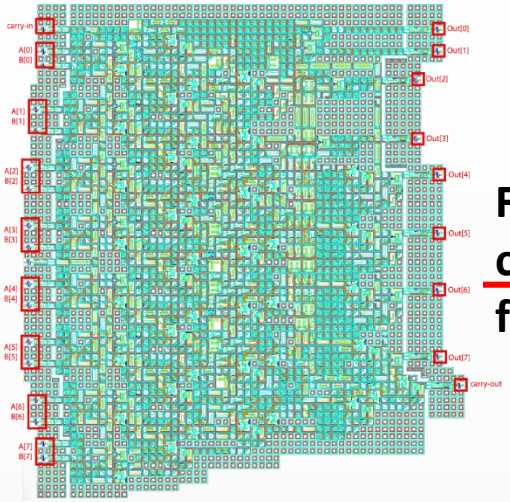




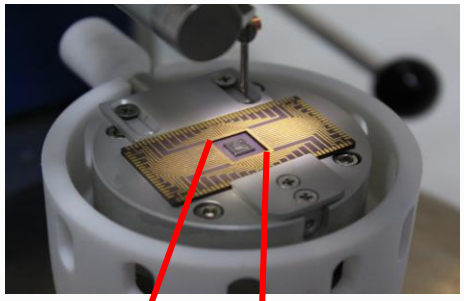


Design to Testing of Digital and Detector Circuits

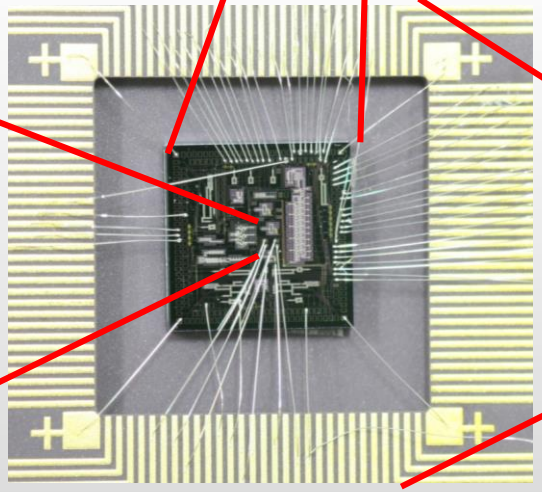
Design

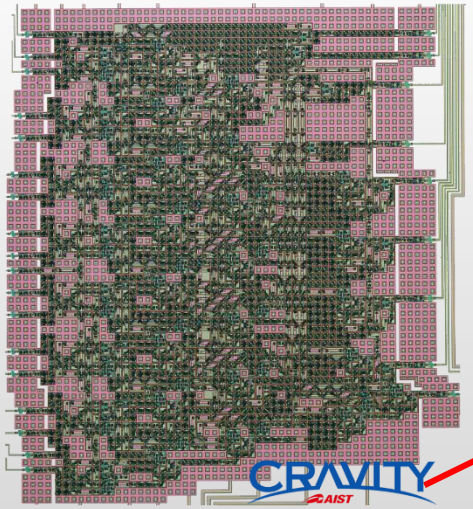


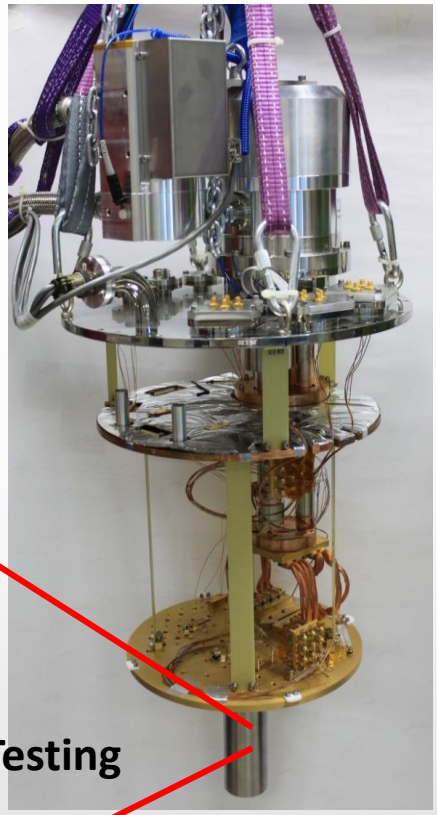
Fabrication by commercial foundries



Packaging



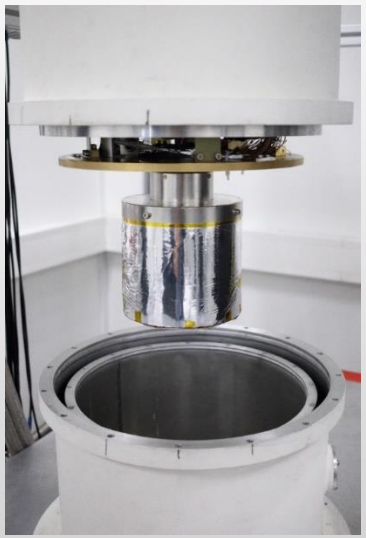




Testing

Measurement Setup

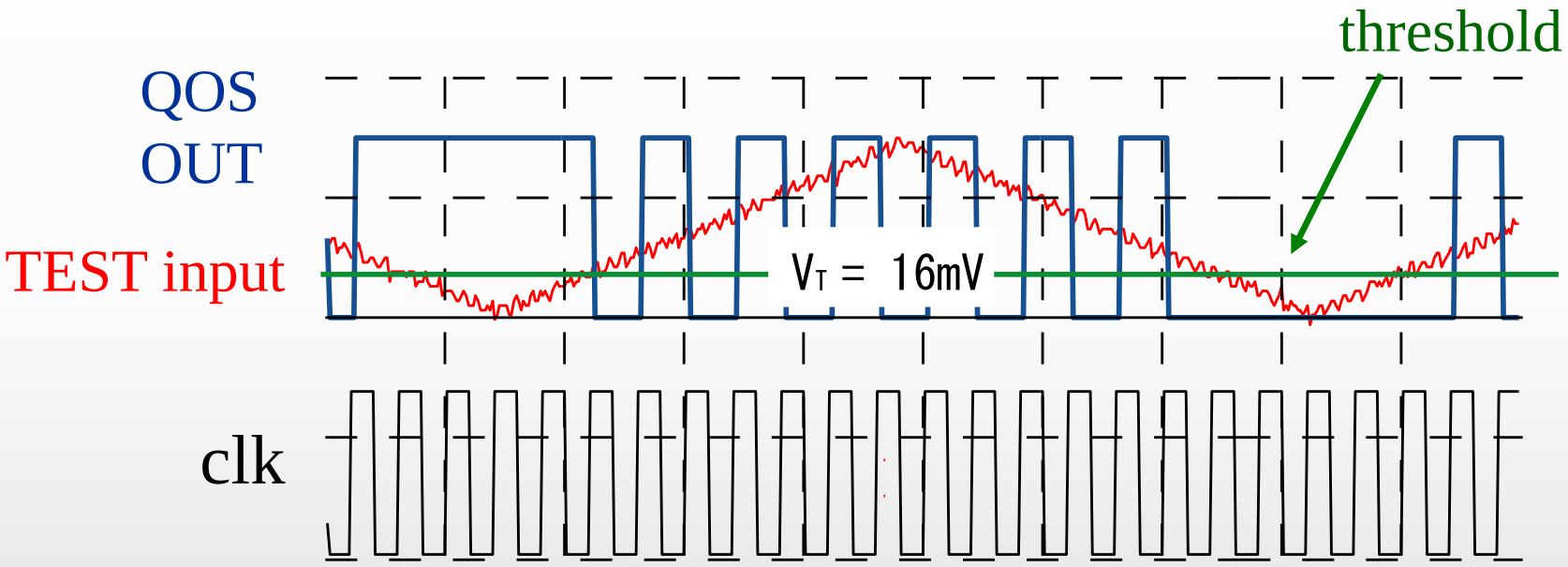
Frequency	Field	Attenuation
14 kHz	Magnetic	60 dB
100 kHz	Magnetic	80 dB
1 MHz	Magnetic	100 dB
1 MHz	Electric	100 dB
100 MHz	Electric	100 dB
100 MHz-10 GHz	Planewave	100 dB
18 GHz	Microwave	100 dB



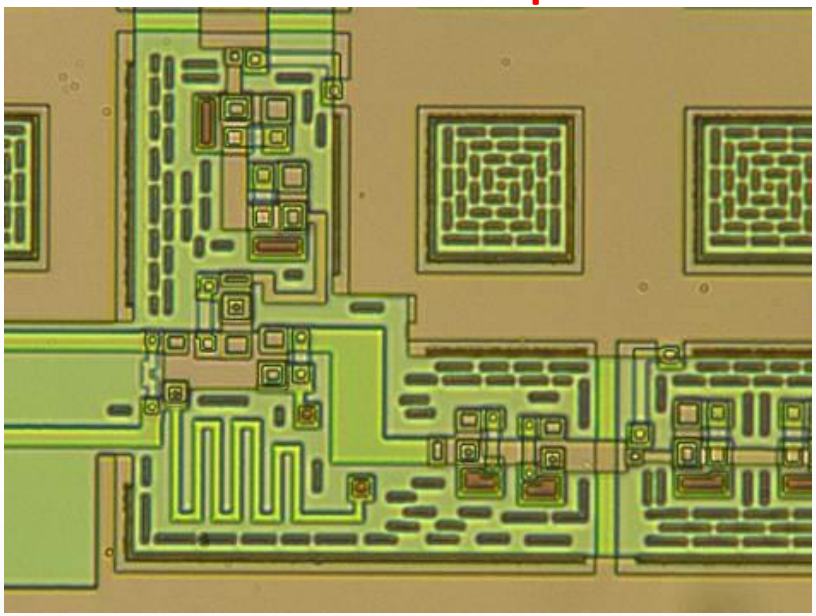
Circuits

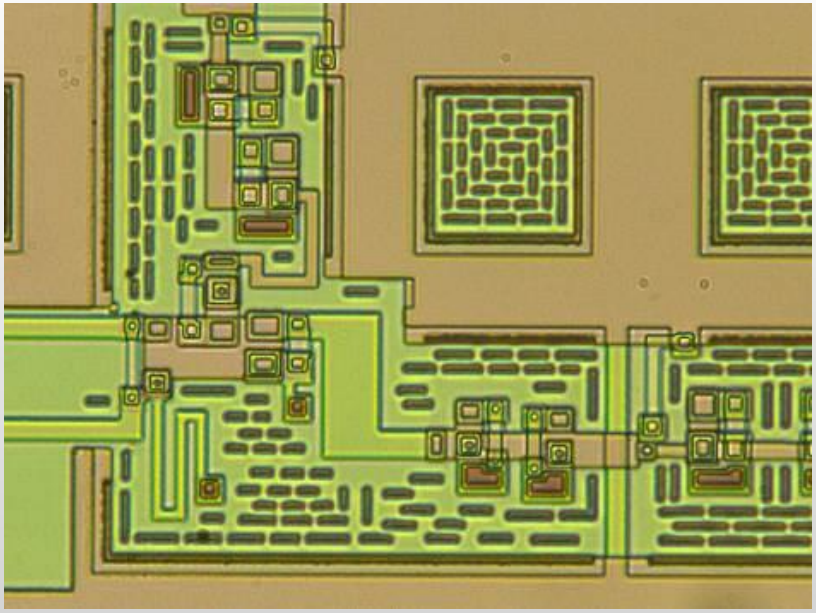
- Time to Digital Converter
- Analog to Digital Converter
- Monolithic Neutron Detector
- Arithmetic Logic Unit

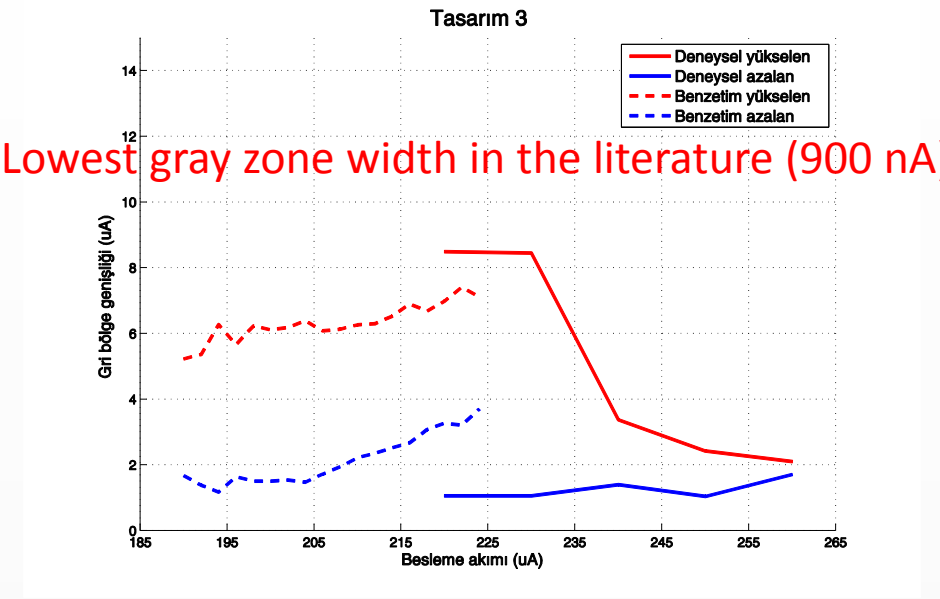
1-bit Comparator (QOS)



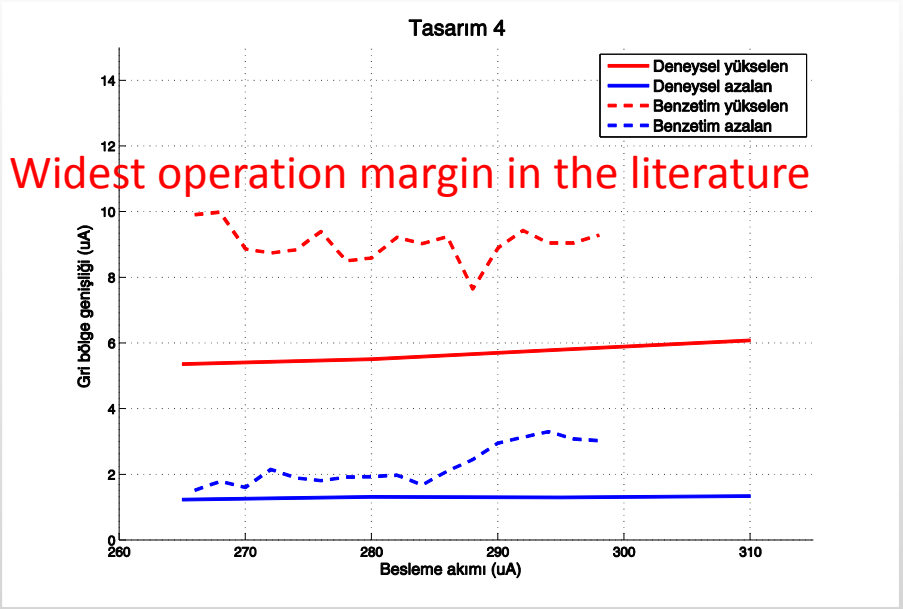
Comparator Circuits





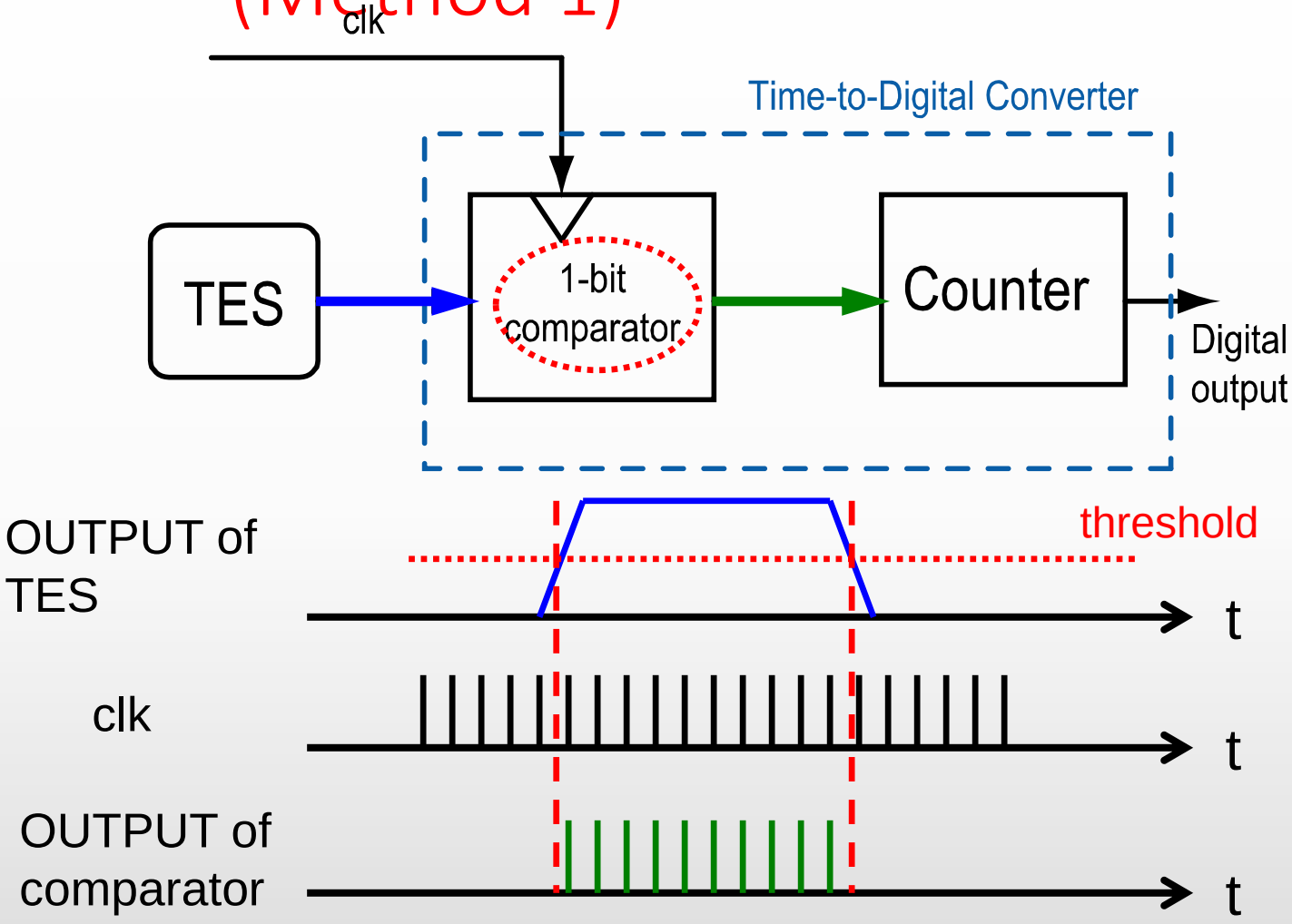


Lowest gray zone width in the literature (900 nA)



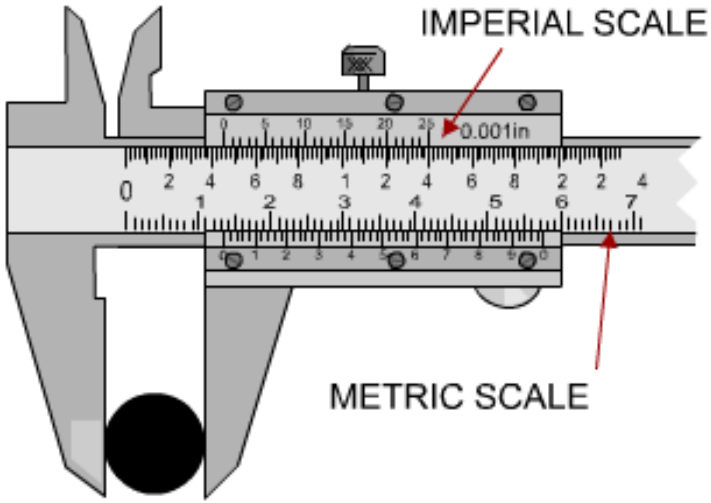
Widest operation margin in the literature

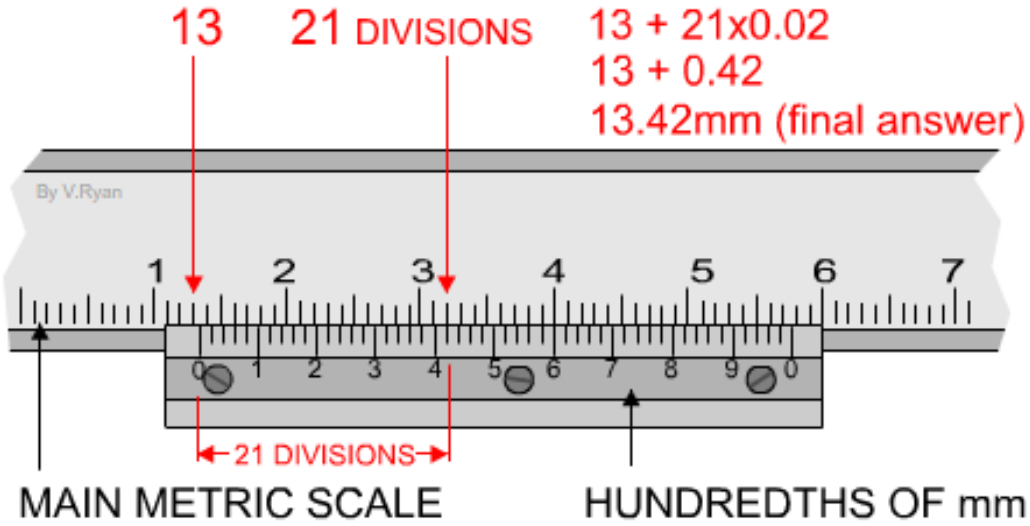
Time-to-Digital Converter (Method 1)



Comparator with high-speed response and high sensitivity

Time to Digital Converter (Method 2)

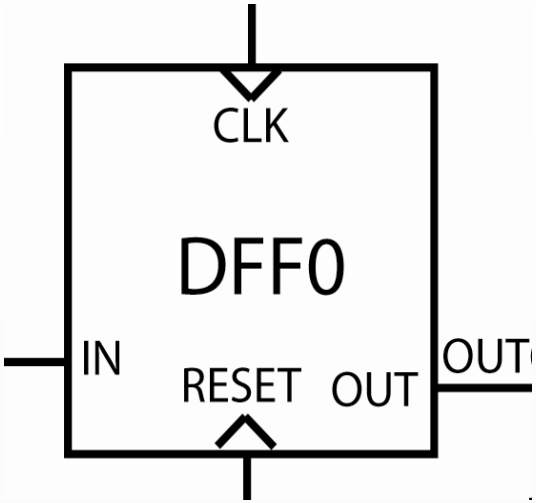


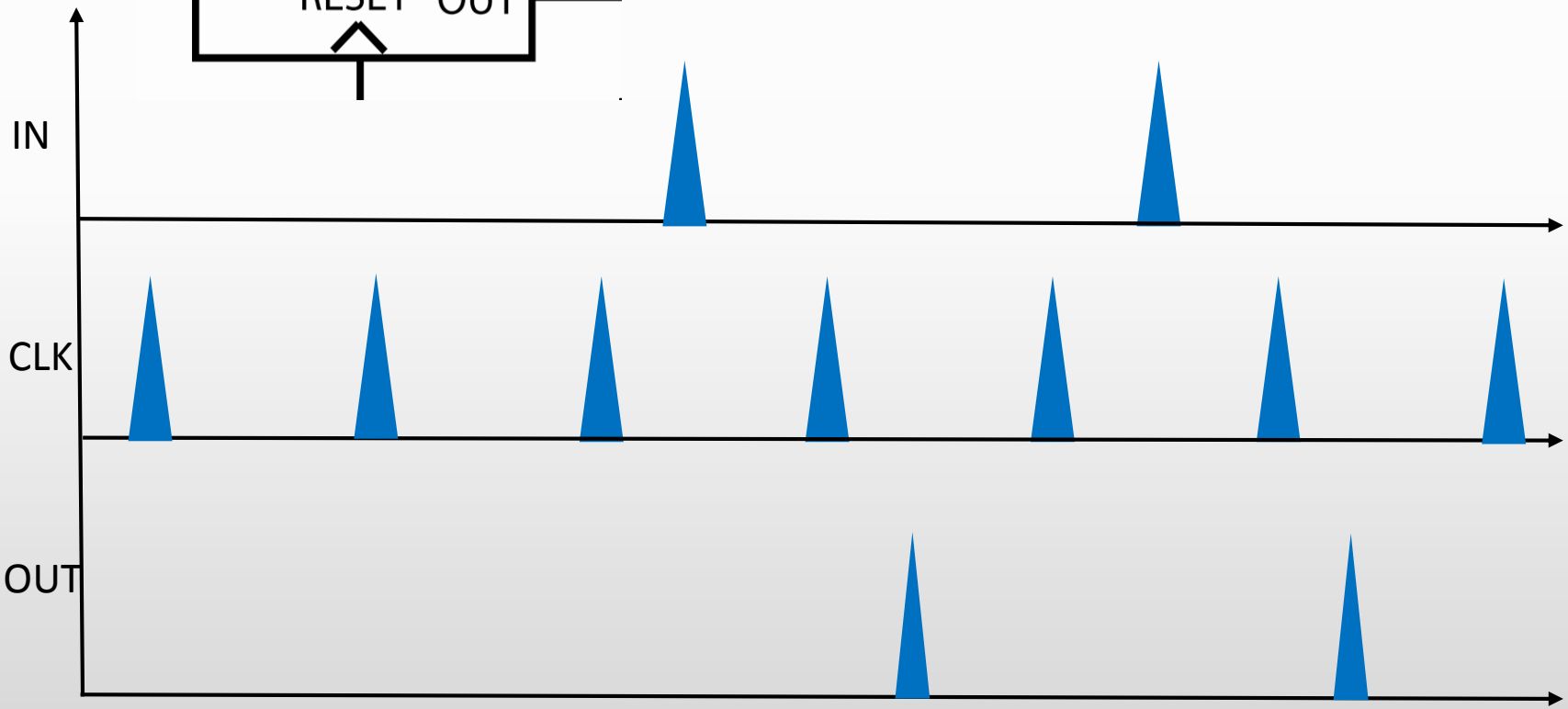


Vernier Caliper

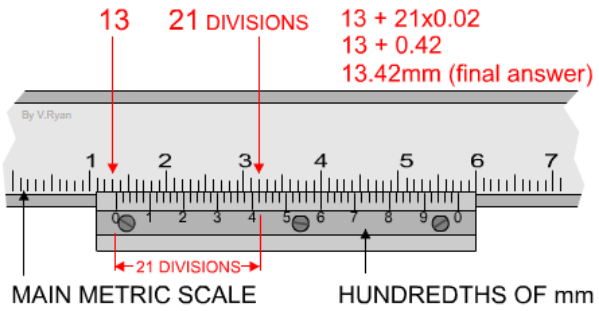
D-Flip Flop

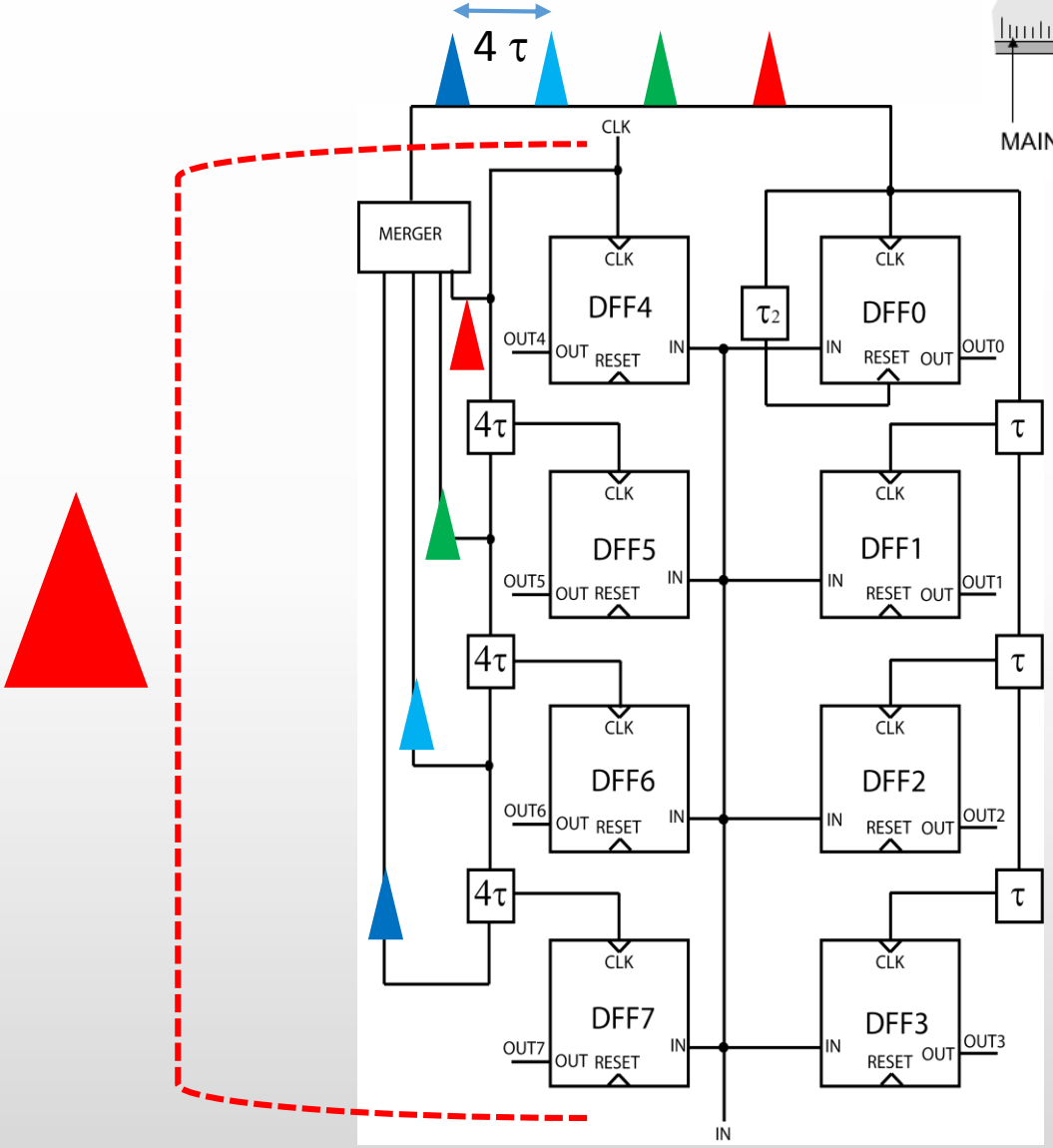
D Flip-Flop



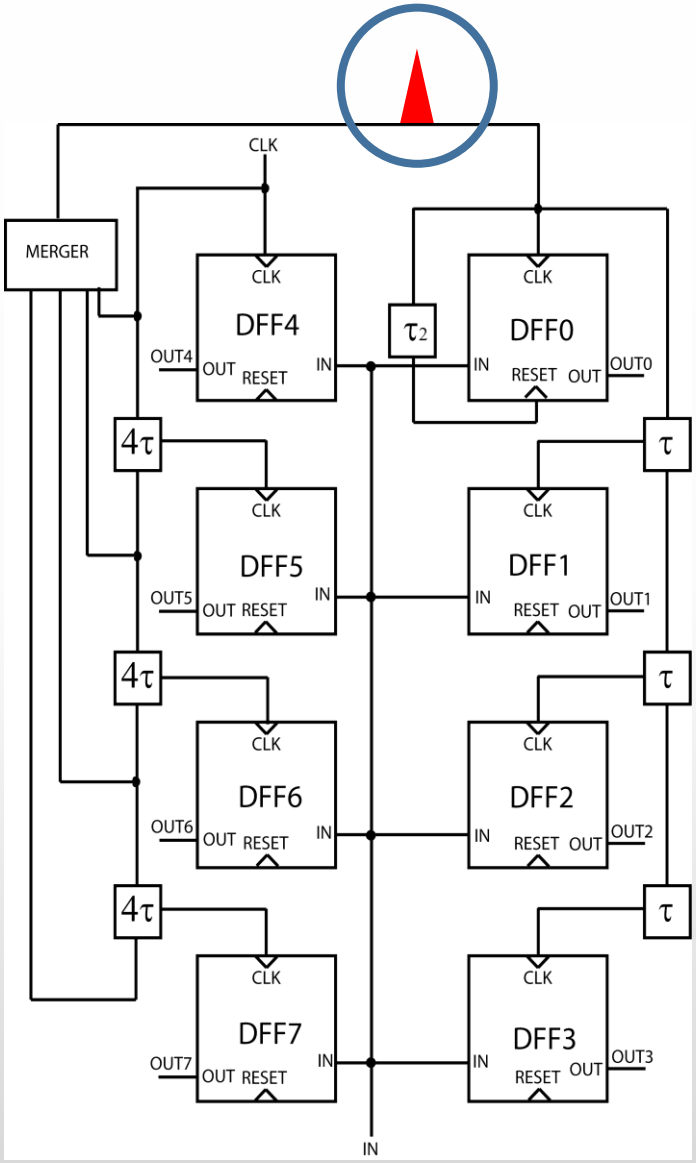


TDC Block Diagram

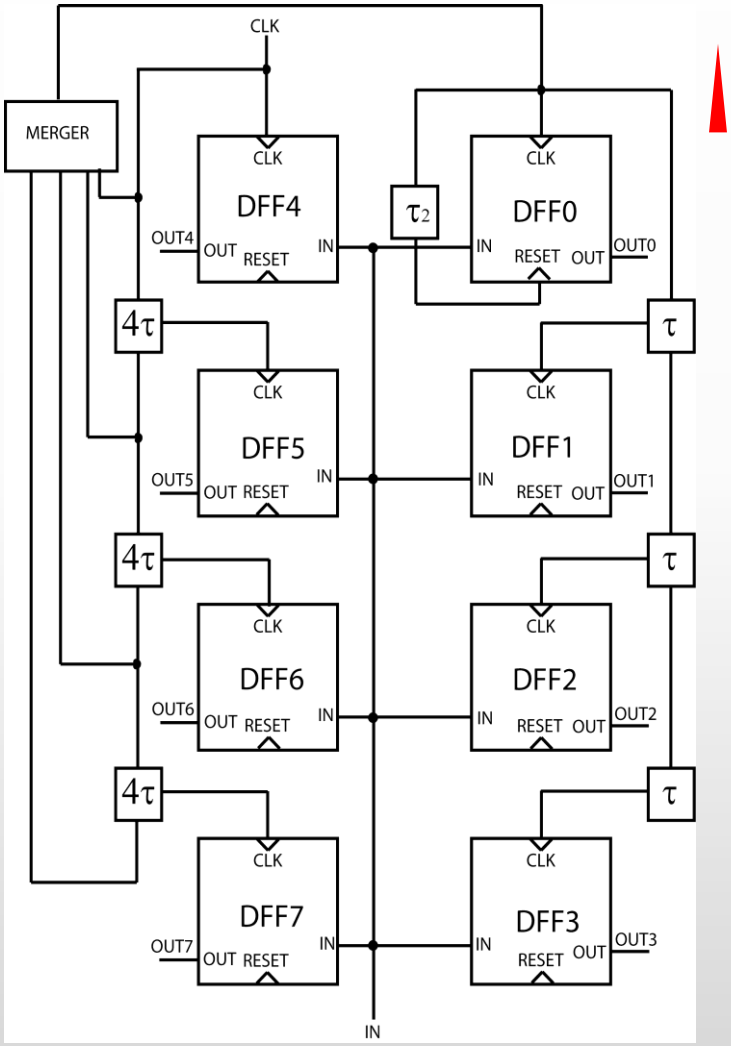




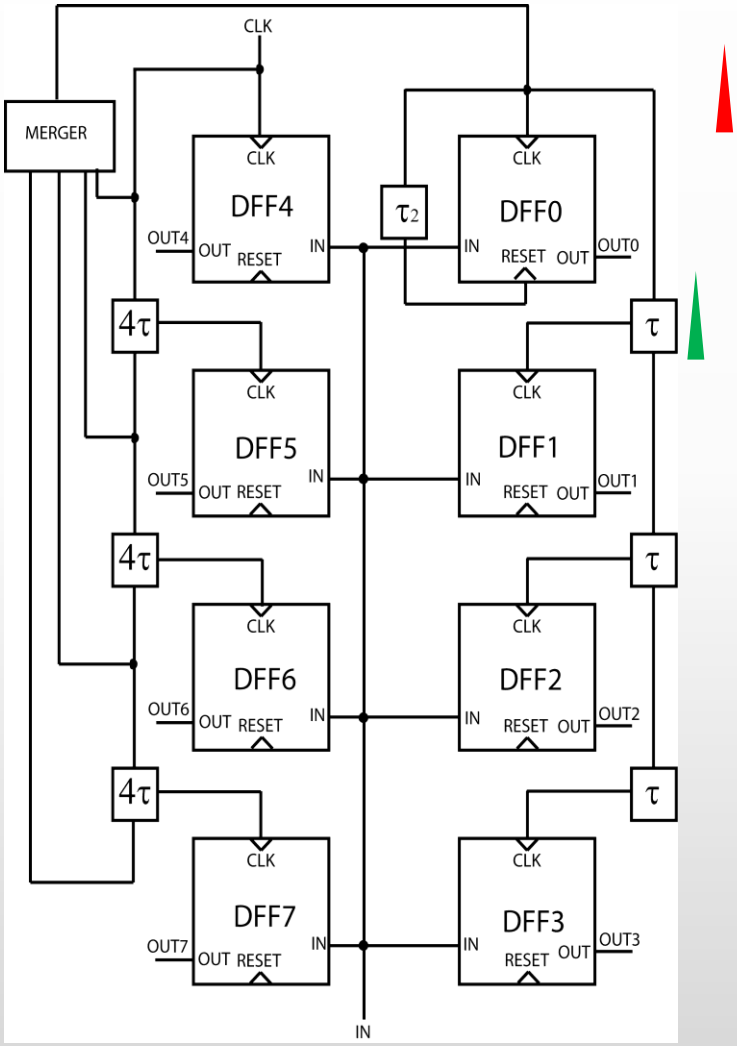
TDC Block Diagram



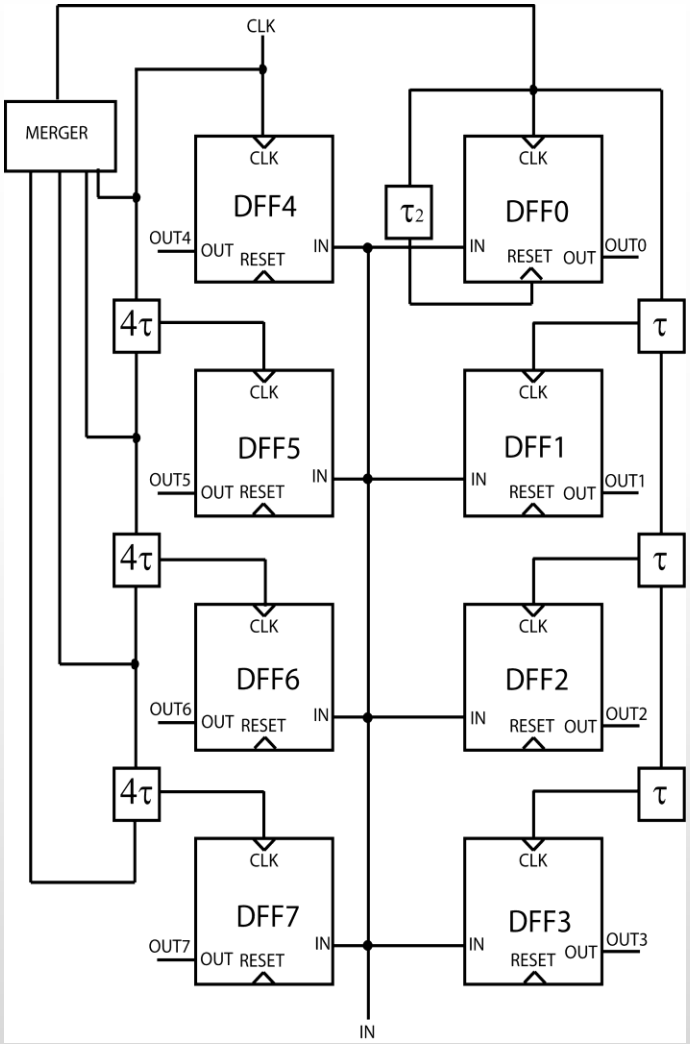
TDC Block Diagram



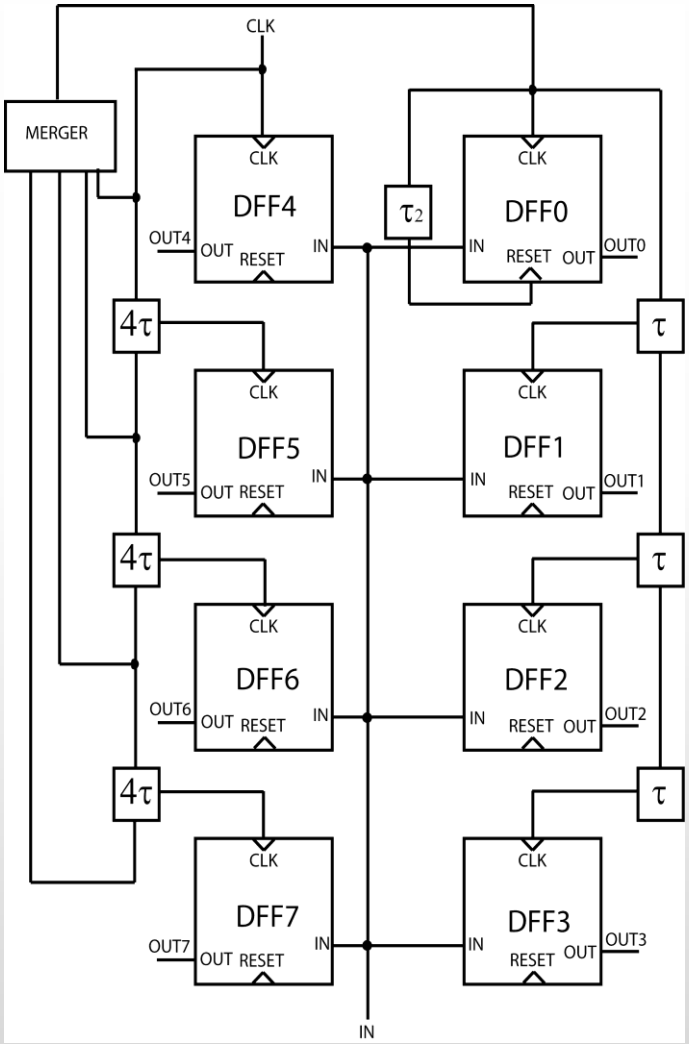
TDC Block Diagram



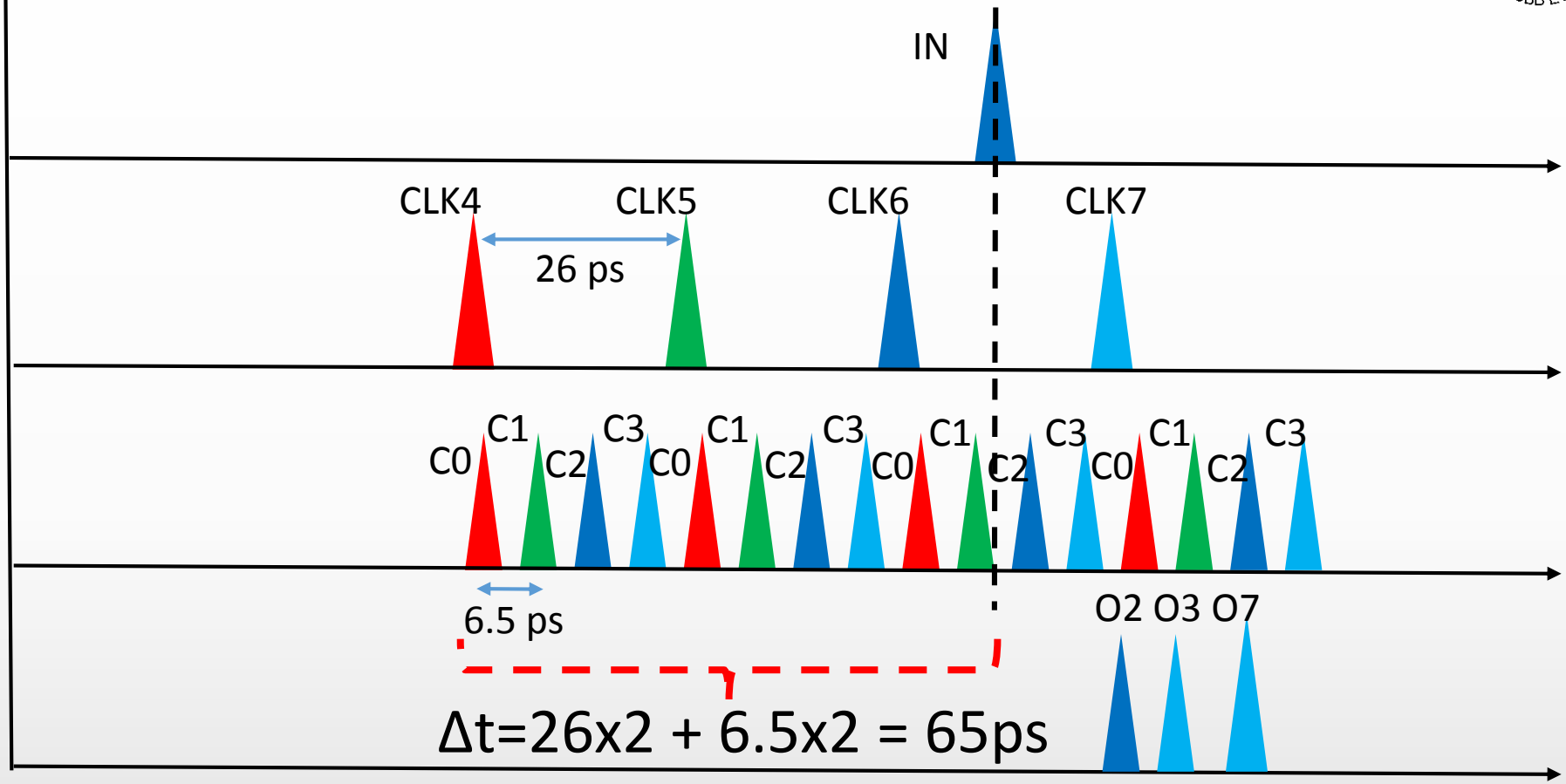
TDC Block Diagram

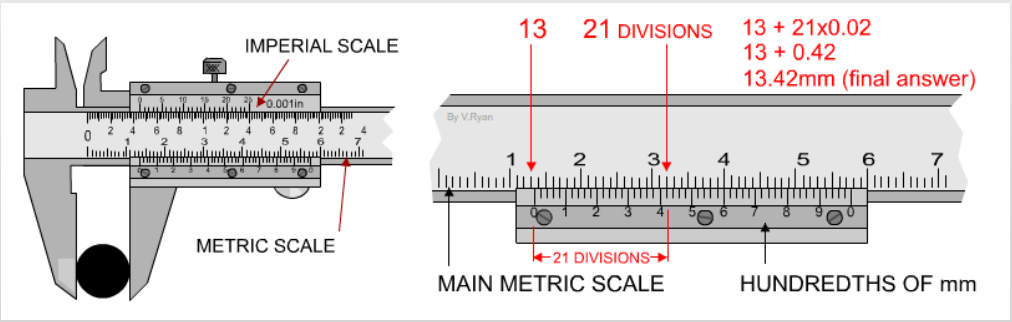


TDC Block Diagram



TDC Timing for Δt=69 ps





1000 1100

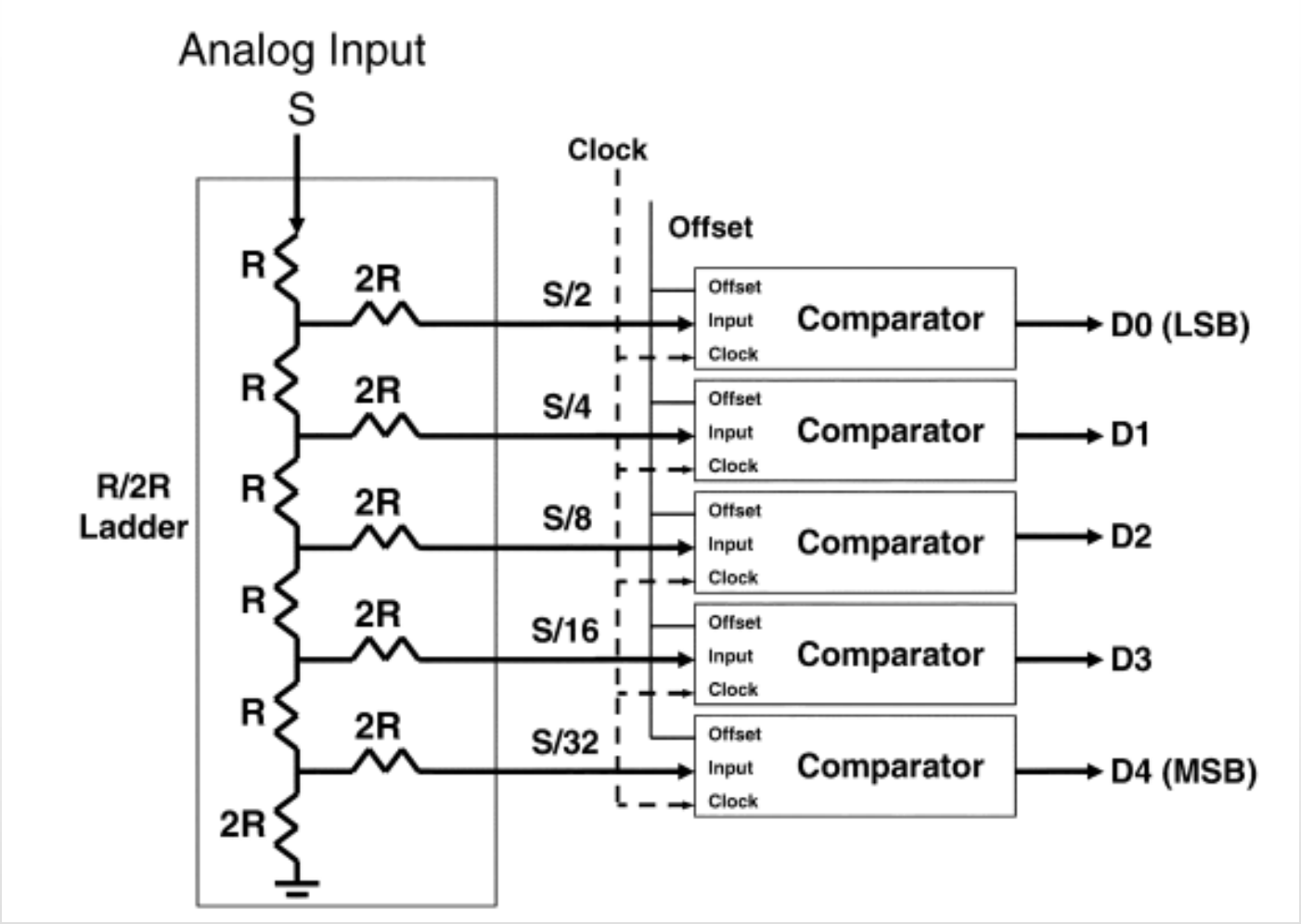
O7-O6-O5-O4 O3-O2-O1-O0

TDC Decoder Look-up Table

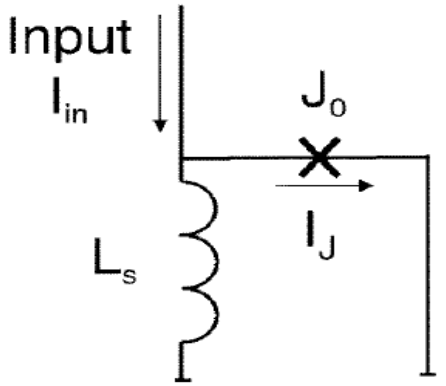
O7 – O4	O3 – O0	TDC OUTPUT	ΔT (ps)
0001	0001	0000	0
0001	001X	0001	6.5
0001	01XX	0010	13
0001	1XXX	0011	19.5
001X	0001	0100	26
001X	001X	0101	32.5
001X	01XX	0110	39
001X	1XXX	0111	45.5
01XX	0001	1000	52
01XX	001X	1001	58.5
01XX	01XX	1010	65
01XX	1XXX	1011	71.5
1XXX	0001	1100	78
1XXX	001X	1101	84.5
1XXX	01XX	1110	91
1XXX	1XXX	1111	97.5

Analog to Digital Converter

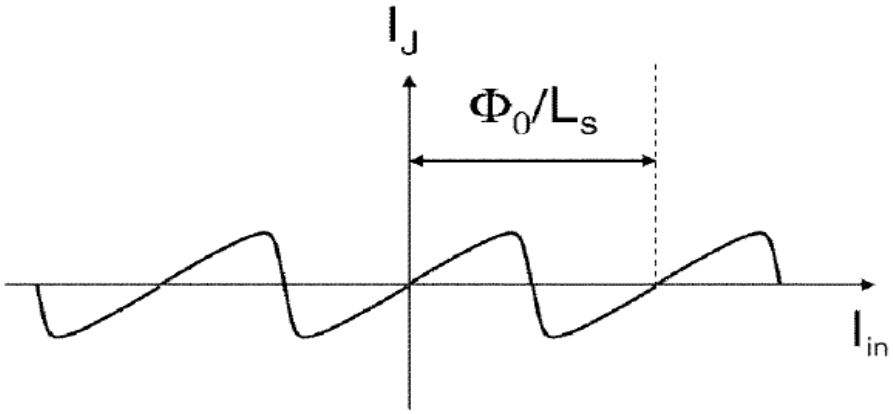
Flash ADC


Analog Input
S
Clock
Offset
R
2R
S/2
Offset
Input
Clock
Comparator
D0 (LSB)
R
2R
S/4
Comparator
D1
R/2R
Ladder
R
2R
S/8
Comparator
D2
R
2R
S/16
Comparator
D3
R
2R
S/32
Comparator
D4 (MSB)
2R

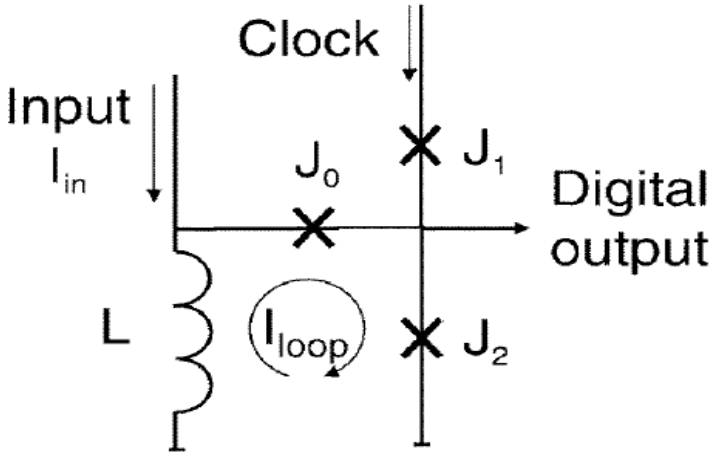
1-bit Comparator



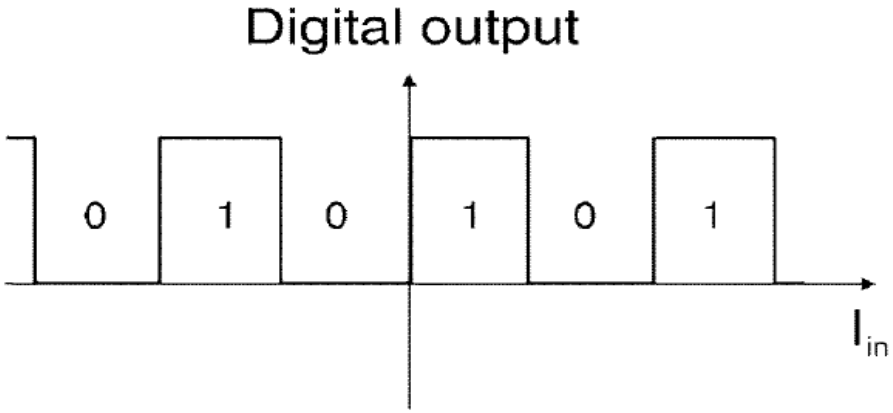
(a)



(b)

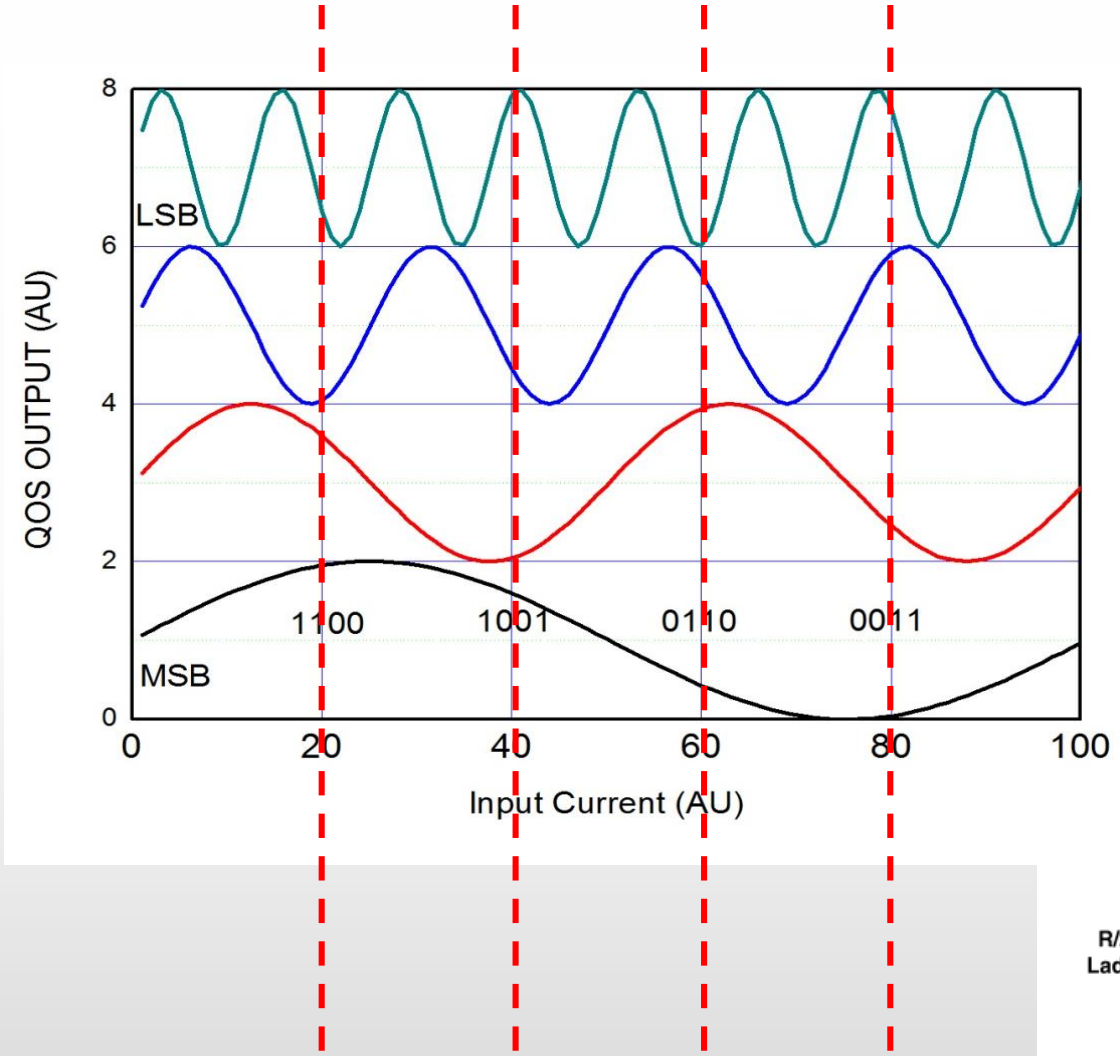


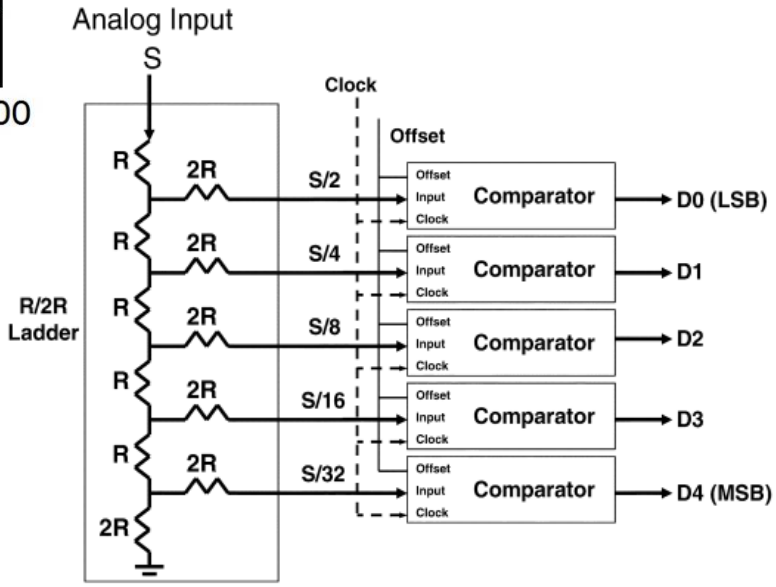
(c)



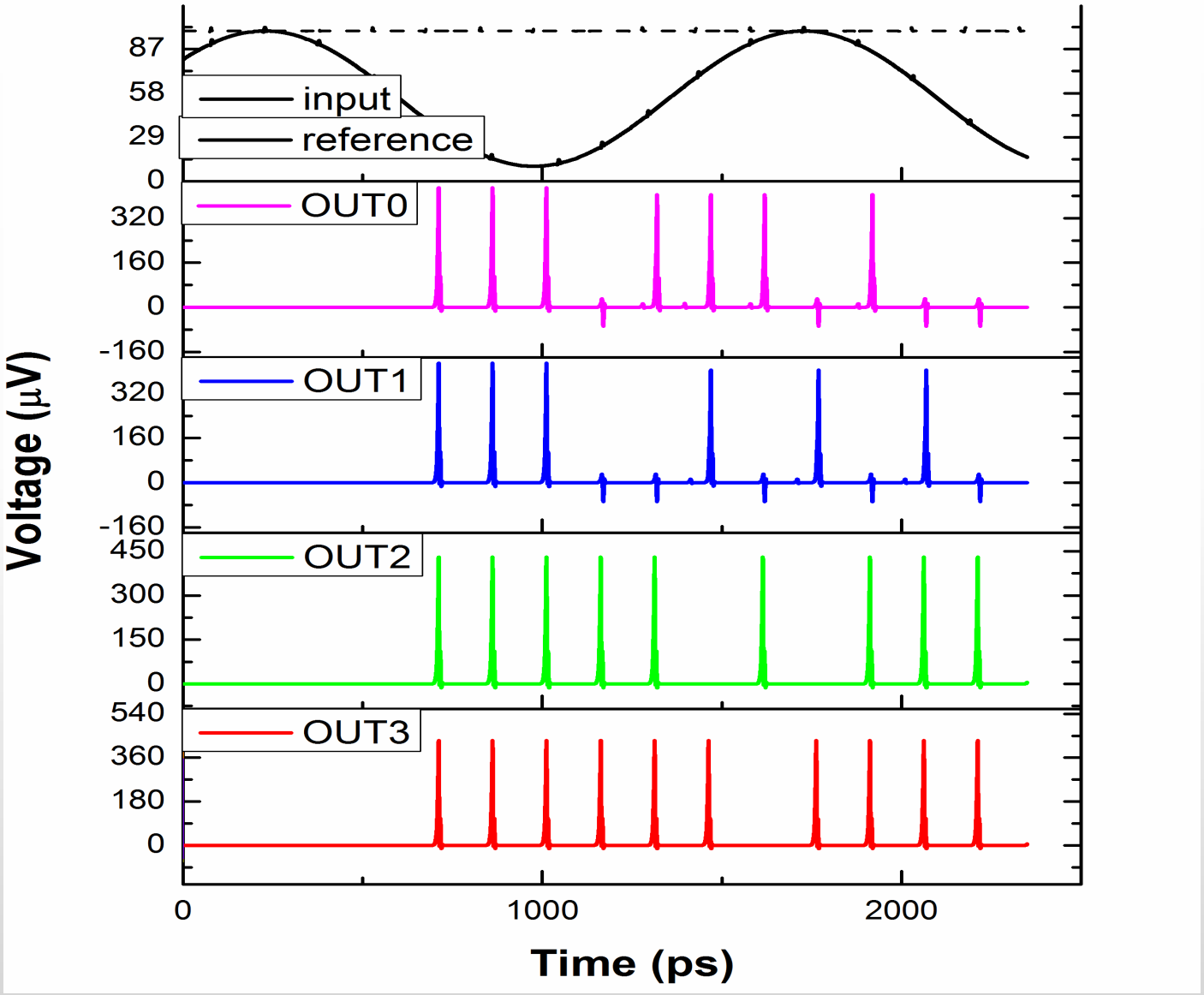
(d)

Flash ADC

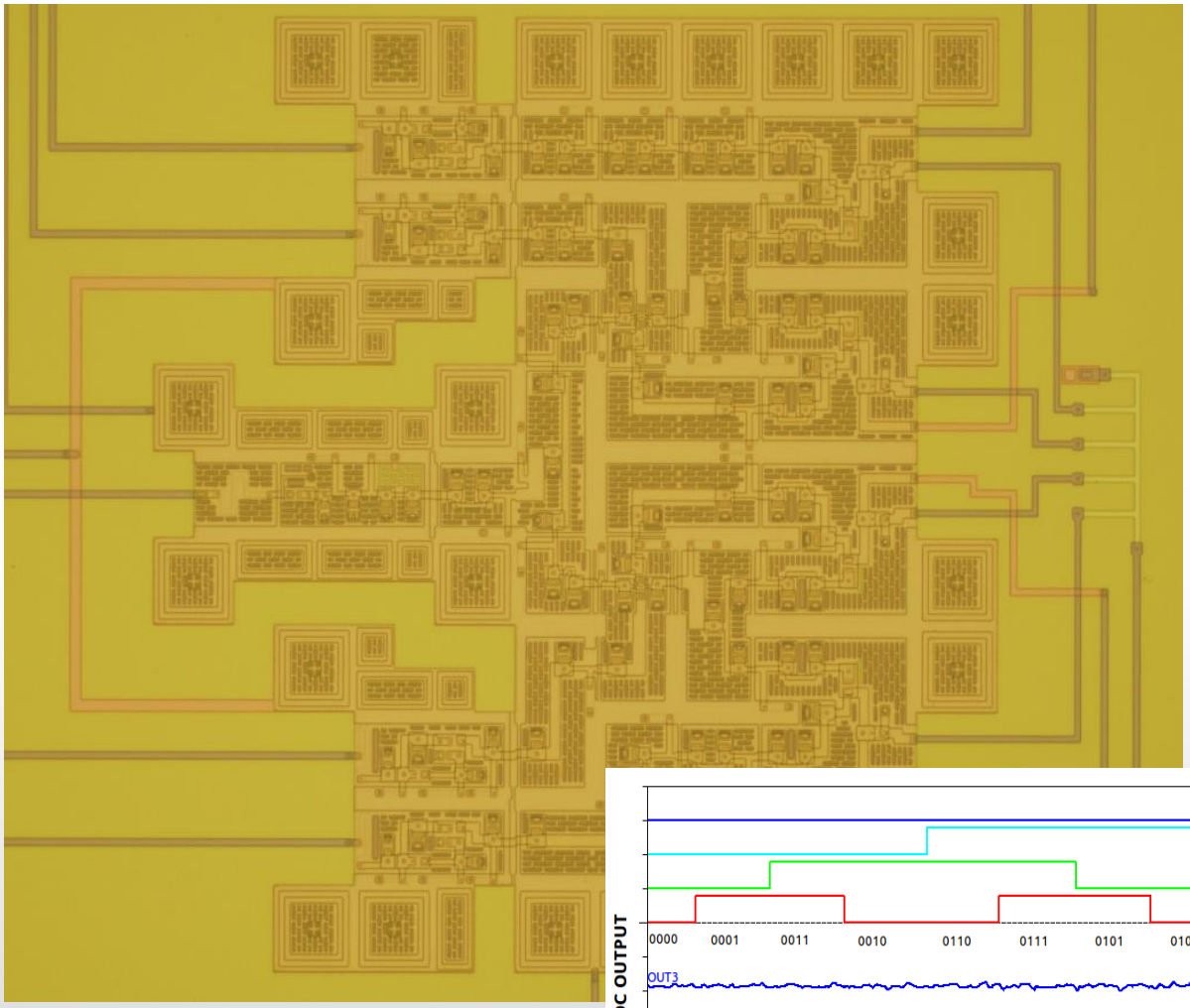

QOS OUTPUT (AU)
Input Current (AU)
LSB
MSB
1100
1001
0110
0011
0
2
4
6
8
0
20
40
60
80
100

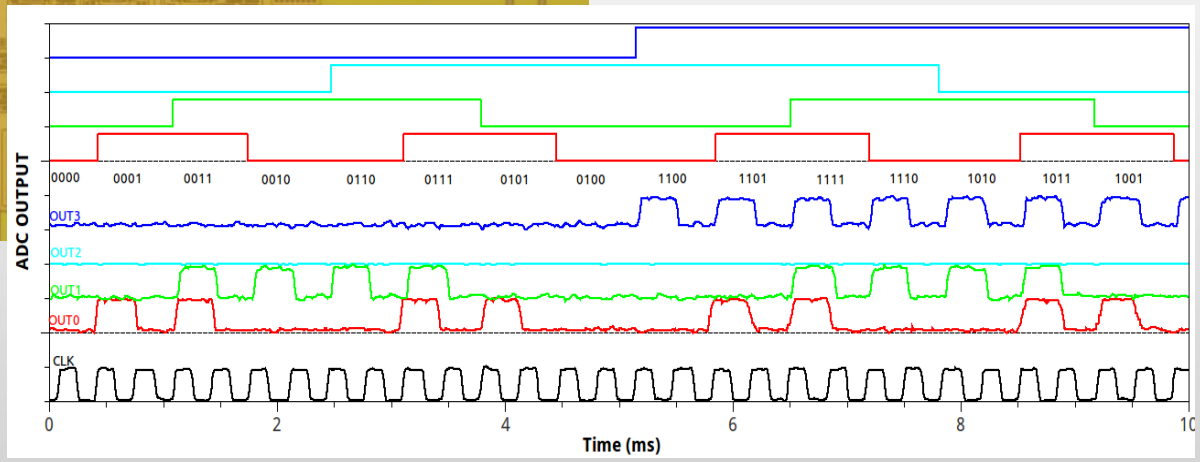

Analog Input
S
Clock
Offset
R
2R
R/2R Ladder
S/2
S/4
S/8
S/16
S/32
Offset
Input
Clock
Comparator
D0 (LSB)
D1
D2
D3
D4 (MSB)

Flash ADC


input
reference
OUT0
OUT1
OUT2
OUT3
Voltage (μV)
Time (ps)
87
58
29
0
320
160
0
-160
320
160
0
-160
450
300
150
0
540
360
180
0
0
1000
2000

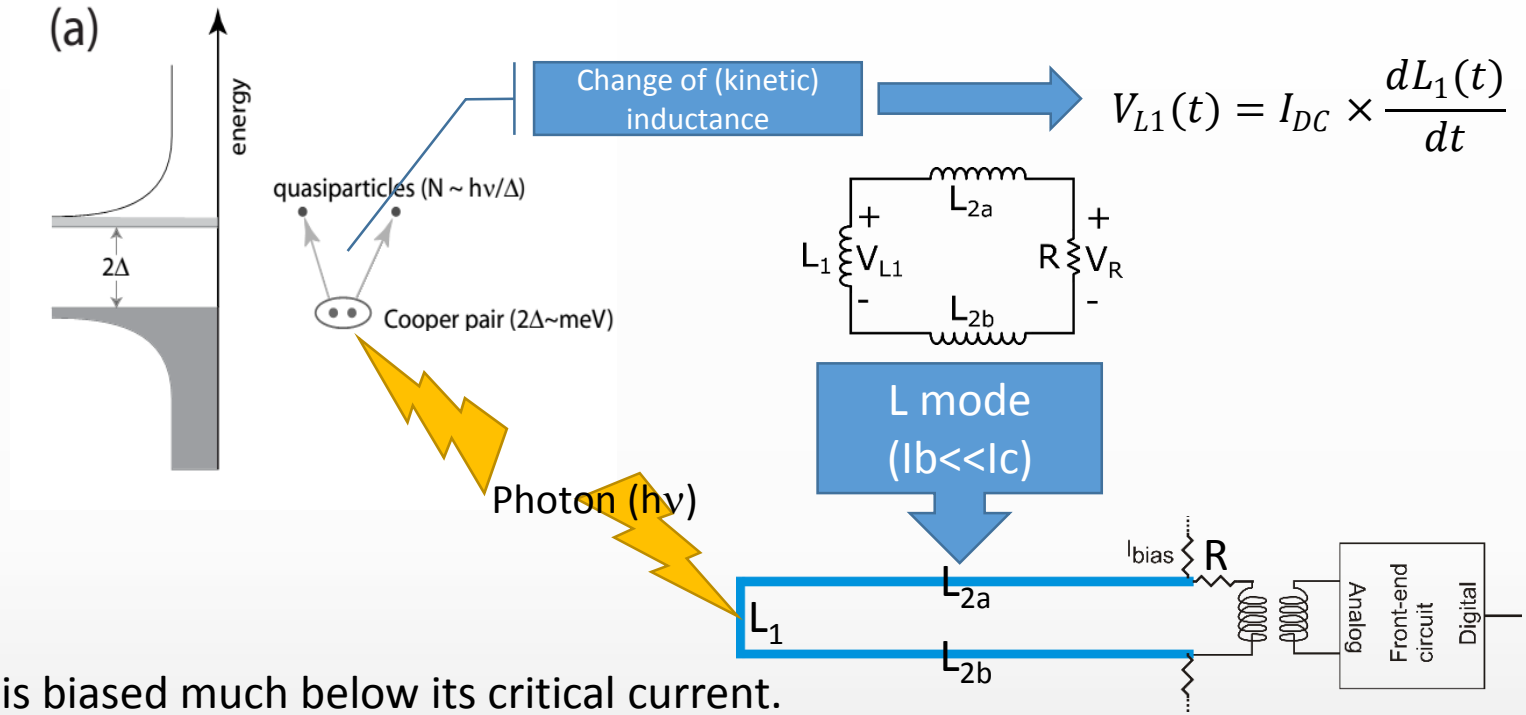
Fabricated Flash ADC (10 GHz, 4 bit)





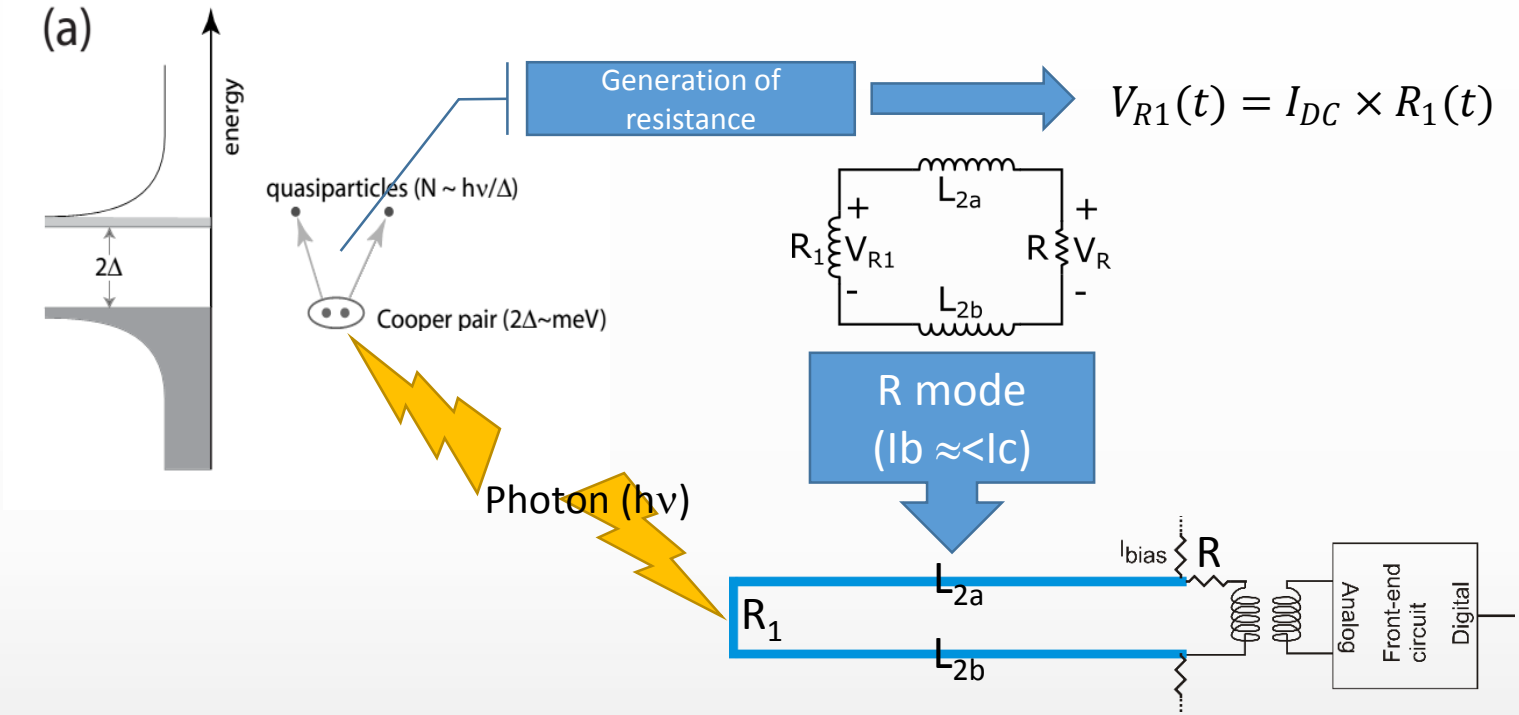
Superconducting Stripline Detectors (SSLD) Towards Megapixel Neutron Imager

SSLD (Kinetic Inductance mode)



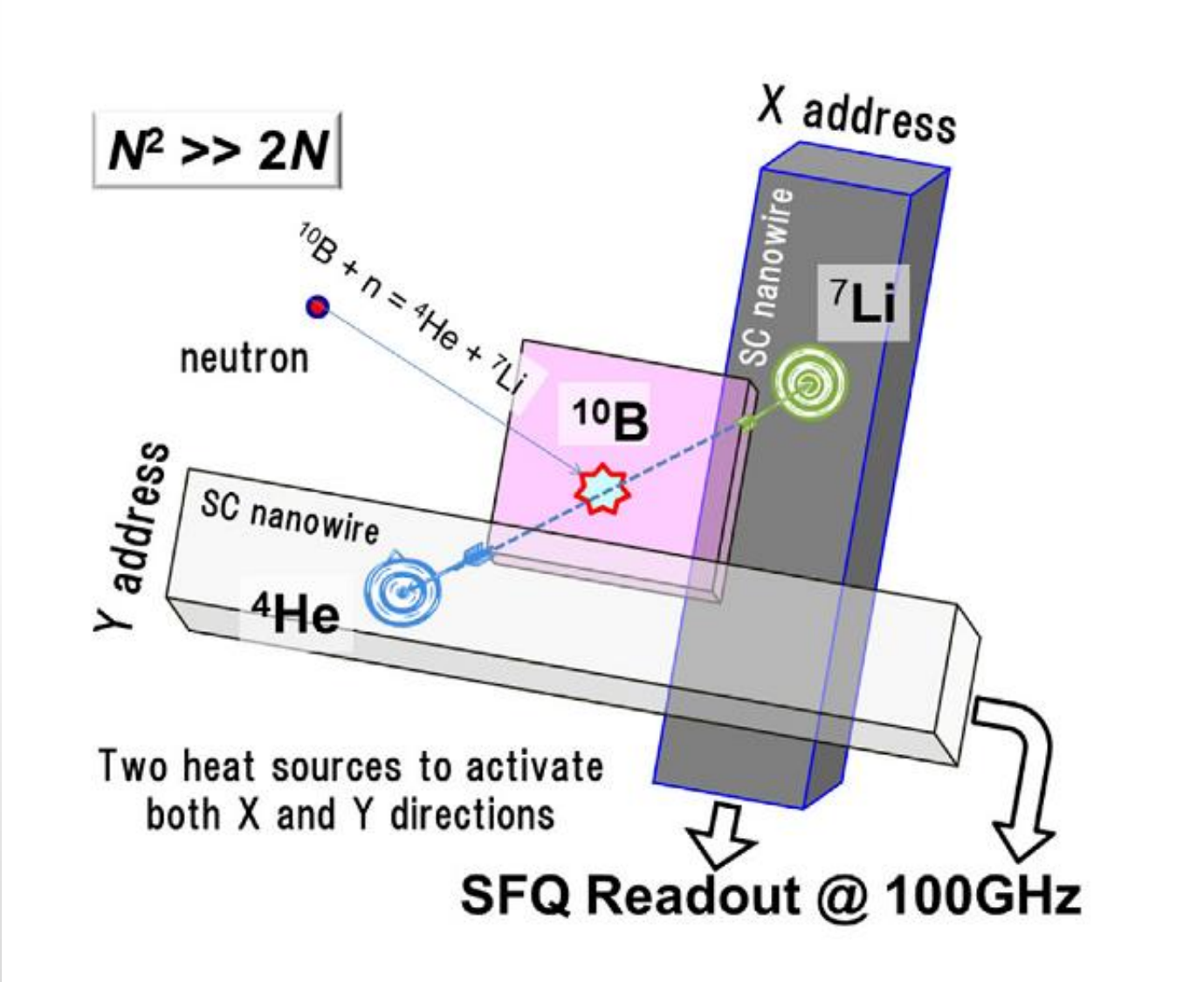
1. SSPD is biased much below its critical current.
2. Arrival of a photon over part of the SSLD (L_1) breaks cooper pairs and generates quasiparticles.
3. Change of number of cooper pairs and quasiparticles cause change of the (kinetic) inductance (ΔL_1).
4. Change of inductance causes a voltage response to be generated (dL_1/dt).
5. This voltage response is converted to current with an series resistance R in the loop ($I= V_R/R$)
6. The current is coupled to the read-out circuit and digitized to be processed by the encoder circuit.

SSLD (Resistive Mode)



1. SSLD is biased just below its critical current.
2. Arrival of a photon over part of the SSLD destroys superconductivity locally.
3. Destruction of superconductivity causes a local resistance increase.
4. Generation of a resistance causes voltage signal under constant bias current.
5. This voltage response is converted to current with an series resistance R in the loop ($I = V_R/R$)
6. The current is coupled to the read-out circuit and digitized to be processed by the encoder circuit.

Boron Layer



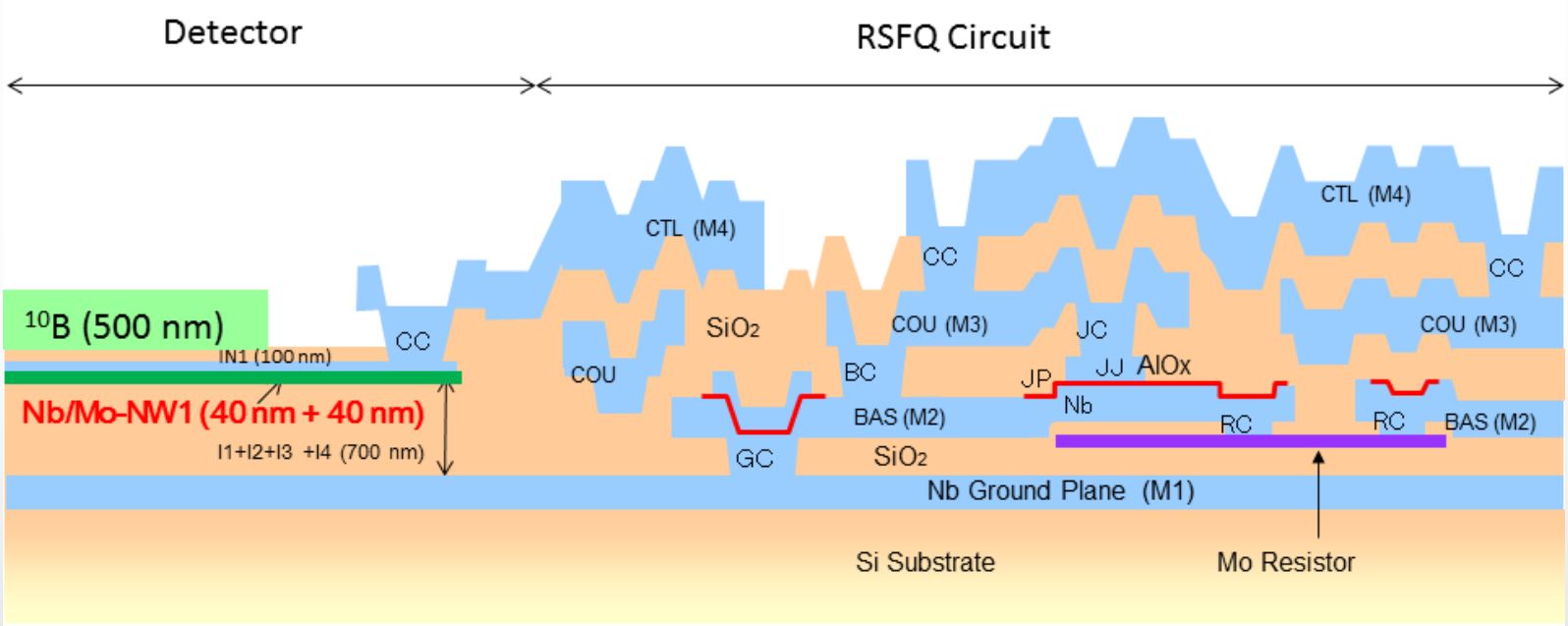
Ishida et al. DOI 10.1007/s10909-014-1159-8

Fabrication Process

NAGOYA UNIVERSITY

ASC2014
August 11, '14
Charlotte

AIST New Process for Monolithic Chip



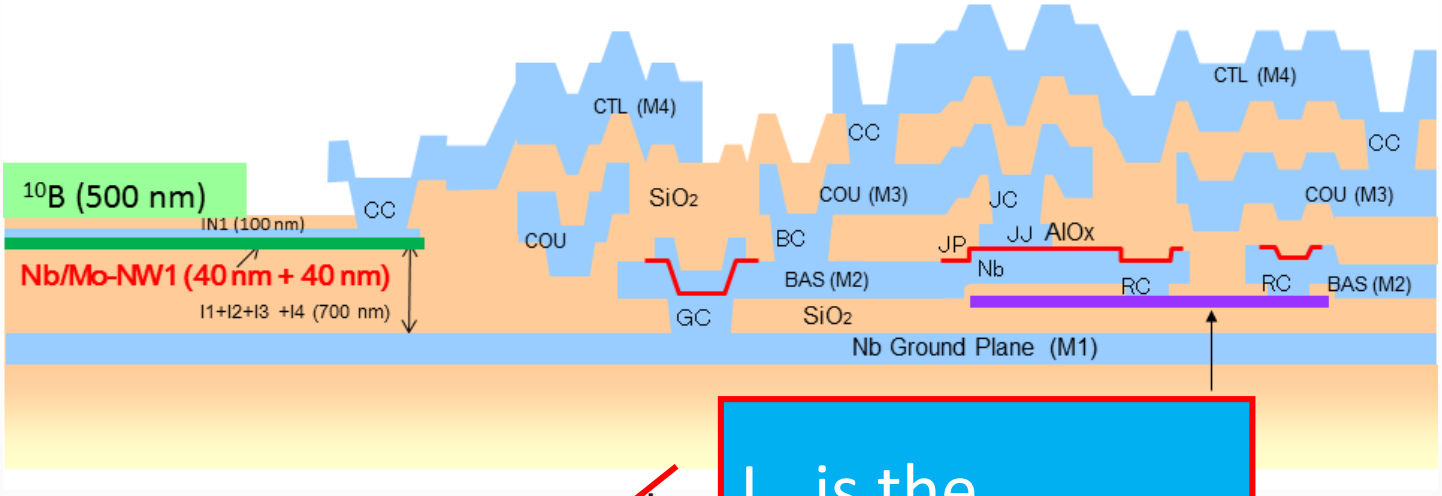
- ✓ J_c of 10 kA/cm^2 is applied.
- ✓ Die size is 22 mm x 22 mm.
- ✓ Test of detector array was carried out with a monolithic chip without a ^{10}B layer.

CRAVITY AIST

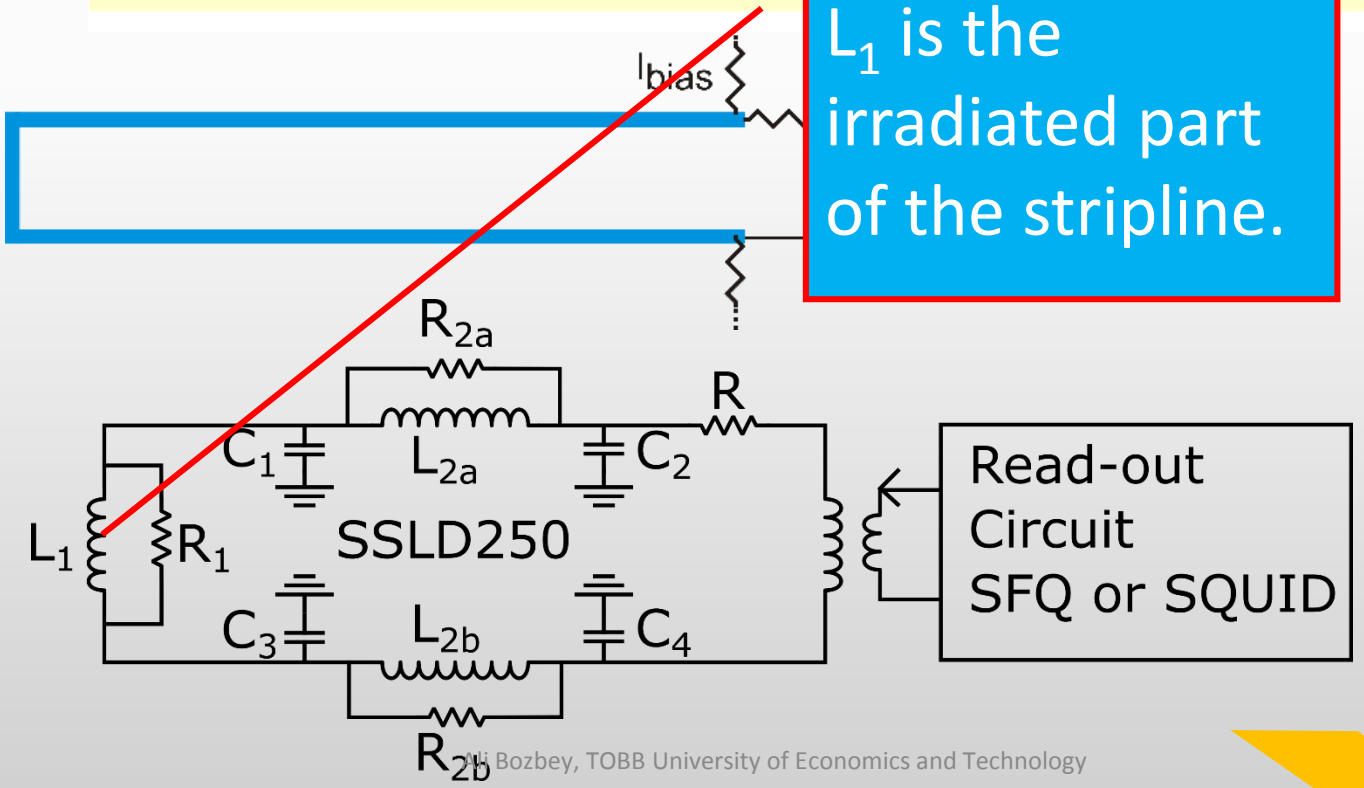
Design Objectives of the SSLD Monolithic Chip

1. Fit inside an AIST new process for a monolithic chip die (22mm*22mm).
2. Achieve 1000*1000 pixel sensor resolution
   - Detector width < 22mm/1000=22μm
3. Have sufficient sensitivity for incoming neutron
4. Have small dead time (~10ns)
5. Use a single bias point
6. Achieve crosstalk free operation and SFQ read-out
7. Operation in both CB-KID or CB-TED modes is acceptable.

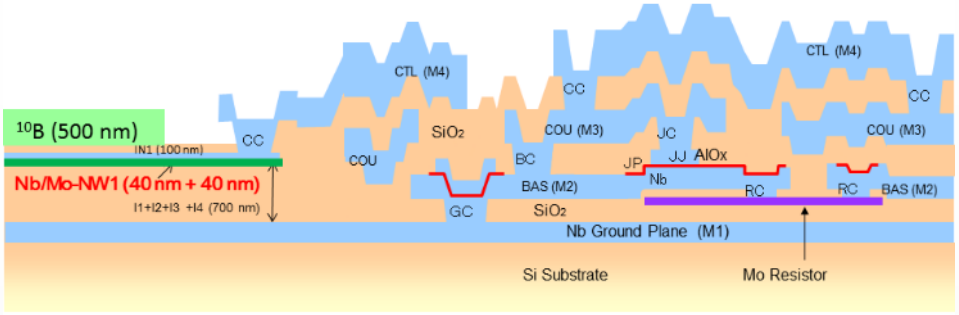
Single SSLD Circuit Model

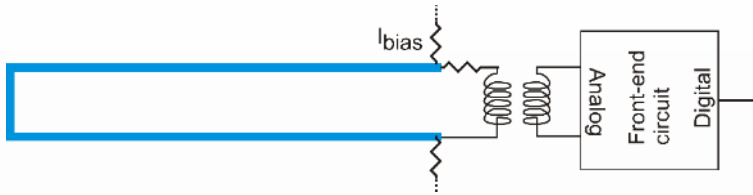


L_1 is the irradiated part of the stripline.



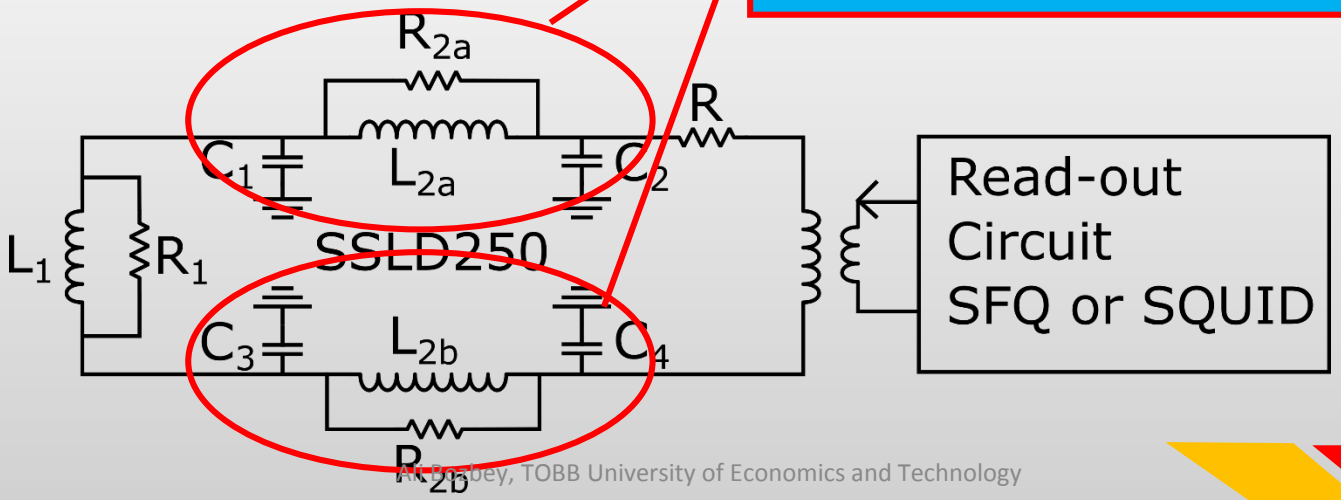
Single SSLD Circuit Model



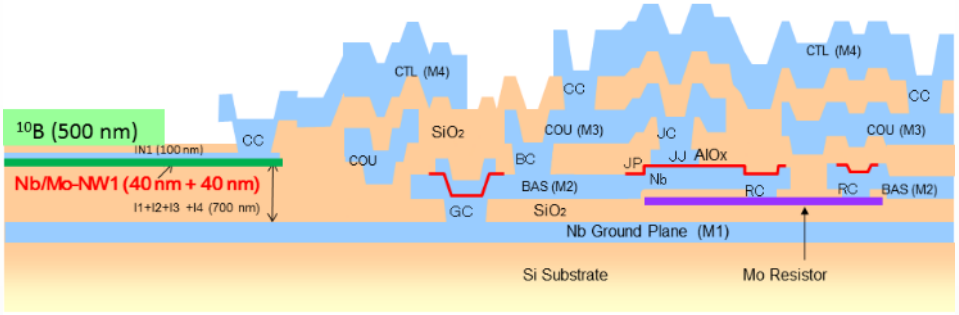


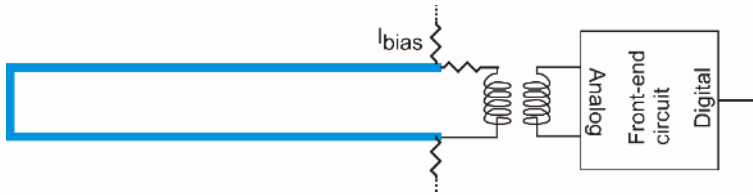
- $L_2 >> L_1$, L_{2a}/L_{2b} ratio is determined by the location of the irradiation on the stripline.
- Shunt resistors represent the resistive layer fabricated under the stripline layer.
- C_1-C_4 : Parasitic capacitance of the stripline

π model for the stripline.

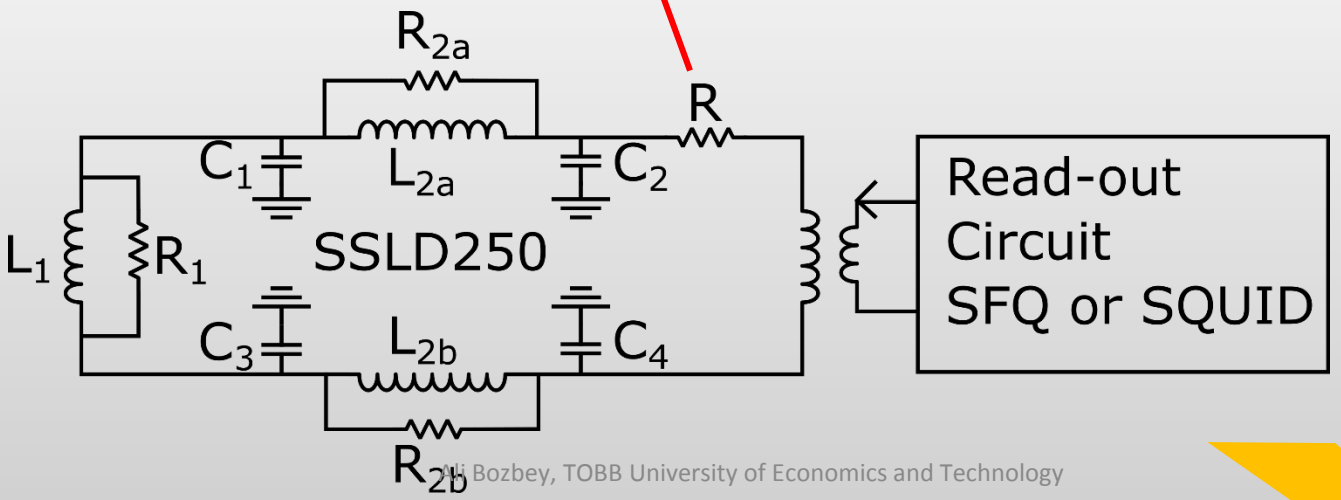


Single SSLD Circuit Model

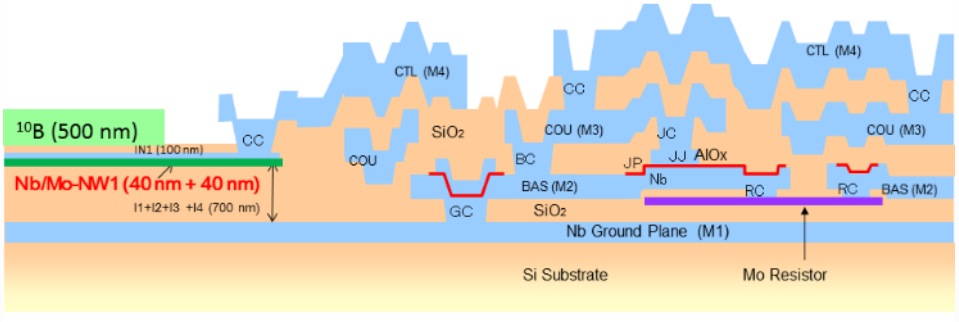


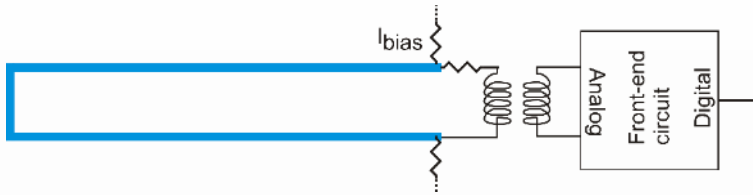


R is the LR loop resistance

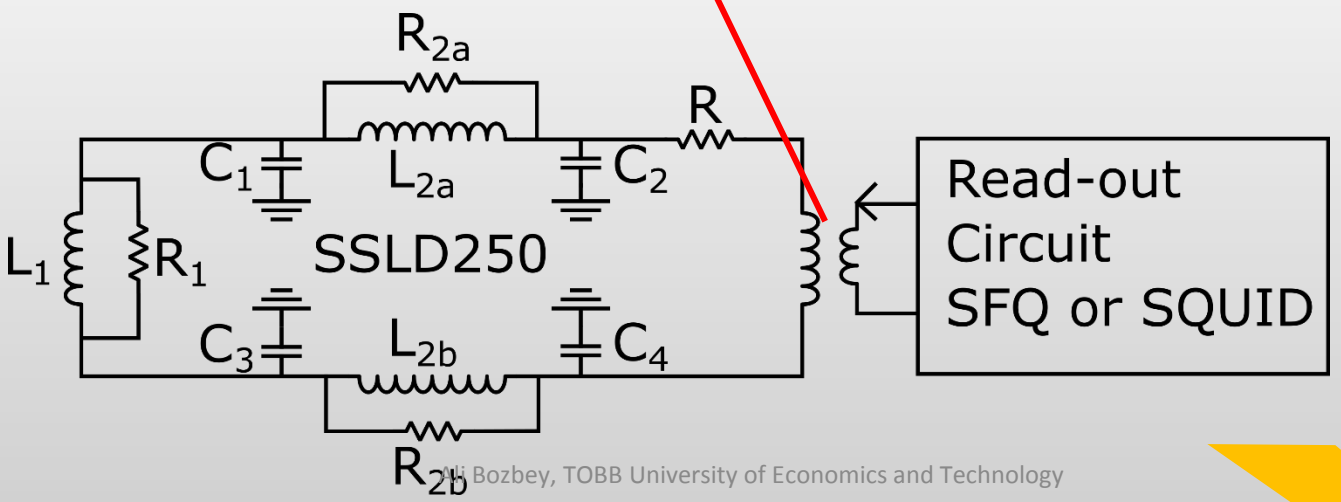


Single SSLD Circuit Model

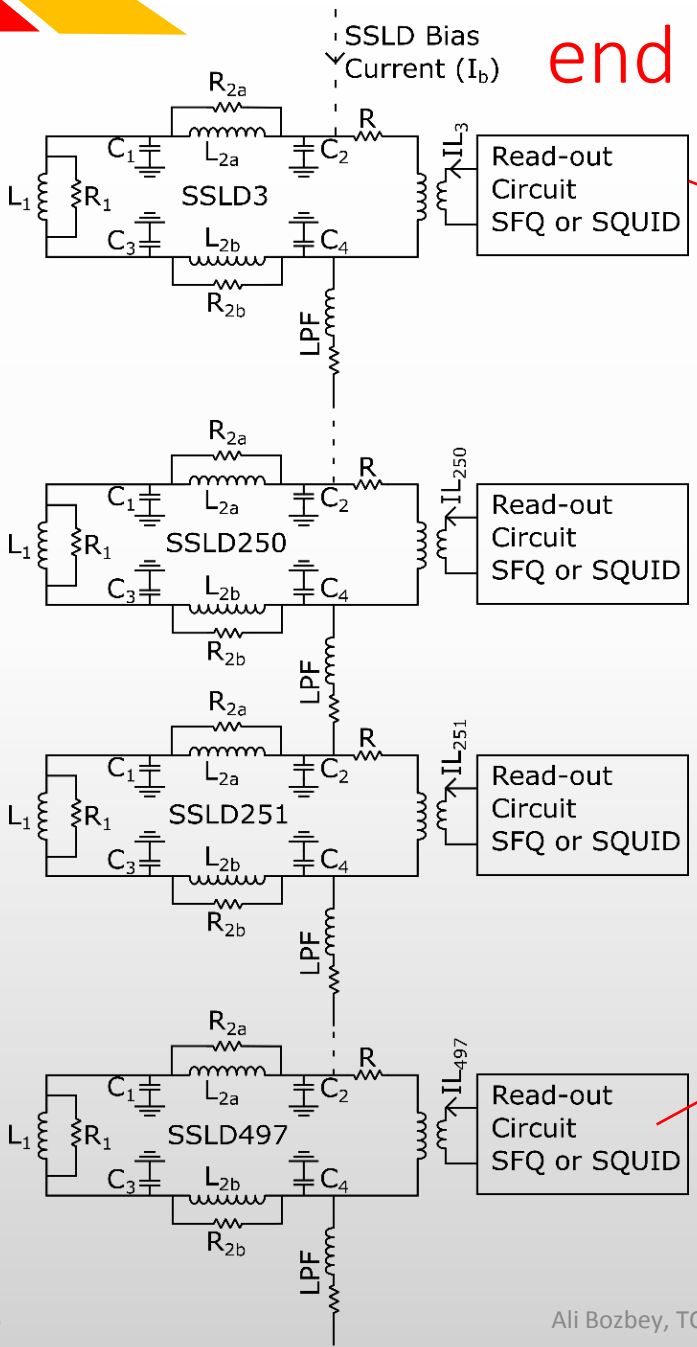


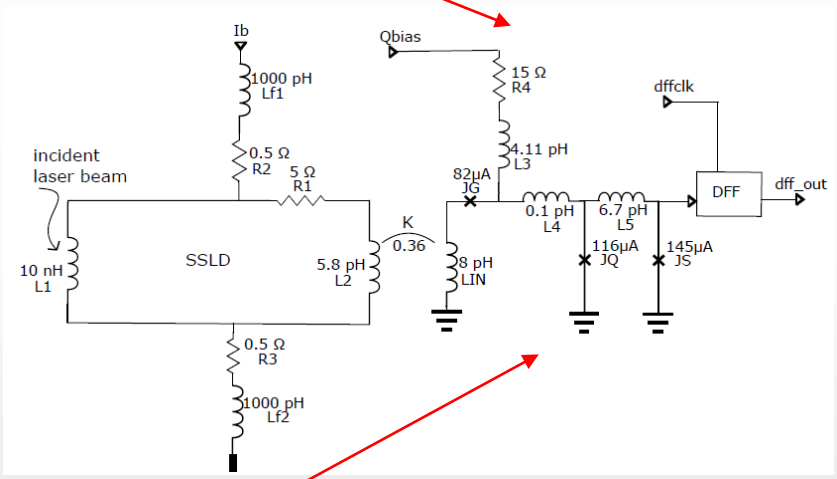


Coil transfers the current associated with the radiation to the read-out circuit.

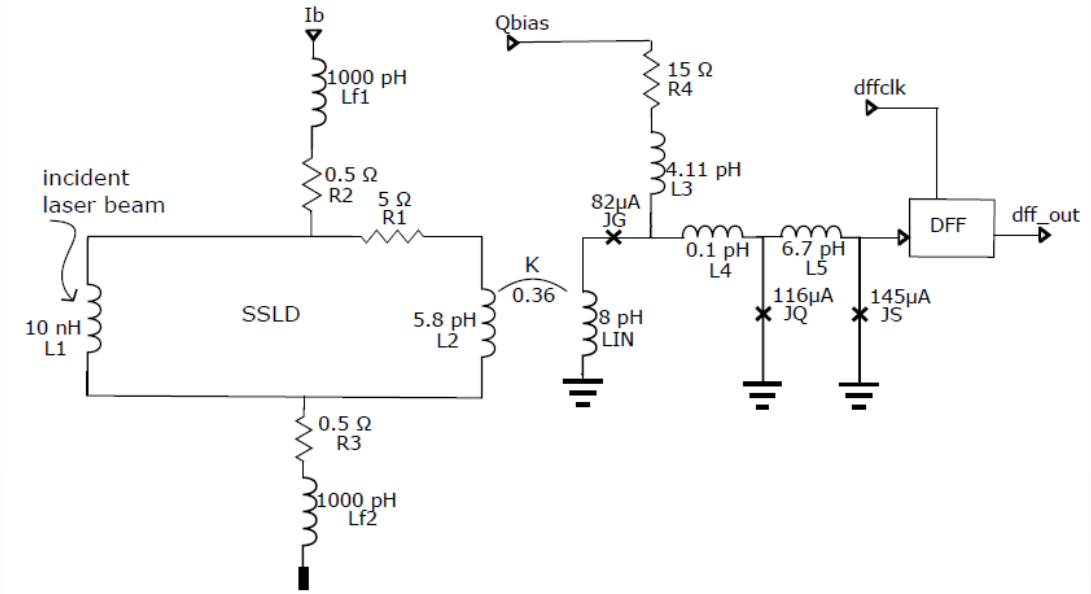


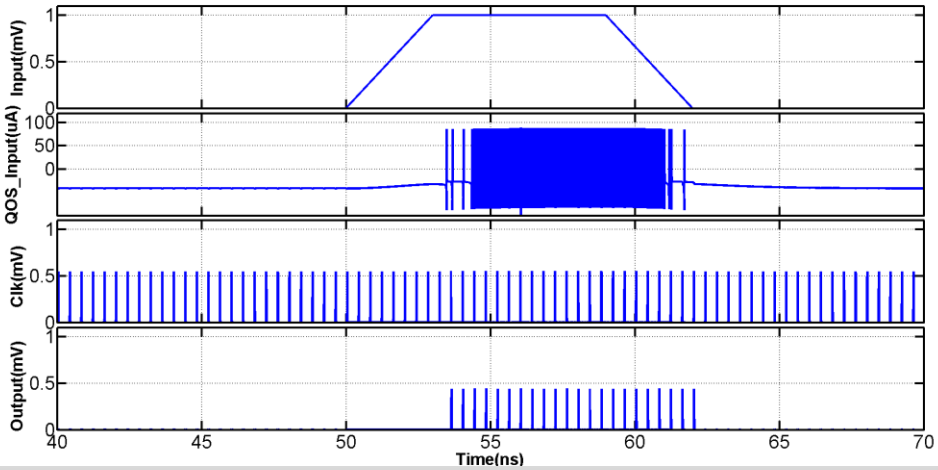
Detector Model and Front-end Circuit

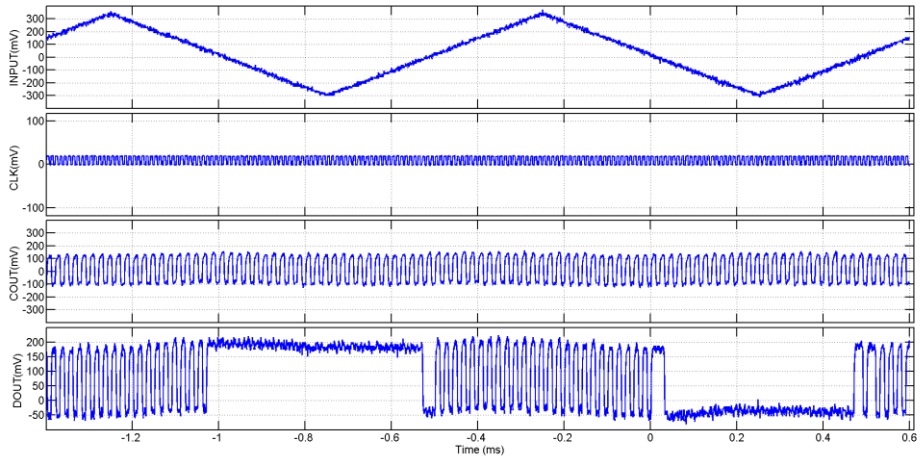




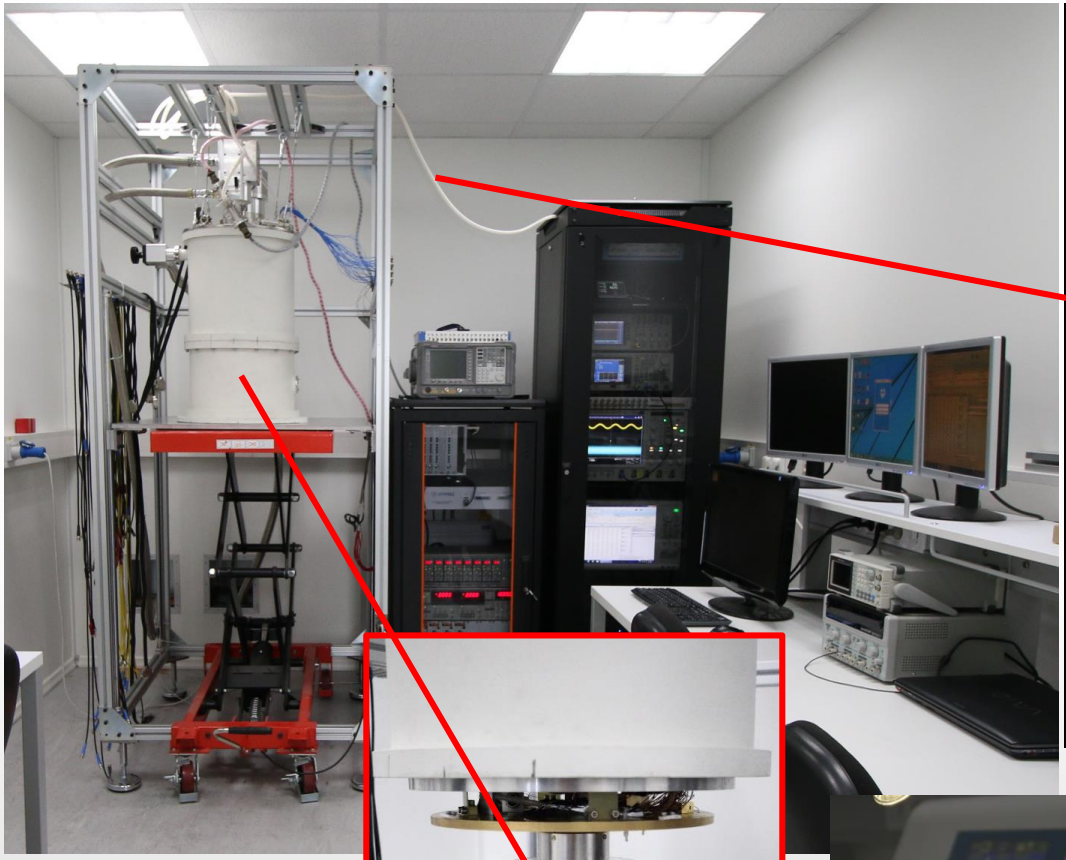
Front-end Circuit: Sim and Exp

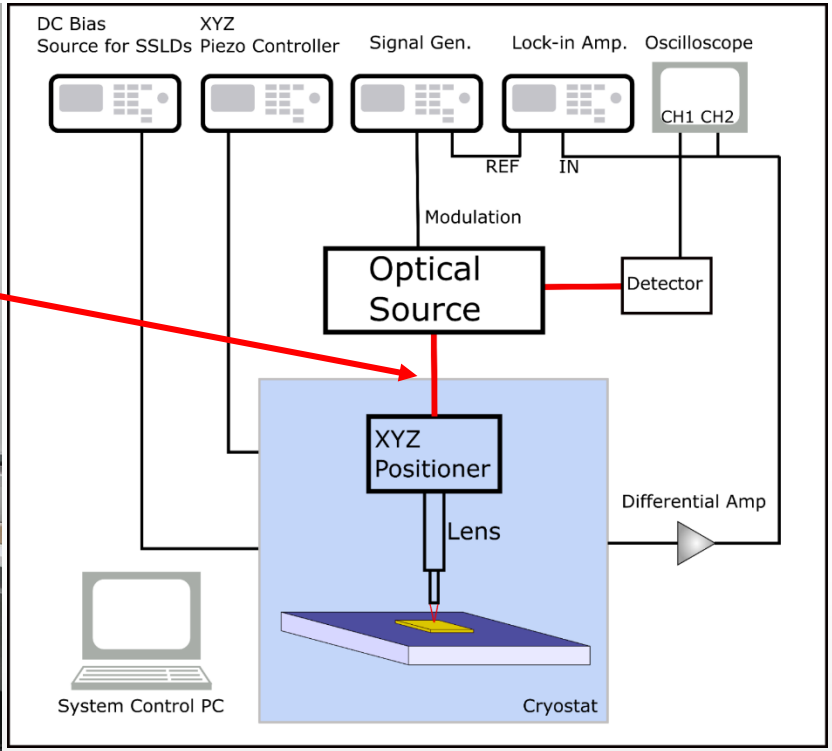


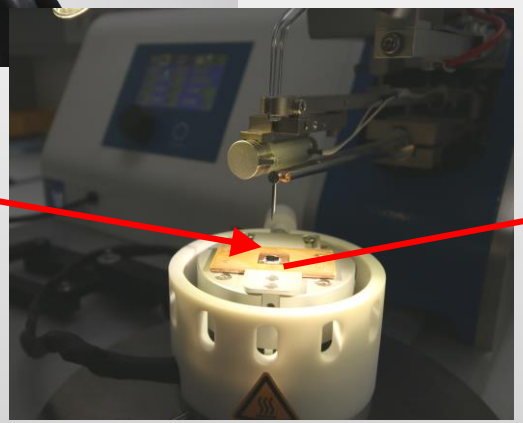


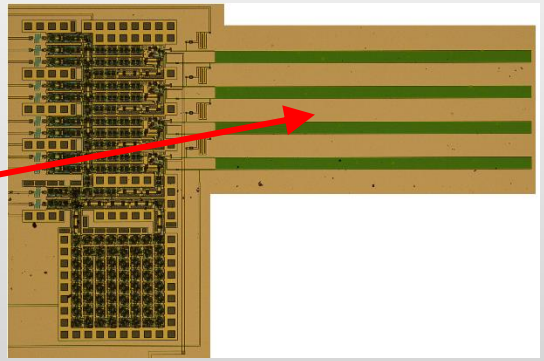


Experimental Setup

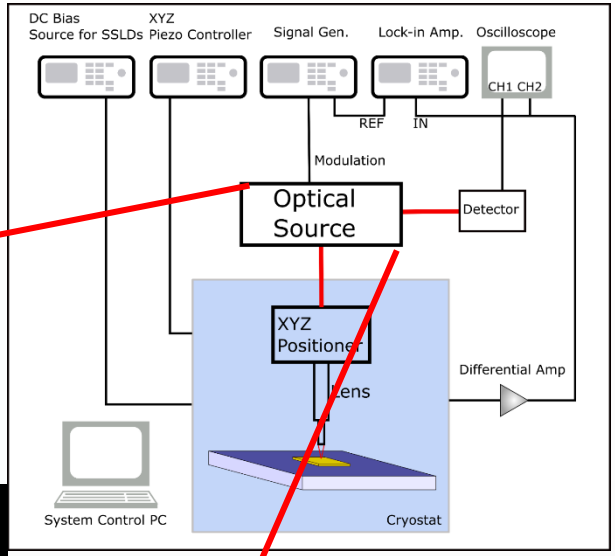


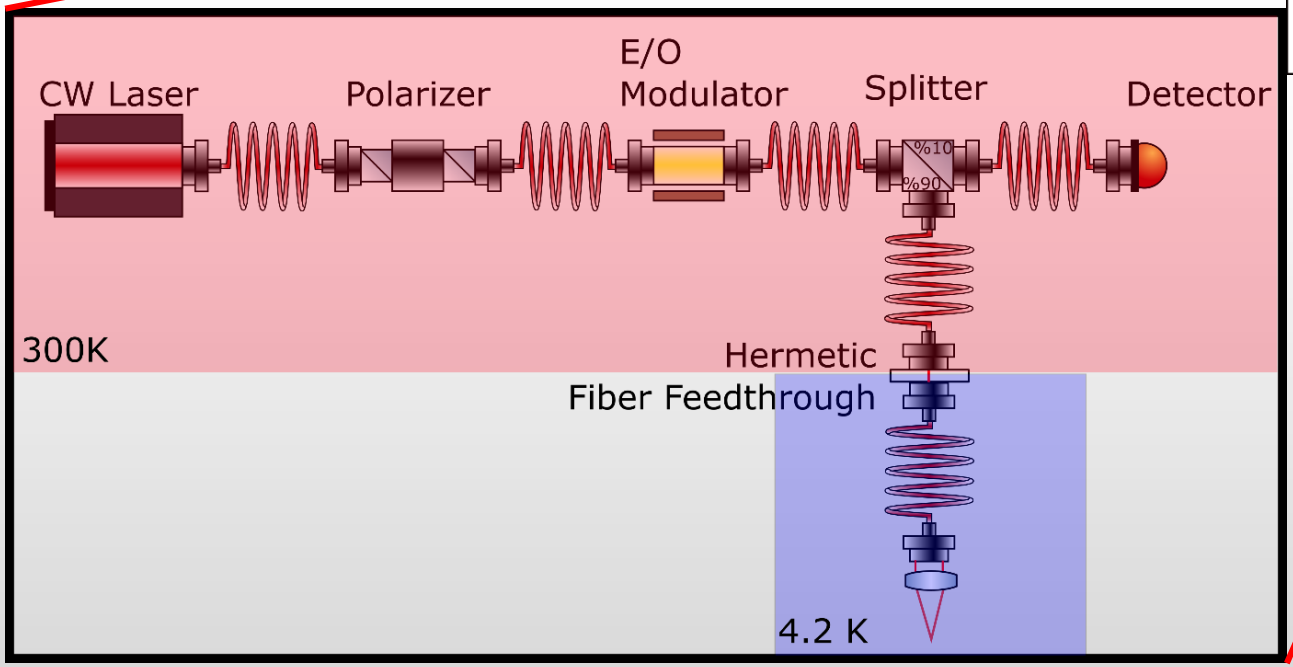




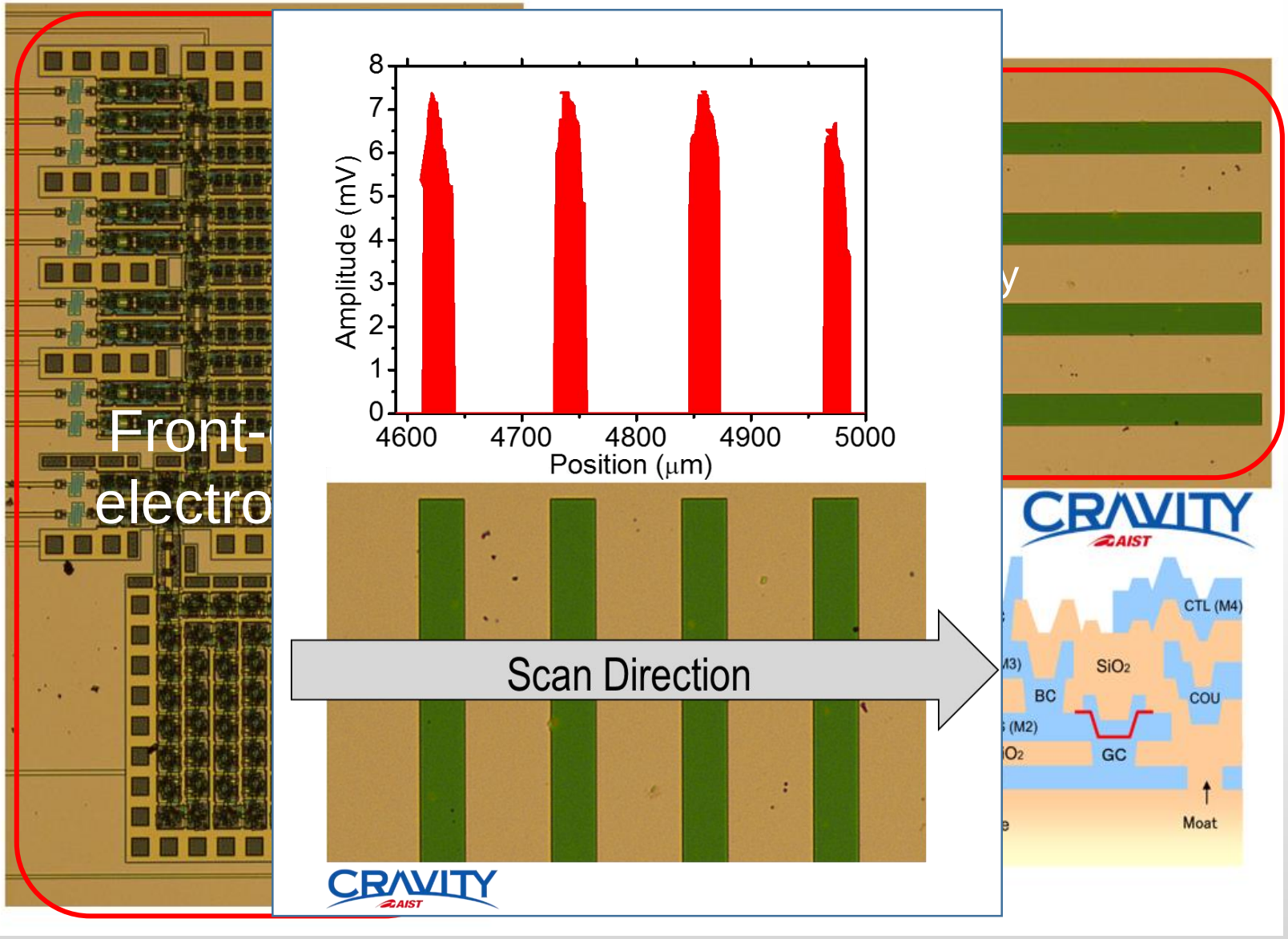


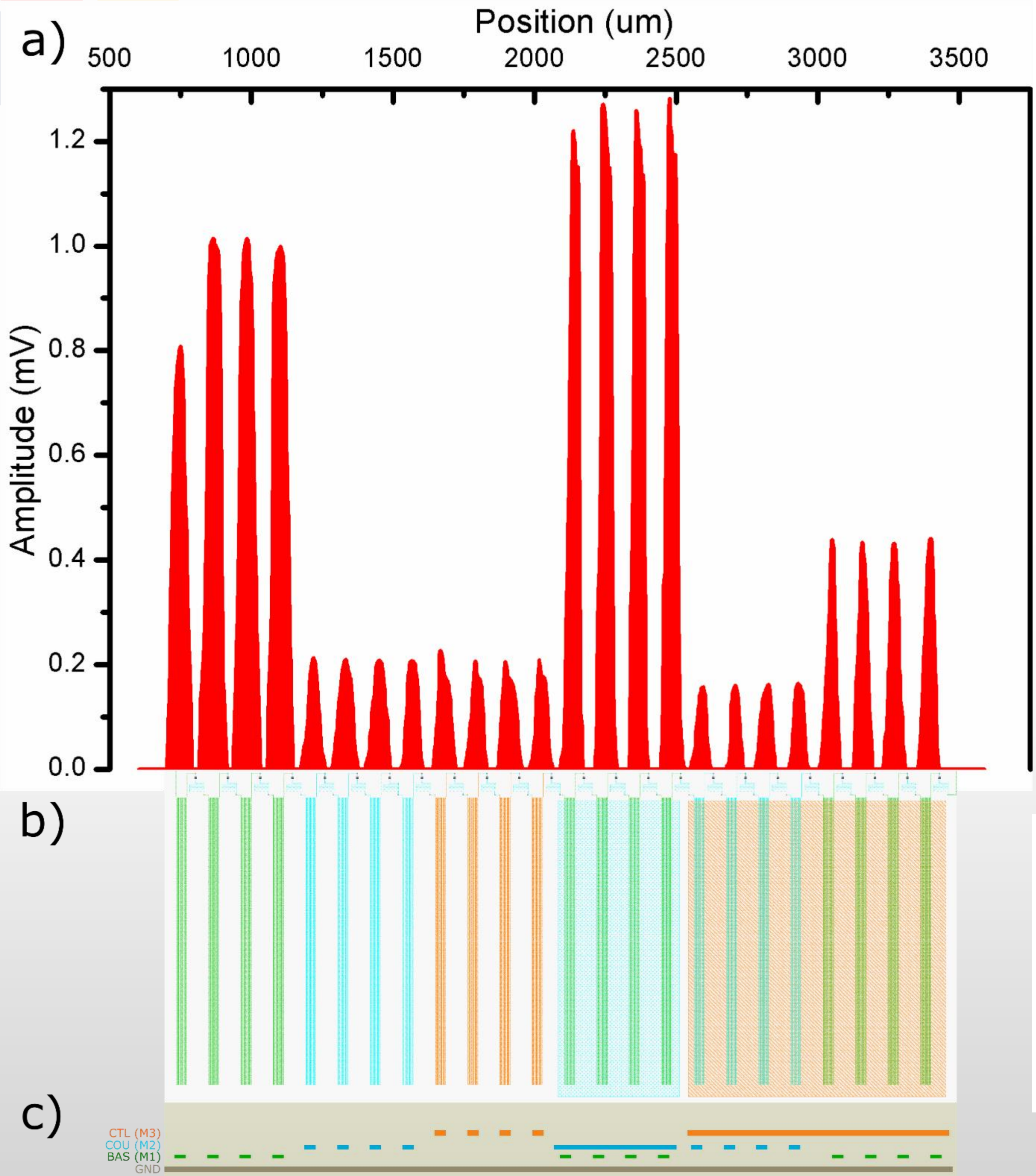
Experimental Setup

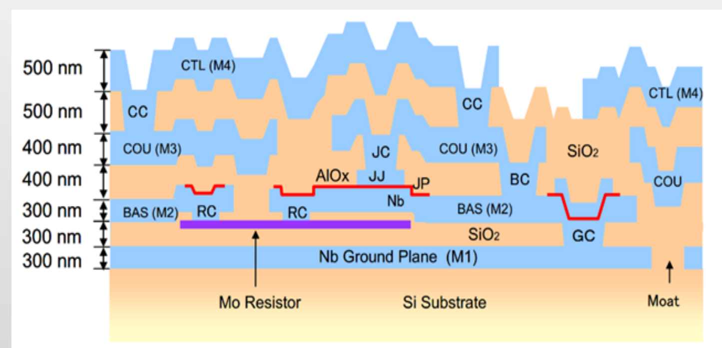




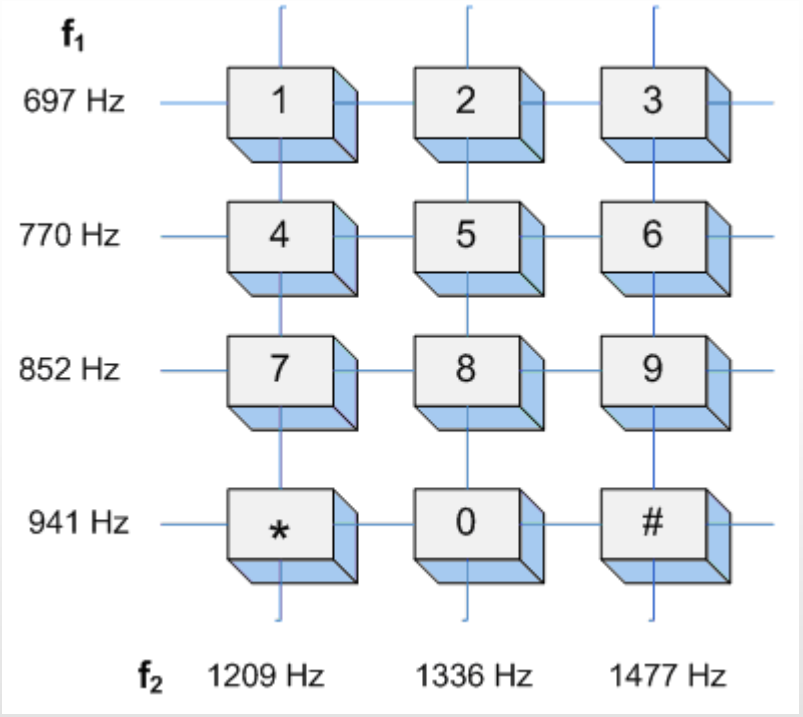
Monolithic IR Detector



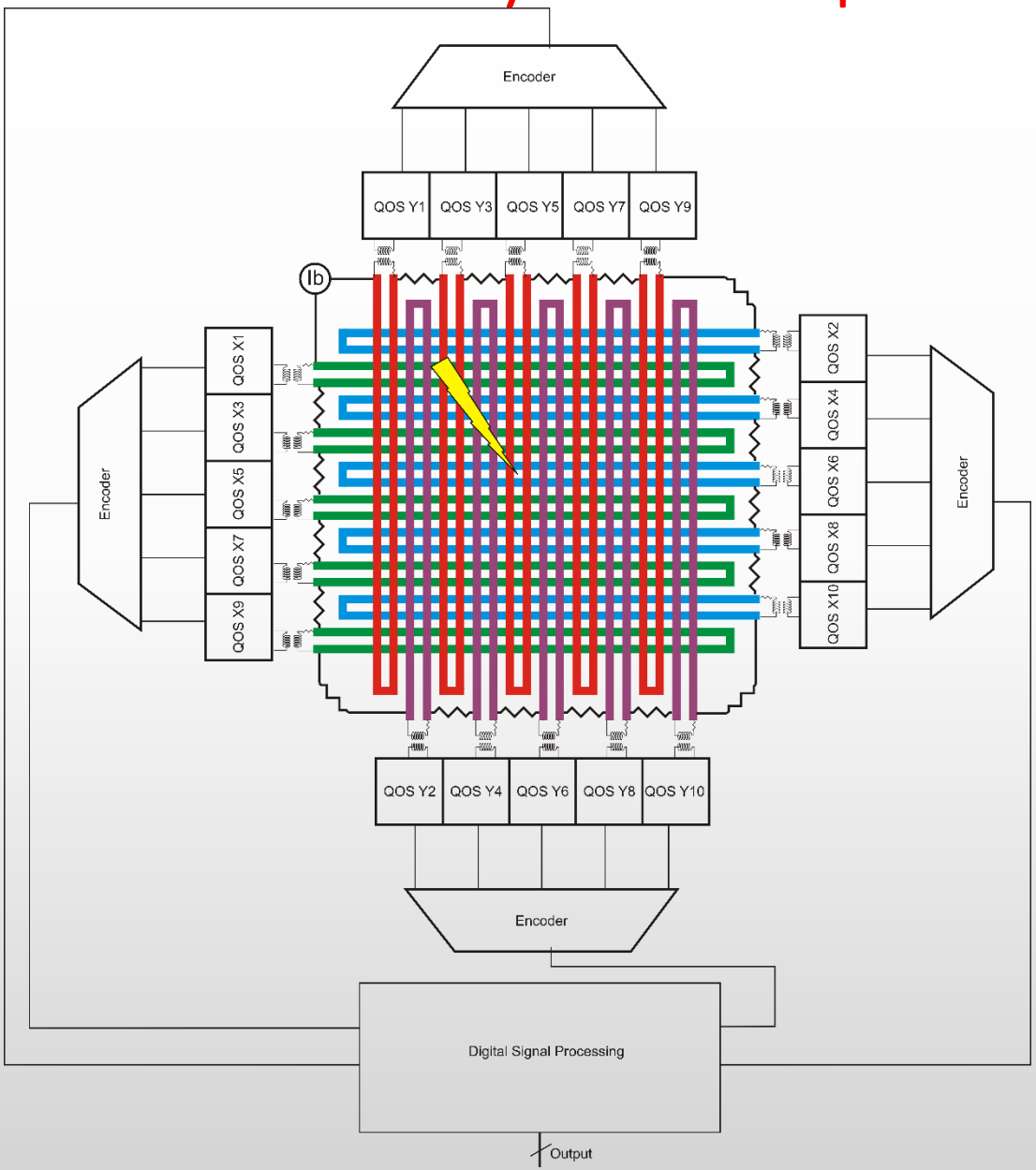

a)
Position (um)
500
1000
1500
2000
2500
3000
3500
Amplitude (mV)
0.0
0.2
0.4
0.6
0.8
1.0
1.2
b)
c)
CTL (M3)
COU (M2)
BAS (M1)
GND


500 nm
500 nm
400 nm
400 nm
300 nm
300 nm
300 nm
CTL (M4)
CC
COU (M3)
JC
AlOx
JJ
JP
Nb
BAS (M2)
RC
RC
CC
COU (M3)
SiO2
BC
COU
CTL (M4)
BAS (M2)
SiO2
GC
Nb Ground Plane (M1)
Mo Resistor
Si Substrate
Moat

Dual Tone Multi Frequency Coding

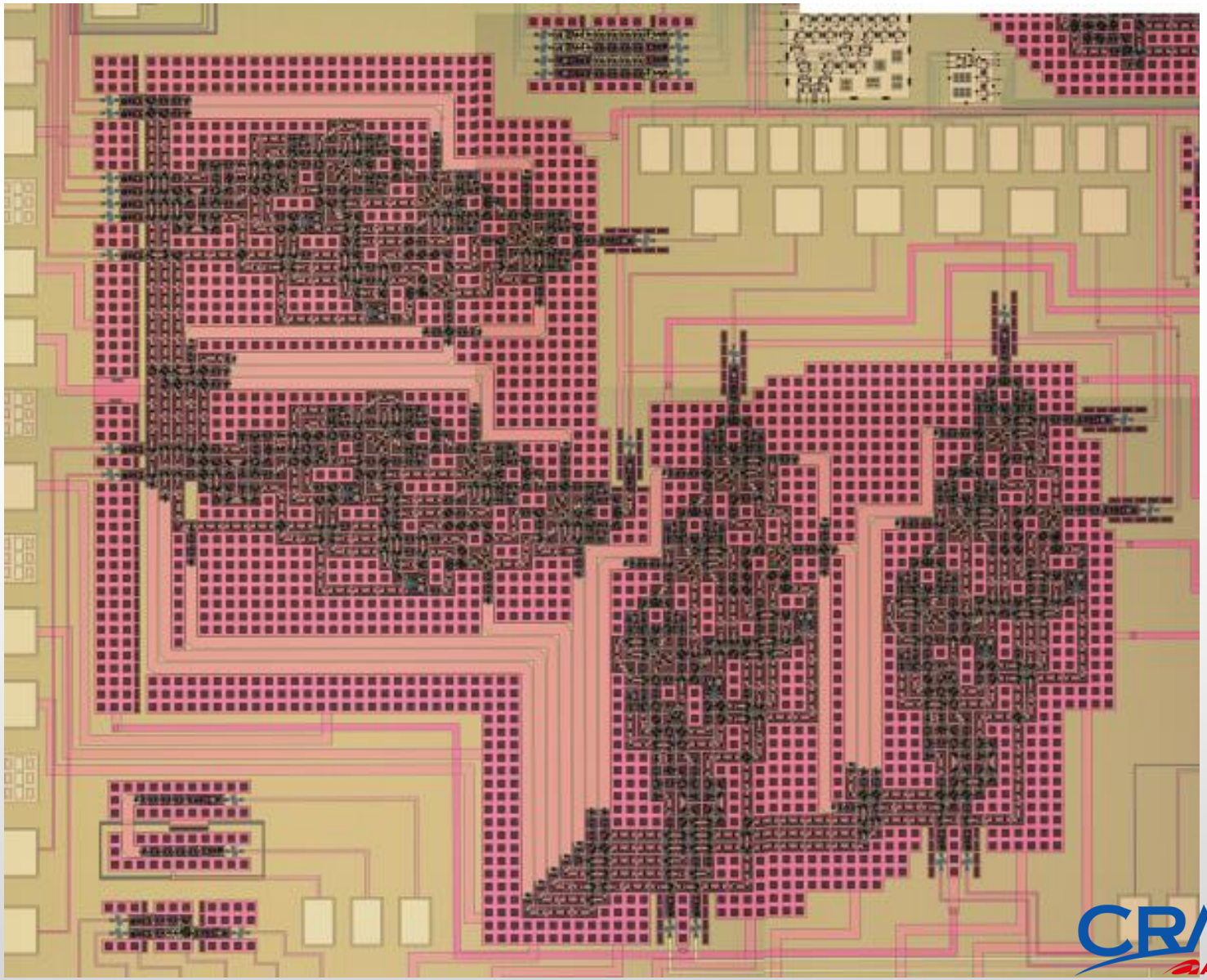


Many Pixel Operation

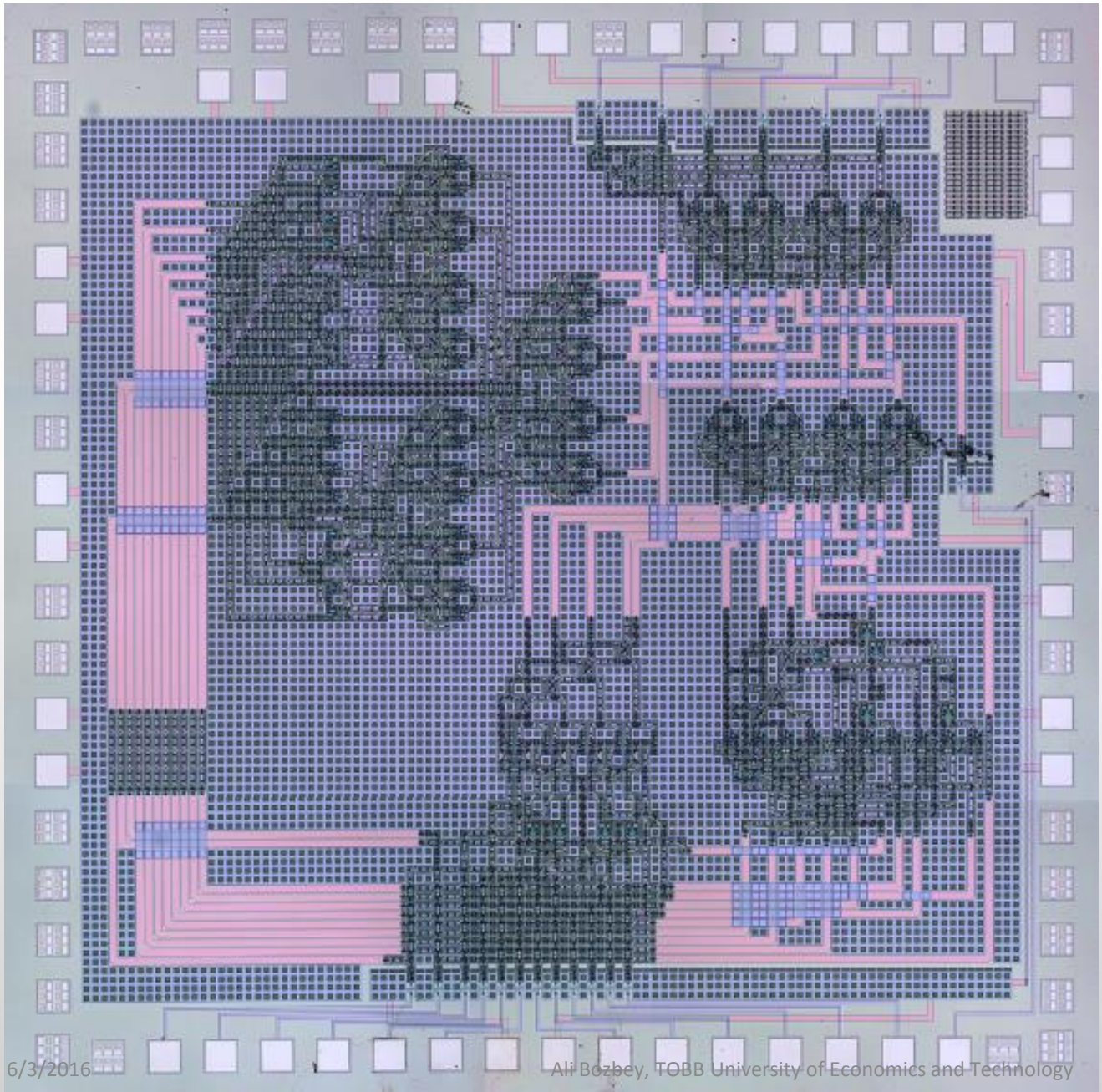


- Only one bias point is sufficient to bias all the SSLDs.
- Each SSLD is separated with low pass filters
- Individual SSLD's are coupled to 1-bit comparator circuits with coupling coils.
- Comparator outputs are fed to encoders to extract the address information for the radiated cell.
- Row and column addresses of SSLD's are determined by front-end circuit and encoder circuits.
  - In the figure, Y5 and X6 are triggered with the incoming photon.

Bit Serial ALU



Bit Parallel ALU



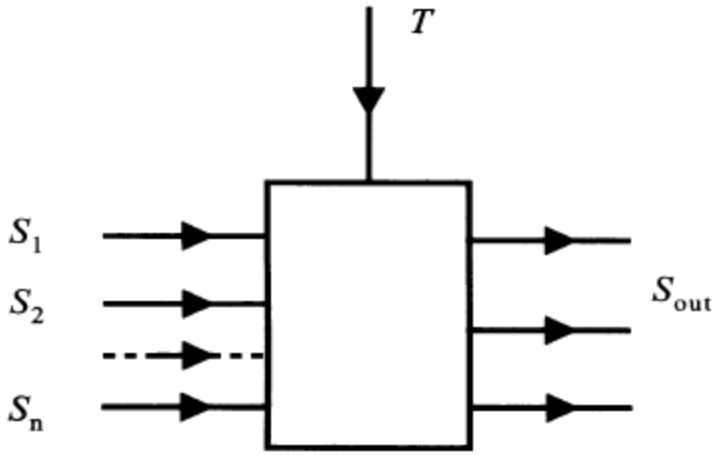
25 GHz,
2.5 mW

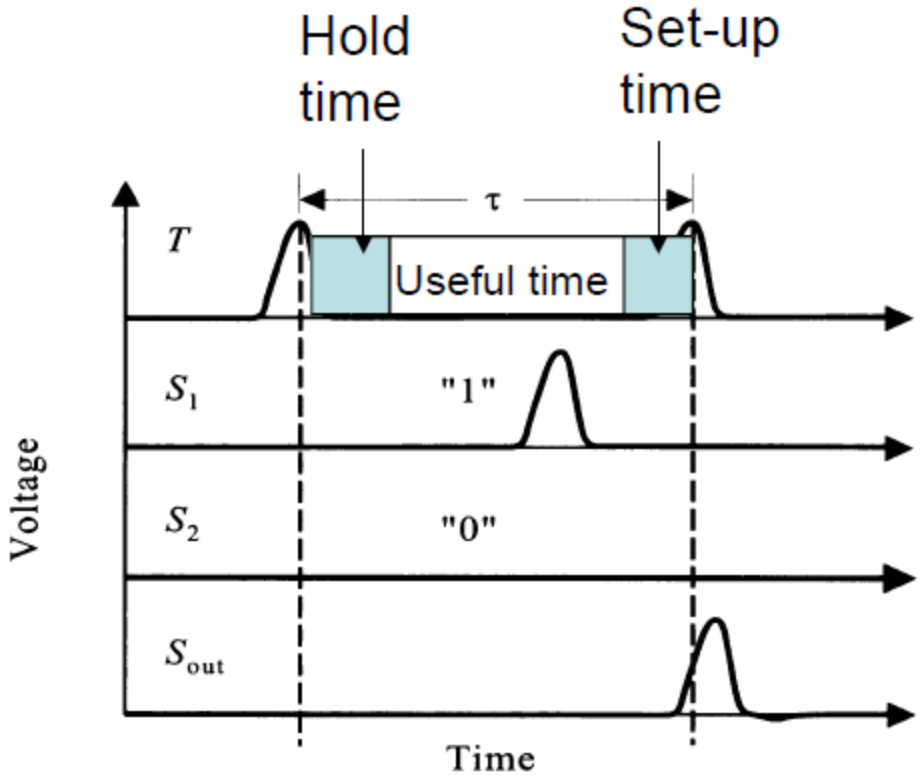
Acknowledgements

- TUBITAK (108E242, 111E191, 114E099)
- Akira Fujimaki and his associates
- Ministry of Development
- Center of Excellence for Superconductivity Research (CESUR)

The circuits mentioned in these slides were fabricated in the clean room for analog-digital superconductivity (CRAVITY) of National Institute of Advanced Industrial Science and Technology (AIST) with the standard process 2 (STP2). The AIST-STP2 is based on the Nb circuit fabrication process developed in International Superconductivity Technology Center (ISTEC).

RSFQ Circuit Syncronization





If there is an SFQ pulse between two consecutive CLK pulses, logic “1”, otherwise logic “0”

Van Duzer