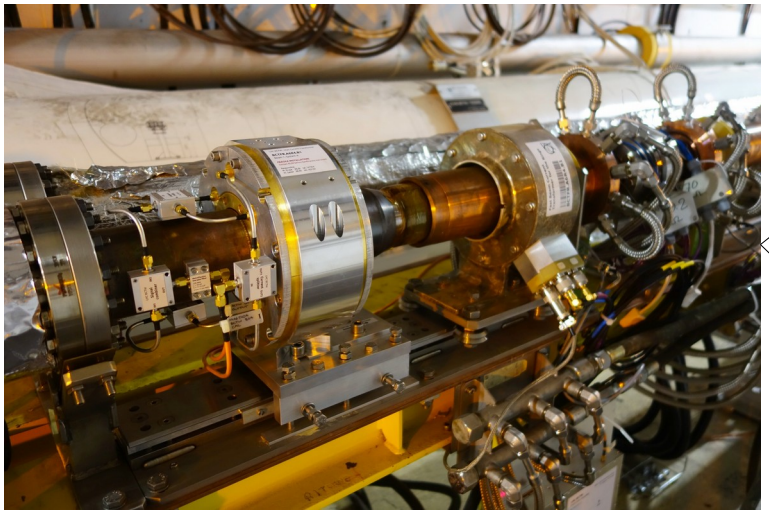
A New Acquisition System For The SPS And LHC Fast BCTs

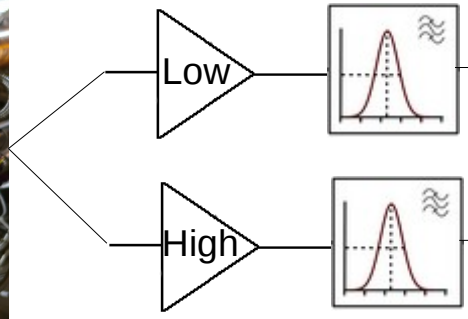
Jiri Kral

Overview

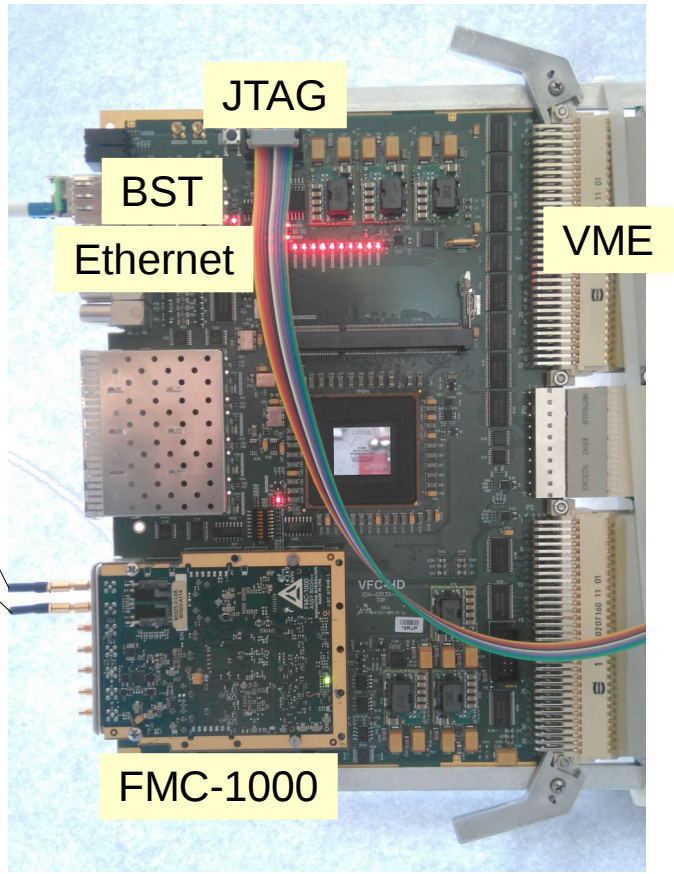
- New LHC and SPS per bunch intensity measurement system
  - Below 1% precision
  - Up to high (2e10 charges) and low gain (2e11 charges) channels
- Based on the VFC board (CERN) with FMC-1000, 1 GHz 2-channel ADC mezzanine (supplier)
- 650 MHz ADC sampling rate currently (1 GHz under investigation)

Hardware





150 MHz bandwidth



BCT

BCTW, FBCT, ICT

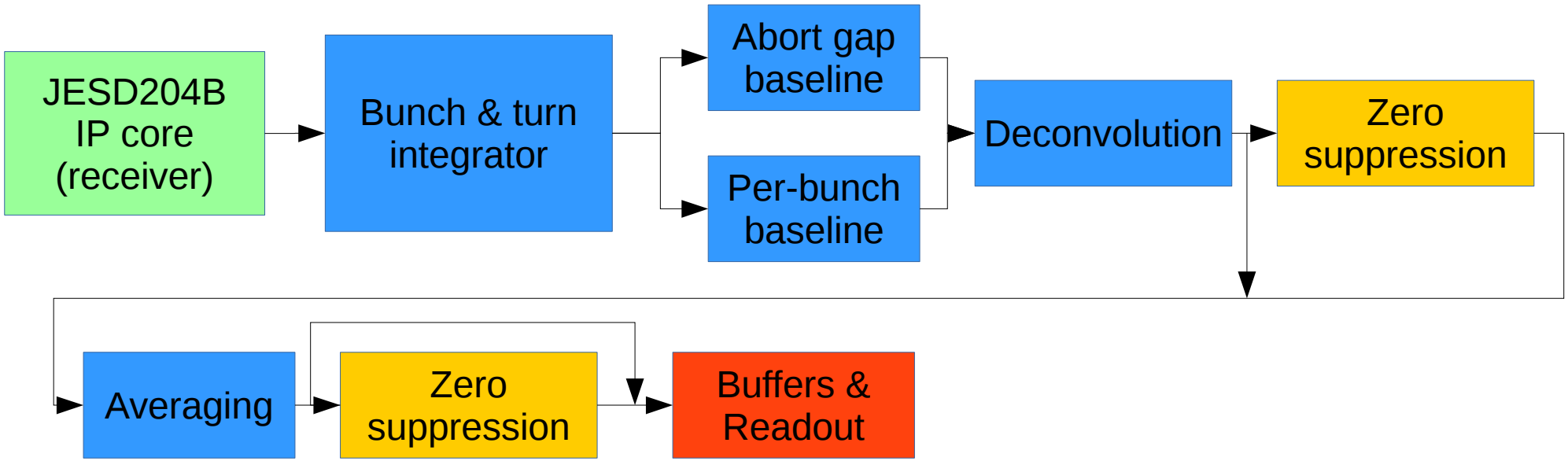
→ Low/High gain amplification Gaussian filter

→ VFC carrier + FMC-1000

→ VME

Data processing in the firmware

- JESD204B line in between ADC and FPGA, 4 x 6.5 Gbit/s
- Integration, baseline subtraction on per-bunch bases
- Deconvolution to remedy tails crossing to the next bunch
- Averaging over N turns (224, …)
- Possibility of zero suppression of the raw or averaged data



Available measurements

- Continuous
  - Per **bunch intensity** integrals, averaged over N turns
  - **Turn intensity** integral, averaged over N turns
  - Beam filling pattern
- Snapshots
  - Raw ADC data
  - Unaveraged bunch integrals
  - Computed baselines
  - Unaveraged turn integral

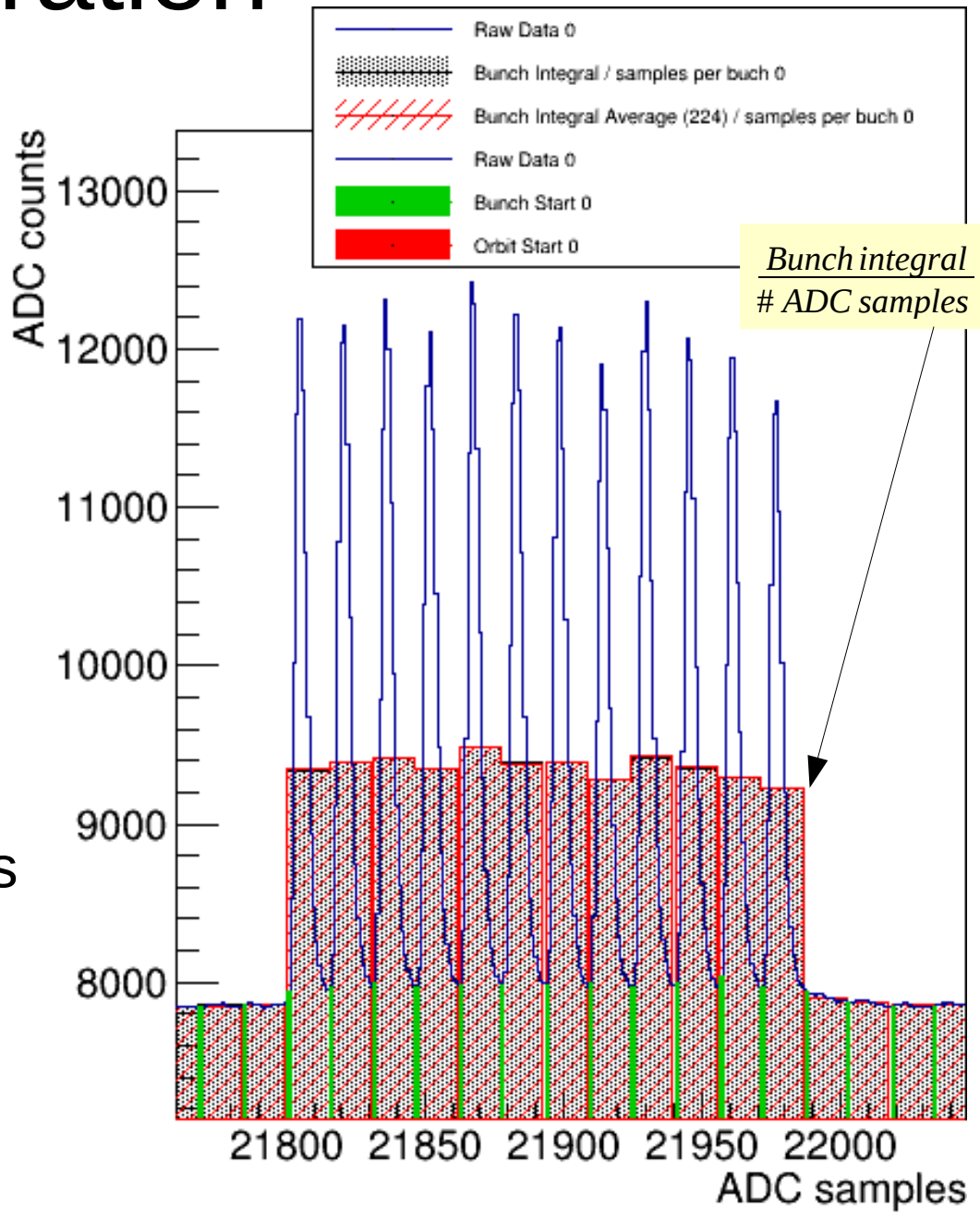
$$\langle I_{bunch,i} \rangle = \frac{\sum_{n=0}^{N_{turnavg}-1} I_{bunch,i,n}}{N_{turnavg}}$$

$$\langle I_{turn} \rangle = \frac{\sum_{n=0}^{N_{turnavg}-1} I_{turn,n}}{N_{turnavg}}$$

- All measurements are time stamped using the BST time

Integration

- Integrating constant # of samples per bunch
- **Free running** 650 MHz ADC sampling clock
  - LHC frequency out of FMC-1000 VCXO range
  - 16 samples / bunch
- Averaging over many turns
  - i.e.: many sampling phases
  - Immune to small phase shifts

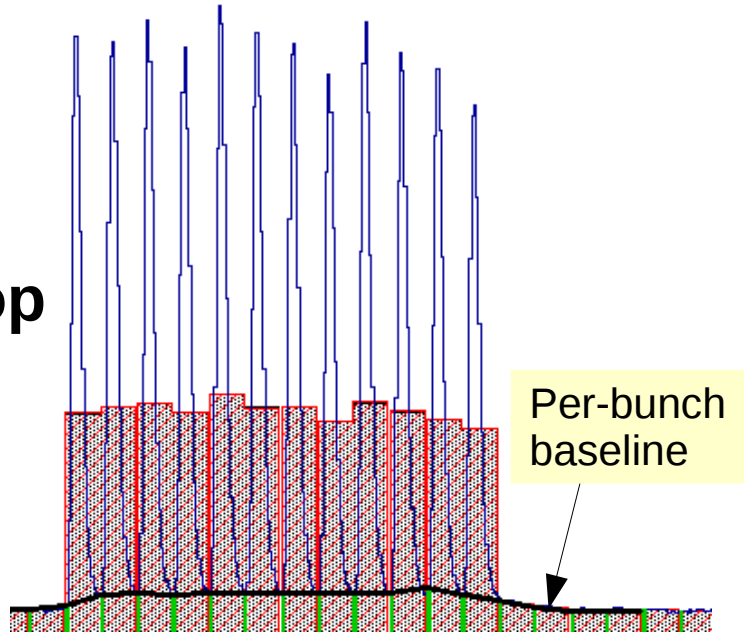


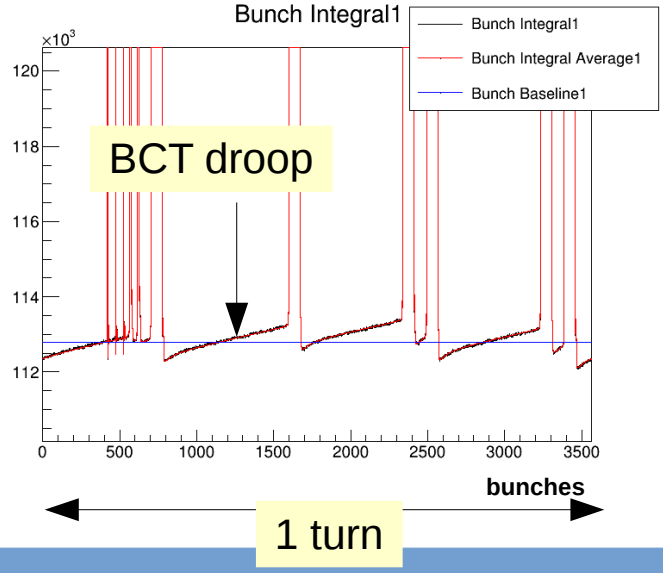
Baseline subtraction

- Per bunch baseline reconstruction
  - Signal overflow to following bunches
  - Per turn not possible due to **BCT droop**
- Linear interpolation in between two points
  - Either with fixed phase
  - Or min of 2 consecutive samples

$$baseline_{bunch} = \frac{\sum_{i=0}^{1} min_{bunch+i}\left(sample_{0,}\, sample_{1}\right)}{2}$$

- Zero suppression with a constant threshold

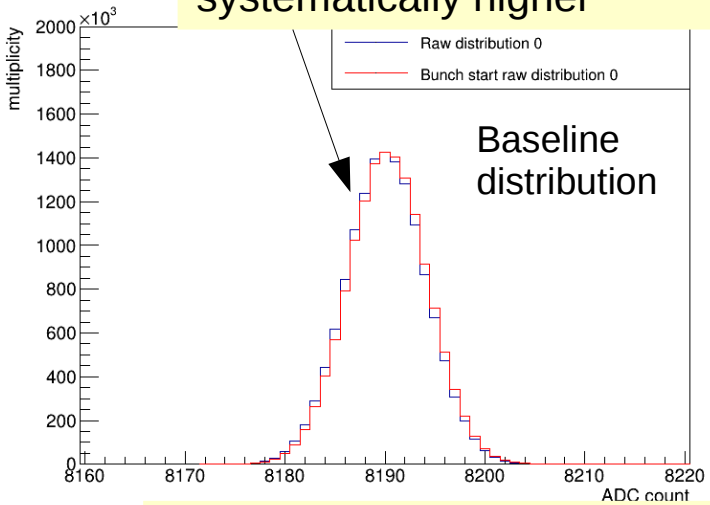




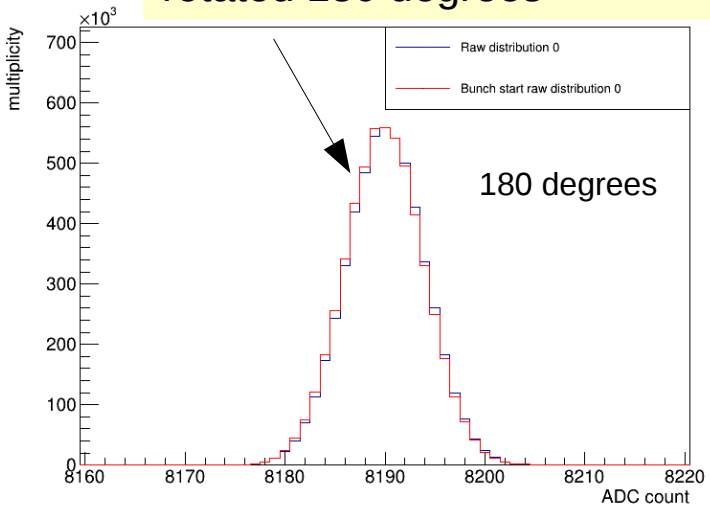
Baseline corrections

- Beam synchronous noise, FPGA switching noise or the baseline *min()* of 2 samples requirement create a **constant offset**
  - Constant per bunch offset correction
- **Rounding error** on turn integral
  - Constant offset turn correction
  - Magnitude close to pilot bunch intensity in low gain channel

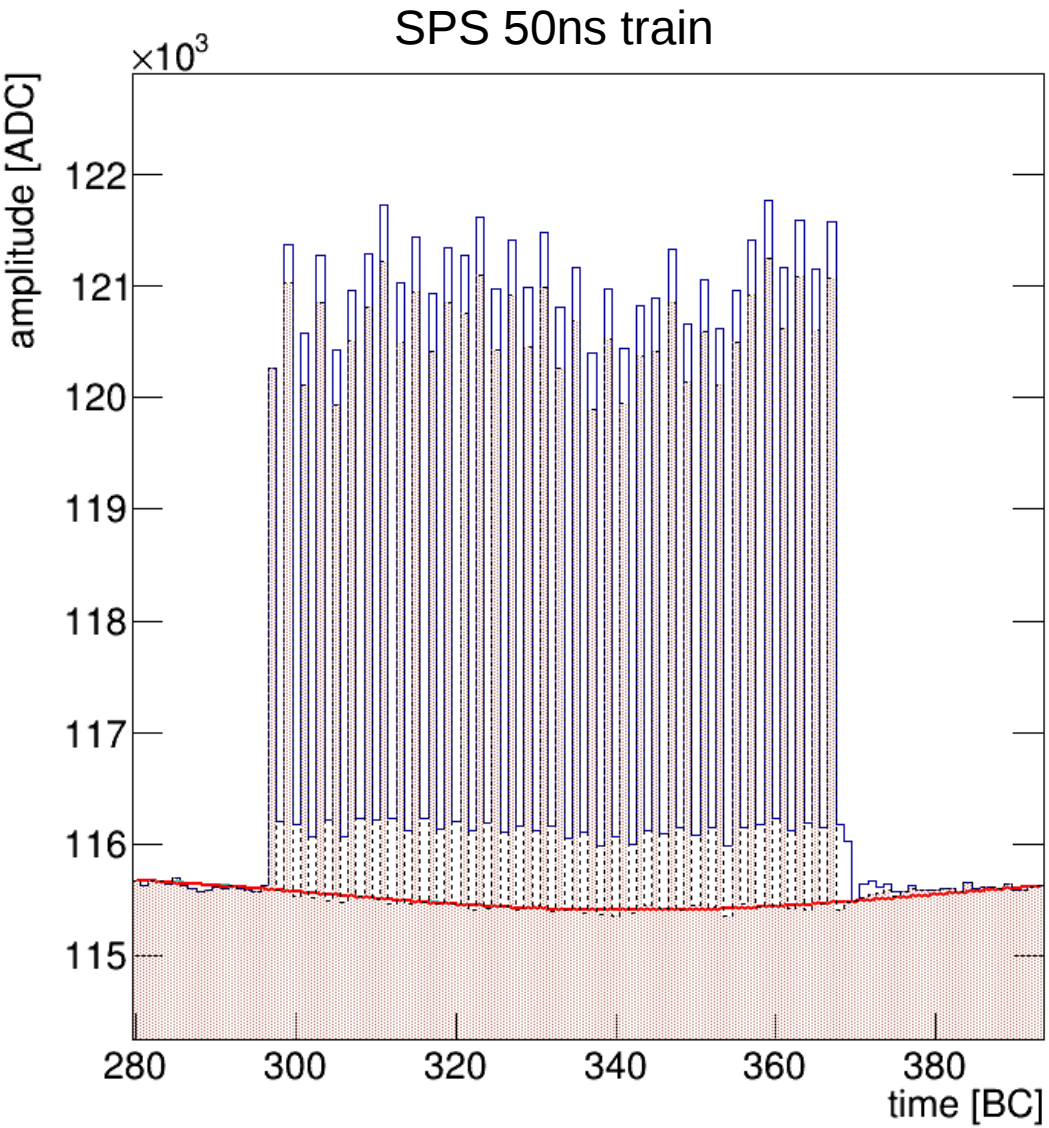
ADC sample 0 of each bunch systematically higher



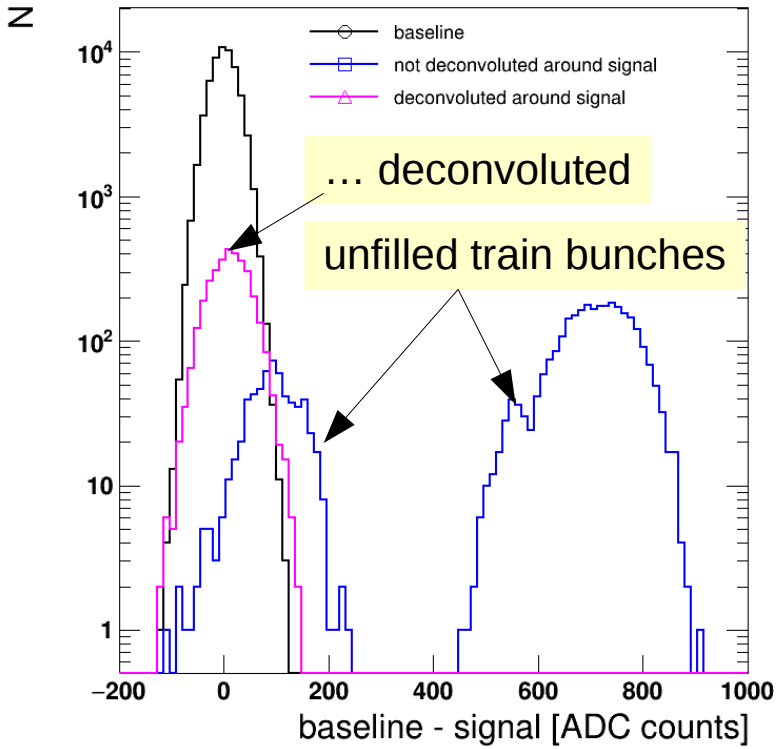
… and lower, when bunch phase rotated 180 degrees



Deconvolution

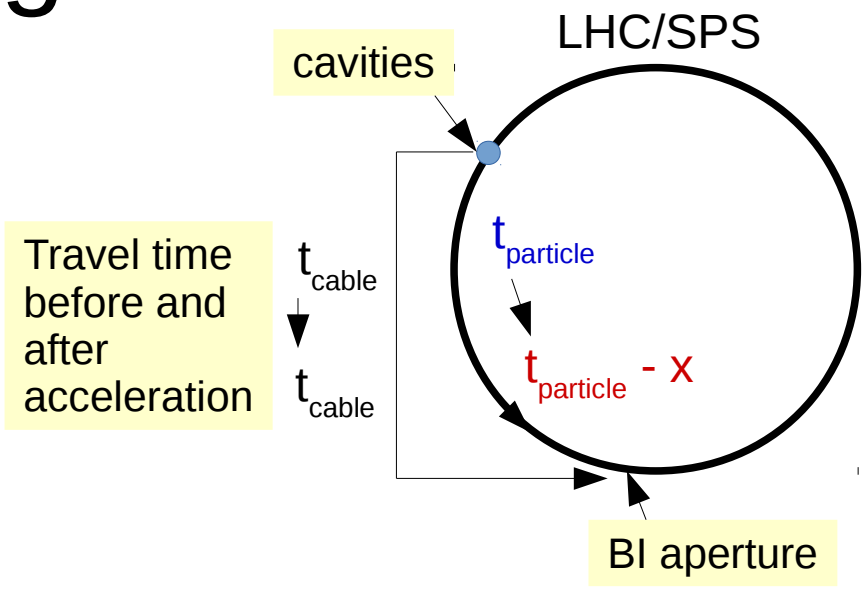


- Simple deconvolution of 10 consecutive bunches seems to give reasonable results

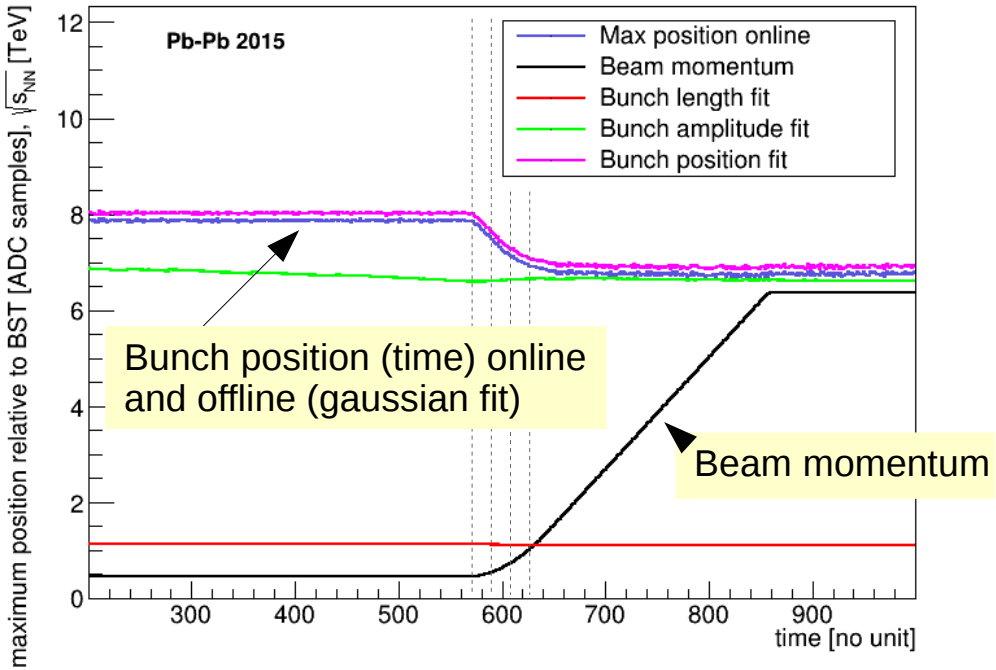


Timing

- After acceleration, the **beam arrives sooner** to the measurement point than clock edge does
  - Change in sampling phase

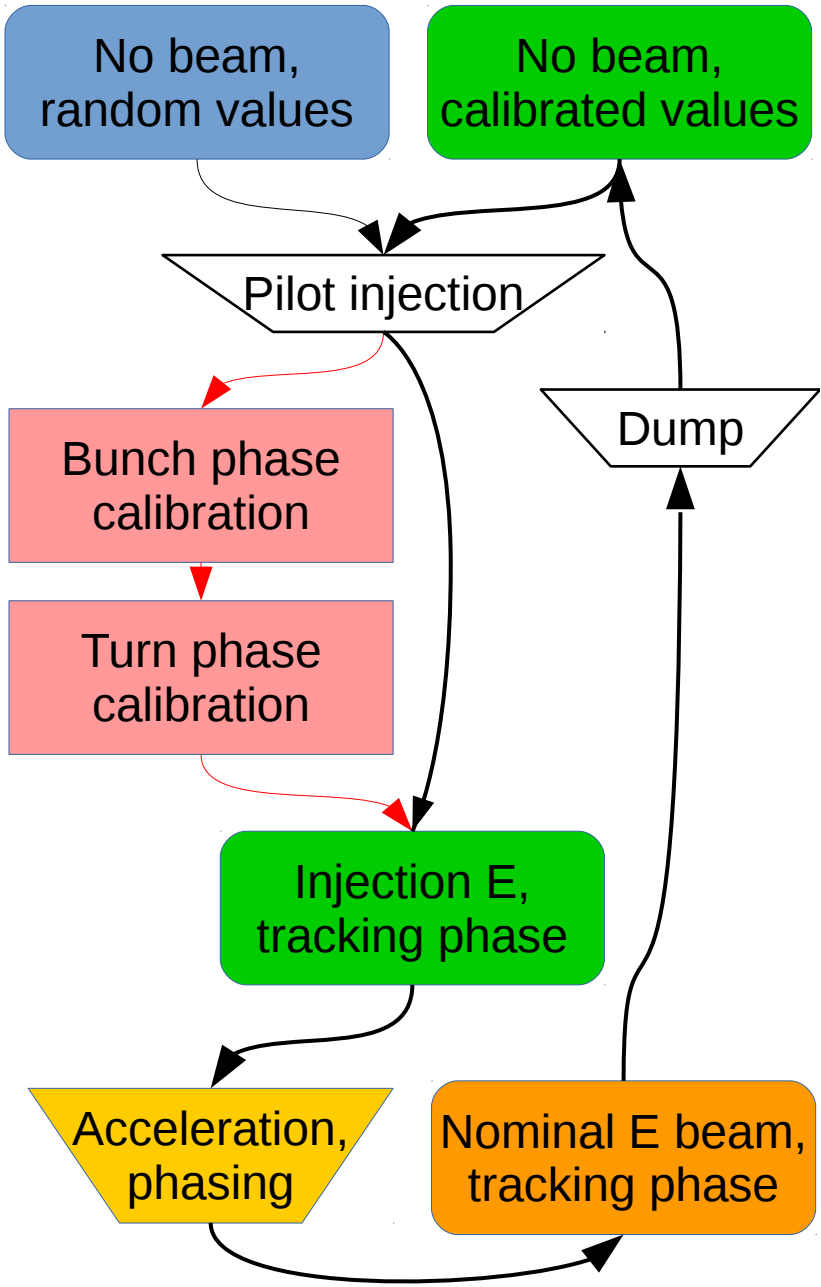


- Shift of up to -12 ns in SPS
- In LHC, -1.5 ns observed for heavy ions



Timing correction

- **On-line peak finding** to identify maximum of each bunch signal
  - Bunch boundaries relative to the maximum position
- BST clock phase shifted and **tuned continuously** to the present beam
  - Supplies bunch boundaries of unfilled bunches
- In case of “adiabatic” change, possibility to track bunches across bunch boundaries (>25ns)
- **Auto-calibration** possible on pilot
  - Of both **bunch and turn phase**

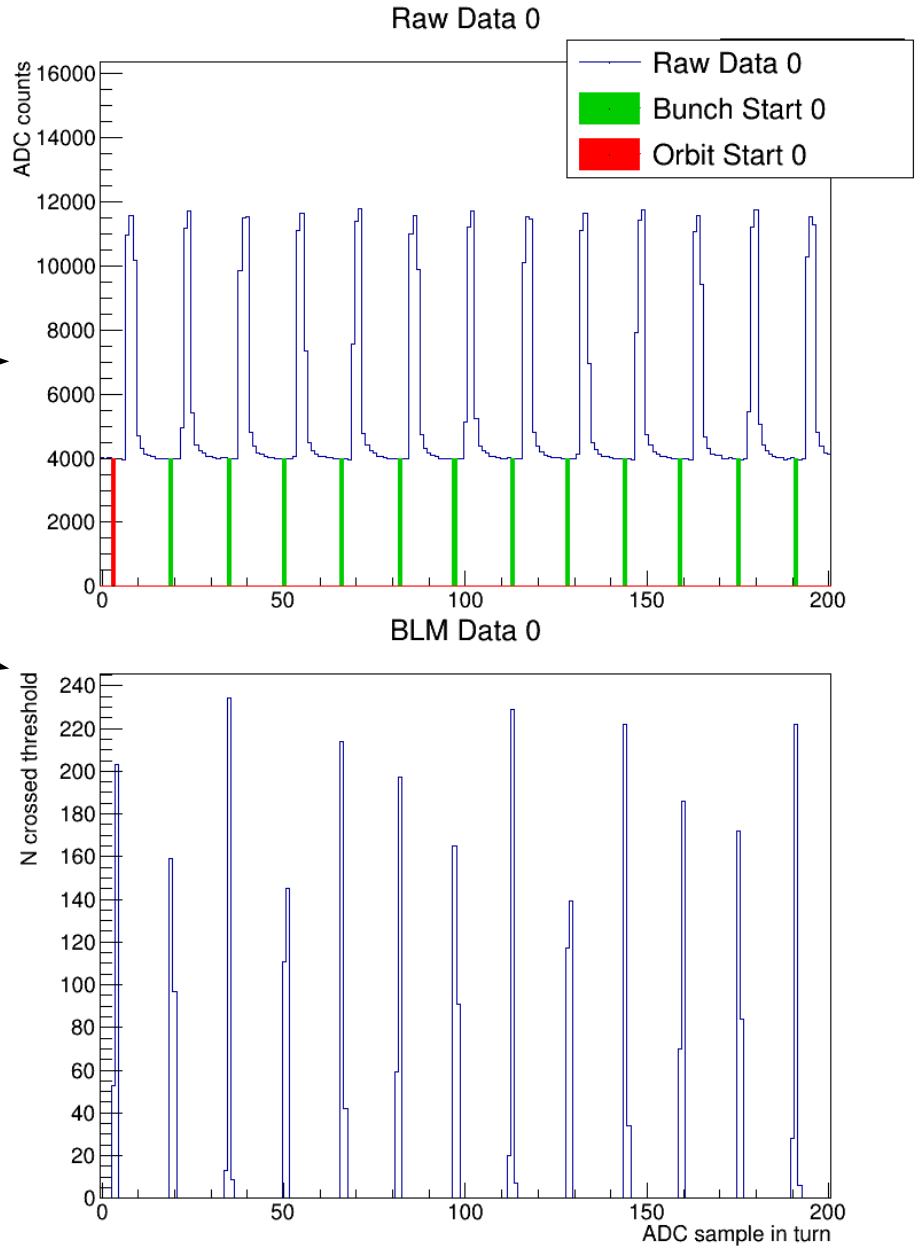


Automation

- **Boot ROM** includes configuration of the VFC board (voltages), FMC-1000 clock generation, ADC and JESD204B link
  - No need for complicated software driven boot
  - Simple ROM updates without need to recompile the FW
- Several **automated calibration** procedures available
  - Bunch baseline correction
  - Turn baseline correction
  - Beam timing
- On-board beam **dump detection** to trigger snapshot
  - Dump trigger might arrive quite late

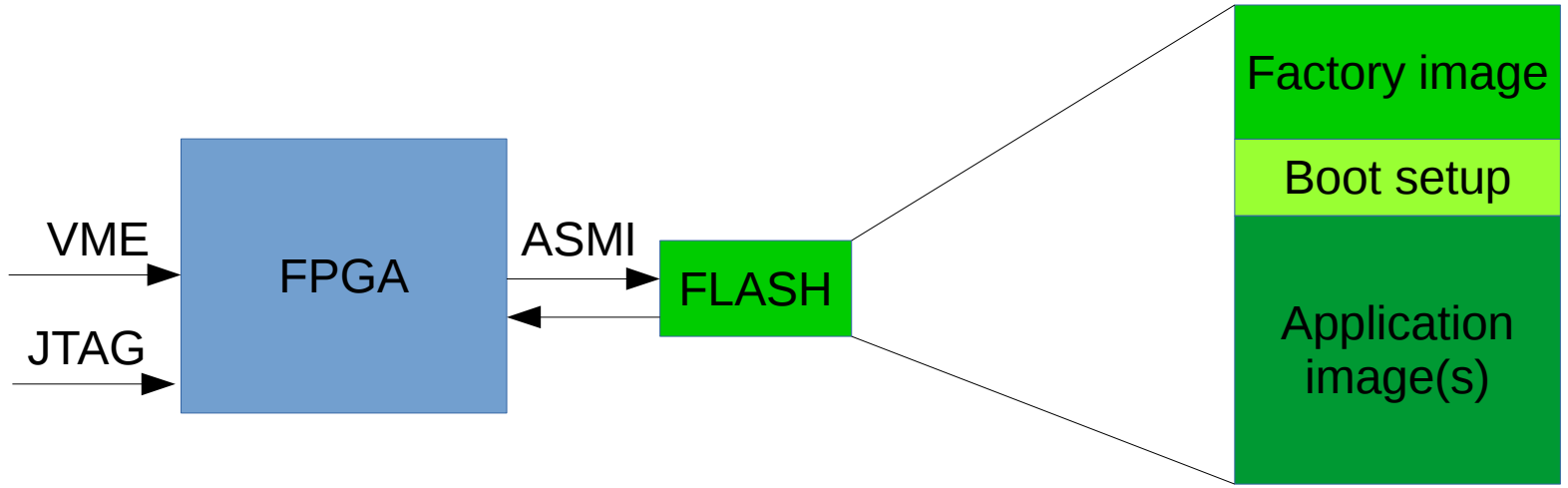
Beam Loss Monitor

- Diamond Beam Loss Monitor FW module was developed
- Shares raw ADC snapshot data
- Implements new histogram of, N = # of ADC samples in turn, values
  - Incremented on first sample that crosses threshold
  - Relative to either BST turn start or external trigger



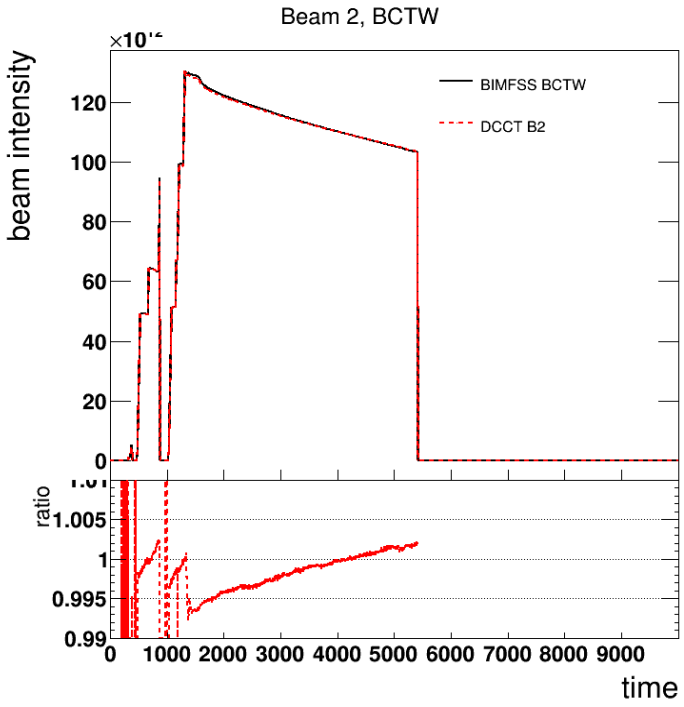
Deployment

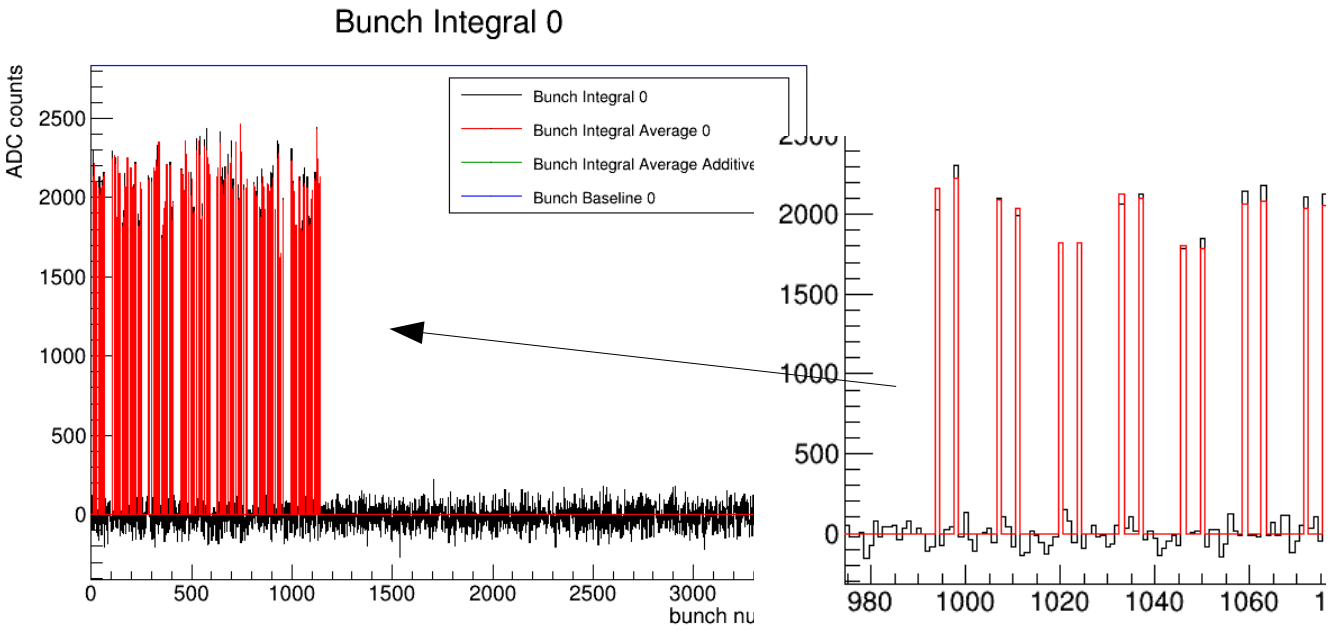
- VFC card includes **flash memory** which can hold the FW
- VFC **factory (golden) image** prepared
  - Accesses flash via VME or JTAG, loads application image
  - Write protected **avoids bricking** the board with a failed flash
  - **Watchdog** reconfigures to factory, if application image fails
- Available to **all VFC card users** (with documentation :)

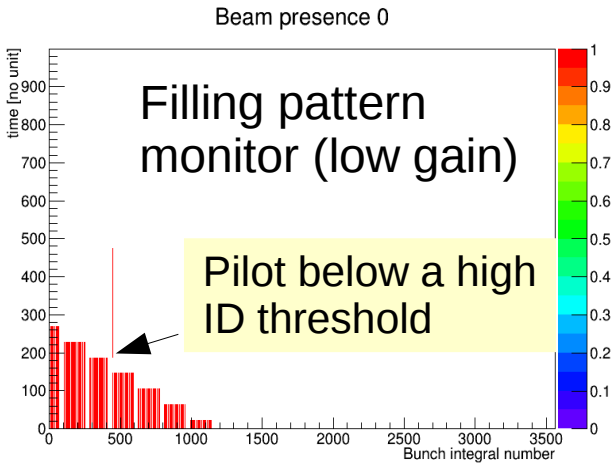


First intensity measurement

- Relative agreement with DCCT **within 1%** for pp
  - Observed **debunching**
  - No absolute calibration, ADC linearity correction, etc.







Filling pattern monitor (low gain)

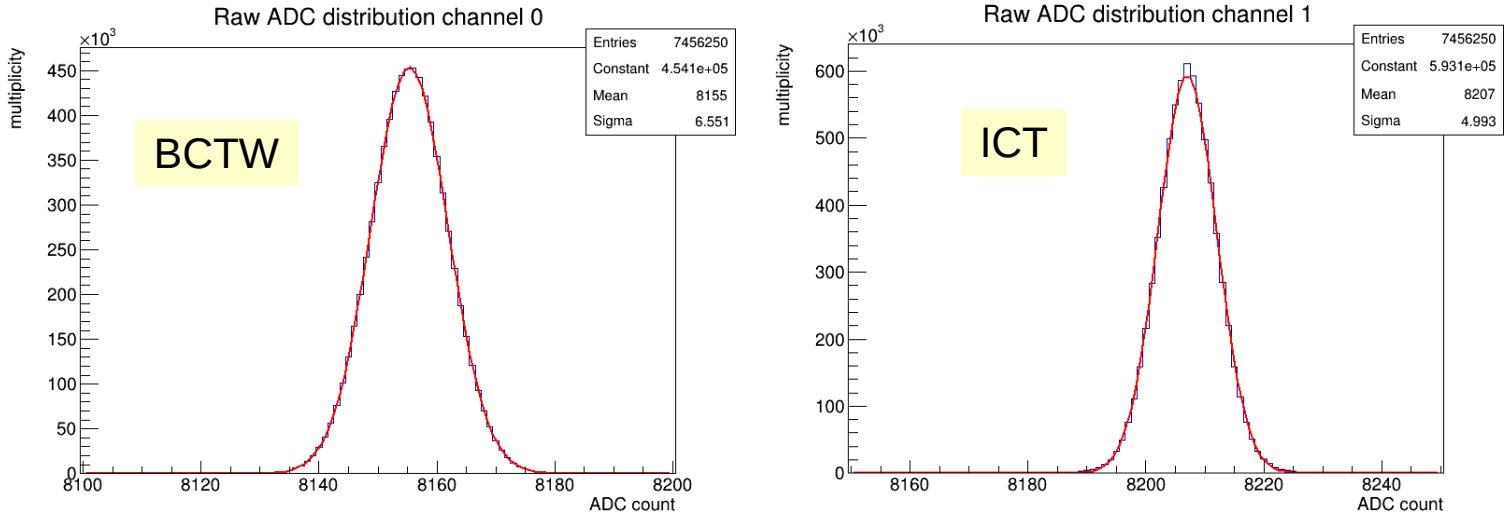
Pilot below a high ID threshold

ICT BCTW noise measurement

- Evaluated BCTW and ICT noise background
  - Different gain and bandwidth (60 MHz ICT, 150 MHz BCTW)
  - Gain aligned using comparison to the DCCT data (f = 1.23)
  - Bandwidth factor from aligning white noise powers (f = 1.58)

$$N_{power}[dBm] = 20\log(\sigma[V]) - 10\log(R) + 30\,;\, R = 50\,Ohm$$

Presumed white noise → proportional power to bandwidth



- Σ_{BCTW} = 6.55 * 1.23 / 1.58 = 5.10 → **$\sigma_{BCTW} / \sigma_{ICT} = 1.02$**
- Noise ratio on bunch integrals: **$\sigma_{BCTW} / \sigma_{ICT} = 1.08$**

1 GHz sampling

- Under investigation
- Several caveats
  - Standard VFC cards FPGA Arria V **GX transceivers** do **not support** necessary JESD204B data rate (> 6.5 GBit/s)
    - Replaced with similar pinout Arria V GT chip
  - The Altera Arria V JESD204B **IP core** does **not support** the necessary data rate (even for GT chip)
    - Transceivers can receive 10 GBit/s data stream
    - Write a simple limited JESD204B receiver
  - 1 out of 4 high speed differential lines is **routed** to transceiver banks which do not support > 6.5 GBit/s
    - Re-wire, PCB revision, FMC connector adapter, ...

Software

- Software under development
- Capable of pulling snapshot data without important impact on continuous measurements readout
- IRQ driven
- Database archival of the main data points that are necessary for the commissioning

Conclusion

- **Firmware** for beam intensity measurement using fast BCTs was **implemented**
  - Foundation for digital processing of BCT data on VFC cards for **not only intensity measurements**
  - “Outreach” to other projects (BLM, factory FW image, …)

- Hardware was tested and evaluated
- Fist measurements were performed on 2015 pp and Pb-Pb fills at LHC and SPS
- Absolute calibration system under development
- Getting ready for the 2016 run and final commissioning

Credits

The boss: David Belohrad

Firmware: Jiri Kral

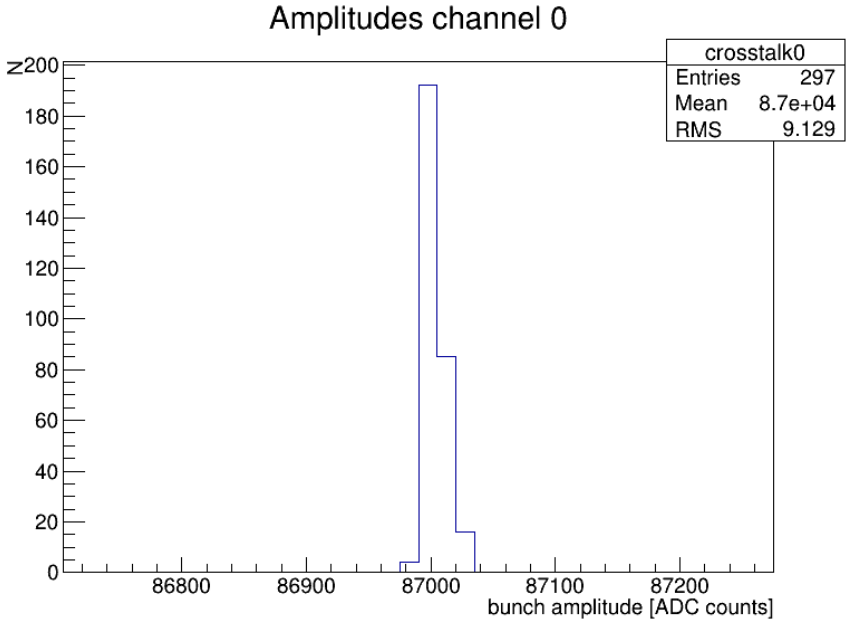
Software: Stephane Bart Pedersen

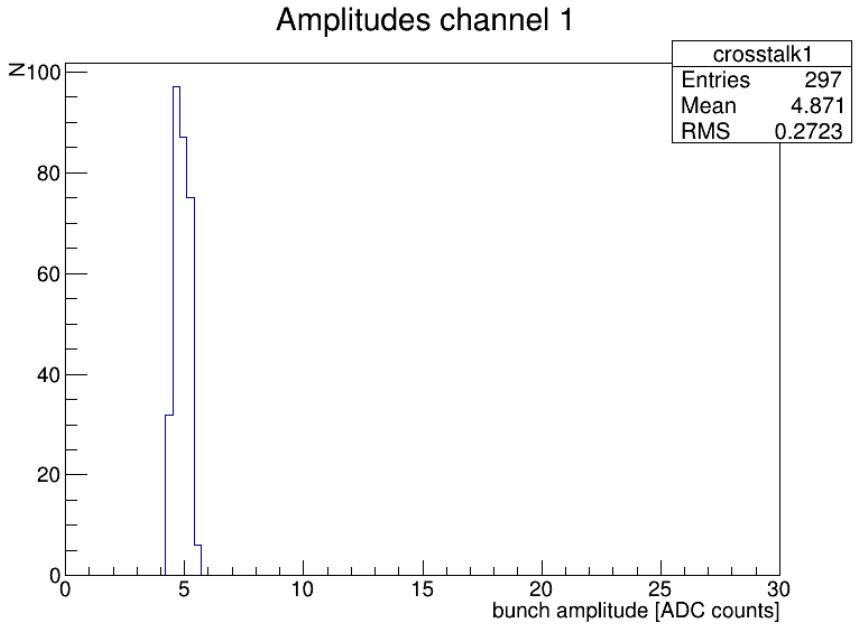
Special thanks to: Andrea Boccardi, Manoel Barros Marin
for the help with the VFC board
Michal Krupa, Marek Gasior
for the BCTW part

Backup

Channel crosstalk

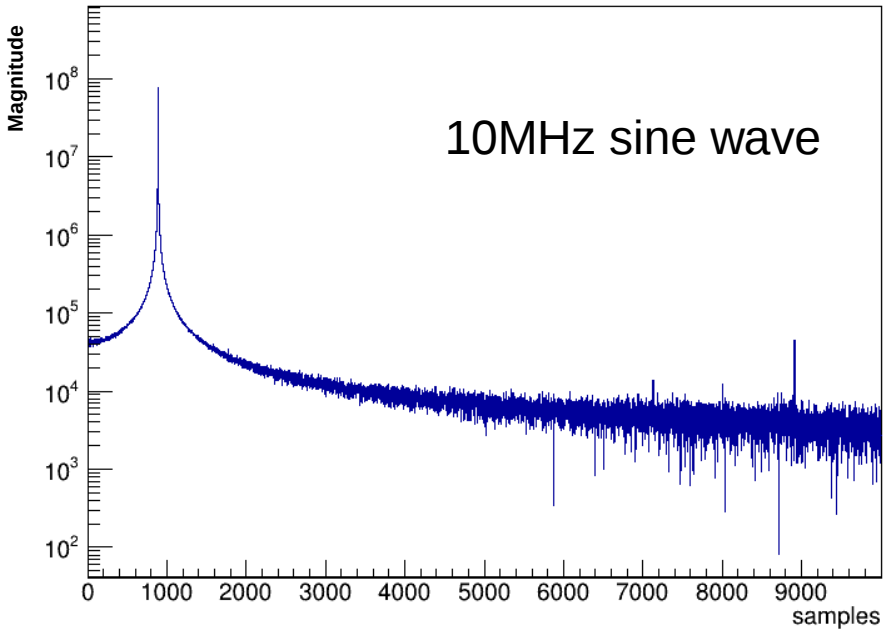
- -80 dB measured (ADC -95 dB according to data sheet)
- Measured in amplitude domain
  - Repetitive pattern of signals simulating bunches injected in one channel, second channel terminated
  - Averaged measurement over ~130k turns
  - Observed induced amplitude

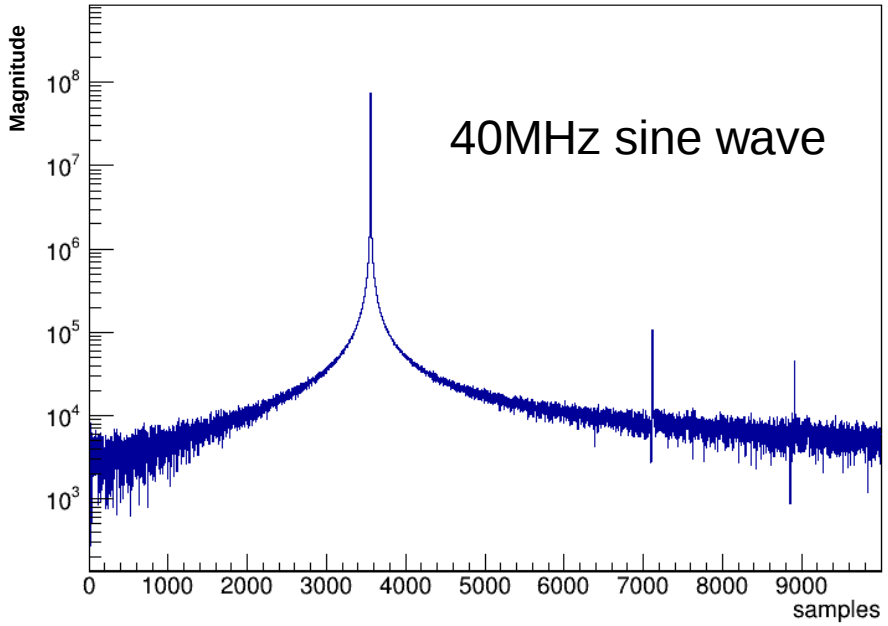




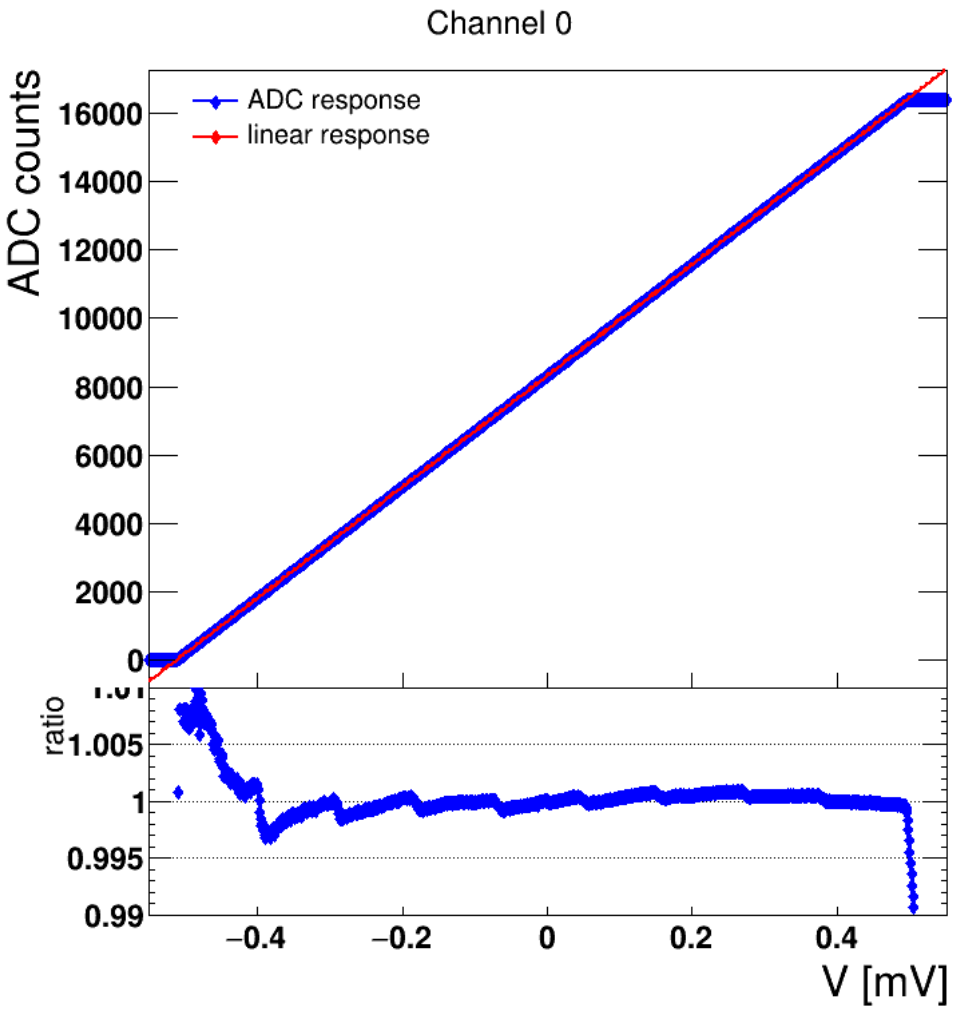
FFT

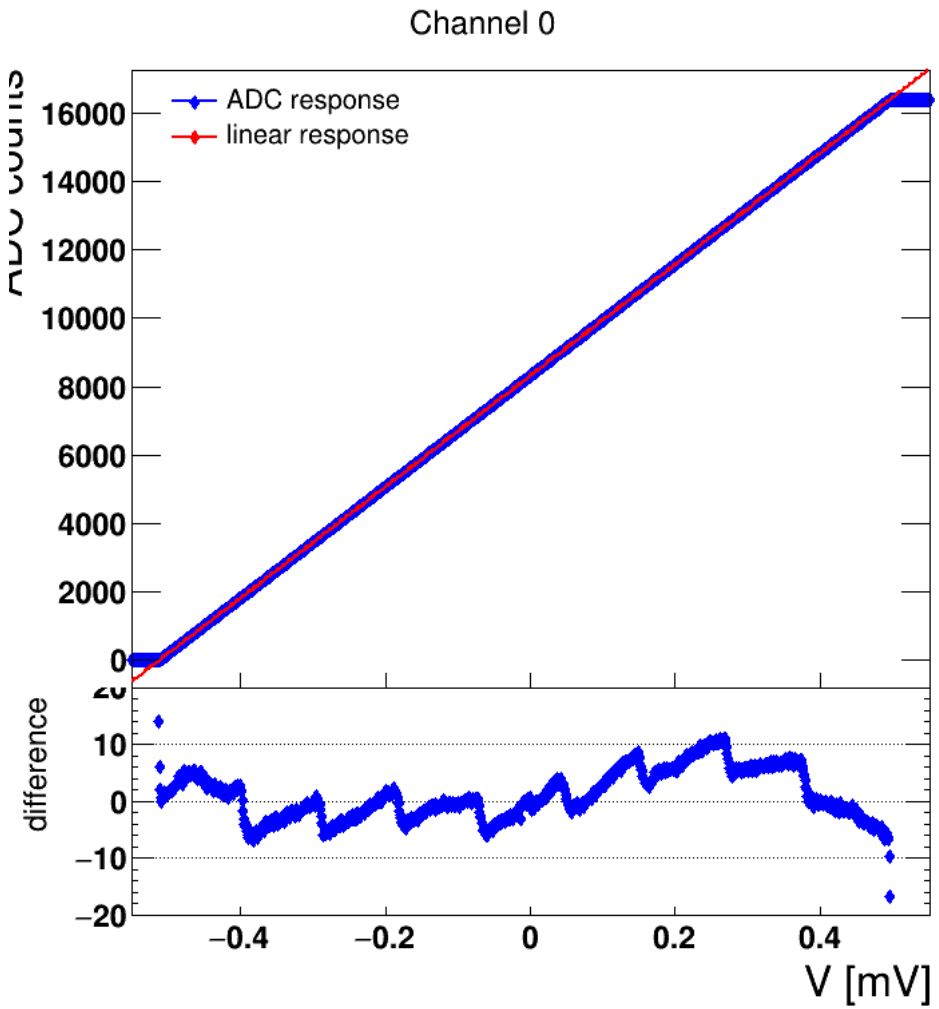
- FFT of sine wave injected into one channel
- Response clean





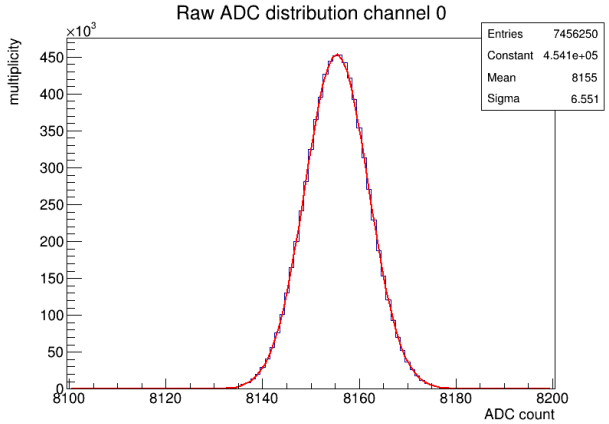
ADC linearity

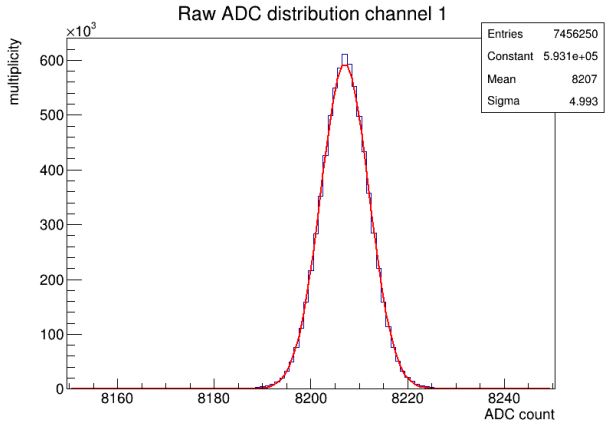




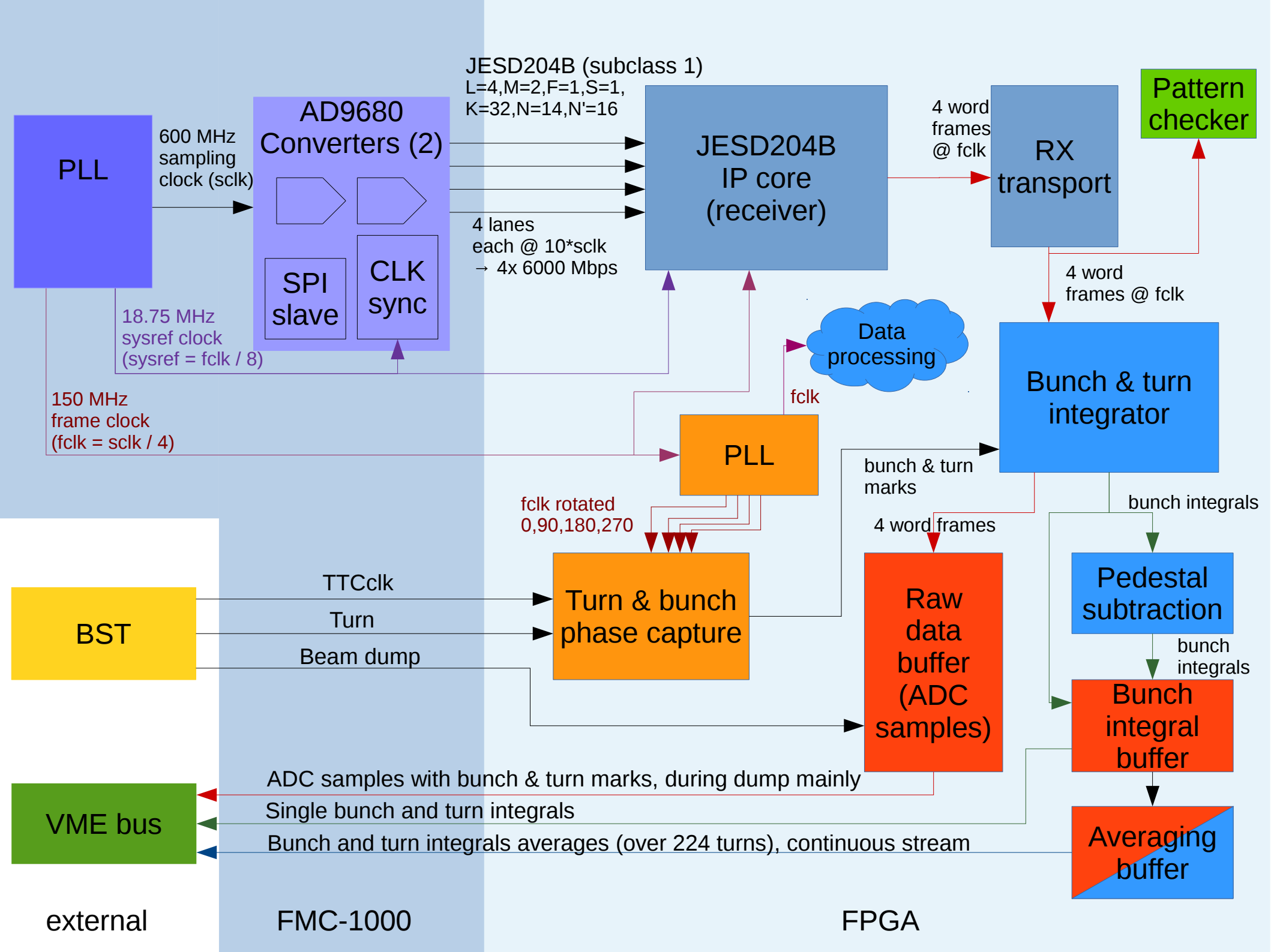
LHC ICT BCTW noise comparison

- ICT installed on B1 (ch1), BCTW on B2 (ch0), 1 RF dist. LG channels used for ICT, FMC card #1, BCTW connected without RF dist.
  - Bandwidth limit for ICT is 60 MHz from RF dist., 150 MHz for BCTW
  - Correction factor 1.58 $N_{power}[dBm] = 20\log(\sigma[V]) - 10\log(R) + 30\,;\, R = 50\,Ohm$ Presumed white noise → proportional power to bandwidth
- Beam intensity measurement by the new device was correlated with B1/B2 ratio from DCCT TIMBER data to scale the unequal gains
  - Correction gain factor computed: BCTW * 1.23 / ICT = 1





- Distribution of raw ADC signal was obtained (without beam)
- Corrected σ_{BCTW} = 6.55 * 1.23 / 1.58 = 5.10 → **$\sigma_{BCTW}/\sigma_{ICT}$ = 1.02**
- Noise ratio on bunch integrals (same method): **$\sigma_{BCTW}/\sigma_{ICT}$ = 1.08**


JESD204B (subclass 1)
L=4,M=2,F=1,S=1,
K=32,N=14,N'=16
PLL
600 MHz
sampling
clock (sclk)
AD9680
Converters (2)
SPI
slave
CLK
sync
4 lanes
each @ 10*sclk
→ 4x 6000 Mbps
JESD204B
IP core
(receiver)
4 word
frames
@ fclk
RX
transport
Pattern
checker
4 word
frames @ fclk
18.75 MHz
sysref clock
(sysref = fclk / 8)
Data
processing
Bunch & turn
integrator
150 MHz
frame clock
(fclk = sclk / 4)
fclk
PLL
bunch & turn
marks
bunch integrals
fclk rotated
0,90,180,270
4 word frames
TTCclk
Turn
Beam dump
BST
Turn & bunch
phase capture
Raw
data
buffer
(ADC
samples)
Pedestal
subtraction
bunch
integrals
Bunch
integral
buffer
ADC samples with bunch & turn marks, during dump mainly
Single bunch and turn integrals
Bunch and turn integrals averages (over 224 turns), continuous stream
VME bus
Averaging
buffer
external
FMC-1000
FPGA