The ELENA Orbit System

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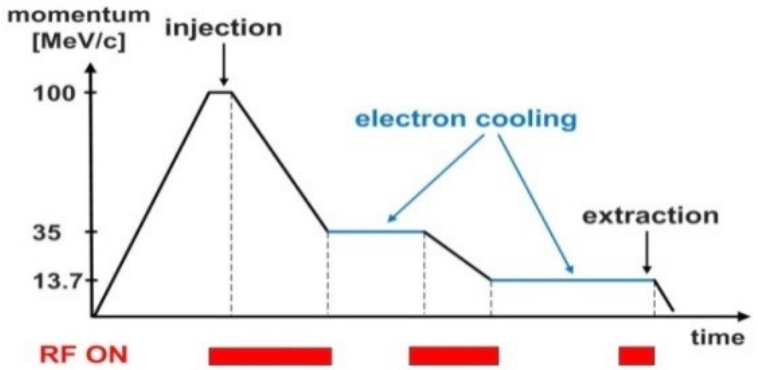
Outline

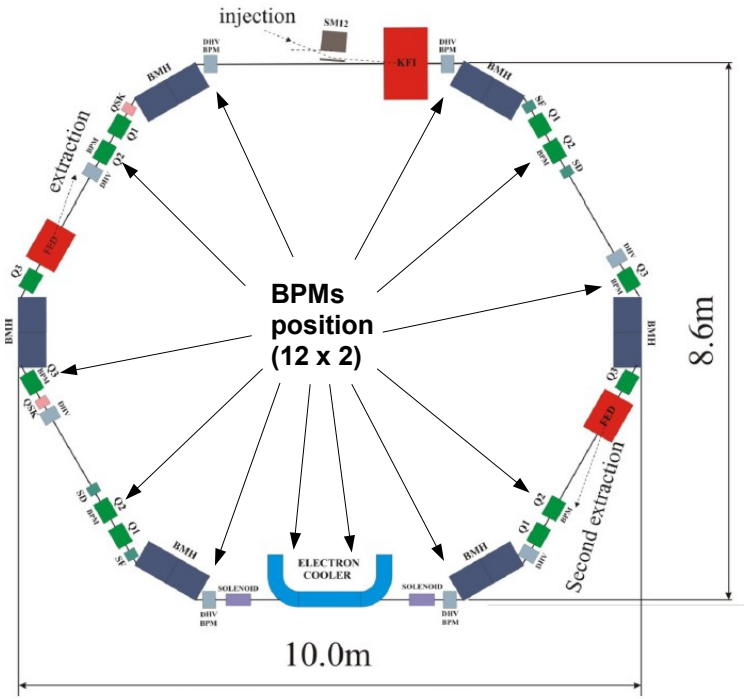
- System overview.
- Measurement principles.
- BPM characteristics.
- Head amplifier.
- Digital acquisition system layout.
- Status and tests.
- Conclusions.

ELENA orbit measurement system overview

- **ELENA further decelerates antiprotons coming from AD from 100 MeV/c to 13.7 MeV/c**.
  - Revolution frequency (f_{REV}) will vary from 1.056 MHz to 148 kHz.
  - Cycle duration of about 25 s.
- **Measurement system.**
  - Based on 20 circular BPMs mounted inside quadrupole and corrector dipoles plus 4 BPMs inside the Electron Cooler.
  - Low noise head amplifier very close to each BPM will deliver Δ and Σ signals to reception amplifiers.
  - Digital acquisition system based on the same hardware as the AD orbit system for digitalization and signal processing.
- **Measurements to implement before/after ELENA commissioning.**
  - Orbit measurement with bunched beam (first stage): with a resolution of 0.1 mm every 10 ms.
  - Trajectory data at injection (second stage): with a resolution of 0.1 mm for at least 100 turns after injection.
  - Intensity measurement for bunched beam (third stage).
  - Schottky intensity measurement for coasted beam (fourth stage).



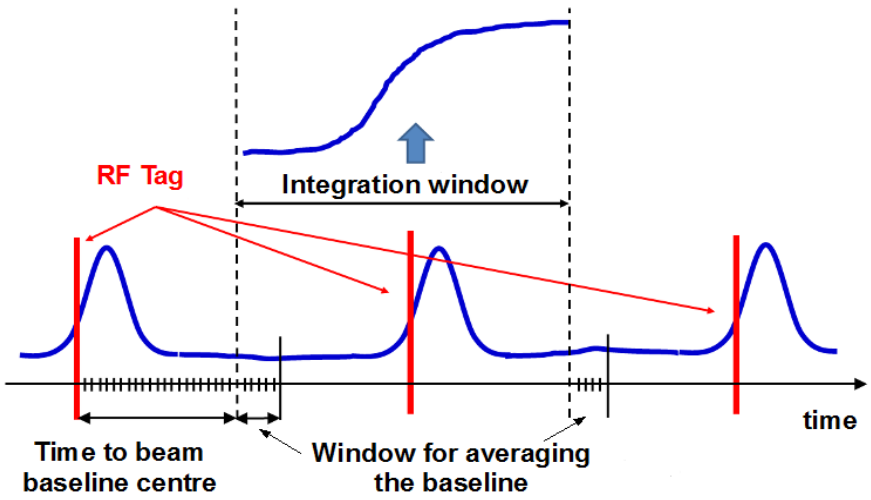
ELENA BASIC DECELERATION CYCLE



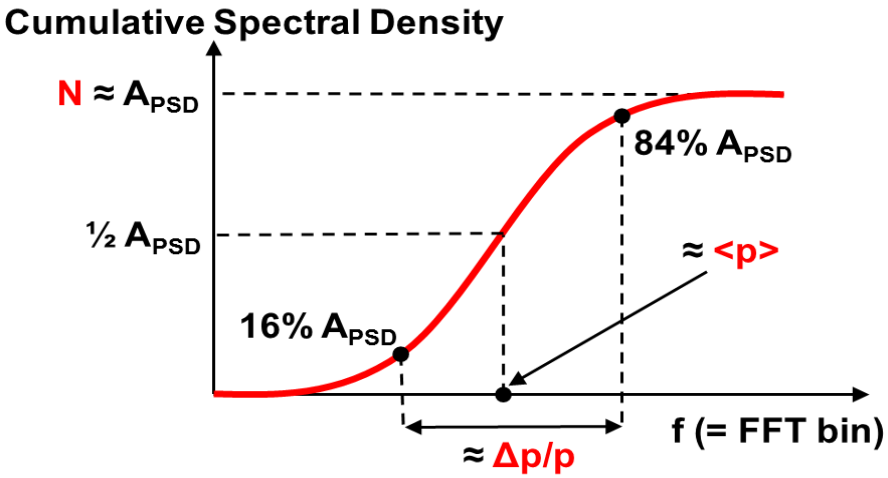
BPM LOCATION IN ELENA RING

Measurement principles

- **Orbit measurement with bunched beam.**
  - Δ and Σ signals digitized and down converted to baseband.
  - After low pass filtering and decimation position calculation from I/Q complex data.
- **Trajectory data at injection.**
  - Δ and Σ signals from head amplifiers digitized by the acquisition system will be stored during at least the first 100 turns.
  - Data provided to front-end software during the same machine cycle.
  - Sampling period of 20 ns.
- **Intensity measurement for bunched beam.**
  - Integration in time domain for every bunch of digitized Σ signal.
  - Subtraction of the signal baseline and averaging for all the BPMs a user-selectable number of revolutions.
  - Time to beam baseline centre determined for each BPM according to its azimuthal position and cable delay.
- **Schottky intensity measurement for coasted beam.**
  - Sum of 20 Σ signals to improve SNR by 13 dB.
  - Measure up to 111th harmonic (40 MHz) of f_{rev} to reduce acquisition time.
  - Time of flight correction for each BPM required.
  - Digital down conversion (DDC), low-pass filtering and decimation.
  - Windowing and squared FFT (power spectrum).
  - Averaging and subtraction of amplifier noise level.
  - Obtain total intensity and Δp/p every second.



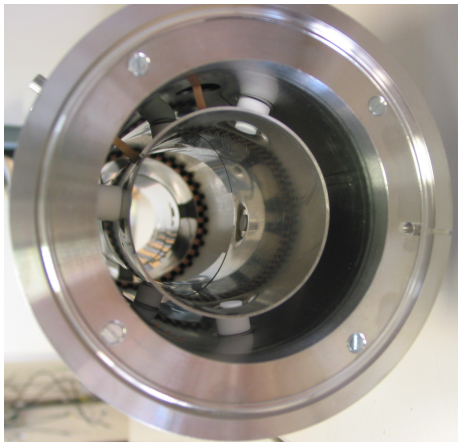
INTEGRATION WINDOW FOR BUNCHED BEAMS

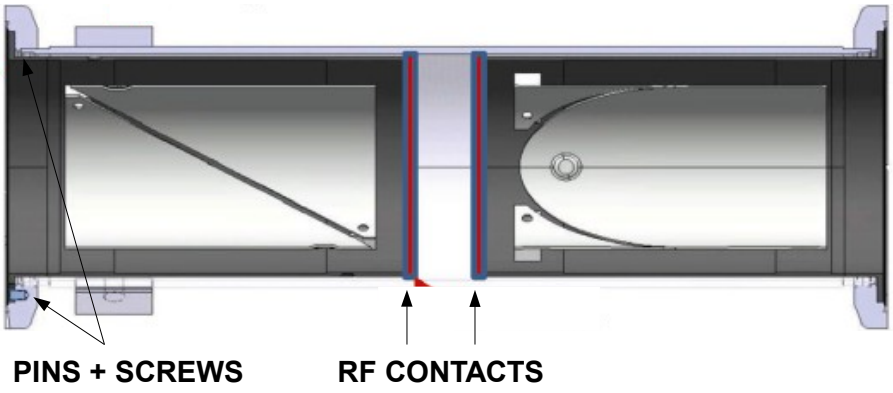


COASTED BEAM PARAMETERS CALCULATION

ELENA BPM

- **BPM assembly.**
  - Two diagonally cut stainless steel electrodes.
  - Electrodes attached to stainless steel support tube with three glass-ceramic (MACOR) spacers.
  - Feed-through and contact pin to read out the signal.
- **Horizontal and vertical BPMs inserted to a common vacuum chamber.**
  - Electrodes, support tubes and inner surface of vacuum chamber NEG coated.
  - Support tubes aligned with pin holes in the vacuum chamber flange and attached with screws.
  - RF contacts at the far end of the support tube to ensure good electrical contact to ground.
- **No Σ electrode foreseen: Σ signal generated in the head amplifier.**
- **Electrode length of 120 mm chosen to optimize the BPM for Schottky measurements: high sensitivity and bandwidth.**
- **BPM differential sensitivity of 90 µVp/mm (1x10^{7} particles).**

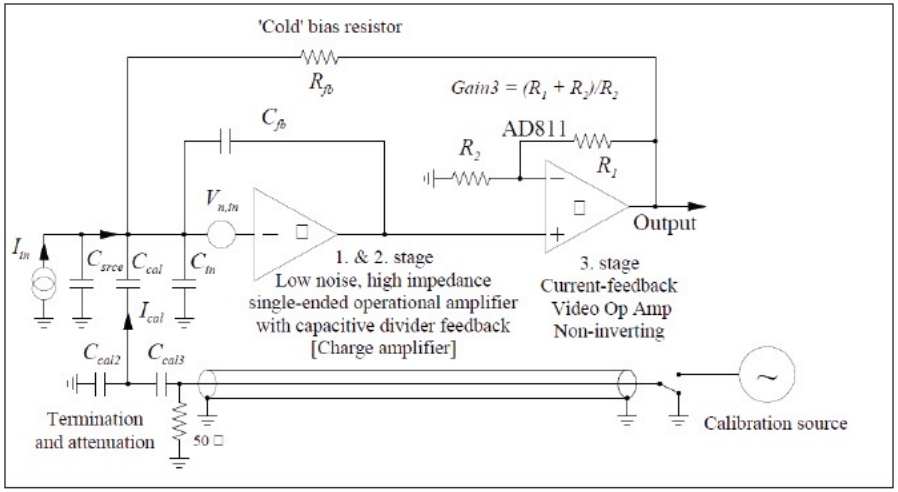




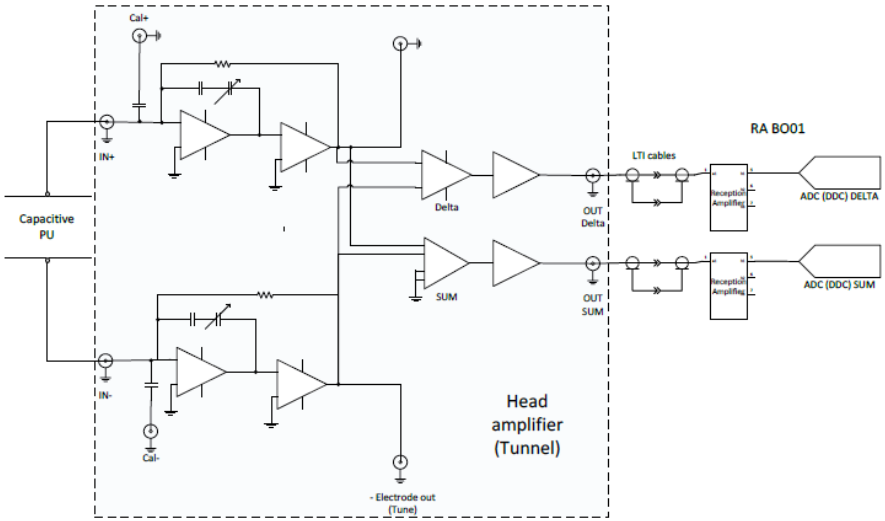
Electrode length	120 mm
Electrode inner diameter	66 mm
Electrode thickness	1 mm
Electrode to support tube gap	10 mm
Electrode capacitance	16 pF
Resolution	0.1 mm
Accuracy	0.3-0.5 mm
Vacuum	3x10^{-12} Torr

ELENA head amplifier and analogue transmission

- **Charge amplifier configuration used as front-end amplifier.**
  - Low noise input stage with 2 JFET (BF862) in parallel (input voltage noise 0.4 nV/Hz$^{1/2}$).
  - For a given signal charge, output voltage only depends on feedback capacitance ($v_o = -Q_{in}/C_{fb}$): charge to voltage converter (C_{fb}= 1pF).
  - Bandwidth 100 Hz-80 MHz. Gain of 42 dB
  - Calibration possible by injecting a known charge through C_{cal} (1 pF).
- **Sum and difference amplifier to generate the Δ/Σ signals.**
  - Using a low noise operational differential amplifier (AD8130) with high CMRR (better than 90 dB up to 2 MHz).
- **Output cable drivers used for Δ/Σ signals (LMH6321).**
- **25 m long Low Transfer Impedance output cables (50 Ω).**
- **Short coaxial input cables (10 cm, 75 Ω) loaded with ferrites and with a triaxial screen for common-mode magnetic shielding (25 dB).**



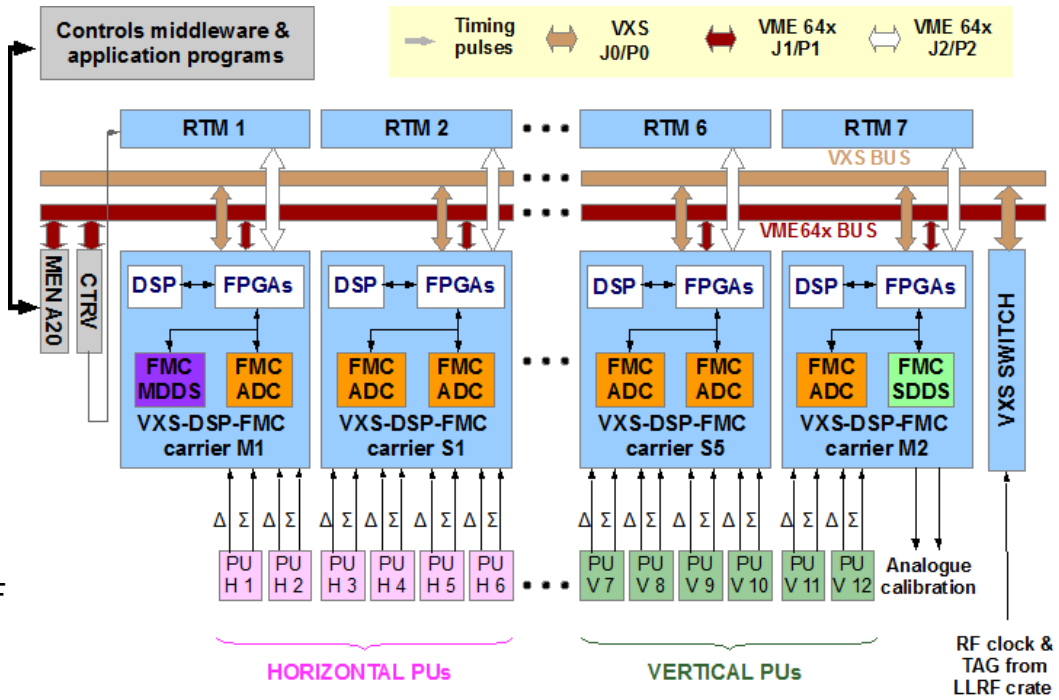
FRONT-END AMPLIFIER FOR EACH BPM ELECTRODE



HEAD AMPLIFIER SIMPLIFIED BLOCK DIAGRAM

ELENA digital acquisition system layout

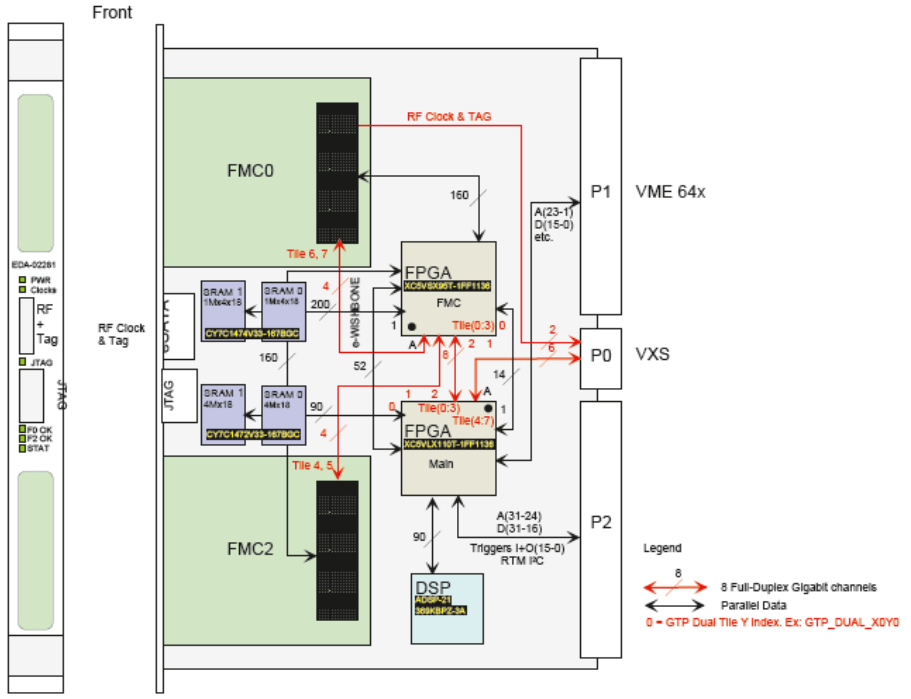
- Digital acquisition system based on an in-house (CERN RF Group) developed hardware family also used in several LLRF systems (PSB, LEIR, ELENA, AD,...) and for the AD orbit system.
- A VME-VXS crate with 7 VXS-DSP-FMC carrier boards.
- A timing module (CTRV) provides the triggers related to the ELENA cycle.
- Digitalization of the BPM signals by 12 FMC-ADC boards.
- Generation of analogue calibration signals by a FMC-SDDS board.
- Common RF clock (programmable higher harmonic of f_{REV}) and a pulsed TAG signal (f_{REV}) synchronise all boards in the system.
- RF clock/TAG generation in two stages: before/after ELENA LLRF system commissioning.
  - By a FMC-MDDS board from f_{REV} (first stage).
  - Obtained from LLRF crate through optical fibre (second stage).
- VXS switch board used to distribute the RF clock/TAG signal and for the communication among VXS-DSP-FMC carriers (100 MSPS/32 bits).



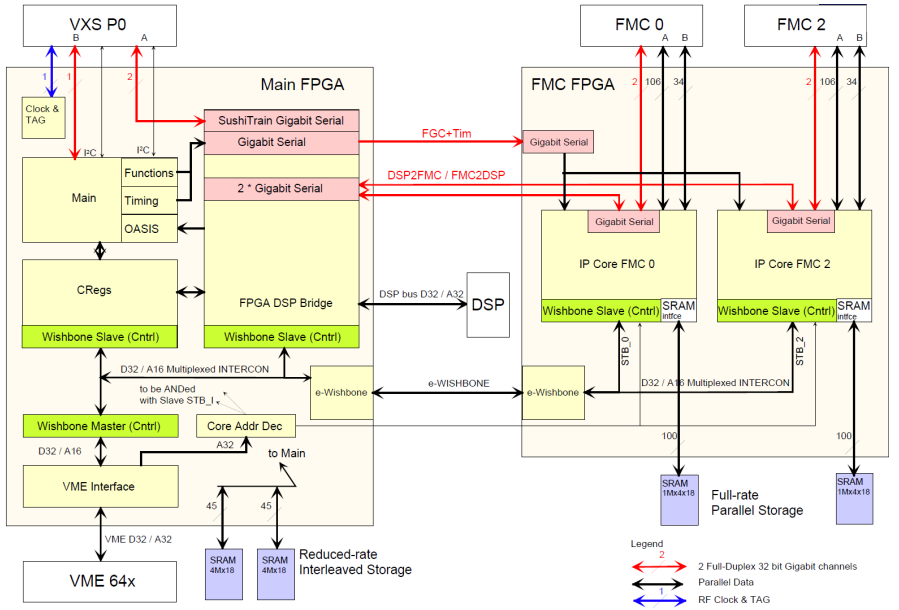
ELENA ORBIT DIGITAL ACQUISITION SYSTEM

VXS-DSP-FMC carrier hardware and firmware

- **6U board.**
  - Two Xilinx Virtex 5 FPGAs: Main (XC5VLX110T) and FMC (XC5VSX95T).
  - SHARC DSP (ADSP-21368) from Analog Devices clocked at 400 MHz.
  - Memory banks (4Mx18 bit at 100 MHz and 1Mx4x18 bit at RF clock).
  - Can host up to two FMC daughter boards with high-pin count format.
  - 2 dedicated full-duplex VXS channels for distributing the RF clock and TAG signal.
  - 6 full-duplex VXS channels bonded to form 3x32bits data paths at 100 MSPS: used to transfer data among carriers.
- **Main FPGA firmware.**
  - Manages the communication with FMC FPGA, VME64x, DSP and VXS.
  - Timing generator (128 ch), vector function generator (16 ch, 32 bit x 1024) and programmable digital signal observation (48 ch, 32 bit x 2048).
- **FMC FPGA firmware.**
  - Implements the custom FMC hardware control and data treatment (IP core FMC 0/ FMC 2): DDC, MDDS or SDDS roles.
  - Communicates to the Main FPGA via 8 Serial Gigabit channels and parallel bus (Wishbone).
- **DSP firmware.**
  - Implements the core data treatment and overall system control.
  - Developed in C code as an Interrupt-driven finite state machine to fulfil time constraints.
  - Three different DSP roles (M1, M2 and S1-S5).
- **Different IP cores (Main FPGA, DSP, FMC common, FMC 0 or FC 2) controlled through register banks accessible by VME64x bus.**



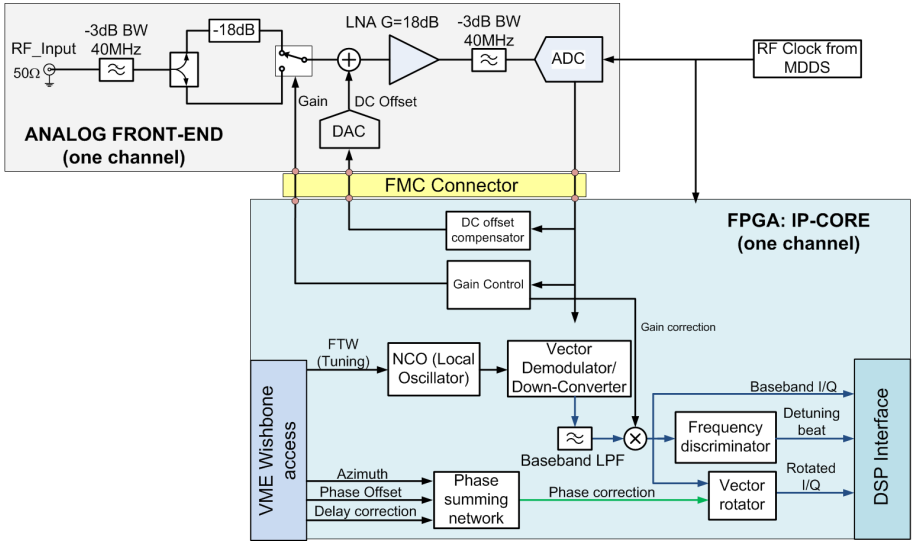
VXS-DSP-FMC CARRIER BLOCK DIAGRAM



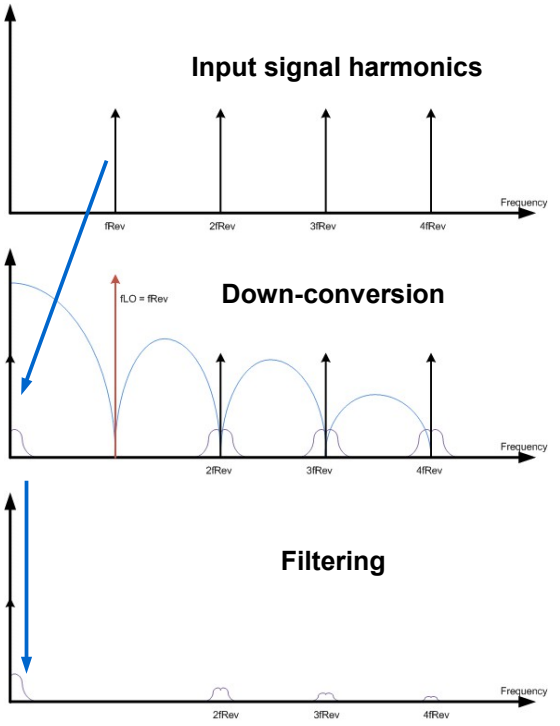
FIRMWARE ARCHITECTURE

FMC-ADC board and DDC firmware

- **FMC-ADC board.**
  - Four independent channel acquisition module.
  - Input signal range ±1V over 50 Ω.
  - ADC (AD9286) with resolution of 16 bits and sampling rate up to 125 MSPS.
  - Channel bandwidth limited to 40 MHz.
  - Selectable gain (0 dB or 18 dB).
  - SNR > 77 dB (12.5 ENOB).
- **Digital down converter (DDC) firmware.**
  - DDC is an homodyne receiver that converts the selected beam revolution harmonic into a baseband I/Q signal.
  - ADC clock and the local oscillator are locked to RF clock.
  - Local oscillator frequency and phase controlled to select the required beam revolution harmonic.
  - Down-converted spectral component keeps its phase and amplitude properties.
  - Baseband low-pass filtering and decimation by means of a first order Cascaded Integrator Comb filter. Decimation (1-255) and differential delay (1-255) programmable.
  - Raw ADC data are also stored other possible measurements (trajectory, intensity).



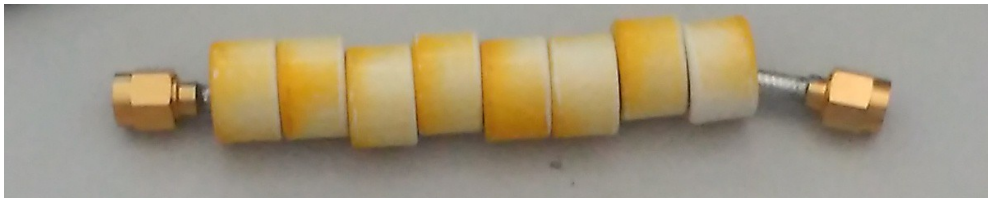
DDC BLOCK DIAGRAM (ONE CHANNEL)



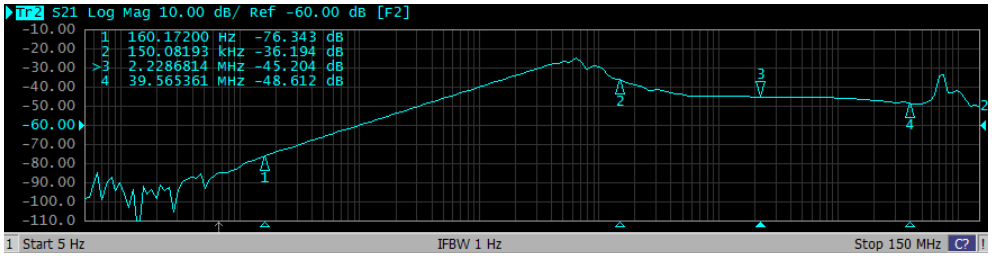
HOMODYNE PRINCIPLE

System status and tests (I)

- **BPMs production ongoing. Problems with NEG coating.**
- **Input analogue cables.**
  - Simulations and measurements to optimize attenuation against common mode currents: minimum of 36 dB between 145 kHz-2 MHz.
  - Measurements with ELENA quadrupole magnets to asses the magnetic field perturbation: results showed very low influence.
  - Measurements to asses the common-mode current attenuation with magnetic field (quadrupole magnet) to be carried out.
- **Head amplifier (collaboration with University of Brescia).**
  - Extensive circuit simulation and testing carried out with two different PCB designs to fulfil tight design requirements.
  - Delta/sigma and output buffer stages fully tested working as expected: design frozen.
  - New PCB design with optimized charge amplifier placement and ultra low noise linear regulators.
  - Prototype to be tested imminently.



10 cm 50 Ω COAXIAL CABLE LOADED WITH 8 FERRITES (3E5 MATERIAL FERROXCUBE, μ_r = 8000).

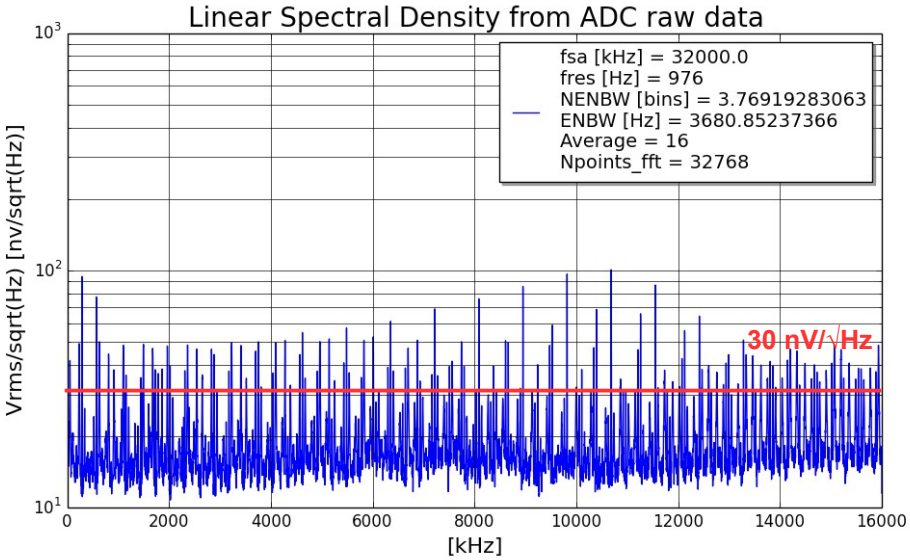


INPUT CABLE ATTENUATION [dB vs. Hz] AGAINST COMMON-MODE INJECTED CURRENT. FREQUENCY BETWEEN 5 Hz AND 150 MHz.

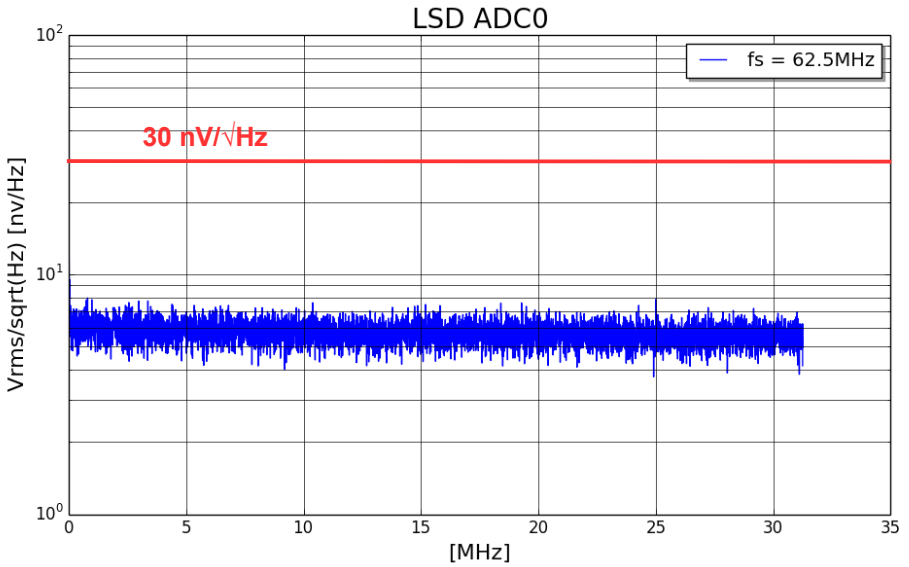
ELENA HEAD AMPLIFIER PROTOTYPE

System status and tests (II)

- **Most of the hardware required for the system already produced and tested.**
- **Current version of the FMC-ADC daughter boards was found to be too noisy for the system.**
  - Noise peaks of up to 100 nV/√Hz in the bandwidth of interest (174.5 kHz - 1.59 MHz) due to on-board DC-DC switching converters.
  - Noise density level of the FMC-ADC board must be lower than 30 nV/√Hz.
- **New AC-coupled FMC-ADC board developed.**
  - Only positive power supply levels generated with linear regulators.
  - Measurements with a prototype show a noise density level below 10 nV/√Hz.
  - Final prototype validation in March and production/test in April.
- **FPGA firmware upgraded.**
  - To allow communication of up to 32 VXS-DSP-FMC carriers via the VXS.
  - Other minor changes to tailor the system for orbit measurements.
  - Small changes required for trajectory measurements to be implemented.
- **New DSP firmware for each VXS-DSP-FMC carrier (M1, M2 and S1-S5) fully developed.**



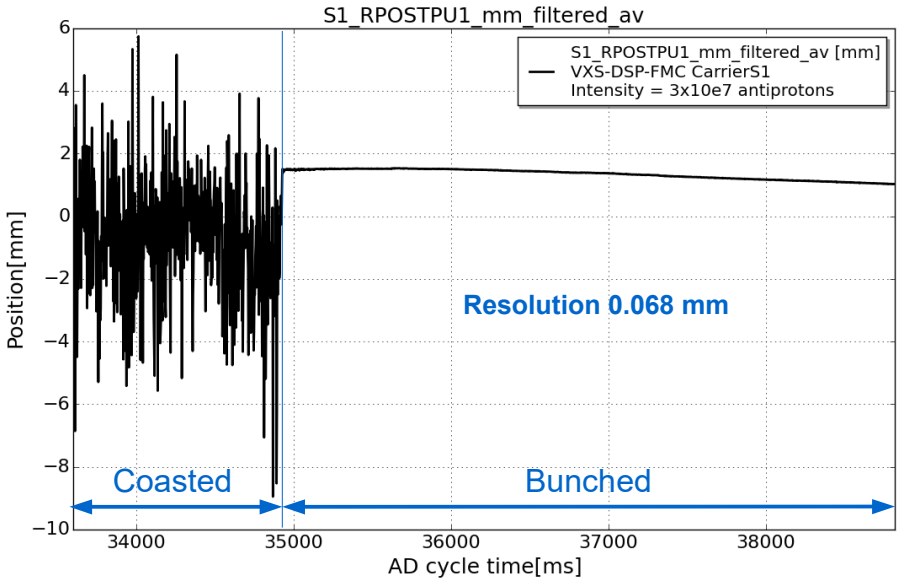
DC-coupled FMC-ADC board noise density level



AC-coupled FMC-ADC board noise density level

System status and tests (III)

- **A prototype version of the system already tested in AD with beam.**
  - A VXS-VME crate with 8 carriers (M1, M2 and S1-S6) and a CTRV timing module.
  - Front-end software based on python scripts .
  - Acquire data from all vertical BPMs and test features of the system in real conditions.
  - Position signal (resolution better than 0.1 mm) during the first flat top/deceleration ramp in the AD cycle (from 35 s onwards beam is bunched).
  - Vertical close orbit during the first flat top (35.55 s) acquired (blue line) agrees with the measurement from the current orbit system (green line).
  - The prototype system is able to measure the vertical orbit during the AD cycle according to the requirements (same as for ELENA).
- **Detailed specifications for the front-end software already written.**
- **Front-end software (Expert GUI and FESA instrument) to be developed by our BE-BI-SW colleagues: based on the AD orbit software.**
- **System initialization scripts to be called by the front-end software already developed.**



Vertical BPM position measurement during the first flat top and deceleration ramp in the AD cycle

Position measurement all vertical BPMs acquired during the first AD flat top (at 35.55 s) with the current orbit system (green line) and the prototype version of new orbit system (blue line)

Conclusions

- BPMs manufacturing ongoing.
- Head amplifier prototype final version already developed and to be tested imminently
- Digital acquisition system hardware mostly tested. New FMC-ADC boards to be produced in April.
- Digital acquisition system firmware directly adapted from AD system for orbit measurements. Some changes required for trajectory measurements already agreed with RF colleagues to be implemented.
- Firmware changes required for bunched intensity/Schottky measurements will be developed after ELENA commissioning.
- Front-end software (low level configuration/Expert GUI/FESA Instruments) to be adapted from AD system.

Acknowledgements

- **Special thanks to...**
  - BE/BI/PI team: Romain Ruffeux, Franck Guy Guillot-Vignot, Juan Carlos Allica and Lars Søby.
  - Flemming Pedersen.
  - BI/SW colleagues: Ewa Oponowicz, Michael Ludwig and Lars Jensen.
  - BE/RF/FB colleagues: Jorge Sanchez Quesada, John Molendijk, Michael Jaussi and Maria Elena Angoletta.
  - University of Brescia colleagues: Marco Bau, Marco Ferrari and Vittorio Ferrari.
  - TE/MSC/MM: Lucio Fiscarelli.
  - BE/BI/QP: Tom Levens.

The ELENA Orbit System

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Back-up slides

Orbit measurement principle

- The analogue front-ends deliver RF difference and a sum signal for each BPM, i.e. 126 signals, which are digitized and down converted to baseband by the digital acquisition system.
- Depending on the level of RF induced EMI, the measurements will be carried out using the first or second harmonic of the bunched beam signal.
- After low pass filtering and decimation of the complex I/Q data the positions are calculated according to:

$$Pos(\mathrm{t}) = k \cdot \left(\frac{1}{\frac{\Delta}{\Sigma}_{cal}} \right) \cdot \left(\mathrm{Re}\left\{ \frac{I_{\Delta}(t) + jQ_{\Delta}(t)}{I_{\Sigma}(t) + jQ_{\Sigma}(t)} \right\} - \frac{\Delta}{\Sigma}_{zero} \right) + BPM_{off}.$$

- The digital acquisition system includes a calibration procedure to obtain the calibration parameters required to calculate the position (Δ/Σ_{cal} and Δ/Σ_{zero}) .

FMC-MDDS and FMC-SDDS boards

- **FMC-MDDS.**
  - RF clock and TAG synchronization signal generator.
  - RF clock signal up to 125 MHz at f_{REV} harmonics from 1 to 255.
  - 10 MHz input reference clock required.
  - Two independent channels synchronized to same input reference.
  - 32 bit DDS core (AD9858) with 232 mHz of frequency step resolution.
  - Possibility of RF clock and TAG signal distribution through VXS switch or front panel eSATA connector.
- **FMC-SDDS.**
  - Generates the analogue calibration signals required by the head amplifiers.
  - Based on 2 dual 16 bit DAC (AD9747).
  - Four independent DC coupled output channels.
  - Programmable gain (0 dB or 18 dB).
  - Bandwidth of 40 MHz and 3.6 V_{pp} full scale output voltage.

FMC-MDDS BOARD

FMC-SDDS BOARD