TWEPP 2016 - Topical Workshop on Electronics for Particle Physics

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Karlsruhe Institute of Technology (KIT)

Book of Abstracts
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MTCA.4 Basics - Introduction in xTCA

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Opening

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Welcome from Local Organizers

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Welcome from KIT

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Particle Physics in Germany

Corresponding Author:

In Germany nearly 30 universities and several research laboratories perform research in particle physics. This includes a strong theory community and the participation in a wide range of experiments, R&D projects, accelerator physics and computing. A strong focus is on the LHC physics programme. The talk will give an overview of the activities as well as the structure and perspective in this field in Germany.

Highlights and Trends of Detector Instrumentation and Technology Development in Germany

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Detector instrumentation and the development of the underlying technologies in Germany take place in a rather diverse landscape of institutions. This includes university groups, Helmholtz centres, Max Planck institutes, Fraunhofer institutes and others. With the creation of the Helmholtz programme "Matter and Technologies" the field of detector instrumentation in Germany has been strengthened further. The talk will summarize selected highlights of detector instrumentation in the broadest sense. Trends and future opportunities will be covered, and again the focus will be on less well-known examples.

Invisibility Cloaking of Metal Contacts on Solar Cells and LEDs

Corresponding Author:

Within the last decade, the idea of invisibility cloaking has turned from Science Fiction to scientific reality. Here, we review the underlying principle based on coordinate transformations and demonstrate application in terms of making metallic contacts on solar cells, detectors, and light-emitting diodes invisible.

The KATRIN experiment - the most precise scale for neutrinos

Corresponding Author:
The Karlsruhe Tritium (KATRIN) experiment is a large-scale international project at KIT comprising about 120 scientists, engineers, and students from 6 countries. Its scientific goal is to improve the sensitivity of current direct neutrino mass experiments by one order of magnitude down to neutrino masses of 0.2 eV, which is of key importance for astroparticle physics. This is achieved by combining a high-intensity molecular gaseous tritium source with a high-resolution electrostatic retarding spectrometer, which is read out by a segmented Si-Pin diode array. As only electrons close to the β-decay endpoint energy of 18.6 keV carry information on the neutrino mass, KATRIN scans the spectral shape of decay electrons in a narrow region of a few eV below the endpoint.

The talk gives an overview of the measuring principle of KATRIN and the status of its central components, which are in the final stages of commissioning, and closes with an outlook to the upcoming first light measurements.

Summary:

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The Accelerators of the FAIR Project

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The FAIR Project at GSI Helmholtzzentrum für Schwerionenforschung in Darmstadt (GSI) will offer unique research capabilities with heavy ion and antiproton beams. The ambitious goals of the scientific communities require to extend the capabilities of the present accelerators at GSI which will be the injectors of the future facility and push the future accelerators to the technical limits. We will report on the status of the upgrade program of the present accelerators and the project status of the future FAIR facility.

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MEMS Sensors: Enabler for the IoT

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Consumer electronics focus on low cost, small size, low power consumption and overall system performance. This leads to combined multi-axis sensing structures, integrated power management schemes and sensor data fusion. Bosch is actively driving this evolution further with novel multiple sensors on one single chip which will become the key element for new IoT applications.

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Development of the ABCStar front-end chip for the ATLAS Silicon Strip Upgrade

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The ATLAS experiment will use an all-silicon tracker in the Phase II upgrade for the HL-LHC collider at CERN. For the Silicon Strip detector of the ITk, a new readout chip ABCStar is under design to meet the new requirements of higher trigger rates and lower latency. We summarize the status of this work and present the new features of the chip.

Summary:

The ABCStar chip is a new generation of front-end readout ASIC for Silicon Strip Detector in ATLAS Phase II upgrade. This chip provides all functions required for processing the signals from 256 strips of a silicon strip detector in the ATLAS experiment employing the binary readout.

The architecture chosen for ABCStar allows a multi-trigger data flow control retaining the Beam Crossing Synchronous pipeline transfer signal (L0 here) from previous versions, an asynchronous Regional Readout Request (PR here) and a second level asynchronous data readout intended for a global readout (LP here).

Besides the essential front-end and power regulation, the main functional blocks of the digital part are: Mask and Edge Detection, pipeline, event buffer, cluster finder, readout logic, command decoder, threshold and calibration control.

The signals from the detector are first processed by the front-end which contains 256 analogue preamplifier-shapers followed by discriminators with individual threshold trimming capabilities. The binary output of the discriminator are sampled at the bunch crossing clocking rate and stored in the pipeline after “edge detection” process. At the reception of L0 signal, the data in the memory that were stored at some fixed latency time before the L0 signal are extracted from the pipeline and transferred to the event buffer and stored as events tagged with an appropriate L0ID number. If a PR or LP signals are received with the corresponding L0ID number, the event is extracted from the event buffer and processed through the cluster finder. The cluster finder block acts as a data reduction circuit, creating a “cluster” byte for channels found with hits. The readout block does formatted packets with the event identification and the associated cluster bytes. The data is transmitted serially to the following HCC chip with point to point connection.

In order to meet the new requirement of higher trigger rates and lower latency, the ABCStar differs from ABC130 and its predecessors, especially in the digital part. It employs the edge detection circuit in front of the pipeline to adapt to the possible consecutive L0s, this also simplify the control logic of the two step memories. A cluster finder block with new algorithm was designed, which is much faster to fulfill the latency requirement in PR readout mode. Other features like the hit counter based calibration mode, L0-tag are also considered to add to the logic design of ABCStar.

At present, we have built up the whole data path for the digital design, and the protocol of ABCStar command and control from the companion chip HCCStar is still in definition phase. The functional verification for the whole digital part using the Universal Verification Methodology (UVM) is also under progress.

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**Using MaxCompiler for High Level Synthesis of Trigger Algorithms**

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Firmware for FPGA trigger applications at the CMS experiment is conventionally written using hardware description languages such as Verilog and VHDL. MaxCompiler is an alternative, Java based, tool for writing FPGA applications and removes some of the need for electronics expertise. This provides potential to lower the barrier for contribution to firmware design. An implementation of the jet and energy sum algorithms for the CMS Level 1 Trigger upgrade has been written using MaxCompiler to benchmark against the production VHDL implementation in terms of accuracy, latency, resource usage, and code size.

Summary:

The use of conventional hardware description languages (HDLs) presents a barrier to contribution to trigger algorithms, leading to a code-base which is understood by only a few expert contributors. By investigating other tools available for firmware design it may be possible to open algorithm development up to a greater number of designers, and to improve the maintainability of the code. In the context of ongoing trigger upgrades at the CMS experiment, an improvement in ease of development and maintainability of algorithms would be highly beneficial. The planned track trigger and endcap calorimeter upgrades, in particular, will have a significant complexity in their algorithms.

Here MaxCompiler is investigated as a tool for the design of trigger applications. The tool uses a Java based language for firmware development, providing a higher level of abstraction than HDLs. Language aspects that ease the development compared to HDLs are explored, as well as design patterns that yield a low latency and resource usage. Other tool features that benefit development are presented, including functional design simulation that simplifies testing an algorithm on data.

The CMS Level 1 Calorimeter Time Multiplexed Trigger jet and energy sum algorithms have been implemented using MaxCompiler to demonstrate the feasibility of using such a tool for an existing trigger application. These algorithms are part of the Run II calorimeter trigger upgrade in which all data from a bunch crossing is passed through a single processor node. The MP7 board, as used in the trigger upgrade and which houses a Virtex-7 FPGA, is targeted. MaxCompiler 'kernels' have been written and compiled to integrate with the rest of the board infrastructure. The latency and resource usage is compared to the original design written in VHDL, to investigate any difference associated with using a higher level language. The design equivalence is demonstrated by comparing the output of each implementation on simulated data.

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Software and Firmware co-development using High-level Synthesis

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Accelerating trigger applications on FPGAs (using VHDL/Verilog) in CMS experiments at LHC-CERN warrants consistency between each trigger firmware and its corresponding C++ model. This tedious and time consuming process of convergence is exacerbated during each upgrade study. High-level synthesis, with its promise of increased productivity and C++ design entry bridges this gap exceptionally well. This paper explores the "single source code" approach using Vivado-HLS tool for redeveloping the upgraded CMS Endcap Muon Level-1 Track finder (EMTF). Guidelines for tight latency control, optimal resource usage and compatibility with CMSSW are outlined in this paper.

Summary:

Acceleration of trigger applications in CMS experiments in the Large Hadron Collider at CERN has been traditionally performed on FPGAs using hardware description languages (HDLs) such as VHDL/Verilog.
Specifics of the large-scale high-energy physics experiments require that each trigger firmware design must be accompanied by a software model that can be used for analyzing its performance, verification of hardware functionality, and other tasks. These software models must be designed in C++ and be compatible with the CMS software framework, CMSSW.

Since CMS upgrades firmware algorithms and trigger hardware at regular intervals, the software models must be constantly kept synchronized with firmware algorithms. The typical approach is to write these models by hand. Since the trigger firmware designs are substantially complex, creating and maintaining the software models that exactly match firmware behavior is a major challenge. The final convergence between the firmware and software model is especially tedious; it usually takes months to find and fix small mismatches.

Since 2002, the CSC Track-finder system of the CMS Endcap Muon Level-1 trigger has maintained the C++/RTL model consistency by using a homemade VPP library which automatically generates C++ and Verilog files from a single source code. This approach worked extremely well for less complex firmware design of the legacy system, providing full consistency between firmware and software model automatically. However, the recent hardware upgrade brought much larger FPGAs and much more complex firmware algorithms, and VPP has become inadequate for this task.

Recent advancements in high-level synthesis tools (HLS) hold the promise of high productivity through the use of design entry in C++ that reduces the difficulty for developing and managing code complexity at the HDL level. However, the major challenge in using HLS is to be able to use C++ constructs to perform fine-grained control of the generated firmware in such a way that it satisfies the constraints of CMS trigger applications:

• Stringent latency requirements.
• Limited FPGA resources.
• Compatibility with CMSSW.

In this paper, we present our exploration into using a "single source code" approach in which we perform software and firmware co-development using Vivado HLS, a C++-based high-level synthesis tool used for Xilinx FPGAs. Vivado HLS enables us to have a single source code which can be used as the C++ model for verification by physicists and to generate the RTL model to synthesize firmware for the FPGA. Based on the lessons learned in our exploration, we developed design patterns and guidelines to execute the fine-grained control of the generated firmware. The results are very promising:

• The code of the upgraded CMS Endcap Muon Level-1 Track Finder (EMTF) was redeveloped in Vivado HLS.
• All latency constraints were met in all modules of the EMTF algorithm.
• HLS resource usage was comparable to (and, in some cases, better than) resource usage of manually written Verilog code.
• Based on the developed guidelines, minor changes were made to the coding style, resulting in all HLS code being compatible with CMSSW.

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SALT Readout ASIC for Upstream Tracker in the Upgraded LHCb Experiment

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SALT is a new 128-channel readout ASIC for silicon strip detectors in the upgraded Tracker of LHCb experiment. It will extract and digitise analogue signals from the sensor, perform digital processing and transmit serial output data. SALT is designed in CMOS 130 nm process and uses a novel architecture comprising of analog front-end and ultra-low power (<0.5 mW) fast (40 MSps) sampling 6-bit ADC in each channel. An 8-channel prototype were already tested and the full 128-channel version was submitted. The design and first tests of 128-channel version will be presented.

Summary:

The present Large Hadron Collider beauty (LHCb) detector performance is limited by readout electronics and data acquisition architecture. After the upgrade of LHC machine it will be capable to deliver more than one order of magnitude higher luminosity than presently used by the LHCb detector. To achieve
this goal various detectors will need a new faster front-end electronics with the read-out running at the 
bunch-crossing rate of 40MHz.

Silicon strip detectors in the upgraded Upstream Tracker (UT) of LHCb experiment will require a new 
readout ASIC called SALT (Silicon ASIC for LHCb Tracking). A project of a 128-channel SALT ASIC 
is ongoing. It extracts and digitises analogue signals from the sensor, performs Digital Signal Process-
ing (DSP) and transmits a serial output data. The ASIC is designed in CMOS 130nm technology, and 
uses a novel architecture comprising an analogue front-end and an ultra-low power (<0.5mW) fast 
(40MSPs) sampling 6-bit ADC in each channel. The front-end comprises a charge preamplifier and a 
fast ($T_{\text{peak}}=25\text{ns}$) non-standard (fast recovery) shaper required to distinguish between the LHC bunch 
crossings at 40MHz. The front-end should work with sensor capacitances between 5-20pF. An ultra-low 
power (<1mW) DLL is used to control precisely the ADC sampling phase.

Digitised data from each ADC channel are processed in a DSP block which first subtracts pedestals and 
calculates mean common mode, which is then subtracted in each channel. The last DSP step is zero 
suppression (ZS). After ZS the data are buffered in SRAM, then a packet is formed and sent to DAQ via 
a number of serial DDR e-links.

An ultra-low power (<1mW) PLL is used in data serialization and fast data transmission circuitry.

Prototypes of all important SALT blocks, i.e. 8-channel analogue front-end, 8-channel 6-bit ADC, PLL, 
DLL and, SLVS I/O were designed in CMOS 130nm, fabricated and tested, showing very good perfor-

An 8-channel SALT prototype comprising all important functionalities was produced and found, in tests, 
to be fully functional. In the first step, the serializers (DDR e-links) and deserializer were checked. Next, 
the DSP operation was tested extensively and all its functionalities were correct. After verification of 
digital processing and data transmission analogue pulses were observed, using DLL to shift the ADC 
sampling phase. Such measurements showed that pulse shape from front-end is correct, gain is about 
0.45 ADC LSB/ke and the noise is below one LSB for input capacitance 10pF. The channel-to-channel 
baseline offset spread can be easily corrected by trimming DACs located in each channel, what was 
verified for all channels.

The full 128-channel prototype was just submitted. It includes also all blocks which were omitted in 
previous prototype: internal generation of common mode voltage, monitoring ADCs, band-gap ref-
ference source, variable number of active e-links, etc.. The first test results of this prototype will be 
presented.

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First results of the front-end ASIC for the strip detector of the 
PANDA MVD

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PANDA is a key experiment of the future FAIR facility and the Micro Vertex Detector (MVD) is the 
innermost part of its tracking system. It will be composed of four barrels and six disks, instrumented 
with silicon hybrid pixel detectors and double-sided microstrip detectors.

PASTA (PAnda STrip ASIC) is the readout chip for strip sensors.

An overview of the chip, of its readout system and of the first results of its characterization will be 
presented.

Supported by BMBF, HIC4FAIR and JCHP.
Summary:

PANDA is a key experiment of the future FAIR facility, under construction in Darmstadt. It will study the collisions between an antiproton beam with momenta between 1.5 GeV/c and 15 GeV/c and a fixed proton or nuclear target, allowing to study QCD at intermediate energies. The Micro Vertex Detector (MVD) is the innermost part of the tracking system of the experiment; it will be composed of four concentric barrels and six forward disks, instrumented with silicon hybrid pixel and double-sided silicon microstrip detectors.

The triggerless operation of PANDA, in addition to the high expected collision rate, poses significant challenges on the detector readout electronics. The PASTA (PAnda STrip ASIC) chip has been developed to read out the strip sensors of the MVD and its architecture is based on the Time-over-Threshold technique.

The first stage of the analog frontend chain consists of a preamplifier which can be connected to both n-type and p-type strips, and a second stage where a constant current discharges a feedback capacitance to extract a linear ToT information.

The leading and trailing edges of the ToT signal are measured with time-to-digital converters with linear analog interpolators, with an architecture inherited from TOFPET [1], thus providing a time resolution adjustable between 50 and 500 ps.

A 64 channel chip prototype has been submitted in a commercial 110 nm CMOS technology; the final prototype size is 3.4 x 4.5 mm².

The chip is hosted and wire bonded on a test board which allows to connect the LVDS input/output lines to the acquisition system, as well as to probe the analog and digital test pads. Additionally, a strip sensor can be placed on the board and connected to the chip channel inputs.

In order to completely characterize the chip, the Jülich Digital Readout System (JDRS) is used. The system, originally developed to read out the pixel electronics of the MVD, is based on a Virtex 6 FPGA on a Xilinx development board. Its structure consists of four layers which handle the ethernet connection between the FPGA board and the PC, the data transfer and formatting and the board-specific and chip-specific functions. Thanks to this modularity, the system can be adapted with relative ease to test different chips in high-rate environments.

The first test of the PASTA chip concerns the functionality of the global controller and of its capability of reading and storing the chip configuration.

The analog frontend chain can be tested by means of injecting a pulse on a test pad and probing the output of the ToT amplifier through dedicated pads.

Finally, it is possible to simulate the comparator output by injecting a pulse in the digital local controller, thus allowing to test the TDC block, consisting of the analog TDC and of the local controller.

The work was supported by BMBF, HIC4FAIR and JCHP.

[1] M.D. Rolo et al.
TOFPET ASIC for PET Applications, 2013 JINST 8 C02050

Power, grounding and shielding / 9

Serial Powering Pixel Stave Prototype for the ATLAS ITk upgrade

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A Serial Powering Stave Prototype has been developed using FE-I4 Quad Pixel Modules in order to investigate a Serial Powering scheme for ATLAS ITk Phase II Pixel upgrade.
The talk will explain the need for a new powering scheme which is different from the currently used parallel (direct) powering in order to power detector modules for the ATLAS ITk Phase II Pixel upgrade. The Serial Powering building blocks will be introduced and the full scale prototype will be described. Detailed investigations of the electrical performance including robustness against noise and power failures will be shown.

**Summary:**

ATLAS ITk is a new inner tracker that will be built for the Phase II upgrade in order to meet the requirements of increased Luminosity.

Current pixel detector modules are powered according to the parallel (direct) powering scheme: each detector module is powered with an independent power supply and a set of cables. With this powering scheme modules can be operated individually, which is a big advantage. However, due to increased granularity of the detector more cables are needed for powering. Increased FE current consumption leads to increase in cable cross section. All these increases power losses in the cables as well as the amount of passive material in the active detector volume. Finally, it results into unwanted interactions of particles with the inactive part of the detector and degradation of the detection performance.

The solution is to use a new powering scheme, different from direct powering. Proposed options are Serial Powering and DC-DC converters scheme. Serial Powering scheme is the main focus here.

A Serial Powering Pixel Stave Prototype has been developed using FE-I4 Quad Modules in order to investigate a Serial Powering scheme for ATLAS ITk Phase II upgrade. The Stave Prototype holds 6 Quad Pixel Modules that are connected in series and powered with a constant current source. Shunt-LDO regulators, that are a combination of shunt and linear regulator, are used at the module level to generate the supply voltage out of the constant current. Some of the modules have on-flex PSPP chip, which allows bypassing a particular module to avoid loosing a complete Serial Powering chain if only one module is failing. PSPP chips are controlled via an additional control and power lines. AC-coupled data transmission is used because modules are on different ground potentials. End of Stave connections provide power for the modules, high voltage for the sensors, cooling and readout lines. The Readout is implemented with the help of the USBpix3 readout system that was developed in Bonn.

Various characterization measurements have been performed with the Stave Prototype. 6 modules were tuned successfully to ATLAS IBL target values. Performance studies with noisy and bypassed modules were made. Both static and dynamic bypassing effects were investigated. The minimum operational threshold of the Serial Powering system was determined with two different methods. 2-trigger threshold and noise occupancy scans with different Trigger lengths were performed with modules tuned to IBL target values and to the minimum threshold.

**ASIC / 87**

**A Prototype of a New Generation Readout ASIC in 65nm CMOS for Pixel Detectors at HL-LHC**

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This paper describes a readout ASIC prototype designed by CHIPIX65 project, part of RD53, for a pixel detector at HL-LHC. A 64x64 matrix of 50x50 \( \mu m^2 \) pixels is realised. A digital architecture has been developed, with particle efficiency above 99.5 % at 3GHz/cm\(^2\) pixel rate, 1MHz trigger with 12.5\( \mu \)sec latency. Two analog front end designs, one synchronous and one asynchronous, are implemented. Charge is measured with 5-bit, analog dead-time below 1%. IP-blocks (DAC, ADC, BandGap, SER, sLVS-TX/RX) and very front ends are silicon proven, irradiated to 600Mrad.

### Summary:

The HL-LHC accelerator will constitute a new frontier for particle physics after year 2024. Major experimental challenge resides in inner tracking detectors: here the dimension of sensitive area (pixel) has to be scaled down with respect to LHC detectors.

This paper describes a readout ASIC in 65nm CMOS with a matrix of 64x64 pixels each of dimension 50x50 \( \mu m^2 \), designed by CHIPIX65 project, part of RD53 Collaboration. It is a demonstrator of a Pixel Phase 2 chip, with compact design, low power and in-time threshold below 1000e\(^-\). All IP-blocks and analog front ends are designed by CHIPIX65 project in the framework of RD53 Collaboration: they have been produced, tested and several have already proven to be radiation hard up to 5-800 Mrad.

The chip implements two different analog front end designs, one with asynchronous the other with synchronous comparator designs, but with main common characteristics: compact design; ENC below 100 e\(^-\) for 50 fF input capacitance; below 5 \( \mu W/\)pixel power consumption; fast rise time, allowing correct time-stamp; signal digitisation using Time Over Threshold; leakage current compensation up to 50nA per pixel.

All global biases and voltages are programmed in the chip periphery, for each value a 10-bits current steering global DAC is used; a band gap circuit provides a stable reference voltage. The adopted strategy is very robust, easily scalable and mismatch effects are kept to a negligible level. Bias voltages and current are monitored by a 12-bit ADC.

A novel digital architecture has been designed in order to maintain a high efficiency (above 99% ) at pixel hit rate of 3 GHz/cm\(^2\), trigger of 1 MHz rate and latency of 12.5\( \mu \)sec. The digital architecture is organized into pixel regions: in order to have a very compact and low power architecture, a large pixel region consisting of 4x4 pixels has been used. A 5-bit ToT charge is stored in a centralised latency buffer: at the arrival of a trigger, a matching logic selects eventually the right memory location and sends the data to the End of Column logic. The particle inefficiency due to this architecture is about 0.1% for an area occupation of 65% and a low power consumption. The readout is obtained using a column drain protocol with a FIFO for each pixel region column, connected to a global dispatcher FIFO that after a 8b10b encoding splits the data into 20-bit trunks and sends them to a serialiser.

Data are sent out from the chip using a differential transceiver converting the CMOS into SLVS JEDEC 400mV standard. Given the small size of the chip, an output rate of 320 MHz for the serialised data can be used, but higher output rates are possible, since SER and sLVDS-TX are designed to sustain up to 1.2 Gb/s. Chip configuration is performed through fully-duplex synchronous SPI-master/slave transaction.

CHIPIX65 demonstrator will be submitted in June 2016.
A new vertical JFET technology, based on a 3D trenched design, has been developed at the IMB-CNM. Conceptually introduced in TWEPP 2015, these transistors are conceived to work as radhard switches in the HV powering scheme of the ATLAS ITk strip detectors. The first fabricated wafers have been fully characterized and the results are presented here. Device performance is very close to specifications and shows excellent agreement with simulations. Radiation tolerance is currently under study. No noticeable effect has been seen from gamma irradiations; the impact of neutron and proton irradiation will be discussed in the final contribution.

Summary:

The current HV powering scheme for the strip detectors in the ATLAS upgrade ITk requires the use of slow-controlled switches to disconnect malfunctioning sensors from the bias, allowing normal operation of the remaining sensors in the same power line. Switches should survive high radiation environment, being able to sustain >500V and drive several mA. As presented in TWEPP2015 conference, IMB-CNM (Barcelona) has developed a new silicon vertical JFET technology, which can fulfill the HV switch specifications.

The VJFETs present a cellular design; each cell has a p-type silicon channel surrounded by a deep trench, typically less than 100µm depth. Filled with highly doped n-type polysilicon, the trenches act as the transistor gate. Source electrode is implemented with a highly doped p-type implant at the top centre of each cell, whereas a blanket p+ implant creates the drain electrode at the back of the wafer, far enough from the trench to assure the device voltage capability. The transistor is normally operating in on-state (with VG=0V), allowing current flow through the channel. If the gate is biased above a threshold value (VOFF), the channel becomes fully depleted and the current flow is drastically reduced, unbiasing the corresponding sensor. The use of high resistivity substrate keeps VOFF below 3V, whereas the high number of parallel cells (more than 10k) ensures a high enough current drive to keep the voltage drop across the device below 1V. In addition, the substrate choice and the vertical configuration enhance the radiation hardness of the transistors, both against displacement and ionizing damage.

The first batch has been fabricated in the IMB-CNM clean room, with a relatively low resistivity substrate (180-650Ω·cm), looking for the highest current capability. Several device layouts were considered, including different channel diameters (23, 29 and 35µm). Characterization results show VOFF<2V, for the narrower channel devices, with on-state current higher than 15mA and Vdrop<0.5V, already meeting the specifications. In addition, the measured curves exhibit an excellent fit with TCAD simulations. Most devices exhibit early breakdown at the blocking mode (High VDS, with VG>VOFF) motivated by the moderate resistivity of the silicon substrates. This is now under study and will be carefully addressed in the final contribution, including IR thermography analysis, simulation prospects for higher resistivity substrates and additional measurements.

Concerning radiation hardness, the first prototypes have been gamma irradiated up to 10Mrad(Si), with no noticeable effects on their characteristics, as predicted from simulations. 50Mrad(Si) irradiation has been also scheduled and the results will be presented in the final contribution. Neutron and proton irradiation are also programmed to study the impact of displacement damage on the VJFET performance.

An additional batch is now under fabrication, with higher resistivity substrates, in order to increase the voltage capability and reduce the VOFF of the wider channel devices, thus obtaining a full compliance with the specifications. The characterization of the second batch will be also included in the final contribution.

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A synchronous analog very front-end in 65nm CMOS with local fast ToT encoding for pixel detectors at HL-LHC

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This work describes the design, in 65nm CMOS, of a very compact, low power, low threshold synchronous analog front-end for pixel detectors at HL-LHC. Threshold trimming is avoided using offset compensation techniques. Fast ToT encoding is possible, as the comparator can be turned into a local Oscillator up to few hundreds MHz. Two small prototypes have been submitted and tested; a X-ray irradiation up to 600 Mrad has been performed. Detailed results in terms of gain, noise, ToT and threshold dispersion are presented. This design will be part of the CHIPX65 demonstrator and of the RD53A chip.

Summary:

The HL-LHC accelerator will start its operation in 2025. It will establish unprecedented benchmarks in particle detection, in particular for the inner tracking systems of the experiments. Silicon pixel detectors and front-end electronics will face new challenges in terms of particle flux (up to $2 \text{GHz/cm}^2$), radiation hardness (1 Grad in 10 years) and increased granularity (pixel size of 25x100 $\mu\text{m}^2$ or 50x50 $\mu\text{m}^2$).

In this paper the design of a new front-end for HL-LHC pixel sensors in 65 nm CMOS technology is presented. It consists of a one stage Charge Sensitive Amplifier with Krummenacher feedback AC coupled to a synchronous discriminator. The latter stage features a low gain differential amplifier and a track-and-latch comparator. The design has an area of 1225 $\mu\text{m}^2$ and a power consumption of 4.4 $\mu\text{A}$.

The offset compensation is performed via internal capacitors using the output offset storage technique, so that no threshold trimming via DACs is required. The latch can be also turned into a local oscillator by means of an asynchronous logic feedback loop in order to implement a fast time-over-threshold counting. This work has been performed and funded by the CHIPX65/INFN project in the framework of CERN RD53 Collaboration.

Two testing prototypes containing a 8x8 pixel matrix have been submitted in October 2014 and in May 2015. Results in terms on gain, noise, ToT and offset compensation are presented. The voltage gain measured in all 64 pixels shows a very good linearity and uniformity with an RMS of 2.2%. The ToT linearity has been verified on a large interval of input charges (1-40 ke). Noise shows a linear increase with the input capacitance: a ENC of 80 e- for an input capacitance of 50 fF is measured for a fast ToT of 90ns for 10ke- signal, important to keep analog dead-time below 1%. The first prototype showed a threshold dispersion after the offset compensation phase equal to 174 e- RMS due to the mismatch of the latch stage; also an undesired baseline time-dependency was found. In order to fix this, the comparator was revised in the second prototype, leading to a reduction of the threshold dispersion to 70 e- RMS and eliminating any time-dependency.

The second chip was irradiated with X-ray up to 600 Mrad: analog signal amplitude, peaking time, noise and fast ToT frequency have been monitored during irradiation. The gain remains almost unaffected, while the peaking time increases from 24 ns to 31 ns. Offset compensation still works properly. A 10% increase in noise for 50fF capacitance has been measured. The ToT frequency decreases linearly with radiation. These results have been compared with simulations using radiation models provided by the RD53 collaboration.

This front-end has been included in the CHIPX65 demonstrator, a 64x64 pixel matrix designed by the CHIPX65 collaboration and will be part of the RD53A final chip.
flash process, which is immune to changes in configuration due to radiation effects. An overview of the features and performances of RTG4 FPGAs will be provided, as well as development software, EcoSystem solutions, devices and systems for prototyping.

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IC-PIX28: Pixel Detectors Read-Out in Bulk-CMOS 28nm

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ICPIX28 is the first 28nm bulk-CMOS readout frontend for High Energy Physics pixel detectors. It performs the conversion of the input charge into a voltage signal, hence detect the charge arrival time and amount of charge information through Time-over-Threshold signal. The front-end is composed by the cascade of a Charge Sensitive Preamplifier and a low-power switched-capacitor logic-inverter-based comparator. A single channel area occupancy is 0.07mm². It operates at 0.9V supply voltage and consumes 4.3µW at 46dB@SNR. 10mV/fC sensitivity at 0.05fC Equivalent Noise Charge demonstrates design efficiency.

Summary:

The necessity to improve the Large Hadron Collider performance is the basis of High Luminosity Large Hadron Collider (HL-LHC) project at the CERN. The main goal is to rise the number of proton-proton collisions that occur in a given amount of time through a 10 times higher luminosity. Increasing the potential data rate, the researchers can detect more rare processes and discover new particles after 2025. The upgrade requires challenging changes in the High Energy Physics experiments and in the electronic readout front-end. Advanced scaled-down electronic with nmetric CMOS technologies development, i.e. bulk CMOS 28nm, is possible and includes Silicon Pixel Detectors (SPDs). SPDs play a key role in both ATLAS and CMS experiments and a careful design is necessary. Typical requirements for this circuit topology are radiation hardness (up to 1Grad), miniaturization (to increase spatial resolution), fast time response (within 20ns), low power consumption (due to huge number of the pixels) and very low Equivalent Noise Charge.

In this scenario, the first read-out front-end for pixels detectors (with 100fF parasitic capacitance) in 28nm bulk-CMOS technology has been developed. Technology choice is imposed by higher radiation hardness and forces analog designers to manage 0.9V supply voltage operation at higher standard process MOS transistors threshold voltage (about 0.5V in nominal conditions), leading to difficult operating point stability. Moreover, large SNR is challenging, since at lower supply voltage, the dynamic range also decreases.

The proposed pixel detector front-end is composed by a Charge Sensitive Preamplifier (CSPreamp, a common source topology with Krummenacher feedback), and a Comparator. Krummenacher feedback fixes the operating point at the input and the output of the CSPreamp helping to automatically compensate the detector leakage current. The Comparator based on switched-capacitor logic-inverter topology allows to save power and provides arrival time and amount of charge information. The IC-PIX28 has been extensively tested in time domain, in terms of operating point and time response vs. input charge. With a detector capacitance of 100fF and an input charge in the range 5fC–14fC, the voltage peak at CSPreamp output linearly grows from 14 mV to 109mV. IC-PIX28 performs 10mV/fC of sensitivity and 46dB of SNR with 0.05fC of ENC. It is enable to manage the signal with almost constant time delay around 17ns and 180ns Time-over-Threshold range. Most advanced 28nm Time-To-Digital Converters (TDC) use about 50ps as minimum time resolution, while old TDCs, actually mounted at CERN have about 10 times higher minimum time resolution (i.e. 500ps). Hence, feeding the IC-PIX28 with the TDC, the equivalent conversion bits ranges from 8.5bits (old TDCs) up to 12bits (advanced 28nm TDC), demonstrating this way the high charge quantization resolution achievable with this front-end. With 0.9V of supply voltage and 0.5V transistor threshold voltage, the power consumption of the overall chain is 4.2µW. The measurements demonstrate the high performance charge sensing for pixel detectors.
KAPTURE-2 – A picosecond sampling system for individual THz pulses with high repetition rate

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Coherent synchrotron radiation requires DAQ systems with picosecond resolution. The Karlsruhe Pulse Taking Ultra-fast Readout Electronics (KAPTURE) is a novel system for a continuous investigation of THz synchrotron radiation. It is capable to sample single THz pulses with sampling times down to 3 ps. To improve performance and flexibility a second version of KAPTURE has been developed. The new system reduces the sampling time to a picosecond and operates with pulse rates of up to 3.6 GHz. The design of KAPTURE - 2 and the first measurements will be presented.

Summary:

Coherent Synchrotron Radiation (CSR) generated by short electron bunches is provided by ANKA and other light sources. Electron bunches at ANKA can be filled in up to 184 buckets with 2 ns between two adjacent bunches corresponding to the RF system frequency of 500 MHz. To detect and study the THz CSR emission over multiple revolutions a detector system based on thin YBa2Cu3O7-δ (YBCO) superconductor film detectors is used. The intrinsic response time of YBCO thin films of only a few picoseconds allows one to resolve the signal of individual bunches even within a multi-bunch regime. To continuously acquire ultra-short pulses, the Karlsruhe Pulse Taking Ultra-fast Readout Electronics (KAPTURE) was developed. KAPTURE is based on a direct sampling pulse method operating with a minimum sampling time of 3 ps and a jitter of less than 1.7 ps. To satisfy the ever increasing demands an updated system, called “KAPTURE-2”, has been developed. KAPTURE-2 is able to sample each pulse with 4 to 8 sampling points with a resolution of down to 1 ps and accepts flexible pulse repetition rates in a range from 0.2 to 3.6 GHz. Low noise combined with wide dynamic range and bandwidth enables the sampling of signals generated by various GHz and THz detectors. To manage the high raw data rate of about 120 Gb/s, KAPTURE-2 is connected to a heterogeneous FPGA/GPU-based readout system. FPGA and GPU are connected by a new Direct Memory Access (DMA) concept, called “GPUDirect”. The readout card is equipped with a Xilinx Virtex-7 FPGA and is connected to the GPU by a PCIe Gen 3 x16 data link, capable of a net throughput of up to 13 GB/s. In a traditional DMA architecture, data is first transferred to the main system memory and afterwards moved to the GPUs for processing. Here, the main memory is involved in several read/write operations, depending on the specific implementation. The total throughput and latency of the system is therefore limited by the memory bandwidth. Using the “GPUDirect” communication, the DMA engine has a direct access to the GPU memory. Therefore latency and hardware requirements of the system are drastically reduced. The GPU real-time architecture is used for pulse reconstruction based on the 4 to 8 sampling points. It results in the peak amplitude of each pulse and the time between two consecutive pulses/buckets with a picosecond time resolution. The GPU node performs also an on-line Fast Fourier Transform (FFT) for the frequency analysis of the CSR fluctuations. Multi-turn measurements of CSR have turned out to be an indispensable tool for storage ring diagnostics in short bunch operation. With KAPTURE - 2 it is possible to study THz behavior with an unprecedented temporal resolution and to resolve bunch-to-bunch interactions.
HEPS-BPIX is a dedicated hybrid pixel detector for the High Energy Photon Source in China. It works in the single photon counting mode, and each pixel chip contains an array of 104 × 72 pixels with a pixel size of 150µm × 150µm. Based on the successful design of the chip, the detector module was assembled by bump bonding with 24 pixel chips and a single large sensor. Six detector modules were then mounted as the final prototype system, covering an area of 9cm × 10cm with 360k pixels. Experiment and calibration results are discussed in this paper.

**Summary:**

The High Energy Photon Source (HEPS) will be the next generation of light source in China and the Test Facility is now being built. However, the existing pixel detector cannot fulfill the requirement in applications like diffraction experiments and protein crystallography, especially for frame rate and dead-time performance. HEPS-BPIX is a dedicated hybrid pixel detector for HEPS. It works in the single photon counting mode with a 300um-thick P-in-N sensor bump bonded with Indium.

With 3 years effort, the readout chip was successful designed and manufactured by a full mask tapeout. The chip contains an array of 104 × 72 pixels with a pixel size of 150µm × 150µm. Each pixel runs a 20-bit counter and can be readout at 1.2kHz frame rate with negligible deadtime. After the full test with the single chip module, i.e., one readout chip bump bonded with a sensor containing a pixel array with the same size, the detector module was finally assembled with 24 chips. Each detector module consists of 8 readout chips and a single large sensor, bump bonded with Indium. The detector module covers a sensitive area of 4.5cm × 3.6cm with 60k pixels. Wire bonding are performed at the two long edges to PCB while at the short edges, two adjacent modules are closely butted with their guardrings for the least dead area. Signals and power supplies are provided through flexible PCBs to the backend readout board at the backside, so that two adjacent long edges can also be closely butted. This hybrid PCB was carefully designed, not only to achieve the least dead area, but also to achieve low noise, good head conductivity and assembly friendly.

The prototype system was grouped by six modules with 360k pixels in total, covering an area of 9cm × 10cm. The data acquisition for the prototype is served with a single server, and each detector module communicates with the server through two 10Gb-Ethernet connections, achieving a full data rate of 862MB/s. A typical power dissipation of 2.2W for all the readout chips in each module, or 15W for all the front end part of the prototype system, is conducted through PCB to the Aluminum supporting. The full detector system consumes 60W at the full speed and can run without water cooling, making it easily portable. A typical x-ray diffraction experiment at the synchrotron light was done with a standard powder sample CeO2. Normalized intensity of all the measure peaks together with their positions is given. Compared with a standard device, it shows that all the measured peak positions are closely agreed with each other. It also agrees with the theoretical predictions given the known lattice of the sample. The prototype system shows less FWHM of the peak due to the smaller pixel size, and good peak-to-valley ratios. X-ray images taken at X-ray tubes with flatfield correction and preliminary results of detector calibrations are also discussed.

**Development of ATLAS Liquid Argon Calorimeter Readout Electronics for the HL-LHC**

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The high-luminosity phase of the Large Hadron Collider will provide 5-7 times greater luminosities than assumed in the original detector design. An improved trigger system requires an upgrade of the readout electronics of the ATLAS Liquid Argon Calorimeter. Concepts for the future readout of the 182,500 calorimeter channels at 40-80 MHz and 16bit dynamic range, and the development of low-noise, low-power and high-bandwidth electronic components will be presentet, including ASIC developments towards radiation-tolerant low-noise pre-amplifiers, up to 14bit ADCs and low-power optical links with up to 10GB/s.
Summary:

The LHC high-luminosity upgrade in 2024-2026 requires the associated detectors to operate at luminosities of up to $7 \times 10^{34} \text{cm}^{-2} \text{s}^{-1}$ corresponding to a signal pile-up from up to 200 events per proton bunch-crossing, with the goal of accumulating a total integrated luminosity of $3000 \text{fb}^{-1}$. To be able to retain interesting physics events even at rather low transverse energy scales, increased trigger rates are foreseen for the ATLAS detector. At the hardware selection stage acceptance rates of 1MHz are planned, combined with longer latencies up to 60/μs in order to read out the necessary data from all detector channels. Under these conditions, the current readout of the ATLAS Liquid Argon (LAr) Calorimeters does not provide sufficient buffering and bandwidth capabilities. Furthermore, the expected total radiation doses of $10^{13} \text{neq/cm}^2$ (NIEL) and 0.3kGy (TID) are beyond the qualification range of the current front-end electronics.

For these reasons a replacement of the LAr front-end and back-end readout system is foreseen for all 182,500 readout channels, with the exception of the cold pre-amplifier and summing devices of the hadronic LAr Calorimeter. The new low-power electronics must be able to capture the triangular detector pulses of about 400-600ns length with signal currents up to 10mA and a dynamic range of 16bit. In 180nm SiGe technology (IBM 7WL) and choosing unipolar shaping, two gain stages can cover the desired dynamic range. An ADC matching this pre-amplifier and shaper will need to provide 14bit digitization range. Such a design is shown to meet the noise requirements and achieve an integral non-linearity below 0.1%. Moreover, in simulations of the complete readout chain using the unipolar shaping approach signal pile-up is introducing a controllable baseline shift, and an additional digital CR shaping stage does not introduce a degradation of the energy resolution.

Alternatively, a development of pre-amplifier and shaper as well as SAR ADCs is performed in 65nm CMOS technology. Due to the lower voltage range, 2-gain and 4-gain designs of the analog part are studied with programmable peaking time to optimize the noise level in presence of signal pile-up. The 65nm ADC uses a SAR architecture and an active SEE detection mechanism by feeding the signals into two ADCs in parallel and comparing their output. In this way, the signal-to-noise ration can be further improved in presence of radiation. Results for an 80MHz 12bit prototype design show ENOB values above 10.8bits after 10kGy irradiation, and similar performance is reached for a 14bit layout.

Furthermore, results for a newly designed VCSEL array driver show that the required 10Gb/s transfer rate at 20-35mW per channel is achieved, suitable for integration into a low-power optical link package.

Results from performance-simulation of the calorimeter readout system for the different options and results from design studies and first tests of the ASIC components will be presented.

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Development of a monolithic pixel detector with SOI technology for ILC vertex detector

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We have been developing a monolithic type pixel detector for the ILC vertex detector with 0.2 um fully depleted SOI CMOS process. We are aiming to achieve 3 um of a single point resolution that is required for the ILC with a 20 um x 20 um pixel. Beam test result of the first prototype sensor that an amplifier and an analog memory are implemented in each pixel is presented. Design of second prototype with the time stamp function to recognize the bunch crossing information is also reported.
Summary:

The ILC needs a vertex detector that has fine space-time resolution to distinguish decay of heavy flavor quark for precise measurement of the Higgs boson. We have been developing a monolithic type pixel detector with silicon-on-insulator technology (SOIPIX) which is fabricated using a 0.2 um FD-SOI CMOS process. SOIPIX has a potential of decrease in pixel size and sense node capacitance compared to a hybrid type pixel detector since there is no mechanical bump bonding. Smaller parasitic capacitance than bulk CMOS process perform higher speed and lower noise. SOI CMOS are isolated from bulk silicon, so that it is less sensitive to single event effects. Additionally, SOI CMOS has an advantage in an integration of circuit because there is no well structure for MOSFET. Therefore, SOIPIX enables us to implement a complex circuit in a small size pixel and fulfill the requirements of spatial and timing resolution for the ILC.

We are designing and evaluating prototype pixel sensor for the ILC, which is named as SOFIST (SOI sensor for Fine measurement of Space and Time) to optimize pixel size and signal readout circuit. Currently we are aiming the pixel size less than 25 um. In May 2016, SOFIST ver.2 was submitted. We integrated an amplifier, comparator, shift register, analog memory and time stamp in each pixel. Signal of charges is kept to the analog memory if it exceeds a threshold of the comparator. To achieve requirement of a single point resolution of 3 um, we will employ that the charges are spread among multi pixels. At the ILC, bunch crossing occurs every 366 ns in 1-msec-long bunch trains with an interval 200 ms. To identify a collision bunch, each pixel records the charge and time stamp of a hit. Column ADC on the chip converts the charge and timing information. These digital data have to be send to backend circuit before next beam train injection. Zero-suppression logic extracts hit pixels and reduces the data to transfer.

Our first prototype sensor, SOFIST ver.1, has the amplifier and two analog memories for storing signal charges up to two hits in a 20 x 20 um^2 pixel, and an 8-bit column ADC on the chip. We plan to test SOFIST ver.1 by using an 840 MeV electron beam in June 2016. Detection of a minimum ionizing particle and tracking of charged particle with multiple sensors are purposes. Second prototype sensor, SOFIST ver.2, will be submitted to a multi project wafer run in May 2016. The pixel size of SOFIST ver.2 is 25 x 25 um^2. Necessary functions; the amplifier, comparator, shift register, analog memory, time stamp, column ADC and Zero-suppression logic, are implemented in the pixel chip. However, pixels for the analog memories and the time stamps are separated to evaluate the functions individually. In this presentation, recent progress of SOFIST ver.1 and 2 will be reported.

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A flexible FPGA based QDC and TDC for the HADES and the CBM calorimeters

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In this presentation the read-out scheme will be introduced. Laboratory measurements have been done to characterize and optimize the analog electronic scheme and the FPGA VHDL code. The adaption process to different detector pulse shapes will be also shown. The results obtained at beam tests at the MAMI accelerator in Mainz and the SPS at CERN will be presented.

Summary:

A Charge-to-Digital-Converter (QDC) and Time-to-Digital-Converter (TDC) based on a commercial FPGA (Field Programmable Gate Array) was developed to read out PMT signals of the planned HADES electromagnetic calorimeter (ECAL) at GSI Helmholtzzentrum für Schwerionenforschung GmbH (Darmstadt). The main idea is to convert the charge measurement of a detector signal into a time measurement, where the charge is encoded in the width of a digital pulse. The PaDiWa-AMPS front-end board for the TRB3 (General Purpose Trigger and Readout Board - version 3) which implements this conversion method was developed. The already well established TRB3 platform will provide the needed precise time measurements and serves as a data acquisition system.
In laboratory measurements a first prototype board was characterized and optimized in order to improve the charge and time precision, dynamic range and rate capability.

During a beam time with secondary photons at the MAMI accelerator in Mainz the read-out concept was successfully used to read-out PMTs of HADES ECAL modules. It showed excellent precision in providing charge and time measurement compared to much more complex read-out systems. During the HADES pion beam experiment the flexibility of the front-end was shown. The front-end electronics could be easily adjusted to small 0.8 inch PMTs.

The read-out concept is also foreseen to be used for the hadron calorimeter in the CBM experiment at the planned FAIR facility (Darmstadt). The adaption process is currently ongoing and tests of the concept will be performed at NA61/SHINE (SPS, CERN) which uses a similar hadron calorimeter.

POSTER - Board: F7 / 151

**Development of Clock-Data Recovery circuit, Serializer and CML Driver in 65nm CMOS for HL-LHC pixel readout chip**

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ATLAS and CMS are presently collaborating on a design of a pixel readout chip in 65nm CMOS technology to be used for the LHC Phase-II upgrade. This work presents a prototype containing part of the I/O interface of this readout chip. The clock-data recovery circuit recovers clock from 160 Mbps incoming data and produces 1.6 GHz clock to be used by serializer. Double data rate serializer combines 20 data streams into 3.2Gbps stream, which is send off-chip by a Current Mode Logic driver. Prototype description together with first measurement results will be presented.

**Summary:**

The LHC Phase-II upgrade will lead to a significant increase in luminosity, which in turn will bring new challenges for the operation of the inner tracking detectors. In order to cope with the envisioned extreme rates (hit rate of $2 \text{GHz/cm}^2$, trigger rate of 1-2MHz) and radiation levels (500Mrad – 1Grad) ATLAS and CMS experiments are currently jointly developing a pixel readout chip to be used in the inner most layers of detectors. The chosen technology is TSMC 65nm CMOS. This work presents three building blocks designed for the input/output interface of the mentioned readout chip: a clock-data recovery (CDR) circuit, a serializer (SER) and a cable driver.

The CDR was designed to work with input data rate of 160Mbps. In addition to recovering clock from input data the CDR produces a 640MHz/800MHz/1.28 GHz/1.6GHz (depending on chosen configuration) fast clock signal that is used by serializer. This signal is an output of a Voltage Controlled Oscillator (VCO), which is based on differential buffers with cross-coupled loads. The gain of VCO can be adjusted to an appropriate value for any technology corner. The fast clock is divided down (by factor of 8 or 10) and fed to a Phase Detector (PD). Both the signal divider and PD were implemented in few flavours, differing by circuit architecture and SEU protection scheme. Output of PD is sent to a charge pump whose output is connected to the VCO input through second order passive low pass filer, thus completing the circuit loop. According to simulation a 550fs (rms) phase jitter of VCO output clock is achieved with a power consumption of 3.6mW (for default CDR configuration).

Double data rate serializer used in this prototype produces a 3.2 Gbps data stream out of 20 input streams. Circuit is based on two chains of D Flip-Flops and multiplexers working in parallel. Four flavours were implemented, differing by the SEU protection method. All of them were build out of modified standard cells, which provide improved radiation hardness. Power consumption varies from 1.4mW to 4mW, depending on a flavour.

Output driver is based on Current Mode Logic (CML) architecture. It provides programmable pre-emphasis (3-tap, with adjustable tap weight and width) and according to simulation is capable of transmitting 4Gbps signal across 2m of ultra-low mass cable.

Presented prototype was designed in a way that allows characterization of full chain (CDR-SER-CML)
and each block separately. In this work the circuit will be presented in detail followed by simulation and measurement results.

POSTER - Board: F4 / 13

6-Bit Low Power Area Efficient SAR ADC for CBM MUCH ASIC

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The paper describes a SAR ADC, elaborated for digitization the shaper signal of the read-out CBM MUCH ASIC. The MUCH ASIC was designed and prototyped by means of the 0.18 um CMOS process of UMC (Taiwan). Each channel of ASIC consist of a CSA, fast and slow shapers, discriminator, ADC and a digital peak detector. ADC has a power consumption of 1.5 mW at 50 Ms/s and an occupied area of 0.0162 mm$^2$ for using an ADC in a multichannel structure.

Summary:

In nowadays multichannel read-out ASICs for physical experiments there is observed a trend to digitization the signal from detector at an early stage and signal processing in digital domain (digital peak detector, digital filtration, base-line correction etc.). It becomes necessary to use the ADC in each channel of read-out ASIC and quite rigid specifications are set to ADCs in terms of power consumption and occupied area.

The ADC was designed for a prototype read-out ASIC for the GEM detectors muon chambers of the CBM experiment. Each channel of the ASIC consists of a CSA, followed by two chains: fast and slow. The slow chain is needed to determine the detector signal amplitude and consists of a shaper, discriminator, ADC and digital peak detector. Fast chain consists of a shaper and discriminator. It determines timestamp. When the discriminator in fast chain generates a signal, the digital logic sends the sequence “start of conversion” pulses to ADC. Digital peak detector tracks the ADC code and determines the maximum amplitude of shaper response.

ADC has been built by the conventional SAR architecture. It consists of: capacitor matrix, successive approximation register, comparator and analog switches. For reduction of occupancy area, the capacitor matrix has two stages. In result the matrix has an overall capacitance of 0.92 pF (the least capacitor of matrix equals 40 fF) instead of 1.56 pF for one stage matrix. That reduces the area of the ADC by one and a half times.

The ADC has a single-ended input and asynchronous internal clock, being equal to 500 MHz. The clock is generated by a built in ring oscillator. That allows to achieve 40 Ms/s rate of ADC.

The ADC layout occupied an area of 0.0162 mm$^2$. The layout height of 90 um is selected to fit the analog chain geometry of the multichannel ASIC structure.

The ASIC has been manufactured by the 180 nm CMOS UMC MMRF process via Europractice. For experimental study the samples were package to CPGA 120 and a test board with the corresponding socket was developed. The first experimental results have been received for the ASIC at lab conditions. They confirmed the functionality of the ADC. The experimental result has shown INL=0.45 LSB, DNL=0.7 LSB for static requirements and ENOB=5.3, SFDR=49.76 dB at 1 Ms/s. Power consumption is equal to 1.5 mW.
Design of a Depleted Monolithic CMOS Sensor in a 150 nm CMOS Technology for the ATLAS Inner Tracker Upgrade

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CMOS pixel sensors with notable depletion have been demonstrated to be feasible candidates for the ATLAS Inner Tracker (ITk) upgrade, replacing the current passive sensors. A further step to exploit the potential of CMOS sensors is to investigate the suitability of equipping the outer layers of the ATLAS ITk upgrade with fully monolithic CMOS sensors. In this work, a monolithic CMOS pixel sensor, named MONOPIX-01, has been designed in the LFoundry 150 nm CMOS technology. The submission is scheduled in May 2016. Design and simulation results will be presented.

Summary:

Standard CMOS pixel sensors have proven to be high precision devices in high energy particle physics experiments, thanks to their fine granularity and low material. Moreover, the use of commercial technologies makes them very suitable for large area trackers due to their low cost. However, existing CMOS detectors in commission or under construction still suffer from limited speed and radiation hardness, excluding them from being used in the extreme radiation environment like ATLAS. A recent trend to exploit the high-voltage/high-resistivity CMOS technologies to increase the depletion of the CMOS sensors have eventually made them feasible candidates for the ATLAS upgrade.

Aimed at qualifying available CMOS technologies to build high performance, cost efficient CMOS detectors for the ATLAS ITk upgrade, an R&D collaboration called “CMOS demonstrator” was started. Various depleted CMOS sensors have been developed in different technologies. Encouraging measurement results have been obtained, demonstrating the feasibility of CMOS sensors being candidates for the ATLAS ITk upgrade. However, these sensors are either passive or active ones with first stage(s) of front-end electronics integrated on the sensor substrate. The data readout and processing rely on a readout chip, bump bonded or glued to the sensor. A more ambitious step to explore the potential of depleted CMOS sensors will be the development of fully monolithic sensors, which may be suitable for the outer layers of the ATLAS ITk upgrade.

This work focuses on the design of a monolithic sensor in a 150 nm CMOS technology, namely MONOPIX-01. This technology features quadruple wells, and a high resistivity (> 2 k\(\Omega\) cm) P-type substrate is used for implementing the sensor. The charge collection node is formed by a deep N-well, which is also used to host the in-pixel readout electronics. A deep P-type layer is used to isolate the N-well from the deep N-well, so that full CMOS capability is achievable in the pixel. The design contains an array of 142 \(\times\) 36 pixels, with two pixel variants featuring different pre-amplifying stages. The pixel size is 250 \(\mu\)m \(\times\) 50 \(\mu\)m. The readout of the pixel array employs the “column drain” architecture. In each pixel, the charge signal is amplified by a amplifier, and then compared to a programmable threshold by a discriminator. Two 8-bit gray-coded time stamps, corresponding to the rising leading edge and trailing edge of the discriminator output, are stored in two in-pixel RAM cells. A readout controller initiates the priority scan after receiving a hit flag from the pixel array, so that the hit pixels are read out successively. The data is serialized and sent out by a LVDS driver with a bit rate of 160 Mbps. For design simplicity, the readout controller will be implemented off chip by the FPGA. The submission is scheduled in May 2016.

Short overview of existing development in the same technology, as well as the design and simulation results of MONOPIX-01 will be presented.
Characterization of ALICE SAMPA ASIC Using Prototype GEM Detector for LHC Run3 and Beyond

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Summary:

The heavy-ion beam of CERN’s LHC is expected to be colliding at 50 kHz (present rate few kHz) during Run3 onwards of the ALICE experiment planned to start in 2020. Due to these new high collision rates, the Multi-Wire Proportional Chambers of the present ALICE TPC will be replaced by readout chambers featuring Gas Electron Multiplier (GEM) foils. A continuous readout system will replace the existing triggered readout.

In the upgraded TPC readout, the current signals from the GEM detector pads will be readout by Front-End Cards (FECs) via custom-made SAMPA ASICs. The SAMPA contains a charge-sensitive preamplifier, a shaper, a 10 bit 10 MHz digitizer and a digital filter, processing and data compression chain. In the FECs, the output of the SAMPA will be multiplexed and transmitted using GigaBit Transceivers (GBTx) via optical links to a Common Readout Unit (CRU). The CRU is an interface to the on-line computer farm, trigger and detector control system. The upgraded readout system will utilize 3400 FECs, each containing 5 SAMPA ASICs (32 channels each), and in total of about 500k channels. The data rate from SAMPA to CRU via GBTx will be 1 TBytes/s.

This presentation will be focused on the characterization of SAMPA ASICs done using waveform generator and GEM detector prototype. The tests performed using waveform generator showed an excellent pulse shape stability and gain linearity at various input charges (5 fC to 110 fC). The noise performance of SAMPA is also quite good (540 ENC @ 12 pF). The average cross-talk between the readout channels varied from 0.3 to 0.8% and the average power consumption is about 8 mW.

The GEM detector prototype consists of a stack of three 10 x10 mm² GEM foils with standard pitch. To initiate the processes of excitation and ionization inside the detector, Am-241, Sr-90, and Fe-55 radioactive sources were used. The Am-241 alpha spectrum was recorded by operating GEM chamber at gain less than 1000 for different readout pad sizes of the detector in ArCO2 (90%+10%) and NeCO2N2 (90%+10%+5%) gas mixture. Similarly, a Sr-90 electron (2.28 MeV) or Minimum-Ionizing-Particle (MIP) and a soft-photon energy (5.9 keV) spectrum is recorded at the detector gain of 2000. The measured energy resolution for the Fe55 photon is 9.7%. The results obtained from these tests are close to the ALICE TPC requirement and it helped to improve the design of second/final SAMPA ASIC.
CATIROC is an upgraded version of PARISROC2 designed to read huge photodetection areas for neutrinos experiments. This "System-on-Chip" is a very innovative concept as it sends out only relevant data by network to the central data storage turning the detector into a smart one. The ASIC integrates a self-triggering mode down to 50 fC which provides time measurement better than 1 ns and charge measurement up to 100 pC. Data are converted internally over 10 bits @160 MHz and read-out at 80 MHz.

The chip was produced in 2015; architecture and testbench measurements will be presented.

Summary:

CATIROC is a successor of PARISROC2 with several improved features concerning the hit rate and the time measurement. PARISROC2 was designed in 2009 to readout huge photodetection areas of next generation neutrino experiments using water Cerenkov detectors, as continuation of the Super-Kamiokande family. Replacing large and onerous photodetectors by arrays of smaller ones is important to make the next generation of such detectors affordable. This relies on the integration of the front-end electronics on the array itself to turn it into a "smart sensor".

CATIROC is designed in AMS 0.35µm SiGe technology and keeps the same architecture as PARISROC2: it integrates 16 independent and self-triggered channels to provide charge and time measurements which are managed by a common digital part.

The main chip specifications are:
- An adjustable gain channel by channel
- Auto-trigger on 1/3 of photoelectron (p.e.) (50 fC at PM gain of 106)
- Charge measurement efficient for 1 p.e. and up to 600 p.e. (100 pC)
- 16 shaper outputs (enabling the use of an external ADC)
- 16 trigger outputs
- Time tagging better than 1 ns
- Internal ADC
- Serial data readout

The charge channel is made of a high and low gain voltage preamplifier followed by a variable slow shaper for small and large signals to ensure a good charge precision (~ 30 fC). The two shaper signals are then stored in two analog memories (each one with a depth of two) working in a "ping-pong" mode in order to minimize the dead time during digitization: while a channel is digitized, the shaper output is sent to the second capacitor.

The time channel is made by the high gain preamplifier followed by a fast shaper (15 ns) and a discriminator.

Thanks to a Time to Amplitude Converter (TAC), the signal is saved into an analog memory, in parallel with the charge, and is converted into digital data by the ADC. Significant modifications compared to Pariscroc2 concern this timing branch. A new time measurement architecture built around a "fine time" and a "coarse time" has been implemented in CATIROC. The "coarse time" has been sped up by a factor of 4 with a 26-bit Gray Counter working at 40MHz. Two TAC ramps are sampled at the same time and an internal module tags the valid one: only the good time value is then converted.

Charge and time are then encoded by a 10-bit ADC at 160MHz (4 times faster compared to PARISROC2). The data are sent-out in a data-driven way at 80 MHz (8 times compared to PARISROC2) on two lines (each for 8 channels) which speeds up the data rate by a factor of 2.

A digital part manages all the acquisition, the conversion and the readout.

Several international experiments are interested by the ASIC such as the two Chinese projects LHAASO and JUNO, and the European project WA105.

CATIROC was received in September 2016. The architecture and the measurements will be detailed in the presentation.
Characterization of SLVS Driver and Receiver in a 65 nm CMOS Technology for High Energy Physics Applications

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This work presents the design and characterization of a SLVS transmitter/receiver pair, to be used for I/O links in High Energy Physics applications.

The prototype chip was designed and fabricated in the framework of the CHIPIX65 project and was completely characterized in the first quarter of 2016. The chip has been also irradiated with X-rays in order to evaluate the effect of the ionizing radiation on the signal integrity.

The full characterization of the driver and receiver will be discussed in the conference paper.

Summary:

A transmitter/receiver pair designed for a possible integration in the RD53A prototype, and conform to the SLVS protocol, was designed in a 65 nm CMOS technology. The proposed link, that can be operated up to 1.2 Gbps, will be used in a harsh radiation environment, so the design is based on thin gate oxide transistors, using a supply voltage of 1.2 V. The SLVS standard describes a differential current-steering protocol with a voltage swing of ±200 mV on a 100Ω termination resistance and a common mode of 200 mV. The driver architecture is based on a Bridged-Switch Current Source (BSCS) scheme. The 2 mA biasing current is switched through a 100Ω termination resistance, placed at the receiver input, according to the input data stream. The output current of the transmitter can be trimmed, by means of three configuration bits, in a range from 500 µA to 2.5 mA. In order to achieve insensitivity to PVT variations, a simple low power common-mode feedback has also been included. The common mode voltage is sensed by two resistors, which are connected to the output nodes and compared with a reference voltage generated by a resistor voltage divider. The CMFB amplifier is based on a two stage Miller OTA. The receiver is based on three different stages: the first one is a fully differential amplifier with a cross-coupled load, rail-to-rail input stage, and with a bandwidth close to 1.2 GHz; the second stage is a differential-to-single ended amplifier with a full swing CMOS output voltage and the last one is a chain of three inverter. The receiver input is AC coupled for a possible use with serial powering. The common mode voltage of the signal at the input of the receiver is restored by a resistor voltage divider. The CMFB amplifier is based on a two stage Miller OTA. The receiver is based on three different stages: the first one is a fully differential amplifier with a cross-coupled load, rail-to-rail input stage, and with a bandwidth close to 1.2 GHz; the second stage is a differential-to-single ended amplifier with a full swing CMOS output voltage and the last one is a chain of three inverter. The receiver input is AC coupled for a possible use with serial powering. The common mode voltage of the signal at the input of the receiver is restored by a resistor voltage divider. The chip was submitted in May 2015 and it was completely characterized during the first quarter of 2016. During the characterization activity, the input of the driver was stimulated with a CMOS Pseudo-Random-Bit Signal (PRBS). The signal integrity of the driver was evaluated by measuring the eye diagram at the termination resistance. The chip has also been irradiated, up to 550Mrad, with the X-rays machine present at CERN in order to evaluate the effect of the ionizing radiation on the signal integrity. The conference paper will report on the full experimental characterization of the SLVS transmitter and receiver.

POSTER - Board: G3 / 58

Development of Radiation-Hard Bandgap Reference Circuit in CMOS 130 nm Technology

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In particle physics experiments a stable sub-1-V reference voltage is needed in spite of harsh ionizing radiation conditions. After such radiation load the bandgap using standard p-n junction of bipolar transistor does not work properly. This is why several sub-1V voltage references based on DT-MOS (dynamic threshold MOS) and ELTMOS (enclosed layout transistor MOS), using CMOS 130nm process were proposed. We present and compare post-layout simulations and the preliminary measurements of the developed devices, which show correct operation (~1mV bandgap stability, linear PTAT) in temperature range -20 to 100 degree.

Summary:

A voltage reference circuit is a device that generates an exact output voltage which in theory does not depend on the operating voltage, load current, temperature or the passage of time. It is commonly used in most of all analog devices and mix-mode signal systems. In particle physics experiments a stable reference voltage is needed in spite of harsh ionizing radiation conditions, i.e. doses exceeding 100 Mrads and fluences above 1e15 n/cm². After such radiation load the bandgap using standard p-n junction or bipolar transistor does not work properly. This is why instead of using bipolar transistors, the DTMOS (dynamic threshold transistors) or ELTMOS (enclosed layout transistors) were proposed.

Five prototype of sub-1V radiation-hard Bandgap references voltage circuit has been developed. Two of them are based on standard Banba architecture and three others have also current-mode architecture, but their design additionally allows to add temperature sensor. Special enclosed layout (ELT) and dynamic threshold DTMOS transistors were used to reduce the TID (total ionization dose) effect like threshold shift or leakage current. Designed devices are expected to give stable (less than 1mV per 120 degree) sub-1-V reference equal to 0.6 V.

Unfortunately measurements of first prototypes showed that the transistors were not properly modeled and simulated by Virtuoso - a tool for IC design. This is mainly due to the originality of used enclosed layout transistors, which layout models are not available by default and need to be drawn manually. To overcome this problems there have been performed calculations based on these measurements to determine what values should be used during designing next prototypes. With these calculations we were able to get to know the real values of currents that flow through the transistors and their exact characteristics, what enable us to design the secondary prototypes, which result are presented. These new bangaps were also equipped in calibration capability - resistance switching which allows to control the stability of bandgaps and change its referenced voltage values.

The first preliminary measurements of second prototypes indicate that this time bandgaps has been designed correctly, achieving very high stability over a wide temperature range. Most of developed prototypes obtain temperature stability under 1 mV. Only in two cases this parameter in about 1.5 mV. Designed temperature sensor exhibit linear PTAT, and around 2.2 mV per degree in all rage from -20C to 100C . Power consumption depending on circuit varies between 45W and 95W and the PSRR values does not fall below 29.5 dB at all bandgaps. Measurements show that bendagps meet their expectations and can be successfully used.

POSTER - Board: D4 / 141

**HVCMOS Sensors for the High Luminosity Upgrade of ATLAS Experiment: The Second Generation of Prototypes and their Electronic Blocks**

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HVCMOS sensors and capacitive coupled pixel detectors (CCPD) are seen as an option to the standard sensor technologies such as hybrid- or strip-detectors for several particle physics experiments, among others ATLAS. The latest important achievement of this development is the production of first reticle size HVCMOS sensor – H35DEMO - that can be readout either as a monolithic detector,
with the readout electronics on the chip, or attached to an external readout chip in form of a CCPD. H35DEMO is currently being tested and the first results are very good.

**Summary:**

Our group is working on the development of HVCMOS sensors and capacitive coupled pixel detectors (CCPD) since 2006. These sensors are seen as an option to the standard sensor technologies such as hybrid- or strip-detectors for several particle physics experiments, among others ATLAS. The latest important achievement of this development is the production of first reticle size HVCMOS sensor – H35DEMO - that can be readout either as a monolithic detector, with the readout electronics on the chip, or attached to an external readout chip in form of a CCPD. H35DEMO is currently being tested and the first results are very good.

In parallel with the demonstration that a HVCMOS sensor fulfils the ATLAS specifications, we are working on several more advanced large area prototypes with nearly complete electronics, i.e. with the system architecture that could be used in the experiment. The submission of the corresponding designs is planned for July 2016. Some of the possible scenarios for the application of HVCMOS sensors in ATLAS are: The use of monolithic sensors in the outer pixel layers. The use of capacitively- or DC-coupled pixel detectors based on a HVCMOS sensor and a new readout chip in the inner pixel layer. The goal is a pixel size of 25um x 25um or less. The use of HVCMOS segmented-strip sensors in the outer tracker regions. Finally, we are considering HVCMOS layers that could generate track trigger. For all of these application cases, dedicated electronic blocks have been developed in our group. For the monolithic sensors we have developed very small, content addressable memory cells that can be used to keep the particle-hit information for relatively long time > 25us and to detect the coincidence of the hit information with a trigger signal. For instance a cell designed in a 180nm process occupies an area of only about 8um x 80um and can store the information coming from four pixels. For the CCPD-sensors designed for the inner pixel layers, we have developed small HVCMOS pixels and the small readout blocks that can be used in the new readout chip. For the track trigger layers, we are designing high-rate and low-latency particle hit data readout blocks. This contribution will give the overview of different readout architectures and the design details of the most important building blocks.

**POSTER - Board: E8 / 166**

**LDQ10P: A Compact Low-Power 4x10 Gb/s VCSEL Driver Array IC**

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Low-power and high-data-rate laser array driver is an important on-detector component of the Versatile Link for the high-luminosity LHC experiments. We report the design and implementation of a low-power and radiation-tolerant 4x10 Gb/s VCSEL Driver array IC (LDQ10P). The entire four-channel VCSEL driver consumes 130 mW and occupies a silicon area of 1900 µm x 1700 µm. By integrating four driver channels into a single chip, LDQ10P can be directly wire-bonded to the VCSEL array and is a suitable candidate for the Versatile Link.

**Summary:**

Low-power, high-speed and radiation-tolerant Gigabit data links are needed for data transmission in High-Energy Physics (HEP) applications. Last year we reported and demonstrated a low-power 10 Gb/s single-channel laser driver IC (GBLD10P) implemented in 65 nm standard CMOS technology, with 40 mW power consumption at 10 Gb/s.

In this work, we present a 4x10 Gb/s low-power VCSEL driver array (LDQ10P) IC with compact chip size suitable to drive a VCSEL array. Each channel in the LDQ10P consists of a high-speed limiting amplifier
(LA) and an output driver with programmable pre-emphasis. To fit the design in a compact silicon area, the LA employs a two-stage differential amplifier but with only one peaking inductor (130 µm × 130 µm) shared between the two stages, boosting the driver speed without the area penalty that would be required by a conventional inductive-peaking LA. In the output driver stage, the feed-forward topology is adopted to further enhance the bandwidth. The feed-forward strength is carefully optimized trading-off between bandwidth and jitter. Moreover, to compensate for potentially slow tail speed of the laser devices and/or accommodate different packaging and load parasitics, an edge-dependent pre-emphasis is implemented in LDQ10P with three possible configurations, rising-edge pre-emphasis, falling-edge pre-emphasis and both-edge pre-emphasis. Compared to our published single-channel 10 Gb/s driver, the design is further optimized to obtain higher bandwidth and lower jitter. The total jitter is expected to be less than 15 ps with PRBS7 at BER of 10⁻¹².

The LDQ10P die size is 1900 µm × 1700 µm and the entire chip consumes 130 mW (including the I2C block) when setting four VCSELs with 4 mA modulation and 6 mA bias current. Two on-chip 7-bit DACs are used to program the modulation and bias currents with a current resolution of 0.16 mA and a range of 10 mA radiation-hard and single-event immune I2C digital circuit is designed to control the IC operation. The driver array has a pitch of 250 µm, compatible with that of the VCSEL array devices. These features allow the IC to be directly wire-bonded to a VCSEL array. To minimize the crosstalk between the channels, extensive simulations and layout optimization including carefully designed power mesh and decoupling capacitor network were conducted. The LDQ10P prototype chip design has been submitted for fabrication in March, 2016. The chip measurement will be carried out during the summer of 2016 and the measurement results will be presented at the TWEPP conference.

POSTER - Board: E2 / 81

Readout Electronics for Silicon Micro-Strip Sensors

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In the future ILC (International Large Detector), Silicon strip detectors will be used in the tracker to measure position and energy of the particles. A specific readout chip must be designed targeted to the accelerator operation and expected performance. A multichannel readout ASIC for Silicon microstrips in AMS 180nm technology has been fabricated. The main intended goals for this readout ASIC are low power, wide dynamic range, low noise and adaptability to different variety of silicon sensors. The details of the design to fulfil the requirements and the experimental results will be presented at the conference.

Summary:

Silicon micro-strips detectors are the baseline for the tracker region of the future International Linear Collider (ILC). Lately, variations of this type of sensors, like resistive micro-strips, Low Gain Avalanche
Detectors (LGAD) and inverse LGAD (iLGAD) [1], have been presented to be considered as the technology for the future tracker.

In this paper, an ASIC fabricated in 180 nm CMOS technology from AMS with the very front-end electronics used to readout silicon micro-strips is presented as well as its experimental results. The front-end has the typical architecture for Si-strip readout [2], i.e., preamplification stage with a Charge Sensitive Amplifier (CSA) followed by a CR-RC shaper. Both amplifiers are based on a folded cascade structure with a PMOS input transistor and the shaper only uses passive elements for the feedback stage. The CSA has programmable gain and a configurable input stage in order to adapt to the different strip flavours (resistive micro-strips, LGADs and iLGADs). The fabricated prototype is 0.865 mm x 0.965 mm and includes the biasing circuit for the CSA and the shaper, 4 analog channels (CSA+shaper) and programmable charge injection circuits included for testing purposes.

The front-end is compliant with the ILC design regarding noise and power constraints. Power constraints require that all modules have to be designed with power-off capabilities and pulsed power mode of operation to match the ILC structure of operation. Furthermore, low power readout ASIC is required to avoid cooling systems inside the detector area. Noise constraints require to maintain a low equivalent noise charge (ENC), therefore special attention have been taken in the design of the preamplifier and the shaper as they are the dominant contribution of noise. Specifically, the main contribution of noise comes from the input transistor, the feedback capacitor of the CSA and the shaping time of the shaper. However, the addition of more elements to the readout circuit like the biasing circuit, input stage adaptors and the programmable gain increases the value of the ENC.

Noise and power analysis performed during simulation fixed the size of the input transistor in W/L =960 um/0.2 um. The shaping time is fixed by design at 1 us and, in this ASIC version, the feedback elements of the shaper are passive, which means that the area of the shaper can be reduced using active elements in future versions. Finally, the different gains of the CSA have been selected to maintain an ENC below 400 electrons for a detector capacitor of 20 pF, with a power consumption of 150 uW per channel.


POSTER - Board: E4 / 32

A New Readout Electronics for the LHCb Muon Detector Upgrade.

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The 2018/2019 upgrade of LHCb Muon System foresees a 40 MHz readout scheme and requires the development of a new Off Detector Electronics (nODE) board that will be based on the nSYNC, a radiation tolerant custom ASIC developed in UMC 130 nm technology. Each nODE board has 192 input channels processed by 4 nSYNCs. The nSYNC is equipped with fully digital TDCs and it implements all the required functionalities for the readout: bunch crossing alignment, data zero suppression, time measurements.

Optical interfaces, based on GBT and Versatile link components, are used to communicate with DAQ, TFC and ECS systems.
Summary:

The 2018/2019 upgrade of LHCb Muon System electronics includes some requirements that cannot be more fulfilled by the current readout system. The muon readout electronics has the purpose to convert the analogue signals extracted from the detector front-end channels into digital logical channels. The main changes of this upgrade involve the speedup of the readout clock, from the current 1MHz to 40 MHz (LHC clock), and the replacement of the optical communication system.

In this work, we present the new Off Detector Electronics (nODE) board and the nSYNC, a VLSI integrated circuit developed in UMC 130 nm technology.

After they have been amplified, shaped, discriminated, the signals coming from the detector, are processed in the new Off Detector Electronic (nODE) boards. They will replace the present ODEs and will be mechanically and electrically compatible with the present boards to avoid infrastructure modifications.

The nODE has 192 programmable input channels and is based on a new radiation tolerant custom ASIC, the nSYNC, which integrates all the required functionalities (clock synchronization, bunch crossing alignment, trigger hits production, time measurements, histogram capability and buffers).

The board uses only optical interfaces to communicate with the data acquisition and TFC/ECS systems. Such interfaces are based on the GBT and Versatile link components to guarantee full compatibility with the new electronic systems foreseen for the LHCb upgrade.

In each nODE there are 4 different nSYNC chips. Each nSYNC communicates to its own GBTx to transmit data to the DAQ system. The communication between nSYNC and GBTx is achieved using an e-link data rate of 320 Mb/s.

An additional GBTx (the Master GBTx) is used to receive the master 40 MHz clock and the TFC commands and to distribute them to the nSYNCs and to the other GBTx. Furthermore, the GBT master is interfaced with one GBT-SCA managing the ECS interface of the whole board.

The main purpose of the nSYNC is to synchronize the data coming from the detectors with respect to the bunch-crossing identification number (BXid). Each nSYNC channel is equipped with a fully-digital TDC that computes the arriving time of the signal inside the master clock period in order to achieve the crucial time alignment of the whole muon detector. The system can work with several time resolutions, that is the number of slices on which the master clock is divided, starting from 8 to 32. The nominal resolution expected for LHCb is 16.

To overcome the bandwidth limitation, the TDC data are zero suppressed inside the nSYNC through a combinatorial algorithm that requires only one clock cycle. The BXid tagged information, the digital hit maps of the channels and the TDC zero suppressed data are combined in data-frame that is transmitted to the DAQ at each clock cycle.

The chip includes also an I2C interface to receive the configuration parameters and to allow the reading of the status registers from GBT-SCA.

POSTER - Board: G1

65nm Receiver with Decision Feedback Equalization for Radiation Hard Data Link at 5Gbps

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We present work to develop a radiation-hard receiver ASIC in 65nm CMOS with Decision Feedback Equalization (DFE), which is a very efficient technique for compensating the distortions caused by cable losses. Achieving the best possible compensation is particularly important for HL-LHC tracking detectors because the readout cable mass is inversely related to the tolerated amount of distortion. This work makes use of link design tools from Berkeley Wireless Research Center to determine the DFE architecture and generate the receiver circuit. Results presented include S-parameter measurements for ATLAS prototype cables, comparative eye-diagrams and plans for receiver layouts.

Summary:

During the Phase-II upgrade the LHC will be prepared for a luminosity increase in order to improve the discovery potential of the machine. This means that the electronics need to be made to withstand increased radiation doses and the new readout system designed to handle higher data rates, something
that is especially crucial close to the particle interaction point where the track density is the highest. For the upgrade of the ATLAS and CMS pixel detectors, located closest to the accelerator beam pipe, this requires a transmission chain that can transfer data from the pixel readout chips to the DAQ system in speeds around 5Gpbs. The cables used in this link system will be chosen based on radiation hardness consideration and low-mass constraints and will cause significantly more signal distortions during transmission than commercial high speed cables. The cable lengths depend on the geometry of the experiments, with ATLAS considering longer cables of up to 6m. In general, the less mass a cable has the greater the signal distortion caused by cable losses. Therefore, the higher the level of distortion that can be recovered, the lower the cable mass that can be used. Lowering mass is very important for tracking detectors, and so the best possible compensation for signal distortion is desired. Our goal is to design a receiver which uses an equalization technique to compensate for distortion and restore the initial signal (this can be used alone or in conjunction with driver pre-emphasis). One such equalization technique, which has gained popularity within digital communication industry applications due to its ability to expand the available bandwidth, is Decision Feedback Equalization (DFE). In this technique, any intersymbol interference (ISI) is removed by making use of previous decisions to estimate the current received symbol and reconstruct and subtract the ISI caused by previous symbols. In this way, the signal integrity can be significantly improved and data transmission speed maximized. A DFE can be implemented as a combination of simple Finite Impulse Response (FIR) filters, which are also called taps. In order to find a specific RX design that matches the ATLAS Phase-II pixel cables a Matlab-based link evaluation tool (LinkELF) has been used for initial high-level analysis of the system based on extracted cable S-parameters. S-parameters are measured on actual prototypes cables using network analyzers. LinkELF simulates the expected eye diagrams before and after equalization as a function of the number of DFE taps. Once the DFE architecture has been determined, the receiver schematics and layouts are generated using the Berkeley Analog Generator (BAG) framework, which is a tool for automated integrated circuit design developed by Berkeley Wireless Research Center. The BAG framework supports a number of CMOS nodes, including 65nm. We will present plans to fabricate a receiver designed using these tools.

POSTER - Board: D6 / 162

A Fully Monolithic HV-CMOS Pixel Detector with a Time-to-Digital Converter for Nanosecond Time Measurements

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The Time Over Threshold (TOT) is usually measured by counting the number of clock cycles that the output of the preamp is over the threshold but the time resolution obtained is limited by the clock frequency and power consumption. Future HEP experiments will require a time resolution of few nanoseconds so that new approaches are needed. This paper presents a circuit to measure the TOT with a Time-to-Digital Converter (TDC). The circuit is very compact, low power and used to readout a matrix of HV-CMOS pixels. The chip is designed with a 150nm process from LFoundry.

Summary:

HV-CMOS sensor technologies in several different commercial vendors are being developed to study which one offers the best features to suit the High Luminosity-LHC (HL-LHC) ATLAS upgrade. There is a special interest on the 150 nm HV-CMOS technology from LFoundry because allows backside processing and stitching. Moreover, it provides an extra isolation layer to avoid punch-through between an n-well nested inside a deep n-well. This feature allows the integration of CMOS comparators and even digital electronics inside the pixel area. To study this technology, a submission through an MPW is scheduled for July 2016. The reticle is fabricated in 2 different substrate resistivities: 1k Ω·cm and 2k Ω·cm. It has an area of 1 cm x 1 cm and is split in 3 regions to prove different ideas, not only for ATLAS but also for other experiments like the Mu3e. One of these regions has a total area of 0.25 cm x 1 cm and includes a matrix with a new pixel type that provides a time resolution in the nanosecond range.
The proposed solution measures with resolution of nanoseconds when the preamp output crosses above and below the threshold level instead of measuring the number of clocks that the output is over the threshold. The two times, t1 and t2, are subtracted off-line to measure the TOT. The nanosecond resolution is obtained by using a global time stamp to determine t1 and t2 coarsely. A Time-to-Digital Converter (TDC) divides the period of a time stamp in 10 equal time intervals in order to give a fine measure of the time. It is composed of chain of Delays Elements (DE) instead of a ring oscillator in order to minimize the power consumption. The DE are tuneable in order to adjust the introduced delay to the time stamp period. The TDC produces a 5 bits number. The most significant bit indicates in which half of the time stamp period the event occurred and the less fourth the in which of the 5 subintervals. The analog front-end electronics are integrated into the pixel and include a preamp and a comparator. There are two versions of the analog part, one includes a fully CMOS comparator and the other one a comparator made of only NMOS transistors. The purpose is to study the performances of the isolation layer. The output of the comparator is sent to a digital ReadOut Cell (ROC) placed at the periphery. It is similar to the digital readout cell of the FEI3 chip, that is, it includes an event detector, a priority encoder and the address is hardwired. When a hit is detected, the ROC stores an 8 bit global time stamp and simultaneously activates the TDC to measure the time finely. The operation is repeated when the output of the preamp crosses below the reference level of the comparator. A complete description of the circuit and its operation will be presented at the conference.

POSTER - Board: C6 / 134

Development of 32-Channel System for Processing Asynchronous Data from the CBM GEM Detectors

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The 32-channel system for processing asynchronous data from the GEM detectors is presented. It has been developed as part of ASIC intended for the muon chamber of the CBM experiment and allows to run up to 10 MHz channel rate. The system provides the generation of data packages, consisting of the digital codes of signal amplitude, arrival time and channel number. Control and data exchange with host are provided by 2 serial interfaces: the slow I2C one and the high-speed (320 MHz) one. The results of testing the main blocks, prototyped in UMC CMOS 180nm process are given.

Summary:

The paper describes the elaboration at the 32-channel system of processing the asynchronous data from the CBM muon chambers at the FAIR. GEM detectors are supposed to be used to restore muon tracks, appearing as result of accelerator beam interaction with a fixed target. The readout electronics should be asynchronous. The total number of channels exceeds 106, while the minimal inter-event time is 100 ns. For each channel the ASIC should provide the measurements of signal amplitude, its arrival time and channel number, keeping power consumption within 10 mW/channel. An 8-channel prototype of system was elaborated for debugging the functional model. It comprises the blocks, performing the following functions: load of initial data and control commands, picking up the information about input signals as well as the high-speed (320 MHz) serialization output data. Test actions are applied to the system by built-in ADC emulators. The prototype has a pyramidal structure, consisting of several FIFO blocks and a control one. It was manufactured via Europractice in the UMC CMOS 180 nm process. Designed for lab tests board includes the input/output analog and digital interfaces for data exchange with FPGA processing board. The tests showed the following characteristics: maximal speed for 5-bit data - 50 MHz, readout one from the output FIFO - 320 MHz. Power consumption and chip area are 43 mW and 450x450 μm sq.
correspondingly. As result of testing one may conclude that in full scaled version it is expedient to use
the single-level pyramidal structure of data acquisition based on FIFO.
The timestamp block was optimized for the 32-channel system. Despite of an enhanced immunity to
failures, the use of majoritarian logic with tripling, realized in the prototype chip, is considered to be
non-optimal in terms of chip area. Thus the block structure has been simplified to a common time
counter in the Grey code for all channels, control logic, using a non-majoritarian principle of enhancing
reliability, and timestamp registers in each channel.
The system features an early stage signal digitization. For amplitude measurements there was designed
digital peak detector block. The function of correcting false operation and noise filtration is built-in
the block.
The interface block accomplishes a multilevel synchronisation with the GBTX chip, according to its
exchange protocol. Synchronization errors are checked by CRC codes and control commands. The
reference frequency is set by an external clock of 160 MHz. The control of the ASIC parameters and
output data transmission is carried out at a speed up to 320 MHz.
Thus the results of laboratory tests of the prototype chip as well as development of the backend part
has proved the relevance of the presented system design. The next step is expected to be manufacture
and test the full-scaled 32-channel version.

**POSTER - Board: N1 / 31**

**Simulation Environment Based on the Universal Verification Methodology**

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This talk presents Universal Verification Methodology (UVM) simulation environments of three re-
cent ASIC and FPGA projects, which have successfully implemented a new Coverage-Driven Ver-
ification (CDV) work-flow in System Verilog: (1) the CLICpix2 65 nm CMOS hybrid pixel readout
ASIC design; (2) the C3PD 180 nm High-Voltage-CMOS active sensor ASIC design; (3) the FPGA-
based DAQ system of the CLICpix chip. Different interfaces (Ethernet, trigger and timing interface,
I2C, SPI) which stimulate the devices under test are handled by complex and versatile testbenches en-
abling an exhaustive system verification and identification of difficult-to-track design flaws.

**Summary:**

The Universal Verification Methodology (UVM) is a standardized approach of verifying integrated circuit
designs, targeting a Coverage-Driven Verification (CDV). It combines automatic test generation, self-
checking testbenches, and coverage metrics to indicate progress in the design verification. The flow of
the CDV differs from the traditional directed-testing approach. With the CDV, a testbench developer,
by setting the verification goals, starts with an structured plan. Those goals are targeted further by
a developed testbench, which generates legal stimuli and sends them to a device under test (DUT).
The progress is measured by coverage monitors added to the simulation environment. This way, the
non-exercised functionality can be identified. Moreover, the additional scoreboards indicate undesired
DUT behaviour. This talk presents the simulation environments of three recent ASIC and FPGA projects
which have successfully implemented the new work-flow and serve as examples of the UVM and System
Verilog usage: (1) the CLICpix2 65 nm CMOS hybrid pixel readout ASIC design; (2) the C3PD 180 nm
HV-CMOS active sensor ASIC design; (3) the FPGA-based DAQ system of the CLICpix chip. Different
interfaces (Ethernet, trigger and timing interface, I2C, SPI) which stimulate the DUTs are handled by
a complex and versatile testbenches enabling an exhaustive system verification and identification of
difficult-to-track design flaws.

**POSTER - Board: N2 / 49**

**SPIDR, a General-Purpose Readout System for Pixel ASICS**
The SPIDR system is a flexible general-purpose readout platform for new and existing R&D ASIC projects, like Medipix3 and Timepix3. The system consists of an FPGA board, which reads out the ASIC and communicates via 1 and 10 Gigabit Ethernet to the back-end DAQ. It can be easily adapted and used as test-bed for other ASICs. The SPIDR system is currently used in various hybrid pixel detector projects such as the LHCb VeloPix. In this presentation we will highlight the architecture of the system and show a few successful applications of the SPIDR system.

Summary:

The SPIDR system is a flexible general-purpose readout platform that can be easily adapted to test and characterize new and existing detector readout ASICs. It is originally designed for the readout of pixel ASICs from the Medipix/Timepix family, but other types of ASICs or front-end circuits can be read out as well.

The SPIDR system consists of an FPGA board with memory and various communication interfaces, FPGA firmware, CPU subsystem and an API library on the PC. The FPGA firmware can be adapted to read out other ASICs by re-using IP blocks. The available IP blocks include a UDP packet builder, 1 and 10 Gigabit Ethernet Mac’s and a ‘soft’ CPU. Currently the firmware is targeted at the Xilinx VC707 development board and at a custom board called compact-SPIDR. The firmware can easily be ported to other Xilinx 7 series and ultra scale FPGAs.

The gap between an ASIC and the data acquisition back-end is bridged by the SPIDR system. Using the high pin count FMC connector only a simple chip carrier PCB is required. A 1 and a 10 Gigabit Ethernet interface handle the connection to the back-end. These can be used simultaneously for high-speed data and configuration over separate channels. In addition to the FMC connector, configurable inputs and outputs are available for synchronization with other detectors. A high resolution Time to Digital converter is provided for time stamping events in the detector.

The SPIDR system is frequently used as readout for the Medipix3 and Timepix3 ASICs. Using the 10 Gigabit Ethernet interface it is possible to read out a single chip at full bandwidth or up to 12 chips at a reduced rate. Another recent application is the test-bed for the VeloPix ASIC, which is developed for the vertex detector of the LHCb experiment. In this case the SPIDR system processes the 20 Gbps scrambled data stream from the VeloPix and distributes it over four 10 Gigabit Ethernet links, and in addition provides the slow and fast control for the chip.

In this presentation we will highlight the architecture of the system and show a few successful applications of the SPIDR system.

POSTER - Board: N3 / 74

The ARAGORN Front-End - FPGA Based Implementation of a Time-to-Digital Converter

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We present the ARAGORN front-end, a cost optimized, high-density Time-to-Digital Converter (TDC) platform. Four Xilinx Artix-7 FPGAs implement 384 TDC channels with a time resolution smaller than 200 ps on a single module. A fifth FPGA acts as data concentrator and master of an onboard SFP+ and a multi-channel optical transceiver slot to interconnect with up to seven boards though a star topology. This novel approach makes it possible to read out in total eight boards yielding 3072 input channels via a single optical fiber at a bandwidth of 6.6 Gb/s.

Summary:

The ARAGORN board comprises four low cost Xilinx Artix-7 FPGAs out of the most recent device family in order to implement the TDC functionality of 384 differential input signals received by four Samtec QMS 208-pin high-speed connectors. The board comprises both a SFP+ optical transceiver module for data readout and an optional CXP transceiver slot. The optical interfaces are attached to the high-speed transceiver tiles of a fifth Artix-7 FPGA which in turn acts as data concentrator device for the TDC-FPGAs. This feature makes up an interconnection with up to seven boards as satellites using an optical fanout cable. Thanks to the pluggable implementation of the CXP transceiver module, the identical front-end layout is maintained independent of the final application.

The TDC application requires the sampling clocks of all front-ends recovered from the high-speed serial links to be phase-synchronous. Control signals have to be distributed with fixed latency to the receiver nodes in order to synchronize system timing. Special care was taken in the configuration of the integrated high-speed transceivers so that system synchronization is guaranteed upon repeated device initializations. Hence a challenge of the design is the jitter attenuation of the recovered clocks with deterministic output clock phase to replicate the uplink data among the CXP transceiver channels.

We decided to implement a shifted-clock sampling algorithm. Thereby, each TDC input channel is linked to a set of eight flip-flop components driven by equidistant phase-shifted clocks running at 311.04 MHz. Time stamps are encoded from the register output and accomplished by a coarse counter. The design allows the user to choose between rising, falling or both edge sensitivity during operation. The readout process is dead-time free with a double hit resolution limited by the sampling clock period. Reducing the overall data rate, a trigger signal can be used to further distinguish the physics events from background. For this purpose, the design includes an algorithm to pass only hits matching a given time window with respect to the trigger arrival time to the output FIFOs.

In conclusion, we present a highly versatile TDC platform with outstanding high-speed optical readout capabilities, strongly reducing the readout expenses. This novel approach permits 3072 input channels to be concentrated and read out with a single optical fiber at a bandwidth of 6.6 Gb/s. Another highlight is the superior channel density of a single module with a form factor of 140 mm x 172 mm comprising 384 TDC inputs, limited only by connector spacing constraints. Accordingly, we succeeded in the development of a very cost optimized design. The TDC implementation maintains a time resolution smaller than 200 ps for all channels using only 16 % of the flip-flop registers and 22 % of the look-up tables (LUTs) of the Artix-7 FPGA device resources. This will allow for FPGA design upgrades if future applications demand for even higher time resolution.

This work is supported by BMBF.

**POSTER - Board: C9 / 1**

**Single Event Effects Mitigation with TMRG Tool**

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Single Event Effects (SEE) are a major concern for integrated circuits exposed to radiation. There have been several techniques proposed in order to protect the circuits against radiation induced upsets (e.g. Triple Modular Redundancy).
The purpose of the TMRG tool is to automatize the process of triplicating digital circuits freeing the designer from introducing manually the TMR code at the implementation stage. It helps to ensure that triplicated logic is maintained through the design process. Finally, the tool streamlines the process of introducing SEU and SET in gate level simulations for final verification.

Summary:

Single Event Upsets (SEU) are a major concern for integrated circuits used in radiation environment, especially for circuits fabricated in modern deep sub-micron technologies. For reliable system operation in environments such as the LHC it is necessary to protect the logic from radiation induced Single Event Upsets (SEU). Many techniques have been proposed in order to protect the circuit against SEU. Virtually all techniques rely on data redundancy. It is assumed that if the information is stored in several places (circuit nodes), it can be properly reconstructed even if some of these nodes are disturbed. Among the SEU hardening techniques, some are based on hardening standard cells while others address the problem on a system level, by utilizing error-correcting coding (ECC), temporal redundancy, or Triple Module Redundancy (TMR).

The Triple Module Redundancy Generator (TMRG) tool developed at CERN automatizes the process of triplicating digital circuits freeing the designer from introducing the TMR code at the implementation stage. As the triplication does come with penalties (increased power and area, decreased speed) it is not always possible to fully triplicate the circuitry. Moreover, not all blocks can be easily triplicated (e.g. I/O ports or some analog blocks). The TMRG tool allows the designer to decide which blocks and signals should be triplicated. The tool handles the conversion process between triplicated and not-triplicated signals. The behavior of the tool is controlled by directives, which can be placed in the Verilog source code or a configuration file. The TMRG tool chain is compatible with the ASIC design flow used in the HEP community and does not over restrict the user’s coding style. In addition, as it can be run in a batch mode, the tool can be seamlessly integrated in a fully automatic digital design flow.

The code generated by TMRG tool will contain redundancy and therefore the synthesizer will want to remove it, compromising the production of SEU/SET robust digital circuits. The TMRG tool chain helps to ensure that triplicated logic is maintained during the synthesis process by generating a set of constrains for the synthesis process. In modern deep sub-micron technologies, the probability of multiple bits upsets caused by the same particle is not negligible. In order not to compromise TMR effort, the redundant cells have to be placed away from each other. Therefore, the TMRG tool chain assist also in the place and route, trying to constrain the placement process. Finally, the tool provides an uniform mechanism to introduce SEU and SET in gate level simulations for final verification.

POSTER - Board: N4 / 96

Versatile ASIC and Protocol Tester for STS/MUCH-XYTER2 in CBM Experiment

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The STS/MUCH-XYTER2 is the new front-end ASIC for the STS and MUCH detectors in the CBM experiment. It uses an innovative protocol ensuring reliable synchronization of the communication link between the controller and the ASIC, transmission of time deterministic commands to the ASIC and efficient readout within a GBT-based data acquisition structure. The paper describes the FPGA-based tester platform for in-hardware functional verification of the digital part of the chip and the protocol before the ASIC is taped-out. The applied methodology may be useful for verification of other ASIC-based designs.

Summary:

The STS/MUCH-XYTER is the new front-end ASIC designed for the STS and MUCH detectors in the CBM experiment. It uses an innovative protocol (STS-HCTSP) for sending the control commands to the ASIC in a time-deterministic way and for efficient reception of the hit-related data. An important feature of the protocol is that it enables a reliable synchronization and resynchronization of the communication link between the readout controller and the front-end ASIC without the full reset. That facilitates debugging of the readout system in case of problems.

The aim of the work was the development of a hardware platform for two purposes:

- the hardware verification of the ASIC control part before the tape-out
- the preparation of the basis for further development of the full readout system. Basing on these two goals, a dedicated hardware platform was prepared based on the AFCK board.

The presented methodology covers a number of specific issues both on the software and on the hardware level.

Due to inherent differences between the FPGA and ASIC technologies, the HDL code describing the STS/MUCH-XYTER2 design had to be adapted for FPGA implementation. Special measures were applied to ensure coherency of FPGA and ASIC implementations.

The dedicated controller module (communicating with the ASIC model under test) was also implemented as an IP core in FPGA. It implements time-critical parts of the communication protocol - transmits commands to the ASIC, handles responses and acknowledgments and receives the hit data.

The high-level procedures of the communication protocol, including the synchronization procedure and reception of data were implemented in a PC software using Python language. The communication between the computer and tester was provided by the Ethernet TCP/IP network with IPbus protocol. That approach allows rapid prototyping in Python prior to the C/C++ implementation of performance-critical parts after the algorithm is tested.

The communication link between the STS/MUCH-XYTER2 ASIC and its controller (AFCK-based boards) in the final system will be provided by the GBTx chip (featuring electrical links on the ASIC side and fast, optical link at the controller-side). As it was not available at the time tests were performed, the tester platform implements the realistic black-box model of the GBTx-based E-Link. The tester platform also provides the AC-coupled differential links equivalent to the SLVS links which will be used in the final system.

The tests performed at the nominal speed of the STS/MUCH-XYTER2 links (160 Mbps uplink and 320 Mbps downlink) have proven the correctness of the ASIC’s back-end model design and the communication protocol. The developed platform will be developed further towards a testplatform for the fabricated ASIC including the real GBT links. It can also be used as a prototype of the final ASIC controller implemented in the Data Processing Board.

The platform and associated methodology may be also reused in pre-production verification of other ASIC-based control and readout systems.
Flex Based Data and Power Transmission for the ATLAS Pixel Upgrade

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The replacement of the whole ATLAS inner detector is foreseen for 2023/2024. The requirements of the data transmission rates for the upgraded pixel detector will be particularly difficult to meet as the projected transmission rates per chip are 5 GBit per second for each readout chip at the inner-most radius. Results from a first prototype (intended for the Alpine layout) of a flex based solution where data, power and bias voltages are transmitted through a common stave flex will be presented.

Summary:
The replacement of the whole ATLAS inner detector is foreseen for 2023/2024. The motivation for this effort is twofold: the radiation damage received by that time will have decreased the detector efficiency sufficiently and the new requirements regarding granularity, bandwidth and radiation hardness posed by the high luminosity LHC cannot be fulfilled by the current inner detector. Particularly, the demands on the data transmission rates within the upgraded ATLAS pixel detector will be challenging.

Taking the expected trigger rates, pixel size and occupancy into consideration results in projected transmission rates of 5 GBit per second for each readout chip at the inner-most radius. Due to the harsh radiation environment the first segment of that connection has to be realized by electrical transmission instead of using directly optical fibre. Experience gained with the current inner detector encourages to place the opto converter in an easily accessible location for maintenance purposes. The exact length of the part to be achieved with an electrical transmission is dependent on the used stave layout but can amount to 7 m.

The presented study focuses on the application of a flex based solution to the Alpine layout. This layout employs so-called mountains which are extrusions set at an angle towards the flat stave on which sensors are mounted. The connection between the module flexes and their corresponding stave flex requires folding. The actual connection between the two parts is realized with micro connectors which were tested for their high voltage capability as they have to carry the sensors' bias voltages as well. A full scale stave flex prototype based on the Alpine layout and designed for FE-I4 based modules (successor frontend is not yet available) has been built and characterized.

The first iteration of the stave flex prototype was implemented in form of three separate single core flexes. In order to minimize matter very thin copper layers of 5 µm were used which results in a X0 below 0.3 %. Its maximum length of 120 cm allows to realize the connection from the modules until the end of stave. The achievable data transmission rates were verified by standard BER tests using a dedicated FPGA board. Pre-emphasis and equalization were employed in order to optimize the transmission and the fulfilment of all prerequisites could be proven. A hybride solution consisting of the stave flex and passive conversion on an end-of-stave board to a twinax cable has been studied as well.

The prototype also provides traces for the front end power and sensor bias voltage. Serial powering is foreseen and the necessary communication and supply lines for the module control chip PSPP are included as well. The power losses over the stave flex have to be minimized in order to avoid introducing heat. This was studied using an infrared camera and temperature sensors. Emulated modules with resistors were used to emulate the load of the real modules. The results were very positive as a loss of less than 10 % was measured.

A System-Level Model for High-Speed, Radiation-Hard Optical
Links in HEP Experiments Based on Silicon Mach-Zehnder Modulators

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Silicon Mach-Zehnder modulators that are resistant to a total ionizing dose of 1MGy have recently been demonstrated. Such devices could potentially be installed close to the interaction points in future LHC experiments. Because they require an external continuous wave light source, radiation-hard optical links based on Mach-Zehnder modulators will need to have a different system design when compared to existing VCSEL-based optical links. A first model for such a system is presented, including estimates for the optical power budget, the electrical power dissipation and the architecture of the proposed system.

Summary:

Silicon Mach-Zehnder Modulators (MZMs) are based on highly doped pn-junctions incorporated into two waveguides forming an optical interferometer. Due to the high doping concentration used, MZMs have been shown to be relatively insensitive to displacement damage well beyond a 1 MeV-equivalent neutron fluence of 2e15n/cm2. Recent investigations on optimized device designs have also led to a high resistance against total ionizing dose (TID) levels of above 1MGy. These values indicate that silicon MZMs have the potential to replace electrical and/or optical links that are currently installed close to the interaction points in LHC experiments.

In order to determine whether such a system can be competitive with, and ideally advantageous over, currently used optical or electrical links, the optical power budget of the optical links and the electrical power dissipation of the components needs to be estimated. Aside from that, open questions regarding integration of MZMs and driver ICs, module packaging and interfacing with the particle sensors have to be addressed.

The last important aspect of such a system concept is that of the light source to use, where to place it and how to connect it to the MZMs. This is especially relevant as silicon is an indirect bandgap material and efficient light sources are thus not available. External continuous wave (CW) light sources must be used with silicon MZMs regardless of their operating environment. In commercial applications, the light source is typically an edge-emitting laser diode tightly integrated with the MZM. Since those laser diodes are sensitive to radiation damage, the light source has to be placed further away from the MZM for radiation-hard links. In this way, radiation damage to the light source could be reduced, enabling the use of MZM-based optical links in very harsh radiation environments.

We present a concept for a silicon MZM-based radiation hard optical link system. The optical power budget and the electrical power dissipation of the envisioned system are quantified and a proposal for a light source and a fiber cabling scheme is given. We finally highlight what components will need to be further investigated to fully assess the viability of using this technology in high energy physics applications.

POSTER - Board: K2 / 100

Development of a Rest Gas Ionisation Profile Monitor for the CERN Proton Synchrotron Based on a Timepix3 Pixel Detector

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A fast non-destructive transverse profile monitor, named PS Beam Gas Ionization monitor (PS-BGI), is under development at CERN for the Proton Synchrotron (PS). This monitor infers the beam profile from the transverse distribution of electrons created by the ionisation of rest gas molecules by the high energy beam particles. The distribution is measured by accelerating the electrons onto a Timepix3 based imaging detector. This detector consists of hybrid pixel detector assemblies mounted on a ceramic printed circuit board and flexible printed cable which have been developed specifically for operation in an ultra high vacuum environment.

Summary:

The challenging High Luminosity LHC (HL-LHC) requirements have led CERN to initiate an ambitious improvement program of the full LHC injector chain. As part of this program the transverse emittance monitors in the CERN Proton Synchrotron (CPS) will be upgraded to provide continuous non-destructive bunch-by-bunch measurement of the beam profile. Measurement of the transverse beam profile is currently performed by fast rotational wire scanners. These scanners cannot provide continuous bunch-by-bunch measurements and the expected future increase of the beam brightness will lead to an accelerated sublimation of the wire. A fast non-destructive transverse profile monitor is currently under development at CERN. This profile monitor, named PS Beam Gas Ionization monitor (PS-BGI), is based on the ionisation of rest gas molecules by the high energy beam particles. The transverse beam profile is inferred from the transverse distribution of the ionisation electrons, the distribution of which is measured by accelerating the electrons onto an imaging detector by means of a guiding electric field. A dipole magnetic field parallel to the electric field maintains the transverse position of the electron by countering diffusive effects. The imaging detector for the PS-BGI must have a time resolution < 25ns to facilitate bunch-by-bunch measurement of the beam profile and a spatial resolution < 0.1mm. The environment in which the imaging detector must operate is very challenging: it must operate inside the CPS ultra-high vacuum (10^-9 mbar), in a 10 kGy/yr radiation area and be tolerant to electromagnetic interference caused by the beam. The system must also be sufficiently robust to run reliably for the duration of the annual injector program. To meet these challenging requirements an imaging detector system has been developed which is based on the Timepix3 pixel detector chip, which has been developed in the framework of the Medipix3 collaboration. The imaging detector consists of four pixelated p-on-n silicon sensors bump bonded to four Timepix3 readout chips. The hybrid pixel detector assemblies are mounted on a ceramic Printed Circuit Board (PCB) carrier which has been developed specifically for operation in an ultra high vacuum environment. The ceramic PCB is connected to electrical vacuum feedthroughs by means of a Flexible Printed Cable (FPC) based on a Liquid Crystal Polymer (LCP) substrate. To facilitate the readout of the Timepix3 chips (8 x 320 MHz SLVDS) particular attention has been paid to the signal transmission of the complete readout chain.

This contribution will focus on the development, manufacturing and first functional testing of the readout system for Timepix3 based imaging detector, with particular emphasis on the requirements, design and manufacturing of the ceramic carrier and flexible interconnect. Finally, first results will be presented on the operation of the Timepix3 chips inside the PS beam pipe vacuum.

POSTER - Board: K1 / 118

HDI Flexible Front-End Hybrid Prototype for the PS Module of the CMS Tracker Upgrade

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The CMS tracker upgrade for the HL-LHC relies on different module types, depending on the position of the respective module. They are built with HDI flexible circuits that are wire bonded to silicon strip sensors. The front-end hybrids will contain several flip-chip bonded readout ASICs that are still under development. Mock-up prototypes are used to qualify the advanced flexible circuit technology and the parameters of the hybrids. This paper presents the PS mock-up hybrid in terms of testing, interconnection, fold-over, thermal properties and layout feasibility. Plans for connectivity testing and simulation results are described.

Summary:

A major upgrade of the CMS Tracker detector is today under development to address the new requirements imposed by the HL-LHC. The new CMS Tracker will use two main types of modules. The outer tracker 2S modules contain two parallel strip sensors of $10 \times 10$ cm$^2$, enabling the identification of stubs required for the track triggering function. The inner tracker PS modules contain a strip sensor and a macro pixelated strip sensor of $5 \times 10$ cm$^2$, providing additional track information along the Z-axis. The front-end electronics of these different modules are based on binary readout ASICs (CBC3, SSA, MPA), flip-chip bonded on different high density interconnection (HDI) flexible printed circuit boards.

The module development for the upgrade started well before the first ASIC prototypes were manufactured. One of the main module building blocks is the front-end hybrid. The first hybrid prototypes were designed for the 2S modules, using the CBC2 prototype. The first full scale front-end hybrid prototype was designed and manufactured in 2014. It enabled the construction of the first 2S module prototypes and it provided valuable feedback to the engineers. Several complications and difficulties were found and this highlighted how important it is to construct module prototypes in order to understand the arising problems.

The MPA, SSA and CIC ASICs of the PS front-end hybrid are still under development, however the corresponding module design is in a well-developed state. This required the design of a new PS type hybrid prototype in its targeted outline, which matches the current 3D design geometry of the module. It contains carbon fiber stiffeners that are glued on the bottom of the circuit to provide sufficient cooling and stiffness. Heating resistors and dummy chips are mounted to emulate the power consumption and mechanical behavior of the ASICs. The circuit also has a flexible fold over part that will bring useful information about the folding process.

Moreover, the PS mock-up prototype will be used for the electrical characterization of the powering, testing, data transfer and calibration features that are intended to be used in the final PS hybrids. It enables the evaluation of miniature power and interface connectors aimed to replace the initially foreseen wire bonded connections. Connectors could reduce the module assembly time and provide less fragile connection. Additionally, a fine pitch spring loaded needle tester pad pattern is implemented and evaluated: two probing patterns are used for contact resistance, cross talk, signal integrity, reliability and alignment tests. The folding impact on the differential impedance brings another subject for verification. Two different test options for the sensor connectivity with the front-end chips are implemented with known failures on the PCB level. One method is using antennae to inject charge into the wire bond pads. Second method is grounding the input channels of the chips and uses the internal charge injection of the front-end ASICs. This is necessary for the qualification of the hybrid connectivity during the production phase.

**Properties of Thin Polyurethane Wire Bond Coatings after Irradiation**

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Thin polyurethane (PU) coatings for aluminum wedge wire bonds are proposed to protect the ATLAS Inner Tracker upgrade from condensation-induced corrosion and oscillations from periodic Lorentz forces. Coating robustness after exposure to an HL-LHC lifetime dose is being evaluated. Mechanical properties of irradiated samples are tested at room temperature and -20°C. Irradiated samples are thermal-cycled to test for radiation-induced intolerance to thermal expansion.

Summary:

Wire bonds sprayed with a fresh coating of polyurethane (PU) have been shown to tolerate direct exposure to water. PU coatings suppress oscillations from periodic Lorentz forces that can be induced in pixel and strip tracking detectors in the intense magnetic fields of an LHC detector. Results were previously reported at room temperature. Performance of PU coatings at -20°C, a typical operating temperature of a silicon tracker, will be reported for samples irradiated at HL-LHC lifetime doses anticipated at locations throughout the ATLAS Inner Tracker (ITk) upgrade. Samples are being thermal-cycled to test for thermal expansion issues induced by radiation curing of PU.

The coated aluminum wire bonds (1% silicon, 25 micron thickness, 28 mm length) are evaluated in a 1.0 T field with an "endcap/disk" geometry (B field parallel to the PC board normal and perpendicular to the wire bond) which is the most vulnerable geometry to Lorentz forces. Bond wire vibrations are excited with 50% duty-cycle square waves. Resonance characteristics are reported as a function of coating thickness, level of irradiation, and temperature.

Characterization of Radiation Effects in 65nm Digital Circuits with the DRAD Digital Radiation Test Chip

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A Digital RADiation (DRAD) test chip has been specifically designed to study the impact of Total Ionizing Dose (TID) (< 1GRad) and Single Event Upset (SEU) on digital logic gates in a 65nm CMOS technology. Nine different versions of standard cell libraries are explored in this chip, basically differing in the device dimensions, Vt flavor and layout of the device. Each library has eighteen test structures specifically designed to characterize delay degradation and power consumption of the standard cells. For SEU study, a dedicated structure based on a shift register is designed for each library. First irradiation results will be presented.

Summary:

Radiation effects concerning on-detector electronic systems are one of the main challenges for the ASIC design engineers. The unprecedented radiation environment considering HL-LHC detector upgrades requires significant investigation of very high total ionization dose effects not only on the single MOS device alone but also on the digital logic gates. Studying the impact of high radiation levels on digital electronics in 65nm CMOS technology is vital for key sub-detectors of the ATLAS and CMS upgrades. ATLAS and CMS pixel detector chips (RD53 collaboration) require radiation tolerance of up to 1Grad for a 10 years lifetime for the inner layers of the vertex detectors. Outer tracker detectors require radiation tolerance of the order of 100Mrad (e.g. the MPA chip for the CMS tracker upgrade) and high speed optical link chips for LPGBT, require very high circuit speeds after radiation damage.
The aim of the DRAD chip is to measure the delay degradation under different TID on different customized libraries composed of ten combinational and two sequential cells each. These libraries differ in minimum device dimensions (both L and W), type of transistors (Normal Vt, Low Vt and high Vt) and layout of the device (normal and enclosed).

The delay degradation is measured using test structures (delay chains and ring oscillators) with different gates (NAND, NOR, XOR, buffers and inverters, flip-flop and latch) for each of the standard cell library. To deal with sequential elements, specific structures have been designed to the measurement of setup and hold time. In addition a 24 bit synchronous counter is included for the study of radiation effects in a typical digital composite circuit. To study the effect of SEU, a large shift register is implemented in each library. High speed structures (VCO and counters) are included only for the fastest library which has enclosed layout and low Vt transistors for future high speed optical link chips. The test structures have been optimized and verified using 200 and 500MRad transistor models from the radiation working group of RD53 collaboration.

A small and portable test system has been developed for the DRAD chip to enable radiation tests to be performed in X-ray facilities, and it can be adapted for other radiation test facilities (Cobalt, Ion beam, Proton beam). The test system is based on a Spartan 6 FPGA evaluation board, an interface board in charge of powering the chip, power monitoring and the conversion between signaling standards, and a small carrier board with a wire bonded DRAD chip. Delay characterization can be performed with a TDC function integrated in the FPGA and/or with the help of an external high speed sampling oscilloscope. The DRAD chip, a 2x2 mm mini@sic, was submitted on March 23 2016 and is expected to be available by the end of May. The test system is in the process of final stage of implementation. The X-ray radiation tests will be carried out this summer, and the measurement results will be presented at the TWEPP workshop.

POSTER - Board: C2 / 170

Component Qualification for the Mu2E Calorimeter Wafeform Digitizer

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The Mu2e experiment at Fermilab searches for the coherent muon conversion to electron in the Coulomb field of a nucleus. The detector is composed of a straw tube tracker and an CsI crystals electromagnetic calorimeter housed in a superconducting solenoid.

The digitizing electronics will be located inside the magnet cryostat and will be operated in vacuum. The harsh experimental conditions, with the presence of a high neutron flux, ionizing dose and magnetic field, make the design challenging and all the components must be individually tested and qualified.

The experimental results of the qualification tests are described.

Summary:

The Mu2e experiment at Fermilab searches for the coherent muon conversion to electron in the Coulomb field of an Al nucleus, with the goal to improve the current experimental limit by 4 orders of magnitude. The Mu2e detector is composed of a straw tube tracker and an undoped CsI crystals electromagnetic calorimeter housed in a superconducting solenoid.

In order to achieve the needed background suppression, the calorimeter provides a time resolution better than 500 ps and an energy resolution of O(5%) @ 100 MeV. To fulfill these requirements a digitizing system, composed of around 150 cards sampling a total of around 2700 channels at a frequency of 200 MHz, is currently being designed.

The electronics will be located close to the calorimeter, inside the magnet cryostat and will be operated
in vacuum. The harsh experimental conditions, with the presence of a high neutron flux, ionizing dose and magnetic field, make the design challenging. All the components and materials must be individually tested and qualified. The main components are the DCDC converter, the ADC and the FPGA and we started selecting and qualifying these parts.

DCDC converter
The more critical part is the DCDC converter because of the presence of a strong magnetic field. Following some studies described in literature we evaluated several parts from Linear Technologies and finally the LTM8033 survived the selection. After some operational tests we defined a qualification procedure and then we started the test campaign. The setup was composed of an automated system capable of measuring and storing input and output voltages and currents with a good degree of precision. The important parameters to check in these kind of tests are the stability of the output voltage and of the conversion efficiency. The DCDC behaviour in magnetic field was tested at the LASA INFN laboratory of Milan Italy, while the performance when irradiated with neutrons was tested at the ENEA FNG facility in Frascati Italy. The test under ionizing dose was performed at the ENEA Calliope facility in Bracciano Italy.

ADC
The digitizer is specified to sample at least with 200 Msamples 12 bits of resolution and operating in vacuum the absolute low power is a fundamental requirement. Also the cost is an important parameter just to the fact that more then 3000 channels will be digitized. At the end we selected the Texas Instrument ADS4229. Also in this case a portable test setup was developed. A standard sinusoidal signal was sent in input to one ASS4229 demo board and the ADC output was stored on disk. We performed the test in the same facilities as the DCDC converter.

FPGA
The selected FPGA is a Microsemi SMartFusionII, model SM2150T. This part is already qualified by the producer so our current idea is not to qualify this part individually but only at the board prototype level. The experimental results of all these qualification tests are described.

POSTER - Board: H7 / 56

The Versatile Link Demonstrator Board (VLDB)

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The Versatile Link Demonstrator Board (VLDB) is the evaluation kit for the Radiation Hard Optical Link ecosystem, which provides a 4.8 Gbps data transfer link for communication between front-end (FE) and back-end (BE) of the experiments. It gathers the Versatile Link main radiation hard custom ASICs: GBTx, GBT-SCA and VTRx/VTTx plus the FeastMP, a radiation hard in-house designed DCDC.

This board is the first design allowing system-level tests of the Link with a complete interconnection of the constitutive components, allowing DAQ, control and monitoring of FE devices with the GBTx – SCA pair.

Summary:
The Versatile Link Demonstrator Board (VLDB) is the evaluation kit for the Radiation Hard Optical Link ecosystem, which provides a 4.8 Gbps data transfer link for communication between front-end (FE) and back-end (BE) of the experiments. It gathers the Versatile Link main radiation hard custom ASICs: GBTx (ASIC dedicated to serialization, deserialization and data and clock recovery), GBT-SCA (Slow Control Adaptor ASIC dedicated to FE control and status monitoring) and VTRx/VTx (optical transceiver/dual transmitter) plus the FeastMP, a radiation hard DCDC designed at CERN. It manages timing signal, trigger, status monitoring, readout data and slow control of FE devices.

Already distributed to 40 teams, this board is the first design allowing system-level tests of the Versatile Link with a complete interconnection of the constitutive components. HDMI connectors allow to test communication with experiments Front-End electronics (up to 20 Front End ASICs can be connected via elink/HDMI to the same GBTx). They also allow to try multiple interconnection schemes between several VLDBs playing all the roles foreseen by the various use cases or to focus on slow control using the GBT-SCA chip. It is a unique tool for initial characterization of the full Radiation Hard Optical Link ecosystem (in particular focussing on the quality of recovered clock delivered to the Front-End electronics, latency of delivered triggers or data link characterization). It is also the ideal guinea-pig to test software and firmware implementation at Back-End level and to control complex systems based on multi-GBT implementations. It can also be used for preliminary on-site system tests. Finally, it is an excellent reference for future board designs using these components.

The VLDB board will be presented as well as several interconnection schemes emulating experimental setups. A demonstrator implementing slow control of various Front-end devices over GBTx and GBT-SCA will be described. Finally, the results of various characterization campaigns of the GBTx and on the full link -based on the VLDB- will be commented, such as clock stability with varying temperature, radiation tests and latency tests.

**POSTER - Board: H9 / 57**

**The MuPix Telescope – A Thin, High Rate Particle Tracking Telescope**

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The MuPix Telescope is a particle tracking telescope, optimized for low momentum particles and high rates. It was build to test and integrate the novel High-Voltage MonolithicActivePixelSensors ("HV-MAPS"), designed for the Mu3e tracking detector. It is also used to test the Mu3e readout concept.

The telescope consists of four layers of the newest prototypes, the MuPix7 sensors, which send the fast serial data self triggered to an FPGA, where the data is time ordered and written to the PC, where online tracking is performed.

The presentation covers the chip architecture, readout concept, online reconstruction and test beam performance.

**Summary:**
The Mu3e Experiment will search for the lepton flavor violating decay of a positive muon into two positrons and one electron with a target sensitivity of 1 in $10^{16}$ decays. A high rate beam, of $10^9$ muons/s will be stopped on a passive target and the low momentum decay particles momentum ($p < 53$ MeV/c) as well as the vertex will be measured with a thin four layer pixelated detector. The high rate ($10^{19}$) of low momentum particles asks for a new detector technology: High-Voltage-Monolithic-Active-Pixel-Sensors (“HV-MAPS”), combining the advantages of thin MAPS sensors with the fast charge collection of classical hybrid pixel sensors, are chosen for Mu3e.

The MuPix7 prototype is produced in a commercial HV-CMOS process. It is a fully monolithic pixel chip with a 32x40 pixel matrix and operates in a continuous, self triggered, non-shuttered zero suppressed readout. Each pixel contains its own amplifier and source-follower and has a point to point connection to its own digital cell in the pixel periphery. Each digital cell has second amplification stage, a comparator and an 8bit time stamp latch. In addition, a finite state machine is realized in the digital part, performing a priority readout. The hit information is 8bit/10bit encoded and serialized on chip. A 1.25 Gbit/s LVDS link is used to stream out the data.

To integrate the HV-MAPS into a larger tracking device, to test the feasibility of the aspects of the Mu3e readout concept and for test beam characterization, a tracking telescope is build:

To keep the readout concept close to the Mu3e concept, 4 stacked layers of HV-MAPS are read out in a self triggered mode and stream the 8bit/10bit encoded data at 1.25 Gbit/s over low-voltage-differential-signaling links to a FPGA, mounted in an PCIe slot of the readout PC. On the FPGA, decoding and time sorting of the incoming data is performed on the fly. The data is directly copied over PCIe to the local RAM. The data transfer is realized either by polling or direct memory access (DMA). A versatile graphical user interface provides direct access to the online monitoring, run control and sensor configurations.

The data is then directly dumped to memory and forwarded to the online monitoring. Here, online tracking on the CPU is performed, which offers online monitoring of alignment, beam properties and sensor efficiencies. GPU tracking has been implemented and used to test the Mu3e online reconstruction setup.

The presentation will focus on the readout concept and the performance at test beams. The online reconstruction will also be addressed, as well as the chip architecture. At the end a short outlook, including our future plans for the telescope and Mu3e are given.

POSTER - Board: H6 / 138

Design Studies for the Phase II Upgrade of the CMS Barrel Electromagnetic Calorimeter

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The High Luminosity LHC (HL-LHC) aims to reach the unprecedented integrated luminosity of 3 ab-1 with an instantaneous luminosity up to $5 \times 10^{34}$ cm$^2$ s$^{-1}$. This poses stringent requirements on the radiation resistance of detector components and on the latency of the trigger system. The barrel region of the CMS Electromagnetic Calorimeter will be able to retain the current lead tungstate crystals and avalanche photodiode detectors which will meet the performance requirements throughout the operational lifetime of the HL-LHC. The new front-end electronics and very front-end system required at high luminosities will be described.

Summary:

The barrel region of the CMS electromagnetic calorimeter (ECAL) is a homogeneous and hermetic calorimeter made of 61200 lead tungstate scintillating crystals. Each crystal is read out by a pair of silicon avalanche photodiodes (APDs) operating at gain 50 and at a temperature of 18$^\circ$C.

The CMS ECAL was designed to cope with the harsh LHC radiation environment for 10 years, up to an integrated luminosity of 500–fb$^{-1}$. After 2025, the high luminosity phase of the LHC (HL-LHC) will begin, with the goal of recording data corresponding to an integrated luminosity of 3000 fb$^{-1}$ in 10 years, with an instantaneous luminosity of up to $5 \times 10^{34}$ cm$^{-2}$ s$^{-1}$,
almost a factor of 5 higher than during LHC Run2. This will give rise to approximately 140 overlapping events per bunch crossing (pileup). In order to preserve good trigger acceptance in these conditions, the CMS Level-1 Trigger will exploit signals from the tracker, requiring a longer latency (up to 12.5 $\mu$s) and a higher trigger rate. The existing ECAL readout is incompatible with these requirements, and the front-end and off-detector electronics must therefore be replaced.

Recent developments in radiation hard optical links will permit the amplification, digitization and transmission of data from all ECAL readout channels to new off-detector electronics, where processors are capable of processing these data with more complex and better-performing algorithms than are currently possible. This will allow the exploitation of the full ECAL granularity at the Level-1 trigger. Such an upgrade will improve the rejection of anomalous signals (spikes) which are caused by direct ionization in the APDs, as well as mitigating pileup effects.

The luminosity increase poses significant challenges to the on-detector components. In particular the APDs are subject to hadron damage. Recent irradiation studies have shown that the APDs will remain operational, however the dark current increases linearly with the neutron fluence. The radiation induced noise becomes the dominating effect limiting the ECAL energy resolution for photons from Higgs boson decays after an integrated luminosity of about 1200 fb$^{-1}$. It is planned to operate the detector at a lower temperature of 8°C to mitigate this effect.

The new ASICs for pulse amplification, shaping and digitisation must also be less sensitive to dark current. Several possibilities are being explored: using CR-RC shaping as presently implemented, with shorter shaping time, using a charge-integrating ADC, or digitizing the signal with a faster sampling rate. These new ASICs will significantly improve the spike suppression capability, exploiting the characteristic differences between scintillation signals and spikes. The on-detector readout will also be designed with the aim of exploiting the timing resolution of the crystals, in order to discriminate between energy deposits coming from different overlapping events based on their time-of-flight.

The status of design studies for the upgraded ECAL electronics for HL-LHC based on simulations, laboratory tests, and test beam measurements will be discussed.

**POSTER** - Board: I1 / 62

**Prototype Readout Electronics for the ALICE Inner Tracking System**

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The ALICE Collaboration is preparing an upgrade of the experimental apparatus. A key element of this upgrade is the construction of a new silicon-based (12 Gpixels, 10m2) Inner Tracking System.
Its readout system consists of 192 readout units that control the pixel sensors, power modules and deliver the sensor data to the counting room. A prototype readout unit has been designed to test the interface between the sensor modules and readout electronics, signal integrity and data transfer reliability, the interface to the ALICE DAQ and trigger, and the system susceptibility to the expected radiation level (both TID and SEU).

Summary:

ALICE (A Large Ion Collider Experiment) is an experiment designed to study the properties of the Quark-Gluon Plasma (QGP). The ALICE Collaboration is preparing a major upgrade of the experimental apparatus, planned for installation in the second long LHC shutdown (2018/2019). A key element of the ALICE upgrade is the construction of a new, ultra-light, high-resolution Inner Tracking System (ITS) consisting of 7 concentric barrels. The basic sensing units are custom designed Monolithic Active Pixel Sensor ASICs implemented in CMOS Technology. There are 25,000 sensors in ITS with a total detection surface of 10m² segmented in 12.5 Giga pixels.

Each sensor of the inner layers is directly connected to the off-detector readout system with a dedicated high-speed link. To reduce the number of data links, in the outer layers sensors are arranged in groups of seven, where only one sensor is connected to the readout system, while the other sensors within the module communicate with this sensor on a local bus. All sensors of each inner barrel module and outer barrel “master” sensors share incoming clock and control lines. The master sensors of the outer barrel modules propagate these signals locally to the other sensors in a module. The clock, control and data links are transmission line segments on the detector modules and thin interconnecting copper cables.

The ITS readout system is a set of 192 Readout Units located 5m from the detector edge. It configures and controls the pixel sensors and power modules. The data stream from the sensors (2 Tb/s) is read out via 3816 high-speed differential custom-made coaxial cables.

A prototype readout unit was designed to test and verify the interface between sensor modules and readout electronics, signal integrity and data transfer reliability, the interface to the ALICE O2 Computing System, the triggering capabilities and system susceptibility to the expected radiation level.

Data from the pixel sensor modules are received by a Xilinx Kintex-7 FPGA. A USB 3.0 interface using the Cypress FX3 controller is provided for data communication with a PC. To verify the FPGA reconfiguration algorithms multiple configuration schemes are available (JTAG, QSPI Flash) including a connection from the GBT-SCA chip to the configuration port of the FPGA. An FMC Mezzanine Card, equipped with GBTx and GBT-SCA chips and Versatile Link transceivers (VTTx and VTRx), is used to test the connection to the control room via GBT link. An optical SFP module is provided as an additional communication channel. The prototype readout unit has been used as a platform for radiation susceptibility tests in a test-beam campaign.

This contribution will describe the features of the prototype readout unit, its performance and results from operation in a radiation environment.

POSTER - Board: J1 / 149

Testing and Integration of the Service Cylinders for the CMS Phase 1 Pixel

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In this talk we present the design, assembly and integration of the service cylinders for the barrel pixel detector. Furthermore, we present results of the testing and calibrations carried out with a set of Phase 1 detector modules.

Summary:
At the end of this year, the present 3-layer CMS pixel detector will be replaced with a new 4-layer pixel system to maintain the excellent tracking performance of CMS at the upcoming higher luminosity conditions at the LHC. The addition of an extra layer, closer to the beam pipe, demands a complete redesign of its services. The barrel pixel detector is attached to four supply tube half cylinders which carry the services along the beam pipe, accommodate the cooling lines and house the electronics for detector readout and control. The supply tubes are a complex system in design as well as in production due to the large number of channels and tight space requirements. In this talk we present the design of the system and discuss the assembly and integration of the barrel pixel supply tubes. Furthermore, we present results of the testing and calibrations carried out with a set of Phase 1 detector modules.

**POSTER - Board: I9 / 83**

**The Common Data Acquisition Platform in the Helmholtz Association**

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**Co-authors:** Andreas Kopmann; Heinz Rongen; Manfred Zimmer; Matthias Norbert Balzer

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Various German Helmholtz centers started 2014 to develop a modular data acquisition platform. This platform integrates generic hardware components like the multi-purpose HGF-AMC Hardware or the UFO smart camera framework, adding user value with Linux drivers and board support packages. Technically the scope comprises FPGA-modules, frontend-electronics-interfaces, FPGA-microcontrollers plus software and high-performance data transmission to computing servers. The core idea is a generic and component-based approach, satisfying specific requirements of different experiments. Its ability to deploy on different hardware is an essential feature; another is MTCA.4-support for compatibility with commercial components.

**Summary:**

Scientific instrumentation tends to more channels with higher resolution and readout rate. Quite often, there is a demand for significant increases in each of these qualities, leading to higher needs in bandwidth and system performance. The resulting complexity rises in a nonlinear way, pushing the required resources beyond the limits of what single institutes can allocate. With the intent to join efforts, various centers in the German Helmholtz Association (HGF) started to develop a modular data acquisition platform in 2014. Based on a cooperation in the area of "Detector Technology and Systems" (DTS) this approach was named DTS platform.

It aims at an integration of versatile hardware components with generic firmware and software approaches, being able to transfer both control system information and high bandwidth to computing nodes. The UFO smart camera framework with its combination of specific hardware and generic firmware plus software gives an excellent idea of the design properties of such an approach. Embedding versatile hardware components like the multi-purpose FPGA AMC Hardware (HGF-AMC) adds additional flexibility. In order to come to clear system interfaces, UFO’s idea of fast links on the FPGA side gave the idea of choosing Linux software drivers as high level interface for the DTS-platform.

This offers a chance to adapt various existing DAQ- and control system packages and gives the chance to develop board support packages. Ease of use and the chance of an early involvement in the development and test workflow are benefits as examples from various HGF centers show. Technically the generic part comprises FPGA-modules, notably frontend-electronics-interfaces, FPGA-microcontrollers with their software and high-performance data transmission techniques towards computing servers like PCIe, Ethernet and Infiniband.
The core idea of the DTS platform is a generic and component-based approach that offers a framework to satisfy the specific requirements of different experiments. With the high degree of flexibility in FPGA’s, the ability to deploy a design on different hardware platforms became a crucial requirement. Nevertheless, the decision to support standards like MTCA.4 in hard- and software came natural. Proper interface descriptions realize compatibility with commercially available components, giving an additional push to the development cycle and giving access to affordable common development hardware.

This work is supported by the programme “Matter and Technology” in the Helmholtz Association in order to improve the cooperation and knowledge exchange between the centers. It aims at reducing costs and development time and will ensure access to latest technologies for the collaboration.

POSTER - Board: J8 / 103

Phase 1 Upgrade of the CMS Drift Tubes Read-Out System

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In order to cope with a twofold increase in nominal LHC luminosity, the second level of the readout system of the CMS Drift Tubes (DT) electronics needs to be redesigned to minimize event processing time and remove present bottlenecks. The uROS boards are uTCA modules, which include a Xilinx Virtex-7 FPGA and equip up to 6 12-channel optical receivers of the 240 Mbps input links. Each board collects the information from up to 72 input links (3 DT sectors), requiring a total of 23 boards. The design of the system and the first validation tests will be described.

Summary:

The readout system of the Muon Drift Tubes (DT) subdetector of the CMS (Compact Muon Solenoid) experiment is organized in several levels. The Readout Board (ROB), located on the detector itself, constitutes the first stage, performing time-to-digital conversion (TDC) of the pulse edges from 128 DTs, storage, and window matching when the level-1 accept (L1A) trigger signal is received. The second level, so-called Readout Server (ROS), is in charge of receiving data from 25 ROBs, performing data integrity verifications, building synchronized event blocks and merging the information into higher-bandwidth links to the next level of the readout chain. The ROS was located in the harsh environment of the experimental cavern, and was relocated to the service cavern during the 2013-2014 long shutdown to ease subsequent upgrades.

Simulations show that the ROS processing time is the current most severe bottleneck in the readout chain, and it will not be able to deliver the necessary performance to cope with the expected twofold increase in luminosity for the LHC in the coming years.

A common uTCA-based design was developed for the DT trigger (TwinMux) and readout (uROS) second-level electronics upgrade, implementing different firmware. The uROS is a single-slot double-width and full-height Advanced Mezzanine Card (AMC) based around a Xilinx Virtex-7 FPGA that includes optic transceivers for slow-speed inputs and high-speed output data transmission up to 13 Gbps.

The DT system is divided in 5 wheels, with 12 sectors each. Each sector’s data is arranged in 25 fibres, making a total of 1500 links, which will be distributed in 23 uROS boards across 3 uTCA crates. Each uROS will receive and deserialize the input data, perform data quality monitoring, and build an integrated event synchronized with the CMS Trigger, Timing and Control system to be delivered through a 5 Gbps high speed link in the uTCA backplane to the so-called AMC13 board, which subsequently...
transmits to the CMS Central DAQ system. The uROS also contains 24 high speed (up to 13 Gbps) optical output links in case of future DAQ upgrades. The uROS will connect to the CMS IP network through the MCH (Micro TCA Carrier Hub) for slow control and monitoring.

The uROS board contains up to 72 fibre-optic input links (grouped in 12-fibre MTP connectors) routed to general I/O pins. The readout links are 240 Mbps pseudo DC balanced following National Semiconductors DS90LV1021 protocol. Specific deserialization has been implemented to ensure reliable data reception.

The first batch of TwinMux boards has already been fabricated, was installed during 2015 technical stop, and is currently in production. One of these boards is used for a test stand for the uROS production and it is installed in CMS and connected to input links coming from the inner detector which have been optically splitted.

In this work we will detail the design of the uROS board and report the results from the first validation tests.

**POSTER - Board: H2 / 112**

**Upgrades to the CSC Cathode Strip Chamber Electronics for HL-LHC**

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The luminosity, latency, and trigger rate foreseen at the High Luminosity LHC presents challenges to efficient readout of the Cathode strip chambers (CSCs) of the CMS end cap muon detector. Upgrades to the electronics are targeted for the inner rings of CSCs in each station, which have the highest flux of particles. The upgrades comprise digital cathode front end boards for nearly deadtimeless operation long latency capacity, new DAQ motherboards with higher-bandwidth links to accept the higher data rate, and a new Front End Driver system that can receive the higher input rates.

**Summary:**

Cathode strip chambers (CSCs) are used to detect muons in the end cap region of the CMS detector. The chambers are arranged in rings in four planes on each end of the detector. The inner rings of CSCs in each station have the highest flux of particles and this presents challenges to efficient readout at the luminosity, latency, and trigger rate foreseen at the HL-LHC.

The existing front end electronics in Stations 2, 3, and 4 are based on switched capacitor arrays with limited buffering capability. Queueing models have shown that significant saturation of the buffers would occur for the luminosity, Level 1 trigger rates, and required Level 1 latency for running at the HL-LHC. In addition, the expected output rate of data is expected to exceed the 1 Gbps bandwidth of the optical links that carry data to the back end, resulting in loss of event synchronization.

The upgrade of the inner ring of CSCs addresses these problems by replacing some types of electronics boards in these rings with upgraded boards. In particular, the existing cathode front end boards on the inner rings of Stations 2, 3, and 4 will be replaced with new digital cathode front end boards. These boards follow the design of those installed in the inner ring of Station 1 in the recent long shutdown of the LHC. The boards use flash ADCs and digital pipelines in place of the switch capacitor arrays used previously. The digital pipeline results in nearly deadtimeless operation and the capability to accommodate long latency requirements without loss of data. Also, new DAQ motherboards will be designed with optical output links with higher bandwidth to accept the higher data rate. Finally, the FED system, which is the interface between the CSCs and the central DAQ of the CMS experiment, will be replaced with a system that can receive the higher input rates.
We present the measurements and calculations that predict the behavior of the CSC electronics under HL-LHC conditions. We describe the design of the electronics systems for the upgrade and show studies of expected performance.

**POSTER** - Board: I3 / 8

**Electronics for the RICH Detectors of the HADES and CBM Experiments**

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The RICH detectors of the existing HADES spectrometer and the CBM experiment (to be built at FAIR) will use 64 channel Multi-Anode PMTs. We designed a complete set of digitizing electronics, consisting of analog and digital frontend modules, power supply and data concentrator cards plugged into a backplane carrying 3x2 MAPMTs on the front side, and all readout modules on the backside. These contain all necessary supply electronics, preamplifiers and FPGA-based TDC as well as the digital data and trigger handling logic and an optical transceiver. We are going to present the electronics along with performance test results.

**Summary:**

The heavy ion spectrometers (HADES and CBM) at the GSI Helmholtz Center for Heavy Ion Research (Darmstadt, Germany) and the FAIR accelerator contain a RICH detector for particle identification. The existing RICH at the HADES experiment is in operation since the year 2000 and is currently being upgraded with a new MAPMT readout plane consisting of 428 64-channel PMTs (Hamatsu H12700). Here we designed a set of read-out electronics which are to be used in the CBM experiment as well, and which is also planned to be used by the Barrel DIRC detector of PANDA with an adaption to the backplane design.

The major components of the read-out solution are the backplane, front-end modules a data combiner and power supply. Each building block consists of 6 PMTs and all required electronics constrained to a volume of 10 cm times 15 cm times 15 cm. The backplane is used as a mounting and interconnect structure for all modules as well as to separate the radiator gas volume from the ambient atmosphere. Front-end modules contain a discrete, low-power amplification stage (< 10 mW per channel) as well as FPGA-based 32 channel TDC (utilizing a Lattice ECP5 FPGA with 85k LUTs).

These provide a leading and trailing edge time measurement precision with an RMS well below 100 ps with on-chip calibration, while the single edge time precision including external calibration is about 10 ps RMS. Data from all 6 PMTs (384 channels) is then transported from the front-end modules via the backplane to a data concentrator card based on a Lattice ECP3 FPGA. From here a 2 GBit/s optical link (common to all subsystems in the HADES detector) receives trigger information and sends all event data to a server farm.
On all inter-FPGA links the TrbNet protocol is used throughout the HADES detector to ensure proper trigger and busy handling, data transport as well as extensive slow control capabilities. Last part of the electronics is the power supply module that allows to power each submodule with all voltages needed. The total power of the assembly is about 20 Watt (6 PMT / 384 channels). The modular electronics allow for a simple adaption of the read-out modules to the high data rates expected for the CBM experiment. In the region of highest occupancy, the data concentrator cards will be replaced with a more capable FPGA and use one or two 4.8 GBit/s optical links. The total data rate of the system will sum up to about 200 GBit/s at an envisioned collision rate of 10 MHz Au+Au.

We are going to present the concept of our very compact electronics setup along with test results regarding precision and noise figures.

This work has been supported by GSI and BMBF grant 05P15PXFCA.

POSTER - Board: 15 / 84

A New Profibus-DP Slave Interface Card for CERN’s Vacuum Sector Valve Controller

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The vacuum control systems of CERN’s accelerators are based on PLCs, which communicate with controllers either with direct I/O, or via Profibus.

In order to improve the communication efficiency of the vacuum sector valve controllers using direct I/O, a low cost Profibus-DP slave interface card has been designed.

This paper describes the steps to design a Profibus-DP slave interface that can match user’s digital parallel bus. It presents the developed hardware and firmware, together with the corresponding assessment tests. It also flags the improvements of this new interface, in comparison with the previous system.

Summary:

The new interface card follows the Eurocard 3U mechanical standard. It is supplied by 5V through the backplane connector. Line drivers interface the I/O to the backplane bus, towards the valve cards. The core of the card is an 8-Bit PIC® microcontroller (PIC18F6527) from Microchip®. It is supplied by 5V, and has 54 digital I/O and integrated SPI capability. The Profibus connection is managed by the VPC3+S ASIC from Profichip®. This ASIC is supplied by 3.3V and has I/O 5V tolerant. It uses SPI to communicate with the microcontroller, needs a 48MHz external oscillator supplied by 3.3V and can provide a clock source of 24 MHz for other devices. Additionally, an isolated 5V supply is used for the Profibus side of the RS-485 transceiver, which is galvanically isolated. For clocking the microcontroller, three options were considered: internal 8MHz oscillator, external crystal for higher speed oscillator, external 24 MHz clock provided by the ASIC. As the microcontroller is able to clock its SPI line with maximum of one quarter of its clock frequency and that the maximum SPI frequency for the ASIC is 6MHz, the optimum clock frequency is achieved by using the 24MHz provided by the ASIC (i.e. 24MHz/4 = 6MHz).

For the reset behavior of the microcontroller and ASIC, voltage supervisors are used. Such a circuit monitors the system’s supply voltage, and in case of abnormal voltage conditions, generates a long-enough reset impulse in order to assure a complete reset of the supervised system.

Concerning the firmware, Profichip® provides a sample project frame, which is used for one of their evaluation boards. The rather extensive package is written in an universal way – many different configuration options are selectable with macros, and parts of the code are activated or deactivated accordingly. Once the Profibus DP state machine is in the data exchange mode, the main user’s function is executed. The communication cycle within the main loop reads the statuses of all the valve controllers, then it
copies them into the ASIC, to make the data available for the PLC. Commands received from the PLC are copied from the ASIC into the microcontroller and then to the valve controllers. To test the card, a set of debugging levels have been programmed. The tests were designed to start with the bare minimum, and then incrementally testing bigger parts of the hardware and firmware. The new card passed all the tests. Regarding the performance, for the old version it used to take 30 to 50ms to read or write one single status page or command into one single valve controller. Now the cycle period is around 1ms. In addition, in the current system, both status pages of all sector valve controllers are read, and every of them can be written within a single cycle. In the worst case, when all valve controllers need to be read and written it will take only 1ms, instead of 880ms.

POSTER - Board: J3 / 139

Precision Timing with PbWO Crystals and Prospects for a Precision Timing Upgrade of the CMS Barrel Electromagnetic Calorimeter at HL-LHC

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The Barrel part of the CMS Electromagnetic Calorimeter is made of 61200 scintillating lead tungstate (PbWO4) crystals, read out by avalanche photo-diodes. For the high luminosity phase of the LHC, a timing measurement with a precision of approximately 10 ps can be exploited for pileup mitigation and vertex assignment. Test beam results on the timing performance of PbWO4 crystals with various photosensors and readout electronics will be shown, along with the results from simulation studies. The implications of the very precise timing requirements on the design of the new readout electronics will be discussed.

Summary:

The CMS Electromagnetic Calorimeter (ECAL) is made of 75848 scintillating lead tungstate crystals (PbWO), arranged in a barrel and two endcaps. The scintillation light is read out by avalanche photo-diodes in the barrel and vacuum photo-triodes in the endcaps. In the current on-detector electronics, the signal is amplified and then sampled at 40 MHz.

The single-channel time resolution of ECAL measured at beam tests for high energy showers is better than 100 ps. This talk will show the time resolution achieved with proton-proton collision data of the LHC. It will also discuss the main factors contributing to the measured performance by comparing the results to the time resolution obtained with laser-based monitoring data.

The precise time information from ECAL has been already exploited successfully during the LHC Run1 to extend the reach of analyses searching for physics beyond the Standard Model, such as those looking for displaced or delayed photons in the final state.

In addition, the time information is a valuable handle to mitigate the pile-up of energy deposits coming from different interactions, which deteriorate the calorimeter performance in term of energy measurement and particle identification, as individual particles appear as less isolated. This will be particularly important during the Phase2 of the LHC, when the instantaneous luminosity is expected to reach peaks of up to $5 \times 10^{34}$ cm$^{-2}$s$^{-1}$, corresponding to about 140 simultaneous events per bunch crossing.

The high level of irradiation to be sustained by the on-detector electronics and the need to cope with an increased trigger latency to preserve the trigger efficiency will require a replacement of the front-end and very front-end electronics of the ECAL for the LHC Phase2. This opens the possibility to explore new electronics design to target a precision in the time measurement of few 10 ps. Such a precise time reconstruction can be exploited to help the vertex assignment of Higgs boson particles decaying into two photons. The $x$ and $y$ coordinates of the vertex, along with the time and location of the arrival of the two photons...
in the detector, can be used to reconstruct the location of the third spatial coordinate of the vertex. With a time resolution of a few 10 ps, one achieve a performance similar to or better than the one achieved in the analysis of Higgs boson decay to photons with the LHC Run1 data.

Test beam campaigns have also been performed to investigate the ultimate time performance of PbWO crystals by looking at different photo-detector configurations and by studying the effect of the travel path of scintillation light.

Along with the aforementioned results on the time resolution achieved during the Phase1 of the LHC, the talk will present the prospects for the high luminosity phase of the LHC, and the results of the test beam R&D programs to explore the possibility of achieving a precision of few 10 ps with an upgraded CMS detector.

POSTER - Board: J5 / 144

Phase 1 Upgrade of the CMS Forward Calorimeter

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The CMS experiment at the Large Hadron Collider at CERN is upgrading the photo-detection and readout system of the forward hadronic calorimeter (HF). The phase-1 upgrade of the CMS forward calorimeter requires the replacement of the current photomultiplier tubes, as well as the installation of a new front-end readout system. The new PMTs contain a thinner window as well as multi-anode readout. The front-end electronics will use the QIE 10 ASIC which combines signal digitization with timing information. This talk will describe the major components of the upgrade as well as the current status.

Summary:

This talk describes the phase 1 upgrade of the forward hadronic calorimeter (HF) for the CMS experiment at the Large Hadron Collider at CERN. The phase 1 upgrade of HF subsystem will entail the replacement of the photomultiplier tubes on the detector, as well as the installation of a new front-end and back-end readout system. The new PMTs contain a thinner window as well as multi-anode readout, which reduce the background from anomalous signals caused by particles passing through the phototubes. The multi-anode readout of the PMTs requires additional front end readout channels, necessitating an upgrade to the front-end electronics. The front-end electronics will use the QIE 10 ASIC which combines signal digitization with timing information, which also can be used to reduce the impact from anomalous signals. The talk will describe the motivations, major components, and current status of the phase 1 upgrade.

POSTER - Board: H4 / 23

The Address in Real Time Data Driver Card for the Micromegas Detector of the ATLAS Muon Upgrade

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The ART Data Driver Card (ADDC) will be used in the ATLAS New Small Wheel (NSW) upgrade to process and transmit the Address in Real Time (ART) signals, which indicates the address of the first above-threshold event. A custom ASIC (ART ASIC) will receive the ART signals and do the hit-selection processing.

To evaluate the performance of the ADDC before the ART ASIC is fabricated, an FPGA based prototype is built. A Xilinx Artix-7 FPGA is used to emulate the ART ASIC. The bench test results of this prototype including performance and latency measurements will be described.

Summary:

The ART Data Driver Card (ADDC) is designed for the Micromegas detector in the ATLAS New Small Wheel (NSW) to transmit the trigger data from the front end ASICs to the trigger processor in the USA15. For the Micromegas detector, the trigger primitive is the Address in Real Time (ART). The ART is generated by each of the 64-channel front end ASIC (the VMM) at every bunch crossing and it is the 6-bit address of the strip with the earliest hit above a given threshold. The ADDC receives the ART signals from the front-end board, does a priority-based hit selection, and then sends the selected data to the back end trigger processor. The hit selection will be processed by a custom ASIC, the ART ASIC. Finally the GBTx ASIC and VTTx transmitter module collect data from up to 32 front end ASICs and transmit them to the trigger processors through an optical fiber link. To take advantage of the dual optical transmitter links on one VTTx module, the ADDC board is designed to handle 64 front end ASICs with 2 GBTx chips. Another ASIC of the GBT chipset, the GBT-SCA, will be used on the ADDC for configuration and control of the ART ASIC and the second GBTx.

Since the ART ASIC is not yet available, to evaluate the performance of the ADDC, an FPGA-based prototype has been built at a smaller scale. This prototype includes most of the major functional components of the final ADDC while a Xilinx Artix-7 FPGA is used to emulate the ART ASIC. This prototype has half density of the final version ADDC, with one FPGA and one GBTx chip on board, and it can handle 32 channels of ART data. Although the ART ASIC itself is not available, the design group has provided the HDL code of the ASIC in advance so we could port it in the FPGA and implement the hit-selection algorithm. Compared to the VTTx module for the final ADDC, this prototype uses the VTRx module, which has 1 transmitter for the uplink data transmission and 1 receiver for the down link configuration. Several tests have been carried out to verify the functionality and stability. The FPGA evaluation board KC705 is used to communicate with the prototype. An ART pattern generator (APG) that can emulate the ART data output of 32 VMM front-end ASICs simultaneously has been developed by the Harvard group. In the integration test, Micromegas hits from an ATLAS New Small Wheel simulation are fed into the APG, the FPGA based ADDC prototype receives and processes the 32-channel ART data, and the results are sent to the MM trigger processor prototype. The evaluation test results of the integration readout chain, including reliability studies, latency and overall performance will be reported.

**POSTER** - Board: L3 / 159

**Performance and Advantages of a Soft-Core Based Parallel Architecture for Energy Peak Detection in the Calorimeter Level 0 Trigger for the NA62 Experiment at CERN**

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The NA62 experiment at CERN SPS has began its data-taking. Its main topic is to reduce uncertainties in the branching ratio of the ultra-rare decay $K^+ \rightarrow \pi^+ \nu \bar{\nu}$. In this context rejecting the background is a crucial topic. The Cal-10 trigger get energy deposit from the calorimeters to suppress decays with $\pi^0$ and muons in the final state. In this work we present the performance of a soft-core based parallel architecture build on FPGAs for the energy peak reconstruction as an alternative to an implementation completely founded on VHDL language.
Summary:

The NA62 experiment at CERN has began this year the data-taking phase scheduled until the next accelerator’s second long shutdown in 2018. The experiment was designed to check the validity of the Standard Model in the region of most suppressed processes involving flavour-changing neutral currents (FCNCs). In particular its main topic is to improve the precision in measuring the branching ration of the ultra-rare decay \( K^+ \rightarrow \pi^+ \nu \bar{\nu} \) using a detectors ensemble to identify and tracks the particles. Among the others detectors involved, several electromagnetic calorimeters are used to suppress the background related to decay \( K^+ \rightarrow \pi^+ \pi^0 \) while the background with muons in the final state is suppressed by a set of 3 hadronic calorimeters. This work focuses on the calorimenter level 0 trigger (Cal-l0) that works on three electromagnetic calorimeters (the Liquid Kripton (LKr), the Small Angle (SAC) and the Intermediate Ring (IRC)), and two hadronic calorimeters (MUV1 and MUV2). The Cal-l0 is a sequence of three connected layers. The first layer, made of 29 electronic boards, collects the data coming from the calorimeters and detects the energy peak underlying parametrized constrains. Most of the first layer, 28 boards each one corresponding to a vertical slice of the LKr calorimeter, sends detected peaks to the second layer. It is made of 7 boards, each one merges information coming from 4 Lkr slices and send the aggregated information to the last level. The third layer aggregates all the information received from the second layer and from the IRC, SAC, MUV1, MUV2 board and sends it to the central level 0 trigger processor. In particular we preset the performances of the peak detection implemented in the firmware using only the VHDL language, as it is now, compared to those one of a parallel architecture of soft-core processor implemented on FPGAs. This solution adds flexibility and simplify the algorithm implementation because of the use of C language to program the soft-core processors and takes advantage of digital signal processing (DSP) blocks available on last generation FPGAs.

POSTER - Board: M1 / 155

Performance and Operation of the Calorimetric Trigger Processor of the NA62 Experiment at CERN SPS

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The NA62 experiment aims to measure the branching ratio of the rare kaon decay \( K^+ \rightarrow \pi^+ \nu \bar{\nu} \) at the CERN SPS. The calorimeter L0 trigger is the part of the TDAQ used to select events with a \( \pi^+ \) in the final state hadronic and to veto one of the most dominate background from events \( K^+ \rightarrow \pi^+ \pi^0 \). It has been developed and installed (it has taken first physics data in autumn 2014). We present the design, performance and operation during the last two years (2015 and part of 2016) high intensity data taking of the calorimeter Level 0 trigger.

Summary:
The goal of the NA62 experiment is a precision measurement of the branching ratio of the ultra-rare kaon decay $K^+ \rightarrow \pi^+ \nu \bar{\nu}$ with 100 expected events and 10% background. Since a high-intensity kaon beam is required to collect enough statistics, the L0 trigger plays a fundamental role in both the background rejection and in the particle identification. For this reason, a complex Trigger and Data Acquisition (TDAQ) system has been designed. This is divided into three different main levels: a hardware trigger (Level 0) and two software levels (Level 1 and Level 2). In particular, the Level 0 Calorimeter (Cal-L0) Trigger is a parallel system based on TEL62 cards able to identify clusters from different calorimeters: electromagnetic (LKR, IRC and SAC) and hadronic (MUV1 and MUV2). The Cal-L0 trigger receives digitized data from all detectors readout through the Calorimeter READout Modules (CREAM) and it performs trigger algorithms, sends trigger primitives to the L0 Trigger Processor, and sends filtered calorimeter raw data to the DAQ system. The Cal-L0 trigger outputs consist of a time-ordered list of the reconstructed clusters together with the arrival times, positions, and energy measurements. The system has been designed to sustain the instantaneous hit rate of 30 MHz, to process data with a maximum latency of 100 us, and to achieve a time resolution of 1.5 ns on the single cluster. These boards are arranged in three different layers of boards: Front-End, Merger (only for LKR calorimeter) and Concentrator. The Front End boards receive trigger sums from the CREAM, perform peak searches in space and compute time, position and energy for each detected peak. The Merger boards (only used for the LKR) receive trigger data from the Front-End boards and merge peaks from different Front-End boards into single clusters. Finally, the Concentrator boards receive reconstructed clusters from the five NA62 calorimeters, perform cluster counting, calculate sums for electromagnetic and hadronic energy and generates trigger primitives for the L0 Trigger Processor. The whole Calorimeter trigger system is composed of 37 TEL62 boards, 185 mezzanine cards and 221 high-performance FPGAs. These boards are arranged in three different layers of boards: Front-End, Merger (only for LKR calorimeter) and Concentrator and each of them is controlled by an on-board PC with fast Ethernet connection.

The system was installed and has started to take the first physics data in autumn 2014. In this contribution we present the architecture of the Cal-L0 trigger processor with particular emphasis on the performances and the operation during the 2015-16 high intensity data taking for the photon veto in the 1-8.5 mrad decay region.

POSTER - Board: L8 / 163

Development of Network Interface Cards for TRIDAQ Systems with the NaNet Framework

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NaNet is a framework for the development of FPGA-based PCI Express (PCIe) Network Interface Cards (NICs) with real-time data transport architecture that can be effectively employed in TRIDAQ systems.

Key features of the architecture are the flexibility in the configuration of the number and kind of the I/O channels, the hardware offloading of the network protocols stack, the stream processing and the zero-copy RDMA (for both CPU and GPU) capabilities.

Three NIC designs have been developed with the NaNet framework for the CERN NA62 L0 trigger and for the KM3NeT-IT underwater neutrino telescope DAQ system.
Summary:

NaNet is a framework for the development of FPGA-based PCI Express (PCIe) Network Interface Cards (NICs) with real-time data transport architecture that can be effectively employed in TRIDAQ systems. Key features of the architecture are the flexibility in the configuration of the number and kind of the I/O channels, the hardware offloading of the network protocols stack, the stream processing and the zero-copy RDMA networking capabilities. Zero-copy RDMA is supported for both CPU and GPU (nVIDIA GPUDirect). Three different NIC designs have been developed with the NaNet framework for use in the low level trigger of the CERN NA62 experiment (NaNet-1 and NaNet-10) and in the DAQ system of the KM3NeT-IT underwater neutrino telescope (NaNet^3). Being the most complete of the three in terms of capabilities, we will focus our description on the NaNet-10 design. Since the beginning of 2016 NaNet-10 has been integrated in the NA62 experiment to implement a GPU processing stage for the real-time generation of refined RICH detectors primitives in order to increase the background trigger rejection and the trigger purity for additional rare decay channels selection.

The target FPGA-based board for this design is the Terasic DE5-NET. It hosts an Altera StratixV device and allows the integration of up to four 10GbE channels plus a PCIe Gen2/3 x8 host interface. We implemented the 10GbE channels using both 10GBASE-R and 10GBASE-KR standards to have a wide device compatibility.

Along with the MAC layer we added a complete hardware UDP/IP protocol offloader, enabling minimal latency and full bandwidth for the data channel. From an architectural point of view, NaNet-10 is a real-time, multiple stream processing system realized through a functional pipeline of hardware blocks executing different tasks on the data streams. Current partition shows 1) 10GbE interface with UDP transport protocol support (UDP_INTF), 2) highly customizable data manipulation block (STREAM_PROC) and 3) low latency, high throughput RDMA-based host/GPU interface (NETWORK_INTF). The UDP_INTF handles the data coming from multiple UDP streams (four in the NA62 RICH detector) and multiplex them in a single channel while the NETWORK_INTF integrates a low latency GPUDirect RDMA hardware engine able to directly inject data in CPU and/or GPU memory.

The STREAM_PROC block is currently customized for the NA62 RICH detector data protocol and executes a sequence of different tasks on the multiple data streams received through the UDP_INTF, eliminating the need of time-costly data re-ordering in GPU memory. In particular its first stage performs a decompression on the stream data coming from the RICH read-out channels; its second stage reformats the decompressed data to get a "GPU-friendly" alignment of data structures in memory; its last stage executes a time alignment of the different data streams to a common timestamp and produces a single, merged, GPU-aligned stream of the data coming from the entire RICH detector.

POSTER - Board: M9 / 131

L-1 Trigger System for Electromagnetic Calorimeter of COMET Experiment

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The COMET detector will include a electromagnetic calorimeter (ECal). The ECal signals will used for energy deposition measurement and for triggering. For triggering, the calorimeters signals will transformed into special short-shaped analog signals. These signals will then digitally processed with special algorithm, which allows one to obtain a set of logic signals necessary for event selection and a time-tag signal for time alignment of time measurements.
Summary:
The COMET Phase-I experiment is seeking to measure the neutrinoless, coherent transition of a muon to an electron (\(\mu^+\to e^-\)) conversion in the field of an aluminium nucleus, \(\mu^-N \to e^-N\), with a single event sensitivity of \(3.1 \times 10^{-15}\).

The COMET detector will consist of several subsystem, one of each will be electromagnetic calorimeter (Ecal). The Ecal system will consists of segmented scintillating crystals (LYSO). It is placed down-stream of the straw chamber detector and serves the following three purposes: to measure the energy of electrons (E) with good resolution, to add redundancy to the electron momentum (p) measurement and to provide the ratio \(E/p\) for electron identification. The Ecal will also provide an additional hit position to the electron track trajectory at the location of the Ecal, to cross-check the tracker-based electron trajectory. The Ecal also provides the trigger signals, carrying the timing with respect to which the electron events are referenced. Independent and redundant measurements of the energy of electrons are of critical importance to separate true signals of \(\mu^-N \to e^-N\) conversion from background tracks that conspire to mimic a signal.

For the photon readout will used avalanche photodiodes (APDs) with typical gains of 50–100. Due to lower gain of APDs compared with that of SiPMs, fast and low noise analogue electronics is required to amplify the APD signal. A preamplifier board was developed. The amplifier output is designed to be differential so that the signal can be transmitted over relatively long distances without suffering from noise. The front-end preamplifier board has 16 channel charge sensitive preamplifiers (CSPs) for the readout and 4 channel analog adders for the trigger.

The ECAL consists of up to 2400 crystals in an approximately circular array. The trigger is required to give a good time resolution (to keep the readout windows around the trigger time as narrow as possible) and good energy resolution (so as to select energy clusters in the signal region rather than background). Since the energy deposition can be divided among couple crystals, it is necessary to do the summation. On the other hand, at \(E \sim 100\text{MeV}\), if from the entry point of particle to the boundary of the summation area is at least one crystal, then almost all energy will be summed. Thus, if we take the sum of 4x4 crystals, when the particle enters in the middle 2x2 crystal, effectively all the energy will be taken into account. It is therefore proposed to select the basic trigger unit (cell) the group of 2x2 crystals (corresponding to one crystal module of the ECAL), and to determine the total energy by using the sum of an array 2x2 trigger cells (i.e. 4x4 crystals). All possible combinations of the sums 2x2 trigger cells will calculated and the maximum energy found in one of these combinations will be used. Now this algorithm is implemented in pre-trigger board FPGA and successfully tested.

POSTER - Board: M7 / 129

ALICE Trigger System in RUN3

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ALICE is the detector at the CERN LHC dedicated to the study of strongly interacting matter. The collaboration plans a major upgrade of the detector in RUN3. The interaction rates will increase to about 50 kHz for Pb-Pb and few hundred kHz for pp. The aim of the ALICE trigger system is to select essentially all of these interactions. The events are read out and the event records are sent to the HLT farm for further filtering. The combination of continuous readout detectors and a minimum bias trigger is used. The overview of the ALICE trigger system is presented.

Summary:
ALICE trigger system in RUN3

R.Lietava for ALICE collaboration

ALICE (A Large Ion Collider Experiment) is the detector at the CERN LHC dedicated to the study of strongly interacting matter. The ALICE collaboration plans a major upgrade of the detector during long shutdown 2, which is at present foreseen to start at the end of year 2018 followed by Run 3 starting in
In Run 3 the interaction rates will increase to about 50 kHz for Pb-Pb, and few hundred kHz for pp and p-A. The aim of the ALICE trigger system is to select essentially all of these interactions; the events are then read out and the event records are sent to the HLT farm for further filtering. To achieve this, the combination of continuous readout detectors and a minimum bias trigger based on the new forward detectors is used, with a few additional inputs to allow for cosmic triggers and calorimeter based triggers to enhance rates for some types of events where the minimum bias trigger is inefficient. The overview of the ALICE trigger system is presented.

FPGA Based Algorithms for the New Trigger System for the Phase 2 Upgrade of the CMS Drift Tubes Detector

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The Phase 2 upgrade of the CMS Drift Tubes detector aims at moving all the readout and trigger electronics from the inner detector to outside the cavern. Trigger algorithms need to be redesigned to handle direct timing information and remove present bottlenecks of resolution and deadtime, approaching to present high level trigger performance. In the present contribution we describe the work that has been performed to emulate the firmware that process 1 ns TDC hits from one DT chamber with the combinatorial problematic of the arrival time uncertainty in a detector with up to 400 ns of drift time.

Summary:

A fundamental task of the CMS (Compact Muon Solenoid) detector is its ability to trigger on and reconstruct muon tracks at high luminosities. This task is performed by various detectors, among them, the DT (Drift Tube) chambers, and maintaining this capability is fundamental during the HL-LHC (High Luminosity LHC) era.

DT Chambers are made of three super layers each consisting of four layers of rectangular drift tube cells, staggered half-width. When a charged particle crosses one cell, it ionizes the gas and the electrons drift at constant velocity to the anode wire. Accordingly, there is a linear relation between the time measurement of the incoming signals (hit) and the muon track position. Due to the particular cell’s arrangement it’s possible to use that time from, at least, 3 cells to apply a mean-timer algorithm to calculate track angle and chamber crossing point and the LHC beam bunch-crossing to which muon hits belong to.

DT electronics will be redesigned due to radiation and maintenance constrains. The new electronics will substitute present on detector electronics with a simplified system in charge of hit time measurement and optical transmission. All the trigger algorithms will be implemented in the FPGA-based back end electronics, which will produce trigger primitives. This new system will allow to improve the hit resolution used in the DT trigger and reduce the single hit dead-time.

In this contribution we present the hardware oriented software algorithm that has been developed in C++ to validate the implementation of the mean-timer paradigm based on the foreseen architecture of the future electronics. The algorithm developed is capable of building muon trajectories and reject background signals producing trigger primitives with bunch crossing identification. Moreover, it also gives a quality level to each accepted track.

In order to be easily translated into a firmware code, its internal architecture is distributed in a parallel way, using software-processing threads, imitating the intrinsic FPGA parallel behaviour. Syntactically complex expressions difficult to be converted into VHDL code have also been avoided. To simulate
variations in the arrival time of incoming DT hits, C++ classes working as FIFOs, ring buffers, etc, ... have been implemented.

The algorithm needs to reproduce the expected system hardware and thus it is responsible of unmixing groups of hits received from each optical link and rearrange them into candidate packages. This unmixing and mixing procedure is one of the main challenges of the proposed architecture, because it can easily grow into an exponential combinatorial explosion. It is important to note that the maximum cell drift time is 400 ns and the bunch crossing separation is 25 ns, so hits need to be stored for a significant amount of time and combined with a possible large number of signals which are received for the duration of the drift time.

The algorithm has been validated with muon candidates, demonstrating good agreement with the generated data, being able to reconstruct bunch crossing, angle and position with good precision.

POSTER - Board: M3 / 69

A High Bandwidth and Versatile Advanced MC Board, TRB_v1

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We developed a new AMC board based on AMC.0, named as Trigger Receiver Board (TRB). TRB is a high bandwidth data-stream processor, using a Xilinx Artix-7 and 2 Kintex-7 FPGA. The Artix-7 takes care of the backplane connection while the Kintex-7s handle the front panel optical links. There are 17 optical links on the front panel, making a total bandwidth up to 150Gbps both in and out. On the backplane side, we implemented 2 Gigabit Ethernet and 8 multi-gigabit transceiver links communicating with the MCH and redundant MCH.

Summary:

Nowadays many particle and nuclear physics experiments are planning to use the micro-TCA or the ATCA standards for their Trigger and Data Acquisition (TDAQ) system. In most of these experiments the first stages of the TDAQ system are based on FPGA-based hardware architecture to select events of interest and suppress background to an acceptable level for the DAQ system. Future projects or experiment upgrades always require larger data throughput, larger number of high speed (optical) Input/Output and much more sophisticated trigger algorithms with longer latency. The micro-TCA and the ATCA standards, with their FPGA-based boards, respond to those requirements. These experiments are also built to run over many years, even up to a couple of decades. Maintenance of the electronics may become an issue and it is therefore of interest to limit the use of many different custom-made electronics boards. Since a couple of years, several evaluation platforms or “generic” micro-TCA boards (AMC) have been introduced.

Last year we made a poster, introduced the prototype version, based on AMC.0 named as Trigger Receiver Board (TRB) version 0. In this contribution we will present the formal version TRB_v1. Compared to TRB_v0, TRB_v1 significantly increased the bandwidth and data processing ability. TRB_v1 has 17 optical links on the front panel (1 pair Avago miniPOD, 1 QSFP and 1 SFP) which can receive data from front-end electronics system with bandwidth up to 150 Gbps. There are 2 gigabit Ethernet links and 8 multi-gigabit transceiver links communicating with the MCH and redundant MCH through backplane, building up the DAQ and slow control path. Among the 3 FPGAs, there are hundreds high speed LVDS signals connected. The 2 Kintex-7s receive data and compress it, then send to the Artix-7. The high level algorithm running on Artix-7 will process the data and send to DAQ though the backplane.

In this contribution we will report the first performance results obtained with this new version and possible applications in particle physics experiments.
Study of Hardware Implementation of Fast Tracking Algorithms

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Real-time track reconstruction at high event rates is a major challenge for future experiments in high energy physics. To perform pattern-recognition and/or track fitting, artificial retina or Hough transformation have been introduced in the field which have to be implemented in the FPGA firmware. In this contribution, we will report on a possible FPGA hardware implementation of retina algorithm based on the Floating-Point Operator IP. Detailed measurements with the algorithm are investigated. Retina performances and capabilities of the FPGA are discussed along with perspectives for further optimizations and for future applications.

Summary:

The artificial retina tracking algorithm based on the vision mechanism in mammals, is a possible solution for fast, massively parallel, track reconstruction. The vision mechanism is able to process the huge amount of data collected from the environment, using neurons to recognize specific patterns in the acquired images. Similarly, this retina algorithm can recognize specific track characteristics from a multilayer detector data flow, comparing the detector hits with stored patterns (discrete parameter space), processing exponential function, performing weighed sum of the "distance" of the track from the patterns (engine) and identify local maxima response among different patterns. Our approach follows the current trends of industry using high-speed, high-bandwidth FPGA devices. Fast tracking algorithm in a realistic FPGA architecture poses two technical challenges: (1) LUTs are able to be used for the calculation of the distance and the exponential function. This kind of efficient implementation costs lower latency, more logic resources and limitation of data precision. (2) It is very convenient to use Floating-Point Operator IP for exponential function in real time track finding. The IP core provides arithmetic operators that can be targeted to any of the latest Xilinx FPGA. We developed retina algorithm based on the Floating–Point Operator IP with AXI4-stream interface. We developed retina algorithm based on the Floating–Point Operator IP with AXI4-stream interface. In order to test the implementation of the algorithm, a series of detailed measurements were taken. We also compared pure logic implementation with the use of DSP blocks. In both schemes, the measurements were performed with a mass of engines computing in parallel. Then we compared the total latency and resources of retina in various system clocks. Moreover retina was also tested on different hardware platforms including Arduino and Kintex-7. We focus the study on the possibility of retina algorithm implementation and optimization between latency and resources. From above, retina is based on a massively parallel calculation and suitable for implementation in FPGAs with a pipelined architecture. The algorithm is very flexible in terms of calculation process and latency so that better performance can be achieved. These results are encouraging and represent a first step towards the development of a fast efficient track-fitting system for applications in future experiments at high luminosity. However in real experiments, the geometry of the detector and the topology of the events may be quite complicated. And in some cases the Hough transformation seems more adequate. This aspect will also be discussed.
This report describes the Tile-Muon Trigger within the TileCal upgrade activities, focusing on the new on-detector electronics such as the Tile Muon Digitizer Board (TMDB) providing (receive and digitize) the signal from eight TileCal modules to three Level-1 muon endcap sector logic blocks.

Summary:
The Tile Calorimeter (TileCal) is the central hadronic calorimeter of the ATLAS experiment at the Large Hadron Collider (LHC). The TileCal provides highly-segmented energy measurements for incident particles. Information from TileCal’s last radial layer can assist in muon tagging in the Level-1 muon trigger by rejecting fake muon triggers arising from background radiation (slow charged particles - protons) without degrading the efficiency of the trigger. The TileCal main activity for the ATLAS Phase-0 upgrade program (2013-2014) was the activation of the TileCal third layer signal for assisting the muon trigger at 1.0<||<1.3 (Tile-Muon Trigger).

Implementation of the data acquisition system for the Overlap Modular Track Finder in the CMS experiment

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The Overlap Muon Track Finder (OMTF) is the new system developed during the upgrade of the CMS experiment. It uses the novelty approach to find muon candidates basing on data received from three types of detectors: RPC, DT and CSC. The upgrade of the trigger system requires also upgrade of the associated Data Acquisition (DAQ) system, that must transmit the data from the RPC detector, but for continuous monitoring of the OMTF, it should also transmit the data from the CSC and DT detectors. The paper describes the technical concepts and solutions used in the currently developed OMTF DAQ system.

Summary:
The CMS experiment is currently undergoing the upgrade of its trigger, including the Level-1 muon trigger. In the barrel-endcap transition region the Overlap Muon Track Finder (OMTF) combines data from three types of detectors (RPC, DT, and CSC) to find the muon candidates.

To monitor the operation of the OMTF, it is important to receive the data which were the basis for the trigger decision. This task must be performed by the Data Acquisition (OMTF DAQ) system.

The new MTCA technology applied in the updated trigger allows implementation of the OMTF DAQ together with the OMTF trigger in the MTF7 board. Further concentration of data is performed by standard AMC13 boards.
The proposed data concentration methodology assumes parallel filtering and queuing of data arriving from all input links (24 RPC, 30 CSC, and 6 DT). The data are waiting for the trigger decision in the input buffers. The triggered data are then converted into the intermediate 72-bit format and put into the sorter queues. The block responsible for the building of events receives data originating from the particular Bunch Crossing (BX) from the consecutive sorter queues, converts them to the 64-bit AMC payload words, and puts them into the output queue. That block also generates the AMC header at the beginning and the AMC trailer at the end of the event data.

The system is implemented in a flexible way, and handling of a new data source requires implementation of two specialized blocks: the input data formatter to translate the link data into the sorter queue data and the output data formatter to translate the sorter queue data into the AMC payload.

The AMC payload format used by the OMTF DAQ provides bit field allowing the context-free detection of the data source.

The system may send data not only from the bunch crossing (BX) in which the L1 trigger was generated but also from a configurable number of BXs before the trigger (up to 3) and after the trigger (up to 4). Therefore, according to the current trigger rules, it is possible that the data from a certain BX may belong to two different events. To handle such cases the OMTF DAQ system uses two output queues alternately for assembling the consecutive events. It is easily possible to increase the number of output queues if a single BX may belong to a higher number of events due to the change of the trigger rules or number of BX-es transmitted before or after the trigger.

The system in current state handles the RPC data. The data handlers for CSC and DT detectors are being developed. The presented methodology may be reused for other triggered DAQ systems concentrating data from various sources with different formats.

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**CMOS Image Sensors in Harsh Radiation Environments**

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CMOS Image Sensors (CIS) have become the main solid state image sensor technology for visible imaging applications. Despite the higher radiation hardness of CIS compared to its CCD counterpart, there are still demanding applications where CMOS imager performances can be significantly reduced by high energy particles. This is the case for the most severe radiation environments where imaging capabilities are required: particle physics, nuclear fusion, nuclear power plants...

After a brief overview of the CIS technology and the review of basic degradation mechanisms in harsh radiation environments, mitigation techniques will be discussed and recent developments will be used as illustrative examples.

ASIC / 168

**SAMPA Chip: the New ASIC for the ALICE TPC and MCH Upgrades**

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This paper presents the SAMPA, a new ASIC for the ALICE upgrade for Time Projection chamber (TPC) and Muon chamber (MCH) read-out frontend electronics. The SAMPA ASIC is designed in 130nm CMOS technology with 1.2V nominal power supply. SAMPA includes 32 channels, with selectable input polarity, and three possible combinations of shaping time and sensitivity. Each channel comprises a Charge Sensitive Amplifier, a shaping stage, and a 10-bit ADC. A DSP block and 11 SLVS output links (throughput up to 3.2 Gbps) complete the chip. Experimental results of the first complete ASIC prototype will be presented.

Summary:

Operating the ALICE TPC (Time Projection Chamber) at a Pb-Pb collision rate of 50 kHz requires to replace the present MWPC based read-out by GEM detectors, which feature intrinsic ion blocking without additional gating and exhibit excellent rate capabilities. As the drift time is higher than the average time between interactions, a trigger-less continuous read-out is required, which is not supported by the present front-end electronics. Also in the case of the Alice Muon Chambers (MCH) detector, the present front-end electronics installation does not cope with the future (higher interaction rate) running conditions and needs to be replaced. Thus, the new read-out ASIC, named SAMPA, is developed to serve both the TPC and Muon Chamber read out.

The SAMPA ASIC integrates 32 channels of the full data processing chain, it is designed in TSMC 130 nm CMOS technology with nominal voltage supply of 1.2 V and it supports continuous and triggered read-out. The SAMPA consumes an area of about 86 mm$^2$. It comprises positive/negative polarity Charge Sensitive Amplifiers (CSA), which transform the charge signal into a differential semi-Gaussian voltage signal, which is then digitized by a 10-bit 10 Msamples/s ADC. After the ADC, a digital signal processor allows baseline shifts correction and zero suppression; unprocessed direct throughput of the full data stream is also possible. The data read-out takes place, either continuously or in triggered mode, by enabling up to eleven 320 Mbps SLVS serial links, allowing a data throughput of up to 3.2 Gbps.

The CSA shaping time can be configured to operate at 160 ns, with sensitivity of 20 mV/fC or 30 mV/fC (TPC case), or at 300 ns, with a sensitivity of 4 mV/fC (MCH case).

Second SAMPA submission included the fist complete designed ASIC chip and a set of mini-chips containing the different functional sub-blocks (analog stage, ADC, SLVS drivers, etc.). Results of the tests performed on both the functional blocks and on prototypes from the first complete ASIC will be presented, and compared with the simulation results. The chip performance and specifications will be fully discussed.
The CMS experiment at the LHC will deploy the first large (16k channel) silicon photomultiplier system in a high radiation environment as the central feature of its hadron calorimeter upgrade. The exceptional 35% photon detection efficiency of the SiPMs is critical for ameliorating the effects of radiation damage of the calorimeter scintillator. The SiPM signals are digitized by the QIE11 ASIC which provides a 1% energy measurement over a 17-bit dynamic range. We will describe the performance and radiation tolerance of the entire system, focusing on the SiPMs, the precision control electronics, and the QIE11-based readout.

Summary:

The CMS experiment at the CERN LHC will deploy the first large (16k channel) silicon photomultiplier system in a high radiation environment as the central feature of the upgrade of its hadron calorimeter, which will be partially installed during winter 2016-2017 and will be completed during the second long shutdown of the LHC in 2019.

The exceptional 35% photon detection efficiency of the SiPMs, along with their small size allowing for a more granular depth readout, is critical for ameliorating the effects of radiation damage of the calorimeter scintillator. The devices are radiation tolerant up to levels higher than expected at the LHC, and the dependence of the dark current on the total fluence is well understood. The SiPMs have excellent uniformity across many devices, with a 1% spread in the gain times photon detection efficiency.

The SiPM control electronics provide precise bias voltage with only 0.5% peak-to-peak variation, a large maximum operating current of 500 \( \mu A \), and 0.1°C temperature control.

The SiPM signals are digitized by the 11th generation of the QIE ASIC family, which provides a deadtimeless energy measurement with 1% resolution over a vast 17-bit dynamic range. The QIE11 measures the signal arrival time with 0.5 ns precision, has a programmable gain, and features internal phasing of the integration window relative to the input clock in 0.5 ns steps across a 25 ns window. With a radiation tolerance of up to 250 krad of total integrated dose and up to \( 1 \times 10^{13} \) MeV-equivalent neutrons/cm\(^2\), the QIE11 is well suited for the radiation environment of the CMS hadron calorimeter.

We will describe the performance and radiation tolerance of the entire system, which was produced in spring and summer of 2016, with focus on the SiPMs, the precision control electronics, and the QIE11 readout. We will also include plans for initial calibration, response monitoring, and operation of the system, which will be used from 2017 onwards and throughout the HL-LHC era.
The data acquisition system (DAQ) for a highly granular analogue hadron calorimeter (AHCAL) for the future International Linear Collider (ILC) will be presented. The developed DAQ chain has several stages of aggregation and scales up to 8 million channels foreseen for the AHCAL detector design. The largest aggregation device, LDA (Link data aggregator), has 96 HDMI connectors, four Kintex7 FPGAs and a central Zynq SoC (System-On-Chip). Architecture and performance results will be shown in detail. Experience from CERN testbeams with a small detector prototype consisting of 15 detector layers will be reported.

Summary:

The CALICE (CALorimeter for Linear Collider Experiment) collaboration is developing highly granular calorimeters, which are needed for particle flow reconstruction. AHCAL (Analog Hadron CALorimeter) group is developing a steel sandwich calorimeter option, which uses individually read out 3x3x0.3 cm³ scintillator tiles with SiPMs (Silicon PhotoMultipliers). This corresponds to 4 millions channels just in the HCAL barrel. The front-end electronics is embedded in the detector layers in between the absorber plates without active cooling. Given the ILC (International Linear Collider) beam structure (<1 ms of collisions followed by 199 ms readout), the electronics use a power pulsing scheme which cuts the power consumption down to ~2%.

The DAQ was developed from scratch to adopt the ILC timing. It is organized in a cascade of components: 1) the SPIROC ASIC, which reads out 36 channels, stores up to 16 events in analog memory cells and digitizes the stored information; 2) the DIF (Detector InterFace), which reads out 72 ASICs from one detector layer; 3) the LDA (Link Data Aggregator), which reads out up to 96 DIFs and sends the data out over Gigabit Ethernet; 4) the CCC (Clock and Control Card), which controls all 16 LDAs in the barrel. Given the ILC scenario duty cycle, the bandwidth of the LDA does not exceed 85 MB/s, even with 100% hit occupancy. Taking into account the auto-trigger nature of the ASIC, which records and sends data only from actual physics hits, the data rate during physics data taking is expected to be lower.

The recently developed aggregation device, the Wing-LDA, contains 4 Kintex7 Xilinx FPGAs and a Zynq SoC (System-on-Chip). The processor part is running Linux and the data is transferred using a DMA (Direct Memory Access) between FPGA and Linux memory, from where it is streamed to Gigabit Ethernet using the TCP protocol. The link between the LDA and individual detector layers is based on HDMI physical connectors and cables with 10MBit/s serial protocol. The links between FPGAs are based on dual 400 Mbit/s serial lines implemented in user logic, encoded in 8b10b and secured by a CRC16 packet checksum with retransmission in case of an error.

The DAQ was tested in beam for the first time in the configuration which is foreseen for the ILC in terms of DAQ hierarchy. It has been tested several times with up to 15 detector layers instrumented with up to about 4000 channels in total. Main tests were done in 2014 and 2015 in test beams at CERN and DESY, where it was operated in a sparse continuous beam (in contrast to the ILC beam structure). The continuous beam then requires to read out and restart as fast as possible. The DAQ finally achieved ~17 readout cycles per second in the beam tests. When recent speed improvements are taken into account, the extrapolated DAQ performance already fulfills the requirements of the fully instrumented AHCAL barrel operated in the ILC mode, even with 100% hit occupancy.

ASIC / 98

SKIROC2_CMS : an ASIC for testing CMS HGCAL

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SKIROC2_CMS is a chip derived from CALICE SKIROC2, providing 64 channels of low noise readout for 50pF Si-sensors over 10pC dynamic range. The pre-amps are followed by high/low gain 25ns shapers, 16-deep 40 MHz analog memory “waveform sampler” and 12-bit ADCs. A fast shaper followed by discriminator and TDC provide timing information to an accuracy of 50 ps, in order to test TOT and TOA techniques at system level. The chip, in AMS SiGe 0.35um, is expected in May. It will be tested and used for beam tests in the autumn.

Summary:

The high granularity silicon tungsten calorimeter (HGCAL) chosen by the CMS collaboration to replace its endcaps for the phase 2 upgrade will provide unprecedented 5D images of electromagnetic showers. The sensors are made of ~1cm² PIN diodes of 100-300um thickness providing a MIP signal around 1-4 fC. With 6 million channels of low noise, high speed and large dynamic range readout electronics embedded on detector, the front-end ASICs are very challenging and innovative. In particular, they will provide charge measurement for large signals by a time over Threshold technique (TOT) and will also measure the time of arrival (TOA) to 50 ps. System issues are very critical in such a design and an important testbeam campaign has been programmed by the collaboration to validate the design and performance. For this reason, it has been decided by the collaboration to start the tests early enough with an existing chip. The first modules were tested in beam at FNAL in April and use SKIROC2, which has been used for more than 5 years by the CALICE collaboration to test a similar calorimeter, but at lower speed and occupancy. Moreover, the timing capability of the sensors, down to 20 ps, provide powerful information for physics analysis and background mitigation. Therefore a pin-pin compatible variation of the chip tailored to CMS needs was submitted in January in an engineering run. It keeps the same architecture with variable gain preamps and variable shaping time dual-gain shapers, which were accelerated to 25 ns. The analog memory was modified to run at 40MHz and provide waveform sampling, this can be used to study timing performance independently and study possible pulse shape variations.

The other modifications concern the timing branch, where the fast shaper was accelerated to 5 ns. Two discriminators provide ToA and ToT informations, thanks to a TDC based on a time-to-amplitude converter with a step of 25 ps. Charge and time are then encoded with the same 12 bits ADCs as in SKIROC2 and read out following the same protocol, so that the chip can replace directly SKIROC2 on the testbeam modules and interface to the DAQ. Simulation results indicate a noise below 2000e- for 50 pF detector capacitance and timing accuracy below 50 ps above 10 MIPS. Power dissipation is below 15 mW/channel. Around 800 HARDROC3 were produced in 2015. The overall performance and production tests will be detailed.

ASIC / 68

HARDROC3, a 3rd generation ASIC with zero suppress for ILC Semi Digital Hadronic Calorimeter

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HARDROC is the very front end chip designed to readout the Resistive Plate Chambers foreseen for the Digital HADronic CALorimeter (DHCAL) of the future International Linear Collider. The very fine granularity of the calorimeter implies thousands of electronics channels per cubic meter which is a new feature of “imaging” calorimetry. Moreover, for compactness, chips must be embedded inside the detector making crucial the reduction of the power consumption down to 12 μW per channel. This is achieved using power pulsing and online zero-suppression. Around 800 HARDROC3 were produced in 2015. The overall performance and production tests will be detailed.
Summary:

HARDROC (HAdronic Rpc Detector ReadOut Chip) is a very front end chip to readout Resistive Plate Chambers. It integrates a semi-digital readout with three thresholds which enables both good tracking and coarse energy measurement.

The first release of this chip (HARDROC2) was produced in large quantities (10,000 samples) to be able to equip around 50 GRPC layers. This chip was extensively tested with cosmics and also in testbeam at CERN to evaluate the performance and to validate the semi-digital electronics readout system in beam conditions.

Major modifications have been integrated in HARDROC3 to make the channels independent using a zero-suppress architecture. Only hit channels are read out to optimize the data rate and to lower the power consumption. Moreover, the dynamic range has been extended up to 30 pC (10 pC in HARDROC2). HARDROC3 is the first 3rd generation chip designed within the CALICE collaboration.

The chip integrates 64 independent channels and also an I2C link (designed by IPNL Lyon) to load the slow control parameters. Each of them has been triplicated for redundancy with triple voting cells. Each channel is made of a variable gain current preamplifier with a low input impedance to minimize the crosstalk. This variable gain is used to reduce the dispersion between channels thanks to a tuning going up to a factor 2 with an accuracy of 1% over 8 bits. This gain tuning is also convenient to switch off a noisy channel.

The amplified current feeds then two paths:

- A slow shaper path for debug which consists of a CRRC2 shaper and a Sample and Hold buffer.
- Three variable fast shapers (Peaking time 20ns) followed by 3 discriminators. The 3 thresholds are set by 3 internal 12 bit counters. The output is latched to hold the state of the discriminators that is sent to the digital part through a 3 to 2 encoder.

For each channel, the 3 trigger outputs are OR wired to generate a signal to start the memorization of the encoded trigger outputs as well as the Bunch Crossing Identification (BCID) delivered by a 12 bit counter. Therefore, there is one memory per channel ensuring the independence of each channel.

The power consumption is 2.5 mW/channel and can be minimized down to 12 µW/channel thanks to a power pulsing mode (0.5% duty cycle).

A temperature sensor has been integrated as well as a PLL to generate fast clocks internally if needed.

A production of HARDROC3 was launched in 2015 to be able to equip large RPC detectors (1m2). Around 800 chips were successfully tested with a robot.

The overall performance of this new HARDROC3 will be described with detailed measurements of all the characteristics. The improvements compared to the previous chip will be highlighted.

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The SoLid anti-neutrino detector’s read-out system

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The SoLid collaboration have developed an intelligent read-out system to reduce their 3000 silicon photomultiplier detector’s data rate by a factor of 10000 whilst maintaining high efficiency for storing data from antineutrino interactions.

The system employs an FPGA level waveform characterisation to trigger on neutron signals.
Following a trigger, data from a spacetime region of interest around the neutron will be read out using the IPbus protocol.

In this talk the SoLid experiment will be introduced, the design of the read-out system will be explained and the performance of prototype versions of the system will be presented.

Summary:

The electron anti-neutrinos emitted from a nuclear reactor can be detected via the inverse beta decay, which produces a positron and a neutron.

The positron is promptly detected in a scintillator.

The neutron can be captured on particular isotopes (lithium-6 in the SoLid detector) to give a secondary scintillation signal up to 1 ms after the positron signal and at distances up to 20 cm from the initial interaction.

Performing anti-neutrino measurements at ground level and close to a nuclear reactor is particularly challenging due to the high rate of background signals that can mimic the positron and neutron from an inverse beta decay interaction.

The SoLid detector uses a novel composite scintillator technology that provides a robust neutron signature and the detector is also highly segmented in order allow topological selection of candidate anti-neutrino events based on the relative positions of the positron and neutron detections.

The scintillation signals are detected using silicon photomultipliers.

The high level of segmentation results in the 2 tonne detector having 3000 SiPM channels to collect data from, with a raw data rate of order Tb/s.

The SoLid collaboration have developed an intelligent read-out system to reduce the data rate by a factor of 10000 whilst maintaining high efficiency for storing data from inverse beta decay events.

The system employs a front end waveform characterisation within an Artix-7 FPGA to trigger on neutron signals.

In additional, data from all channels will be buffered in the FPGA with a low zero-suppression threshold. Following a neutron trigger, data will be read out from a region of the detector surrounding the neutron channel in a 0.5 ms time window which has a high probability to include the positron signal of an inverse beta-decay interaction.

Data will be transmitted to a software level data reduction system using the IPbus protocol.

The on-line software will be able to compare signals from across the region of interest to identify positron candidates and further reduce the rate at which data is stored to disk by removing low amplitude signals that are not coincident with the positron candidates.

The SoLid collaboration will deploy their first detector modules late in 2016.

In this talk the SoLid experiment will be briefly introduced, the design of the read-out system will be explained and results showing the performance of prototype versions of the system will be presented.

ASIC / 82

PETIROC2A, a 32-channel 20 GHz GBW readout ASIC for accurate time resolution and precise charge measurements

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Petiroc2a is a 32-channel front-end ASIC designed in AMS 0.35μm SiGe technology to read out Silicon Photomultipliers (SiPMs) for applications requiring accurate time resolution and energy measurement over a large dynamic range.

Each channel integrates a 20GHz Gain Bandwidth preamplifier followed by an ultra fast discriminator and a TDC. The first incident photons can be measured with a time resolution better than 100ps.
A low gain shaper ensures an energy measurement up to 400 pC. The 32 time and charge measurements are internally digitized by a 10-bit ADC. Measurements will be detailed in this presentation.

Summary:

Particle physics experiments and medical applications are more and more demanding in terms of time and charge resolution to achieve imaging calorimetry or time of flight measurements. Petiroc2a, which stands for PET Integrated ReadOut Chip, is a System-on-Chip designed in AMS 0.35µm SiGe technology which integrates 32 channels optimized for very large dynamic range input charges and for accurate time measurement.

Petiroc2 embeds an internal 10-bit ADC for energy measurement and a 25ps-bin TDC for time measurement. A second-stage trigger level is integrated to provide an efficient energy cut at the very first stage of the front-end electronics to avoid excess data rate in back-end electronics. The power consumption has been minimized to 6mW/channel.

The fast trigger line is made of a 20 GHZ Gain Bandwidth Product preamplifier followed by an ultra-fast discriminator which preserves the bandwidth. A Time to Amplitude Converter (TAC) is integrated for each channel and enables a time measurement with a 25 ps step. This time measurement is then internally digitized by a 10-bit ADC.

The charge measurement line is composed of a variable time shaper (25 ns up to 100 ns) followed by an analogue memory to store the maximum value of the charge.

A discriminator follows each of the charge amplifiers to provide a “OR32_charge” information that is very useful for PET applications to select only events corresponding to the annihilation of two 511 KeV gamma photons.

Petiroc2A can be used either in analogue mode using the 32 trigger outputs and the multiplexed charge output or in full digital mode using the internal ADC and TAC.

The chip was produced in an engineering run in 2015 and available for tests since then. Many test bench measurements were made using a Picosecond pulser showing a bandwidth larger than 1GHz for the preamplifier and its discriminator, ensuring a time walk smaller than 350 ps. Trigger efficiency measurements show that each channel can easily trigger on one photoelectron. As for the jitter, it has been measured down to 15 ps (test bench jitter floor) when the chip is used in the analogue mode but this value increases up to 45 ps when the clocks of the digital part are active and generate coupling effects through the substrate. The TDC time resolution has been measured to 70ps rms which is below the 100ps required for PET applications but that could be significantly improved by reducing the clock coupling and a migration to TSMC130nm with triple well technology is foreseen.

Energy measurements have also been performed showing an Integral Non Linearity better than 1% for charges up to 2500 photoelectrons or 400pC which is over the expected charge for a 511keV gamma in a crystal, assuming a 106 gain of the SiPM.

Measurements using SIPM matrixes will be soon performed using a test board designed to provide a full integrated SIPM read-out ASIC for time of flight application.

Measurements will be detailed in this presentation.

Systems, Planning, installation, commissioning and running experience / 116

Prototypes and tests of the LHCb Scintillating Fiber detector front end electronics.

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The on-detector electronics of the LHCb Scintillating Fiber Detector consists of multiple PCBs assembled in a unit called Read Out Box, capable of reading out 2048 channels with an output rate of 70 Gbps. There are three types of boards: PACIFIC, Clusterization and Master Board. The PACIFIC boards host PACIFIC ASICs, with pre-amplifier and comparator stages producing two bits of data per channel. A cluster-finding algorithm is then run in a FPGA on the Clusterization board. The Master Board distributes fast and slow control, and power. We describe the design, production and test of prototype PCBs.

Summary:

The Front-End (FE) electronics interfaces to the Silicon SiPMs on one side and to the experiment data-acquisition and control system on the other. All SiPM signals are amplified, shaped and digitized in the 64-channels PACIFIC ASIC; four PACIFIC ASICs are located on each PACIFIC Board. In order to reduce the data volume, the digitized channel data is routed to a flash-based IGLOO2 FPGA running a cluster-finding algorithm. Each Clusterization Board hosts two such FPGAs, processing the data of 256 PACIFIC channels. The cluster data is then further sent to GBTX serializers located on the Master boards; four Clusterization Boards are connected to one Master Board. A Readout Box (ROB) contains two Master Boards, eight Clusterization Boards, and eight PACIFIC Boards, and can service an entire SciFi module (2048 SiPM channels). The inter-connections between the three types of boards are realized through FMC connectors. The data serialized by the GBTX ASICs on the Master Board are shipped over optical fibers. The FE architecture is such that the cluster data of each SiPM are sent over a single fiber to the Back-End (BE) Electronics. Each ROB has also a complete interface for the distribution of bias voltages to the integrated circuits and to the SiPMs, of Timing and Fast Control (TFC) signals and of signals from and to the Experiment Control System (ECS). The communication with the TFC/ECS system goes via the GBT serial protocol: each Master Board hosts one Master GBT with an optical link connected to the LHCb SOL40 detector control system. The Master hosts also 11 FeastMP DC-DC converters, providing the necessary voltages to all devices in the ROB. Each ROB consumes about 100 W, and is individually cooled by demineralized water lines at 19°C.

We produced and commissioned two ROB prototypes, including mechanical enclosure, cooling and shielding. We could successfully configure all devices on the ROB via the GBT serial links on the Master Board, using SOL40 firmware implemented on a prototype back-end electronics consisting of a mini-DAQ system based on the AMC40 architecture. In addition, we successfully demonstrated data transmission through the ROB, and could ship cluster data to the AMC40 mini-daq. We adopted the GBT “widebus” serial protocol at 4.48 Gbps, and a first implementation of the LHCb Tell40 DAQ framework in the AMC40, that processes incoming GBT data and produces 10GbE packets.

We were able to perform a complete system test and demonstrated that the design of the SciFi FE architecture is mature to pass to the production phase. A total of 288 ROBs are needed to service the entire SciFi detector (576 Master, 2304 Clusterization and PACIFIC Boards), for a total of about 590,000 readout channels. For the quality assurance of this large quantity of boards, a test system is under development. During production, this system, capable of injecting into each ROB channel a pulse with adjustable charge and time phase, will be able to provide a complete functional test.

ASIC / 126

First experimental results with TOFPET2 ASIC

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The TOFPET2 ASIC is a low-power, low-noise, readout and digitization chip for SiPMs sensors implemented in 110nm CMOS technology optimized for time-of-flight measurements. The circuit has 64 independent channels including quad-buffered TDCs and charge integration ADCs in each channel, and is an evolution of the TOFPET1 ASIC, which was developed in 130nm CMOS technology for Positron Emission Tomography (PET) applications. Relative to the first chip, TOFPET2 implements new frontend amplifiers, charge integration, improved timing and increased event rate. The chip tape-out was done in November 2015 and first tests started in end March 2016.

Summary:
The input pre-amplifier is a low impedance current conveyor based on a regulated common-gate topology. Two trans-impedance post-amplifier branches are optimized for time resolution and charge integration. One voltage mode discriminator with configurable low threshold generates a fast signal for accurate time measurement. Two other discriminators have configurable thresholds to reject dark counts, to start the integration window, and to trigger the event data readout. Each channel has quad-buffered analogue interpolation TDCs (time binning configurable at 20 or 40 ps) and charge integration ADCs with linear response at full scale (1500 pC). The TDC measures the fine time within a clock period complementing the coarse time provided by a clock counter (200 MHz). The signal amplitude can also be derived from the measurement of time-over-threshold (ToT).

The performance of the TDCs was evaluated with test pulses. The time resolution of each of the 64 channels in the chips was measured with digital test pulses provided by an external pulse generator. The average of the measured values is 26 ps. Time measurements of laser pulses detected with S12642-0808PB-50 MPPC 8x8 pixel array were performed scanning the clock period at 10 different delay settings. The time resolution obtained is 38 ps. No de-convolution of the test pulse jitter and no time walk corrections were applied.

Additional measurements with radioactive sources are planned and should be presented at the conference.

Systems, Planning, installation, commissioning and running experience / 3

A micro-TCA based data acquisition system for the triple-GEM detectors for the upgrade of the CMS forward muon spectrometer

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We will present the electronic and DAQ system being developed for TripleGEM detectors which will be installed in the CMS muon spectrometer. The microTCA system uses an Advanced Mezzanine Card equipped with an FPGA and the Versatile Link with the GBT chipset to link the front and back-end. On the detector an FPGA mezzanine board, the OptoHybrid, has to collect the data from the detector readout chips to transmit them optically to the off-detector micro-TCA boards using the GBT protocol. We will describe the hardware architecture, report on the status of the developments, and present results obtained with the system.

Summary:
In this contribution we will report on the progress of the design of the electronic readout and data acquisition (DAQ) system being developed for Triple-GEM detectors which will be installed in the forward region (1.5 < |η| < 2.2) of the CMS muon spectrometer during the 2nd long shutdown of the LHC, planed for the period 2018-2019. The architecture of the Triple-GEM readout system is based on the use of the microTCA standard hosting FPGA-based Advanced Mezzanine Card (AMC) and of the Versatile Link with the GBT chipset to link the front-end electronics to the micro-TCA boards. For the on-detector electronics a new front-end ASIC, called VFAT3, is being developed for the CMS Triple-GEM system. Its architecture is based on the TOTEM VFAT2 chip which is currently used to test the CMS Triple-GEM prototypes and the new data acquisition system. On detector, a Xilinx Virtex-6 FPGA mezzanine board, called the OptoHybrid, has to collect the data from 24 front-end chips and to transmit the data optically to the off-detector micro-TCA electronics as well as to transmit the trigger data at 40 MHz to the CMS.
Cathode Strip Chamber (CSC) trigger. Two versions of this OptoHybrid have already been designed. They are used to readout the CMS Triple-GEM prototypes equipped with VFAT2 chips and both have been tested with beam at CERN. The microTCA electronics provides the interfaces from the detector (and front-end electronics) to the CMS DAQ, TTC (Timing, Trigger and Control) and Trigger systems. Each micro-TCA crate can house 12 AMC boards. Currently the GLIB board designed by CERN is used for the system developments. For the final system more powerful boards based on the Virtex-7 or Kintex-7 Xilinx FPGA are envisaged. During the LHC yearly extended technical stop of winter 2016-2017, 8 Triple-GEM detectors will be installed inside CMS. They will be read-out with the existing VFAT2 chip and with the data acquisition system described above. To prepare this installation, called slice-test, a dedicated test bench has been set-up at CERN to integrate the GEM with the CSC electronics. This work also includes the development of the DAQ software based on xDAQ and of the detector control system.

In this contribution we will describe the hardware architecture and expected performance, report on the status of the developments of the various electronic components and present preliminary results obtained with the microTCA-based readout system developed for the slice-test.

Invited Talk / 198

Radiation tolerant issues for LHC accelerator

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Electronic systems located in LHC underground areas can suffer by radiation induced failures. The knowledge of the radiation levels around the LHC accelerator and the cause of faults permits to improve the LHC availability every year. The shielding, relocation and equipment upgrade are the ingredients to mitigate the radiation effects. A test protocol exists for the equipment upgrade which requires radiation tolerant design. The methodology and the facilities are available to improve the radiation tolerance of the electronic systems that requires high reliability. This presentation will go through all these steps to explore the key elements that can make possible to reduce the radiation induced failures.

ASIC / 113

A fast, ultra-low power 10-bit SAR ADCs in CMOS 130 nm technology

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The design and measurement results of four ultra-low power 10-bit SAR ADCs, fabricated in CMOS 130-nm technology, are presented. All prototypes use very similar architecture with main difference in split in the capacitive DAC network. The prototypes are fully functional, achieve excellent linearity (DNL < 0.3 LSB and INL ~0.5 LSB), and show very good ENOB above 9.5 for 0.2 Nyquist input frequency, up to maximum sampling rate 40-50 MSps, depending on prototype. All prototypes consume less than 900 uW at 40 MSps achieving an excellent FOM 20-30 fJ/conversion-step.

Summary:
In modern and future detectors of particle physics experiments an ultra-low power, area-efficient Analog-to-Digital Converter (ADC) is highly demanded. This work discusses the development of 10-bit Successive Approximation Register (SAR) ADC for readout system of luminosity detector at the future linear collider (ILC/CLIC). The presented design meets the most important requirements like ultra-low power consumption, excellent linearity and possibility of multichannel integration. The maximum sampling rate above 40MSps makes it also suitable for readouts of LHC experiments.

A fully differential architecture was chosen for ADC design. The ADC contains a pair of bootstrapped switches, differential Digital-to-Analog Converter (DAC), a dynamic comparator, and an asynchronous dynamic control logic. A fully dynamic architecture allows to eliminate static power consumption and to obtain power pulsing without additional effort. The Merge Capacitor Switching (MCS) scheme results in 93% switching energy reduction in comparison to conventional scheme. The minimum allowable capacitor was used as the DAC unit capacitance, moreover a split DAC architecture was applied to reduce total capacitance. Three different split architectures were designed in order to investigate the technology limits, namely the matching and parasitics. The asynchronous control logic was used to avoid a fast bit-cycling clock distribution. The ADC layout occupies 100 um x 800 um.

All prototypes were fabricated in CMOS 130 nm technology. Two prototypes use a default DAC split architecture 6-1-3 (6 MSB bits in first sub-DAC, split capacitance equal to LSB capacitance, 3 LSB bits in second sub-DAC) and differ slightly in control logic implementation, where various improvements increasing the meta-stability hardness and extending the maximum sampling rate above 50 MSps, were introduced. Two other prototypes, apart from using improved control logic, have different split in the capacitive DAC. They use 6-2-3 and 5-1-4 DAC networks and their input capacitance was reduced two times.

The 6-1-3 prototypes achieve an excellent linearity, with DNL below 0.3 LSB and INL ~0.5 LSB, and excellent effective resolution. For 0.2 Nyquist input frequency the ENOB of 6-1-3 prototypes remains between 9.7 - 9.5 bits up to 40 MSps sampling rate, and above 9.3 bits up to 50 MSps for the improved prototypes. For Nyquist input the ENOB starts to decrease from 9.5 to 9.1 bits for sampling rates 30-40 MSps. The 5-1-4 and 6-2-3 show worse linearity (DNL ~1 LSB, INL ~0.9 LSB) and their ENOB is in range 9.3-9.0 over the range of sampling rates and input frequencies.

Power consumption of the default 6-1-3 configuration is below 700-uW at 40 MSps. It gives excellent FOM below 28 fJ/conversion-step, the lowest, to the authors knowledge, FOM obtained in 130 nm CMOS for similar ADC specifications. Also other configurations show excellent, although slightly higher, FOMs. The measurement results and comparison of different prototypes will be given in this talk.

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**On-detector electronics for the LHCb VELO upgrade**

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The LHCb Experiment will be upgraded to a trigger-less system reading out the full detector at 40 MHz event rate with all selection algorithms executed in a CPU farm. The upgraded Vertex Locator (VELO) will be a hybrid pixel detector read out by the VeloPix ASIC with on-chip zero-suppression. This paper will present the systems overview and design of the VELO on-detector electronics, including the front-end hybrid, the opto-conversion and power distribution boards. Results will be shown from the evaluation of these prototypes of these boards.

**Summary:**

The upgrade of the LHCb experiment will be installed during the shut-down of LHC operations in 2019-2020. It will transform the experiment into a trigger-less system reading out the full detector at 40 MHz event rate. The event selection will be performed by high-level software algorithms implemented in a CPU farm. The Vertex Locator (VELO) surrounding the interaction region is used to reconstruct
primary and secondary decay vertices and measure the flight distance of long-lived particles. It will be a hybrid pixel detector read out by the VeloPix ASIC, which is part of the Medipix/Timepix family. The highest occupancy ASICs will have pixel hit rates of 900 Mhit/s and produce an output data rate of over 15 Gbit/s, adding up to 1.6 Tbit/s of data for the whole VELO.

This paper will present the architecture and the design of the VELO on-detector electronics, and describe how it interfaces to the front-end ASIC and the LHCb readout system. Its two main components are the opto- and power board (OPB) and the front-end hybrid. The OPB is situated immediately outside the VELO vacuum tank and performs the opto-electrical conversion of control signals going to the front-end and of serial data going off-detector. Moreover, it performs the DC/DC conversion of supply voltages and provides the local control of the front-end. The board is designed around the Versatile Link components developed for high-luminosity LHC applications. The front-end hybrid hosts the VeloPix ASIC and also a GBTx ASIC that provides the control signals for the VeloPix. The hybrid and OPB are linked by 60 cm long electrical data and control links running at 5 Gbit/s.

This system is an example of a full implementation of a front-end readout and control system for an LHC detector, based on the radiation tolerant opto-modules, DC/DC converters and the GBT chipset developed for the LHC upgrades. Prototypes for all components of the system have been produced and tested, the results from these tests and the experience gained from designing and operating the system will be presented.

**ASIC / 34**

**MATRIX: a 15 ps resistive interpolation TDC ASIC based on a novel regular structure**

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This paper presents a 4-channel TDC chip demonstrator with the following features: 15-ps resolution, 1280 ns dynamic range, dead time < 20 ns, up to 10 MHz of sustained input rate per channel, around 60 mW of power consumption and very low area in a 180 nm technology. The main contribution of this work is the novel design of the clock interpolation circuitry which is based on a resistive interpolation mesh circuit (patented) a two-dimensional regular structure with outstanding performance in terms of power consumption, area and low process variability.

**Summary:**

This paper presents a 4-channel TDC chip demonstrator with the following features: 15-ps resolution, 1280 ns dynamic range, dead time < 20 ns, up to 10 MHz of sustained input rate per channel, around 60 mW of power consumption and very low area (910x215 µm2) in a 180 nm technology.

The main contribution of this work is the novel design of the clock interpolation circuitry based on a resistive interpolation mesh circuit (RIMC). The RIMC (see picture attached) is a matrix where the timing difference between columns (sub-delay) is determined by the resistor value and the parasitic capacitance of the node, while the delay between rows is determined by the drive strength of the inverter. End-to-end delay between the first and the last node for a given row is higher than the inverter delay, and thus at least one clock transition occurs (either rising or falling) within 15 picosecond period.

This novel architecture has many advantages in terms of design time, scalability, reusability, power consumption, area and process variability issues. The atomic circuit of this repetitive structure is just a current starved inverter (3 transistors) and a resistor, which speeds up design time. The number of rows of the RIMC determines the dynamic range and thus the oscillation frequency of the mesh (800 MHz for this design), while resistor value together with the number of columns may determine TDC resolution (15 ps). This allows high reusability of previous designs and scalability. The use of starved...
inverters as delay elements makes this solution very efficient in terms of power consumption and area. Moreover, the RIMC is used as a voltage-controlled oscillator (VCO) for the PLL, leading to an extra chip area reduction. Lastly, this circuit presents excellent properties in terms of process variability since the mesh structure averages delay variations that may occur due to mismatch in transistors and resistors. Apart from the RIMC the TDC comprises four time capture matrices (TCM) that store RIMC clock phases (fine timestamp) when a rising edge is produced at any of the inputs of the TDC. Captured data is encoded, buffered and transmitted via a serial interface when an event occurs. Since the acquisition dead time is less than 20 ns, the peak event rate that this chip can process is 50 MHz, while the sustained rate is 10 MHz per channel. Dynamic range is extended by means of a 10-bit coarse counter which counts the number of complete clock periods at 800 MHz (coarse timestamp), and thus extending dynamic range up to 1280 ns. A fine synchronization circuitry is provided to allow coincidence measurements between different chips. The internal 800 MHz clock is synthesized by means of a PLL with configurable input clocks (50 / 100 / 200 MHz).

Chip prototype was submitted on February 2016 and encapsulated prototype samples of MATRIX are expected by June 2016.

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Systems, Planning, installation, commissioning and running experience / 153

GBT based readout in the CBM experiment

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The CBM experiment at FAIR will use GBTX and Versatile link based readout systems for several subdetectors.

Particularly challenging is the readout of the silicon tracking system (STS) which requires features like a minimal number of frontend connections, AC coupling and time deterministic messages.

The paper gives a detailed description of the readout concept for the STS, emphasizing the common features with the GBT based readout in other CBM detectors.

A CBM common readout board with 3 GBTX is presented which provides the full GBT functionality for all systems and can be interfaced to various prototype readout chains.

Summary:

The CBM experiment at FAIR is a fixed target heavy ion experiment planned to operate at high interaction rates up to 1e7/s and using self-triggering frontend electronics. The silicon tracking system (STS) is the main tracking detector in CBM, consisting of 8 stations of silicon strip sensors located inside a 1T dipole magnet.

The GBTX transceiver ASIC and VersatileLink optical modules were chosen to implement a data aggregation stage between the STS-XYTER frontend ASICs connected to the strip sensors via low mass cables and the data processing boards (DPBs), a common FPGA-based layer. Readout boards (ROB) with the GBT and Versatile Link devices are located inside the magnet close to the active sensor area.
Based on the specific conditions in the STS setup and the GBTX features, the readout concept for the STS was developed:

The frontend board (FEB) carries 8 STS-XYTER2 ASICs which implement an E-Link interface. Up to 5 FEBs connect to one of the ROBs, which are stacked in the limited space at the sides of the STS box. Each FEB operates at the bias potential of the connected sensor. Consequently the E-Link interfaces are AC coupled.

A single GBT clock and a single downlink per FEB are used for ASIC configuration, control and time synchronization. A configurable number of 1 to 5 uplinks per STS-XYTER depending on the local data rate is used for data readout and for control responses.

The ROB for STS will implement 3 GBTX together with 1 VTRx and 1 VTTx module. The resulting 42 readout E-Links at 320 Mbps in widebus mode can be matched efficiently with 8,16 or 40 readout links per FEB. The backend interface of the GBTX communication is implemented in the DPB layer which resides outside the experimental cavern. The DPB also includes the backend of the specifically developed STS-XYTER readout protocol and the interfaces to data acquisition, detector control and the timing system.

Similar readout concepts were devised for other CBM detectors with frontend systems based on custom ASICs, namely the muon detector (MUCH) which uses the same XYTER as frontend ASIC, the TRD and the TOF detectors. This will allow for shared developments and partial reuse of hardware, firmware and protocols.

A common CBM readout board (C-ROB) is being developed that implements the full GBT and Versatile Link functionality needed by all systems. The C-ROB serves to setup prototype readout chains and provides sufficient data aggregation to readout moderately sized detector assemblies in laboratory and beam tests. The required subset of E-Links, clocks and SCA functionality is connected to 2 FMC connectors. Prototype readout chains of the various frontend systems can be interfaced via individual mezzanine cards.

For the final CBM readout chains, systems will adapt the C-ROB in order to fulfill specific needs such as smaller ROB dimensions and efficient cooling for the STS, a single GBTX ROB for TOF, or duplicated GBTX/VTTX blocks for the TRD readout.

ASIC / 152

Developments of two 4 × 10-Gbps radiation-tolerant VCSEL array drivers in 65 nm CMOS

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We present designs and test results of two ASICs, VLAD and lpVLAD. Each is a 4-channel, 10-Gbps-per-channel VCSEL array driver fabricated in a 65 nm CMOS technology. lpVLAD deploys a novel high-efficient output structure to achieve a record low power consumption of 25 mW/ch when delivering 2 mA bias and 6 mA modulation currents at 10-Gbps. Eye diagrams of both two designs under
post-layout simulations easily pass 10-Gbps requirement. The full-channel optical link test will be carried out in June and the results will be reported in the conference.

**Summary:**

VCSEL-based high-speed, low-power, radiation-tolerant short-range optical data links are in high demand for detector data transmission in the LHC upgrades as well as in other physics detector developments. Benefited from the commercial array optical transceivers advancement, we have developed an array optical transmitter module (ATx) with radiation-tolerant optical components. Besides, another critical component and key challenge is a high-speed radiation-tolerant VCSEL array driver ASIC. In this paper, we present designs and test results of two 4-channel, 10-Gbps-per-channel, radiation-tolerant VCSEL driver ASICs, VLAD and lpVLAD, which are both fabricated in a commercial 65 nm CMOS technology.

Each channel in VLAD consists of an input matching impedance, a two-stage pre-driver (1.2 V), an output driver (1.2 V and 2.5 V) and their biasing circuits. The ASIC receives differential CML signals of 400 mVp-p, complying with the lpGBT output. The two output pads of each channel are directly wire-bonded to the anode and the cathode (GND) pads of the VCSEL, providing a bias current from 1 to 10 mA, and a modulation current from 3 to 9 mA. The total power consumption is 35 mW/channel at the default output of 1.5 mA bias and 7 mA modulation currents at 10 Gbps.

lpVLAD, the low-power version of VLAD, differs from VLAD in the output driver. This novel output structure uses a pair of PMOS and NMOS switches to modulate the VCSEL. The push-pull complementary switches fully utilize both differential outputs of the pre-driver and increase the VCSEL modulation efficiency to 100% theoretically. A single stage current generator is used to provide the VCSEL bias current, and a feed-forward signal from the pre-driver is used to stabilize the off-current to the VCSEL. This new driving method results in an ultra-low power consumption of 25 mW/ch when delivering 2 mA bias and 6 mA modulation currents at 10-Gbps. The lpVLAD is able to provide a bias current from 1 to 6 mA, and a modulation-current from 5 to 8 mA.

An I2C digital control module with triple-modular-redundancy structure adapted from CERN is used in both VLAD and lpVLAD. The 1.2 V and 2.5 V power bus topology is carefully designed. Current return paths and the grounds of the on-chip capacitors for the 1.2V and 2.5 V powers are separated with single-point connection to minimize possible multi-channel crosstalk.

Eye diagrams at the VCSEL under post-layout simulations for both VLAD and lpVLAD easily pass 10-Gbps data rate requirement in each channel when all four channels work simultaneously. We tapeout the designs in February 2016 and expect to test the ASICs in June and July 2016. The radiation-tolerant performance and full-channel optical link test including BER-OMA and crosstalk will be fully evaluated, and the results will be reported.

**Summary:**

**FELIX: a PCIe based high-throughput approach for interfacing front-end and trigger electronics in the ATLAS Upgrade framework**

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The ATLAS Phase-I upgrade requires a Trigger and Data Acquisition (TDAQ) system able to trigger and record data from up to three times the nominal LHC instantaneous luminosity. The FELIX system provides this in a scalable, detector agnostic and easily upgradeable way. It is a PC-based gateway, routing between custom radiation tolerant optical links from front-end electronics, via FPGA PCIe Gen3 cards, and a commodity switched Ethernet or InfiniBand network. FELIX enables reducing custom electronics in favor of software on commercial servers. The FELIX system, results of demonstrator, design and testing of prototype are described.
The ATLAS Phase-I upgrade requires a Trigger and Data Acquisition (TDAQ) system able to trigger and record data from up to three times the nominal LHC instantaneous luminosity. A new detector-independent readout architecture, named Front-End LInk eXchange (FELIX), provides this in a scalable, detector-agnostic and easily upgradeable way. During LHC Long Shutdown 2 (2019-2020), new ATLAS on-detector electronics for the Liquid Argon (LAr) Calorimeters and new muon detectors will be installed. Radiation-hard Giga Bit Transceivers (GBT) will be used for data transmission. By means of time multiplexing, the GBT protocol provides up to 42 independent logical data links, yet sharing the same fiber. Through such links FELIX receives and identifies different information streams. Subsequently data packets will be routed via a commercial switched network. In the opposite direction, FELIX receives packets from the network and forwards them to specific on-detector modules. Another task of FELIX is to handle input from the Time, Trigger and Control (TTC) system to recover the LHC clock and to forward the synchronous trigger information. This information will be distributed to on-detector electronics over low-and-fixed-latency GBT links, and also to new and upgraded off-detector first-level trigger systems. For readout of the latter a lightweight protocol with higher throughput than the GBT protocol is envisaged to be used.

The functions described above are implemented in FPGAs. The Hitech Global HTG-710 is used as demonstrator card: it is equipped with an 8 lanes PCIe Gen3 (64 Gb/s) interface and with two CXP transceivers providing interfaces for 24 bidirectional optical links (max. 13.1 Gb/s). Moreover a custom mezzanine was designed to receive and decode the TTC clock and data information. The firmware is also for Xilinx VC-709 evaluation board, which has same type of FPGA and PCIe interface as HTG-710, but less optical interfaces. This board targets detector and trigger system test setups.

Drivers and software tools have been developed for testing and configuration of the boards. Data routing and the connection to the COTS (Commercial Off-The-Shelf) network is implemented in a software pipeline running on the FELIX host PC. The packet processing performance satisfies the requirement of FELIX.

A PCIe board with a Xilinx Kintex UltraScale FPGA, a 16 lanes Gen3 PCIe interface, and 48 bidirectional optical interfaces in the form of eight Mini-POD transceivers (max. link speed 14 Gb/s) will probably be the baseline choice to be used in the Phase-I FELIX systems. The optical links, PCIe interface, and TTC decoding circuits of the first prototype have been verified to function well. Integration testing with the complete FELIX firmware and software is ongoing.

In this paper, the FELIX system will be introduced. Then the optimization to the fixed low-latency GBT core from CERN will be discussed. Furthermore results of the demonstrator testing, and progress of the prototype design and testing will be presented.

POSTER - Board: E3 / 18

Readout Channel with Majority Logic Timestamp and Digital Peak Detector for Muon chambers of the CBM Experiment

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A prototype readout channel was manufactured in UMC CMOS 180 nm for the purpose of the CBM experiment at the FAIR accelerator. The channel includes a preamplifier with fast and slow CR-RC shapers, discriminator with a differential threshold setup circuit, 6 bit SAR ADC (40 Msps, 1.5mW
power consumption), digital peak detector and block of the time stamp registration. The control data, clock and output data are supplied through SLVS transmitter and receiver. The slow and fast channels have 1500 el and 2000 el ENC accordingly at a 50 pF detector capacitance. Power consumption is 10 mW/channel.

Summary:
The design and tests of the self-triggered readout channel for muon chambers of the CBM experiment are presented. The MUCH detector is built with GEMs. Since the sensors will have different granularity, the requirements to the front-end electronics are also different for the central and peripheral parts. Thus, the preamplifier is followed by two circuits: a slow channel, optimized for S/N ratio in order to use it in the periphery, and a fast one, adapted to the hit rate of the inner detector part, where the occupancy is the highest. The fast channel is also supposed to be used for the timestamp determination. Both channels are realized with CR-RC shapers with different peaking times, 60 ns and 260 ns accordingly. The measured ENC of the fast and slow shapers are no more than 2000 el and 1500 el correspondently at 50 pF of the equivalent detector capacitance. The channel is optimized to operate with the negative charge polarity. The preamplifier dynamic range is 100 fC. The channel occupancy is up to 1 MHz.

The shaper outputs are connected to the drivers, which make a single-ended to differential signal conversion. Further the signals are supplied to the differential comparator inputs. For regulating the threshold of the comparator a current 5 bit DAC is used. The DAC sets the threshold up to 80 mV with INL – 0.20 LSB and DNL – 0.25 LSB.

The signal from either slow or fast shaper (depends on occupancy) is processed by a 6 bit SAR ADC (INL – 0.45 LSB, DNL – 0.70 LSB) with a 40 Msps sampling rate and 1.5 mW power consumption. The ADC is followed by a digital peak detector. The peak detector has a function of the false peak find prevention due to the presence of noise spikes.

The chip has fast and slow discriminators. The fast discriminator output is connected to a timestamp block. Both fast and slow discriminators can be used by the logic for hit overlap detection. When the event in the channel occurs, the fast discriminator fixes the time of a 14 bit counter in the Gray code. The timestamp block also utilizes the majority logic to indicate the proper time of the event.

The final chip version is considered to be compatible with the GBTx data processing board. Thus, the data exchange is supposed to be via e-links. In the current version the data from ADC, peak detector and timestamp are serialized and sent out via SLVS transmitter at 320 Mbit/s. The 160 MHz clock signal is supplied via the SLVS receiver.

The ASIC layout area is 3240x1525 um$^2$. The chip has been fabricated by the UMC MMRB 180 nm CMOS process as a double miniasic via Europractice. Measurements of the ASIC were carried out, including the lab tests of the analog blocks with probe station. The results of the functionality and noise tests and their comparison with the simulation are presented.

**POSTER - Board: E1 / 164**

**Front-End and Back-End Solutions in the CBM STS Readout ASIC**

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STS-XYTER2 is a new full-size CBM Silicon Tracking System and Muon Chamber prototype readout ASIC designed in UMC 180 nm CMOS technology. It is a self-triggered amplitude and time measurement chip implementing a digital back-end compatible with a GBTx-based data acquisition scheme with scalable data bandwidth. We present details on the front-end and back-end solutions used in this ASIC and simulation results.

**Summary:**
We present the architecture of the STS-XYTER2 ASIC, a full-size, 128-channel prototype chip for the Silicon Tracking System (based on double-sided silicon strip sensors) and Muon Chamber (gas sensors)
detectors at the Compressed Baryonic Matter experiment at FAIR, Germany. The charge processing channel includes a charge sensitive amplifier, shaper amplifiers forming two signal paths for timing measurement via a fast discriminator and low-noise amplitude measurement by a 5-bit continuous-time ADC with digital peak detector and is required to operate at average rate of 250 kHz/channel. Different operating conditions (including environment) and constraints of two target applications required flexibility and careful design to meet extended system-wise requirements. The circuit implements switchable shaper peaking time, gain switching and trimming, pulsed reset of the amplifier for increased input charge rate and faster recovery from overload, fail-safe measures and diagnostic modes for wafer-level and in-system testing and calibration. The chip required a robust and effective hit data streaming and control mechanism. The back-end implements fast channel read-out, timestamp-wise hit sorting and data streaming via scalable interface implementing a dedicated protocol (STS-HCTSP) for chip control and hit transfer with data bandwidth from up to 47 MHz. It also includes options for link diagnostics, failure detection and throttling features. The chip is designed to operate within a GBTx-based data acquisition scheme.

**POSTER - Board: D1 / 94**

**ASPIC and CABAC: Two ASICs to Readout and Pilot CCD**

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For several years, a group of engineers and physicists from LAL and LPNHE have been working on the design of two front end ASICs dedicated to Charge Couple Devices (CCD). ASPIC (Analogue Signal Processing Integrated Circuit), designed in AMS CMOS 0.35µm 5V technology, is meant to readout and process the analog signals of CCDs. CABAC (Clocks And Biases ASIC for CCDs), designed in AMS CMOS 0.35µm 50V technology, produces the clocks and biases needed by the CCDs to work at their full potential. This paper presents the performances of the final versions of these two ASICs.

**Summary:**

The digital camera of the LSST (Large Synoptic Survey Telescope) project will be made of 189 CCDs of 4096x4096 pixels each. In order to pilot and readout these CCDs in parallel, two front end ASICs have been designed over the past 9 years taking into account the specific requirements of LSST experiment while being generic enough to be suitable for different types of CCD. At first, the efforts were put on the design of the integrated circuit ASPIC (Analogue Signal Processing Integrated Circuit) dedicated to the readout and process simultaneously eight CCD output signals. It has been designed in AMS CMOS 0.35µm 5V « C35B4 » technology and mainly features an amplification of each one of the 8 input signals with a programmable gain and a correlated double sampling using a Dual Slope Integration which allows subtracting an important part of the noise. It took 7 years (2007 to 2014) and 3 versions of ASPIC to match the challenging specifications: 25 mW power dissipation, 0.5% linearity, 13 µV noise and 0.05 % crosstalk between channels. A fourth version was nonetheless designed and submitted in 2014 to improve some aspects of the circuit such as the substrate coupling between channels. This version showed good performances and worked as intended associated (or not)
to a CCD. More than one thousand ASPIC4 have been produced in 2015 and will be tested in May-June 2016.
Since the end of 2011, another ASIC was designed by the group in parallel to ASPIC. It is named CABAC, which stands for Clocks And Biases ASIC for CCDs, and is meant to pilot the CCDs by providing different sets of clocks (4 parallel and 4 series) and biases (power of the output stage of the CCD and 3 polarizations). These parameters are highly configurable which allows tuning them efficiently for any type of CCD. Nevertheless the first version of CABAC (CABAC0) was developed taking the e2v CCD as a reference since it was the one that would most likely be used for LSST camera. It was also a safe way to start a design in a technology (AMS CMOS 0.35µm 50V « H35B4D3 ») never used at IN2P3. The tests showed encouraging results and useful experience. The second version of CABAC was almost a new prototype since it was developed in order to be compatible with another type of CCD, one working with negative voltages (contrary to e2v one). Unfortunately the tests carried out end of 2014 showed an excessive fragility of the ASIC despite satisfactory performances when all the precautions (complex power on sequence) were taken. Therefore a new version (CABAC2) was designed beginning of 2015 and tested in May 2015. The results, over a sample of 100 ASICs, showed a 95% yield. It was proven that all the clocks and biases could be adjusted finely.
The performances and the design of these two ASICs will be presented in this paper.

POSTER - Board: F8 / 11

SLVS Transmitter and Receiver for Readout ASIC

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Scalable Low Voltage Signaling (SLVS) Transmitter (Tx) and Receiver (Rx) IP blocks are designed in the UMC 180 nm CMOS technology as component of the readout ASIC for the muon chambers (MUCH) of the Compressed Baryonic Matter (CBM) experiment at FAIR (Darmstadt, Germany). These blocks are a prototype of the physical layer of the e-link interface that is used for ASIC-GBTx connection. The experimental results at 320 Mbit/s are presented.

Summary:

In a series of the new generation of particle physics experiments (including CBM experiment at FAIR) the readout system has a following structure: several frontend ASICs are connected to a Gigabit Transceiver (GBTx) chip. Data from FE ASIC are sent to GBTx (transfer speed up to 320 Mbit/s per link), then serialized and sent to an off-detector processing system via optical link (speed up to 4.8 Gbit/s).

Connection between ASICs and GBTx is implemented by an e-link interface, its physical layer is implemented in accordance with SLVS or LVDS standards. Therefore, as part of work on the development of FE ASIC for muon chambers of the CBM experiment, the design of SLVS transmitter and receiver is necessary for providing compatibility with the e-link interface.

The SLVS standard was chosen in comparison with LVDS because of lower voltage swing (200 mV) and common-mode voltage (0.2 V). It reduces the impact on sensitive pads (e.g. charge sensitive amplifier inputs) and power consumption of the transmitter. The low common mode voltage simplifies the structure of the receiver.

The SLVS transmitter is implemented by a switched current sources based on H-bridge of N-channel MOS transistors, replica bias controls output common mode voltage. E-link standard allows a few of different transmitter output current values for different transmission speeds (up to 2 mA), but in this case only the maximum current value is provided.

The SLVS receiver is implemented by a P-MOS transistors input comparator with output buffer. Because of low common mode voltage, the provision of rail-to-rail input for this comparator is not necessary.
The transmitter and receiver are fabricated in late 2015 as part of a readout ASIC in the UMC 180 nm CMOS process which is the standard for electronics at FAIR. The test structure contains the transmitter with serial input and differential output, which can be measured via differential probe, and the receiver with differential input and internal pad at the output for measurements via Picoprobe on probe station.

The measurements were performed at the following conditions: 40, 80, 160 and 320 MHz clock signals for transmitter and receiver and a data stream with PRBS (length $2^{11} - 1$) at the 40, 80, 160 and 320 Mbit/s speed. Transmission line is a 20 cm PCB stripline.

**Tx parameters:**

- Supply Voltage: 1.8 V
- Power consumption: 6.6 mW (at 320 MHz)
- Clock jitter standard deviation (at 320 MHz): 15 ps
- Total jitter (at 320 Mbit/s and $10^{-12}$ BER): 750 ps
- Eye height (at 320 Mbit/s): 350 mV
- Silicon area: 180x125 um$^2$

**Rx parameters:**

- Supply Voltage: 1.8 V
- Power consumption: 1.2 mW (at 320 MHz)
- Clock jitter standard deviation (at 320 MHz): 70 ps
- Total jitter (at 320 Mbit/s and $10^{-12}$ BER): 1.4 ns
- Eye height (at 320 Mbit/s): 1.4 V
- Silicon area: 150x55 um$^2$

The obtained parameters confirm the correct operation of designed blocks.

**POSTER - Board: E7 / 147**

**A Low-Power 10 Gbps Serial Link Transmitter ASIC for Particle Detectors in 65nm CMOS**

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This paper presents a 10 Gbps serial link transmitter ASIC designed in a 65 nm CMOS technology. The ASIC mainly includes an LC-VCO PLL, a 16:1 serializer and a CML driver. Simulation results show that the PLL achieves a 6-to-12 GHz tuning range and an RMS jitter of 0.67 pS. The serializer has a deterministic jitter of 11 pS and a programmable output swing from 200mV to 800mV (pk-pk). The PLL and the serializer consumes 53.6 mW and 73 mW from a 1.2V power supply, respectively.

**Summary:**
The large volume data production in recent high energy physics experiments requires high speed data links between the on-detector and off-detector subsystems. This paper presents a low-power 10 Gbps serial link ASIC in a 65nm CMOS technology. The ASIC includes a low-jitter LC-VCO PLL, a data scrambler and DC-balance encoder, a 16:1 serializer and a CML output driver.

A charge-pump Σ-Δ fractional-N PLL is developed for clock generation. The major challenge for the PLL is to achieve low jitter and SEE robustness. An LC oscillator is chosen because of its low noise performance. The PLL works in either integer-N or fractional-N mode. Programmable resistors in the loop filter along with programmable charge pump current provide control over loop bandwidth against different VCO gains and divider ratios. The PLL loop bandwidth is optimized to tradeoff the in-band and out-band noises. The PLL is designed to cover an octave frequency from 6GHz to 12GHz. NMOS negative transconductance is adopted due to its lower parasitic. The inductors of the VCO is optimized for high Q-factor as well as wide tuning range. The VCO core consists of a single-turn inductor, an 8-bit binary weighted digitally-controlled MIM capacitor array (DCCA), accumulation-mode varactors, and a digitally-controlled automatic leveling control loop. Since the required negative transconductance varies with the oscillation frequency, the biasing current is made programmable to ensure the oscillator to operate at the edge of the current-limited regime for a maximum voltage swing without excessive waste of power. The clock distribution network consists of buffers, divider-by-2 and multiplexers to deliver the final clock signals.

The high-speed serializer is a 16:1 multiplexer with a 4-stage binary-tree structure, namely 16:8, 8:4, 4:2 and 2:1 multiplexer in a chain. The 4 multiplexer stages are driven by 0.64, 1.28, 2.56 and 5.12 GHz clock signals, respectively. The low-speed stages are protected by TMR and the high-speed stages are designed with SEE immunity on the sensitive nodes. The serializer provides a complementary signal to a CML driver, which drives a 50 Ω impedance trace to the VCSEL driver in an optical module.

The 10 Gbps serial link transmitter ASIC is designed in a 65-nm CMOS process. Simulation results indicates the PLL achieves a 6-to-12 GHz tuning range and an RMS jitter of 0.67pS. The serializer has a deterministic jitter of 11 pS (pk-pk) and its output swing can be programmed from 200mV to 800mV (pk-pk). The power consumption of the PLL and the serializer including the CML driver are 53.6 mW and 73mW from a 1.2V power supply, respectively. The 10 Gbps serial link ASIC will be submitted for fabrication in August. Extensive electrical and radiation performance testing will be carried out and the testing results will be provided in the final paper.
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We present design and test results of a dual-channel serializer ASIC, LOCx2, for detector front-end readout. LOCx2 interfaces an ASIC ADC, ADS5272 and ADS5294. LOCx2 may take data from any 12-bit or 14-bit, multiple channel ADCs with sampling rate from 32 to 43 MSPS. We also present the design of LOCx2-130, a drop-in backup to LOCx2 based on a 0.13 µm bulk silicon CMOS process. Power consumption and transmission latency for LOCx2 is 900 mW (88 mW/Gbps) and 27 ns, and 350 mW (37 mW/Gbps) and 38 ns for LOCx2-130.

Summary:

ASIC serializers are needed for particle physics detector front-end optical readout due to the demand on data bandwidth (about 200 Gbps per board), channel density, low power consumption, low transmission latency and radiation tolerance. LOCx2, an ASIC based on a commercial 0.25 µm silicon-on-sapphire (SOS) CMOS technology, has been developed to meet the demands, in particular those from the optical readout on the trigger digitizer board (LTDB) in the ATLAS Liquid Argon Calorimeter trigger upgrade project. As we recently experienced prototype manufacturing difficulties in this SOS process, we developed a drop-in backup ASIC named LOCx2-130, using a 0.13 µm bulk silicon CMOS process. We submitted LOCx2 through an engineering run in April and plan to test in July and August, including irradiation tests. We plan to submit LOCx2-130 in August. We will present the design and test results of LOCx2, and the design of LOCx2-130.

LOCx2 has two serializing channels sharing one LC-VCO PLL. In each channel there is an interface block called LOCic that takes the upstream ADC data. LOCic is designed to interface ASIC ADCs, ADS5272 and ADS5294. With a programmable input timing adjustment, LOCx2 can take data from any 12-bit or 14-bit, 4 or 8 channel ADC chips that have a sampling rate from 32 to 43 MSPS and with serial outputs. LOCic prepares the data for serial transmission using a custom encoder. An 8-bit CRC in each transmission frame is used to detect possible bit flip errors. The serializer in LOCx2 is 16:1 followed by a CML output driver, working at 5.12 Gbps. LOCx2 is configured and controlled through I2C. According to the post layout simulations, LOCx2 consumes 900 mW under a 2.5 V power supply when both channels function at the design speed of 5.12 Gbps. The transmission latency is 27 ns. A previous prototype measures 850 mW and 27 ns for power consumption and latency, respectively.

LOCx2-130 has a similar interface to that in LOCx2. This interface is digitally synthesized with the transmission latency minimized. LOCx2-130 can transmit 16 channels of ADCs, with 12-bit or 14-bit in each channel. In the case of 12-bit, a 16-bit CRC is used for error detection. There is no error detection when 14-bit ADCs are connected. The serializer and the PLL are adapted from a design that originates from the GBTx ASIC. The I2C here and the one in LOCx2 are adapted from CERN’s IP. According to the post layout simulations, LOCx2-130 consumes 350 mW under a 1.5 V power supply when both channels function at the design speed of 4.8 Gbps. The transmission latency is no more than 38 ns.

Both LOCx2 and LOCx2-130 will be packaged in plastic QFN100. The tests will be carried out using a clamp socket. Testing results and knowledge obtained on QFN packaging and testing with clamp socket will be reported.

POSTER - Board: C5 / 99

Integrated Input Protection Against Discharges for Micro Pattern Gas Detectors Readout ASICs

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Immunity against possible random discharges inside active detector volume of the MPGDs is one of the key aspects that should be addressed in the design of the front-end electronics. This issue becomes particularly critical for systems with high channel counts and high density readout employing
the front-end electronics built as multichannel ASICs implemented in modern CMOS technologies, for which the breakdown voltages are in the range of a few Volts. The paper presents the design of various input protection structures integrated in the ASIC and test results using an electrical circuit to mimic discharges in the detector.

Summary:

One of the major problems that have to be addressed in the design of the front-end electronics for readout of MPGDs is its immunity against possible random discharges inside active detector volume. A commonly used solution to this problem is an input protection circuit built of discrete Surface Mount Device (SMD) components. Such a solution has, however, several drawbacks, including large area occupied by the SMD components and associated stray capacitance at the input, necessity of using advanced and expensive Printed Circuit Board (PCB) technologies, demanding assembly techniques, and high cost of the SMD components themselves. These issues become particularly critical for systems with high channel counts and high density readout employing the front-end electronics built as multichannel ASICs implemented in modern CMOS technologies.

With continuous downscaling of the CMOS technologies the breakdown voltages of transistors are becoming lower and lower and for any CMOS device input protection is needed to prevent damages during handling and assembling of such devices. Therefore, the problem of Electro Static Discharge (ESD) is being continuously investigated in the field of CMOS integrated circuits. The vendors of the CMOS technologies deliver recommended ESD protection circuits, which are qualified according to the standards used in the electronics industry. Within these standards the voltages vary in the range from 2kV to 10kV. Although the voltages are comparable with the voltages used for biasing the MPGDs the equivalent electrical circuit of a MPGD is different compared to the circuit used in the ESD protection. First of all, in case of a discharge occurring in the MPGD the resistance of the discharging path is much lower. Thus, a protection circuits against discharges in MPGDs have to handle much higher currents and the typical circuits recommended for protection against ESD are not adequate at all.

On the other hand, immunity of the front-end circuit against sparks occurring in MPGDs depends on the design of the front-end circuit itself, in particular on its input impedance. Therefore, the input protection circuit should be tuned specifically for a given type of the MPGD and given design of the input stage if one wants to minimize additional capacitance and resistance at the input, which will affect the noise performance of the system.

We demonstrated before \cite{1} that integrated input protection could be quite robust against discharges expected in MPGDs. However, the prototype circuit was designed using a conservative approach resulting in large input capacitance. In this paper we will present test results of newly designed input protection structures. These structures have been designed using smaller devices resulting in smaller input capacitance. In addition, structures with series resistors have been implemented, which allow us to evaluate the trade-off between the input capacitance and the series resistance introduced by the protection circuits from the noise minimizing point of view. The ASIC was manufactured in the 350nm CMOS process.

\cite{1} T. Fiutowski et al.: Front-end electronics for Micro Pattern Gas Detector with integrated input protection against discharges, 2016 JINST 11 C01036

**POSTER** - Board: F3 / 150

**MGPA++ A Pre-Amplifier for CMS Barrel ECAL at HL-LHC**

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Upgrades are planned for the CMS barrel ECAL readout electronics. One option for an upgraded pre-amplifier is an improved version of the existing multi-gain pre-amplifier (MGPA). The upgraded MGPA is designed for shorter shaping time to optimize noise performance with photo-detectors damaged by radiation. It also has the ability to identify pulses generated by charge deposited directly in the photo-detectors rather than resulting from scintillation light.

Initial studies in ASIC design for an upgraded MGPA, together with work to evaluate the performance of the design are presented.

**Summary:**

The CMS barrel ECAL uses Avalanche Photo-diodes (APDs) attached to lead tungstate scintillating crystals. Signals from the APDs are amplified by a charge sensitive pre-amplifier with multiple outputs (MGPA). The outputs are sampled at 40 MSample/s by ADCs with 12-bit resolution.

Upgrading the CMS barrel ECAL pre-amplifier will maintain performance at a high-luminosity LHC. Radiation damage in the APDs will increase the leakage current so the shaping time will need to be reduced to optimize the signal to noise ratio. In addition it is necessary to identify pulses generated by charge deposited directly by ionising radiation in the APDs rather than resulting from scintillation light. Currently these pulses are identified and rejected offline with little rejection possible on-line. At a high-luminosity LHC pulses from direct charge deposition would result in an unacceptably high trigger rate.

The current MGPA has three outputs with a relative gain of 1:6:12 with the amplitude of the output pulses being proportional to the total charge of the input pulse. The outputs of the MGPA is sampled at 40 MSample/s by ADCs with 12-bit resolution. Advances in ADC technology mean that it will be possible to design the upgraded MGPA with only two outputs charge sensitive outputs and use ADCs with a higher sample rate and possibly higher resolution.

Charge deposited directly in the APD results in pulses that are shorter in time than pulses generated by scintillation light. By having an additional output that responds to the peak height of the pulse, in addition to the outputs that respond to the total charge of the pulse, the upgraded MGPA allows pulses from direct charge deposition to be identified.

Initial design studies into ASIC design of an upgraded MGPA are presented together with initial results from both simulation and laboratory tests.

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**POSTER - Board: B2 / 161**

**A Temperature Compensated Triple-path PLL for DUNE Experiments**

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Many HEP applications require circuits to continuously operate over large temperature range. In particular, the DUNE experiment requires circuits be capable of operating at cryogenic temperature. We present a novel temperature-compensated triple-path PLL (TP-PLL) for this application. The TP-PLL is capable of automatically compensating its frequency as temperature changes while maintaining stable operation and good jitter performance. A prototype TP-PLL at 2.56GHz has been implemented using 65nm CMOS process. It occupies an area of 0.08 mm2, consumes 13.2 mW, and has a frequency drift reduction by 99%.

**Summary:**

Phase-locked loops (PLL) is a key circuit block in data links for High-Energy Physics (HEP) applications. Once started, the data links are required to work continuously with very low bit error rate over a wide operation temperature range. In particular, the DUNE experiments require data links be capable of continuously operating at cryogenic temperature of 77 K for 20-30 years.
We present a novel triple-path PLL (TP-PLL) that is capable of automatically compensating the VCO frequency drift over large temperature variations in a closed loop manner meanwhile maintaining stable bandwidth and low phase noise and jitter. The VCO in the presented TP-PLL has three control paths, the proportional path (PP), the integral path (IP), and the temperature compensation path (TCP). Each of the three paths employs its own varactor in the VCO LC tank for frequency tuning. First of all, the main PLL loop is split into two paths, the IP and the PP. Each of the PP and IP has its own charge pump and a portion of the loop filter: a resistor in the PP and a capacitor in the IP. The separation of the IP and PP allow for individual control on the gain of each path, resulting in well defined and almost fixed control voltage on the PP to maintain good phase noise of the VCO. Second, an auxiliary path, the TCP, is added to the main PLL loop. The TCP employs a large VCO gain (KVCO_TMP) to effectively compensate for the VCO frequency drift over large temperature change. It consists of a gain stage and a low-pass filter, which detects and amplifies the voltage change on the main control path and based on this information tune the TCP varactor to compensate for the VCO frequency drift. Since the temperature compensation is done on the TCP loop, not the main loop, the bandwidth and stability of the PLL is kept intact. The separation of TC path from the PP and IP allows a very small VCO gain on the latter two, which is important to maintain low phase noise and spurs for the VCO and therefore low jitter performance of the PLL. In addition, the different gain settings on the PP and IP work as a capacitor multiplier, allowing for the implementation of a large loop filter capacitor using small silicon area.

A prototype chip utilizing the proposed trip-path architecture with a center frequency of 2.56 GHz was designed and fabricated in 65 nm CMOS technology. The VCO frequency temperature drift in the proposed TP-PLL is reduced by 99% around the center frequency. The TP-PLL chip occupies an area of 0.08 mm² and consumes 11 mA from 1.2 V supply voltage. The prototype chip was submitted for fabrication in Feb. 2016 and the measurement of the chip will be carried out in the summer of 2016 and results will be presented at the TWEPP conference.

**POSTER - Board: F1 / 79**


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We present the development of uTRiG, a mixed signal Silicon Photomultiplier readout ASIC in UMC 180nm CMOS technology, dedicated to the Mu3e experiment. It extends the ultra-fast timing performance of the STiCv3 chip with a fast digital readout for ultra-high rate applications. The high timing performance of the silicon proven, fully differential SiPM readout channels and 50 ps time binning TDCs are complemented by a redesigned digital readout logic and a gigabit data link, allowing event rates up to 1.3 MHz/channel. The design of uTRiG and the characterization results of the data link will be presented.

**Summary:**

uTRiG is a mixed signal Silicon Photomultiplier (SiPM) readout ASIC in UMC 180nm CMOS technology, being developed for ultra-fast timing and ultra-high rate applications. The ASIC is dedicated to the readout of
the tile detector and the fibre detector of the Mu3e experiment, which is searching for the lepton-flavour violating decay of $\mu^+ \rightarrow e^+ e^+ e^-$.

To reduce the combinatorial background at high rates and to facilitate event reconstruction, a good timing resolution of 100 ps sigma and 500 ps sigma is required for the Mu3e tile detector and the Mu3e fibre detector, respectively. An event rate as high as 1.3 MHz/channel poses another challenge for the development of uTRiG.

uTRiG will feature 32 fully differential analog front-end channels, 50 ps time binning TDCs and a digital part to process and transfer the event data via a gigabit LVDS serial link with 8b/10b encoding to the Data Acquisition (DAQ) system. It benefits from the development of the STiCv3 ASIC by inheriting the analog front-end and the TDC, which both have been silicon-proven to provide excellent timing performance.

To cope with the high event rate, a customized LVDS transmitter cell has been developed to boost the data transmission rate of the chip to 1.28 Gbps. A single-ended to differential pre-driver and a Bridge-Switched Current Source LVDS driver with common-mode feedback have been implemented, both optimized for a gigabit data transmission rate using 1.8 V transistors. A prototype ASIC was fabricated in 2015 to validate the LVDS transmitter cell, also including a demonstrator digital part with a dual-edge serializer cell to transfer data at both the rising and the falling edge of the driving clock. Preliminary tests has showed that the performance of the LVDS data link exceeds the requirements of the Mu3e experiment.

An external validation functionality is also implemented to reduce the load of the LVDS data link. The event data recorded by the analog front-end and the TDC will stay in the FIFO memory and will not be read out without an external validation signal. The arrival of the external validation signal opens a matching window, selecting the valid event data to be read out. The offset and the width of the matching window is 1.6 us and 3.2 us at maximum respectively. Both can be configured with a resolution of 200 ns. The external validation functionality can be turned off such that all the recorded data will be read out.

The design of uTRiG and the characterization results of the LVDS data link will be presented.

**POSTER - Board: D3 / 59**

**Pixel Architectures in HV/HR CMOS Process for ATLAS Inner Detector Upgrade**

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Some pixel architectures designed in LFoundry 150 nm HV CMOS process for the ATLAS Inner Detector upgrade will be presented. These pixels can be readout standalone or can be connected to
the FE-I4 readout chip via bump bonding or glue. Negative high voltage is applied to the HR (>2 kOhms.cm) substrate in order to deplete the DNW (Deep N-Well) charge collection diode, ensuring good charge collection and radiation tolerance. In these pixels, the front-end has been implemented inside the diode using both NMOS and PMOS transistors. The pixel pitch is 50 µm x 250 µm for all pixels.

Summary:

In this work, some pixels designed in LFoundry 150 nm HV CMOS process and implemented in a sensor demonstrator chip LFCPIX developed for the upgrade of the ATLAS Inner Detector will be presented. Modern CMOS processes offer multiple well structures in order to isolate the MOS transistors from the substrate. Thanks to this feature, it is possible to implement the pixel front-end electronics inside a DNW that forms also the cathode of a charge collection diode. It is possible to apply a high voltage (about -100 V) to the substrate without changing the operating parameters of the transistors.

Firstly, a new CSA (Charge Sensitive Amplifier) with complementary NMOS and PMOS input transistors has been proposed and designed for this pixels. The two input transistors contribute to the total transconductance of the input stage, improving speed and noise performances for a given power dissipation. Four different pixel flavors compatible with the input of the FE-I4 chip have been designed using all this new preamplifier.

The first pixel flavor generates a negative analog pulse proportional to the impinging particle. The signal is inverted using a low-gain amplifier. The second one generates a saturated negative pulse thanks to a high gain inverting amplifier. There is also a second version of this pixel with offset-correction of the amplifier using an in-pixel 4 bit DAC. The last pixel uses the classical approach using a preamplifier and a discriminator with in-pixel DAC based offset correction. The hits are memorized on a latch in the two last pixels.

The bias current of the preamplifier is ~14 µA, and the total bias current of the pixel is ~20 µA including the discriminating stage. Simulations show an input referred noise of ~130 e- and a peaking time ~20 ns. The TW (Time Walk) of the discriminator is less than 10 ns and needs a priori no TW compensation in this process.

All these pixels have been implemented in a demonstrator chip submitted to fabrication in March 2016. The pixel size is 50 µm x 250 µm for all pixels. The layout of the pixel has been optimized carefully to minimize coupling from digital signals into the collection diode. A special chip level bias circuit for the pixels was also designed and implemented in this chip. This circuit, which is a regulator, provides an adjustable bias current for all in-pixel preamplifiers.

The first preliminary experimental results of these pixels are expected at the time of the conference.

POSTER - Board: E5 / 46

Multiple Use SiPM Integrated Circuit (MUSIC) for SiPM Anode Readout

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This paper presents an 8 channel ASIC for SiPM anode readout. The Multiple Use SiPM Integrated Circuit (MUSIC) is based on a low input impedance current conveyor (patented). It provides a differential channel summation and individual SE (analog or ToT) channel readout. MUSIC is designed using AMS 0.35um SiGe technology. Full die simulation yields these specifications: 500MHz bandwidth for channel sum and 150MHz for individuals channels, output pulse width at half maximum
Summary:

Many radiation detectors in astrophysics, particle physics, medical imaging and other fields utilize multi-anode PMTs (Photo Multiplier Tubes) or PMT with large photo-cathode area (1 inch or more). Recently, Silicon Photomultipliers (SiPMs) sensors have become candidates to substitute PMTs due to their high gain, fast response, high quantum efficiency and low-amplitude after-pulses.

This paper presents MUSIC (Multiple Use SiPM Integrated Circuit), an 8 channel ASIC for SiPM anode readout. It is devised to fulfill several purposes, including the readout of SiPM arrays in cameras for Gamma-Imaging Atmospheric Cherenkov Telescopes (IACTs), either in summation or in individual channel mode (analog or Time-over-Threshold).

A novel low impedance input stage based on bipolar current mirrors with double feedback loop is used for SiPM anode readout (patented). The low frequency feedback loop controls the DC voltage at the input node, whereas the high frequency feedback path keeps low input impedance over high signal bandwidth. This kind of input stage allows for summing the currents delivered by SiPMs without adding together their capacitances, so that the timing behavior of the SiPM is not affected. The input current from the sensors is copied and scaled at the readout stage in order to implement different functionalities, as detailed next:

- The summation of any combination of readout channels is provided as a dual-gain output in differential mode.
- 8 individual single ended analog outputs.
- 8 individual binary outputs encoding the amount of charge in the width of the output pulse, using the technique called time-over-threshold.

Note that for each individual channel the user must select either the analog or binary output, since both signals share the same output pad. As additional features, MUSIC includes: (1) a trigger pulse obtained by performing a fast OR between any selection of digital signals and (2) 8 output currents for an external slow integrator. Moreover, the circuit can make use of a tunable pole zero cancellation (PZ) of the SiPM recovery time constant (up to 100 ns) to deal with sensors from different manufacturers (it can be bypassed in any operational mode). Each main functionality (sum or A/D) has a selectable dual-gain mode. Lastly, any block and channel can be disabled (power down mode) with a specific control signal.

MUSIC is designed using AMS 0.35 μm SiGe technology. Full die simulation yields the following specifications: (1) Total die size of 9 mm²; (2) 64-QFN 9x9mm package; (3) bandwidth of 500 MHz for the differential channel sum output and bandwidth of 150 MHz for single ended A/D channel outputs; (4) low input impedance (∼32Ω); (5) single photon output pulse width at half the maximum (FWHM) between 5 and 10 ns; (6) power consumption of 30mW/ch for individual channels and 200mW for the 8 channel sum; (7) 15 bits dynamic range for summation and 10 bits for individual analog readout. Encapsulated samples will be tested in spring of 2016.

POSTER - Board: F5 / 148

A Low-Power 10-bit 250-MS/s Dual-Channel Pipeline ADC in 0.18 μm CMOS

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This paper presents a 10-bit 250-MS/s time-interleaved pipelined ADC. A distributed clocking scheme is developed to eliminate timing skew between channels without introducing load capacitance to the driving buffer. The channel offset and gain mismatch error is calibrated in digital domain. In addition, a switch-embedded opamp-sharing technique is developed to reduce ADC power consumption and eliminate the memory effect. The simulated SNDR and SFDR are 61.84 dB and 78.2 dB, respectively. The ADC core consumes 28mW under a 1.8V supply at 250 MS/s sampling rate.

Summary:

High-speed and radiation-tolerant ADC is widely needed for LHC upgrade and other collider detector developments. With continued scaling of CMOS technology, successive-approximation-register (SAR) ADC has recently become attractive for low-power medium-speed applications. However, for high-speed and high-resolution applications, pipeline ADC is still the most practical and cost effective solution. One of the key aspects in designing pipeline ADC is to achieve a high signal-to-noise and distortion ratio (SNDR) with good power efficiency.

Time-interleaved pipeline ADC is an effective approach to obtain both high-speed high-resolution and good power efficiency. This paper presents a 10-bit 250-MS/s dual-channel pipeline ADC. Each channel operates at 125 MS/s and consists of a sample-and-hold amplifier (SHA), eight 1.5 bit-per-stage MDACs, and a 2-bit flash ADC. The opamps of the SHA and MDAC are shared by the two channels utilizing a current-reused opamp-sharing technique. To reduce the ADC noise floor, a wider swing input signal (2Vpp) is used in the sampling network and then the input signal is attenuated to 1.6Vpp by the SHA to ensure the MDAC operate properly under the supply voltage of 1.8V. This improves the ADC SNR by reducing the noise contribution of the sampling network without suffering from the linearity degradation.

The time-interleaved pipelined ADC, however, exhibits offset and gain mismatch between channels and is sensitive to timing skew of the clocks distributed to them. The channel mismatch error is calibrated by obtaining the matched long-term mean and RMS values from the two channels and the calibration is based on a least-mean-square (LMS) scheme. To minimize the timing skew error, a single-edge distributed bottom-plate sampling network is developed. The sampling network ensures a precise symmetrical sampling clock that is also insensitive to clock duty cycle. To reduce the resistance of the switch in the sampling network, bootstrapped switch is used and an improved bootstrapped switch structure is developed to minimize the charge injection impact on the ADC performance. Furthermore, a switch-embedded opamp-sharing technique is developed to lower the ADC power consumption and to eliminate the memory effect.

The proposed 10-bit 250MS/s pipelined ADC is designed in a 0.18-μm CMOS technology. Simulation results show that the ADC core consumes 28mW of power under a 1.8V supply at 250 MS/s sampling rate. The simulated SNDR and SFDR of the ADC are 61.84 dB and 78.2 dB, respectively. The ADC will be submitted for fabrication in July and extensive electrical and radiation performance testing will be carried out. The testing results will be presented in the final paper.

POSTER - Board: D5 / 91

Characterization of the Column-Based Priority Logic Readout of Topmetal-II- CMOS Pixel Direct Charge Sensor

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We present the detailed study of the digital readout of Topmetal-II- CMOS pixel direct charge sensor integrated 72x72 pixels each capable of directly collecting charge through exposed metal electrodes in the topmost metal layer. In addition to the time-shared multiplexing readout of the analog output from Charge Sensitive Amplifiers in each pixel, hits are also generated through comparators with individually DAC settable threshold. Hits are read out via a column-based priority logic, pertaining both hit location and time information. We study the detailed working behavior and performance of this readout and demonstrated its potential in imaging applications.

Summary:

We have successfully implemented a CMOS IC, Topmetal-II-, for direct charge collection and imaging. It is a highly pixelated sensor with 83 µm pitch between 72x72 pixels fabricated in a standard 350 nm CMOS technology. The sensor utilizes exposed metal patches on top of each pixel to directly collect the charge. Each pixel contains a low-noise charge sensitive preamplifier (CSA) to establish the analogue signal and a discriminator with a tunable threshold to generate hits. Hits are read out digitally through a column-based priority logic scheme. A Priority Logic Module in each pixel responds to the output of the comparator, which compares the CSA output to a set threshold. A Column Read Module reads the hit and resets the pixels. A digital multiplexer (MUX) polls the status of each Column Read Module and assembles the hit pixel’s address and time information, then ships them off the sensor. The threshold is set by a 4-bit DAC in each pixel, aiming to reduce the spread of the Baseline and Transition in the whole pixel array.

Firstly, we disable all the 4-bit DACs and set the proper level for the baseline of the discriminator. Then, we apply the external trigger to excite each pixel and scan the reference voltage of the discriminator by a few steps. Through this scanning, both the number of hits and injected pulses will be recorded via the Data Acquisition (DAQ). Based on the DAQ analysis, we’re able to draw the S-Curve for each pixel. Moreover, we plot the distributions and histograms of both Baseline and the Transition. According to these preliminary results, we developed a software module to generate the configuration data for 4-bit DAC for every pixel. Afterwards, we retest and redraw all the plots. The results show that the sensor achieves a threshold distribution of the whole matrix with Mean = 13 mV, RMS = 3.4 mV, and the RMS value of both Baseline and Transition reduce by a factor of 5 with proper 4-bit DAC settings. Additionally, the step size of 4-bit DAC has also been proved to have good uniformity with Mean = 9 mV, RMS = 0.4 mV.

We operated the Topmetal-II- sensor at an identical setting as in the digital readout tests. A purple LED was driven by a narrow pulse to emit a beam of light with wavelength = 390 nm, filtered by a “T” shaped photo-mask. Since the sensor was quite sensitive to the light, the irradiated pixels reacted to generate hits. We successfully reconstructed the image of a perfect “T” on the sensor. In this experiment, we also measured and analysed the 10-bit time information of pixel hits, which verified the correctness of the readout implementation.

To improve the performances of Topmetal-II-, besides decreasing the Mean value of the threshold for each pixel, we can further reduce the distribution of both Baseline and Transition values. Most of these optimizations are ongoing in future series of Topmetal sensors.

POSTER - Board: B3 / 26

2.5Gb/s Simple Optical Wireless Communication System for Particle Detectors in High Energy Physics

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We successfully demonstrated simple and low cost 2.5 Gb/s optical wireless transmission at 10 cm distance, aiming to be employed in high-energy physics experiments using off-the-shelf VCSEL and PIN photodiode with proper ball lens. The measured tolerance to misalignment is around ±1mm at Bit Error Rate of $10^{-12}$.

Summary:

Particle physics experiments generate large amounts of data, whose transmission requires huge infrastructure of optical fibers. This increases the material budget, limits space and also introduces excessive labor cost for cables installation and management. High-speed Optical Wireless Communication (OWC) can be a viable solution to reduce the complexity of optical fiber networks for future upgrades. We are designing an OWC system for particle detectors, having as a reference application the inner tracker of Compact Muon Solenoid (CMS) operating in Large Hadron Collider (LHC) at CERN. The proposed OWC solution is not intended to completely substitute the optical fiber links, but it will be rather used to introduce the radial connectivity between silicon strip sensors.

We have designed a 2.5 Gb/s OWC link, which comprises a VCSEL (1550nm) transmitter and a PIN photodiode with ball lens at 10 cm of transmission distance. In future, this simple and low cost design may be integrated on silicon strip sensors inside CMS or other short distance links in particle detectors.

After careful design of the receiver, we achieved a tolerance to misalignment in the range of ±1mm, which is important because, only passive alignment in range of ±0.25 mm is acceptable in particle detector systems. In this paper, we report the design of the OWC link and detailed tolerance to misalignment study, based on different diameter lenses at the receiver. By this analysis, we designed the custom packaging for the photodiode and a 4mm ball lens. The results of this activity will also be presented in the paper.

We are aiming to deploy the OWC link in high energy physics environment therefore, we have selected VCSEL and InGaAs PIN photodiode because of their radiation tolerance [J. Troska et al, IEEE Trans on Nuclear Sci, 58, 6, Dec 2011]. Moreover, we selected fused silica and quartz glass type lenses, since they only can provide proper irradiation properties, i.e. much better than BK7 glass at 1550nm [S.M. Javed Akhtar., et al, Optical Materials, Vol 29, 12, Aug 2007]. Since these glass types are still tested for lower dose in future we will plan irradiation test in order to qualify the optical components and especially the lens in environments with high radiation level.

**POSTER - Board: B1 / 47**

**Versatile Transceiver Production and Quality Assurance**

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The Versatile Link project has developed a radiation-hard optical link for LHC phase 1 detector upgrades. The project has reached its final stage and we have launched the series production of the Versatile Transceivers (VTRx) and Versatile Twin Transmitters (VTTx). This paper provides an update of the production status and a detailed description and results of the quality assurance programme. The QA programme includes qualification and acceptance testing at CERN and production testing at the manufacturer’s premises.

**Summary:**

The LHC detector upgrades planned for LHC long shutdown 2 will increase the bandwidth requirements on the optical links. The Versatile Link common project has developed an optical link architecture operating at 4.8 Gbps that foresees radiation-hard, low-mass and low-power opto-electronic transceiver modules to be deployed in the upcoming upgrades. The modules are available in three versions: single-mode and multi-mode Versatile Transceiver (VTRx) operating at 1310 nm and 850 nm, respectively, and multi-mode Versatile Twin Transmitter (VTTx) operating at 850 nm. The choice among these versions depends on the architecture of the readout system as well as on the fibre plant already present in the experiments.
The front-end components in the LHC experiments, including VTRx and VTTx modules, are situated in an extremely harsh environment where they have to withstand high radiation doses and strong magnetic fields. VTRx prototypes have previously been thoroughly tested during the development phase and the selected parts have been validated for the final assembly. During the series production CERN will deliver qualified known good active components (transmitter sub-assemblies, receiver sub-assemblies, and laser drivers) to the chosen assembly house, which will assemble and test around 30,000 modules.

The VTRx quality assurance programme includes qualification tests, production tests, and lot acceptance tests. First, before the active components are delivered for assembly, component qualification tests are carried out at CERN to ensure that they meet the Versatile Link specifications. Then the components are delivered for assembly and pre-production of a few hundred modules. The pre-production devices go through functional and environmental tests including temperature, magnetic field, and irradiation tests, which will be described in detail in this paper. After a successful pre-production qualification the series production will be launched.

During production the modules are tested at the assembly house using a test setup and procedure developed by CERN. The test setup measures automatically the main parameters, checks that the specifications are met, and saves the results into a database. An operator is required only to change the DUT, start the measurement, and monitor the results. The production testing covers 100% of the modules. At CERN, received modules will be checked once more in lot acceptance tests. This final stage of quality control includes visual inspection and functional tests in lab environment for a randomly selected subset of modules from each received lot. The lot acceptance tests ensure that the modules are received in a perfect condition. It also serves as a cross-check for the production test results.

Traceability is guaranteed by identification (ID) numbers marked on the modules. The results from each stage of the QA programme are saved with the ID information and can be monitored. Details of the stored data and results that are available for the users and QA reports will be provided.

**POSTER - Board: 89 / 130**

**First Implementation of a Two-Stage DC-DC Conversion Powering Scheme for the CMS Phase-2 Outer Tracker**

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A novel, 2-step DC-DC conversion powering scheme will be used for the “2S” silicon strip modules of the HL-LHC CMS tracker. Each module is equipped with a service hybrid, which carries two DC-DC converters along with a LP-GBT and a VTRx+ module. The first DC-DC converter generates 2.5V, required for the opto-electronics, while the second stage converts 2.5V to 1.25V, required for all other ASICs. We will present a service hybrid prototype, describe its performance and demonstrate the feasibility of an on-module, 2-step powering scheme with system tests.

**Summary:**

The challenging conditions at the HL-LHC necessitate a replacement of the CMS Tracker in 2026. The module concept is driven by the requirement that tracker information is to be used in the Level 1 trigger. The dependence of the track bending angle in the magnetic field on the transverse momentum (pT) is exploited and high transverse momentum tracks are identified by comparing hit patterns in closely spaced sensor layers. So-called pT modules carry two sensors with a distance of a few millimetres; two strip sensors are used for radii above 60cm (2S modules), while one strip and one macro-pixel sensor are used for smaller radii.
The modules require two supply voltages: about 1.25V for the readout chips (e.g. the CBC), a data concentrator ASIC (CIC) and the low power version of the GBT (LP-GBT), and 2.55V for the VTRx+ module that provides conversion between electrical and optical signals.

In order to reduce the material associated to cabling, and to limit power losses on the supply cables, CMS will adopt a DC-DC conversion powering scheme for its outer tracker. Since each module requires two voltages, a two-step scheme has been chosen. The first stage DC-DC converter receives 11V and converts this to 2.55V, while the second stage DC-DC converter converts 2.55V into 1.25V. Each module carries its two DC-DC converters, which are located on a PCB named “service hybrid”, together with the LP-GBT and the VTRx+. The service hybrid is mounted on one module side for 2S modules, and split into a power and a readout part – on two modules sides for the PS module. The distance to the sensors is only a few millimetres.

A first prototype of the service hybrid has been produced, which carries a FEAST2 DC-DC converter as first stage and a commercial DC-DC converter as second stage, along with a prototype VTRx+ module. A low mass shield made from a 150µm thick aluminium foil covers both DC-DC converters. We present first results on using a 2-step DC-DC powering scheme for the CMS tracker, including both standalone characterization in terms of e.g. efficiency and conducted and radiated noise, as well as system tests with 2S module prototypes, using prototypes of the final power supply and realistic cabling. This work demonstrates the feasibility of the chosen concept.

**POSTER - Board: N7 / 120**

Spotting and Curing Noise Issues in the Silicon Vertex Detector of the Belle II Experiment

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The Belle II experiment will use a Silicon Vertex Detector based on DEPFET pixel (PXD) and double-sided microstrip (SVD) technology. In 2014 at a combined SVD/PXD beam test we observed electrical noise in the SVD system which caused many headaches for more than two years. Since then Electromagnetic Compatibility (EMC) tests using some of the best equipment available in an EMC tight hall, but also using cheap and even self-made probes helped to improve the SVD prototype. At another combined beam test in April 2016 we finally identified the noise source. It was not the suspected PXD...

**Summary:**

A new silicon detector based on two different technologies is planned to be installed in the Belle II experiment at the High Energy Accelerator Research Organization (KEK) in Tsukuba, Japan. It consists of several modules and Front End Electronics (FEE) arranged cylindrically in 6 layers around the interaction point. The inner two layers are based on DEPFET pixel technology (PXD), the outer four layers on double-sided microstrip technology (SVD).

The SVD consists of 172 silicon sensors. A total of 1748 readout chips (APV25) process and send the analog signals over 15 meter long copper cables to 48 A/D Converter (FADC) boards located in crates on top of the Belle II detector structure. From the FADCs the data are then sent out to the central DAQ by optical fibers.

Several power supply units located near the FADC crates provide the High Voltages (+/-50V) required to bias the sensors, and the Low Voltages (LV, 10V) to power the FEE. Fifteen meter long cables transport the power into the magnetic and radiation zone to dock boxes, where DC/DC converters transform the LV into 2.5V and 1.25V, which are then fed into the the APV25 chips on the sensor hybrids by 2.5 meter long cables.

A combined SVD/PXD beam test in January of 2014 at DESY in Hamburg, Germany, revealed excessive noise in the SVD system which rendered the data almost useless. No-one of the involved persons was
prepared; no-one really knew how to measure and to handle it systematically; it has been cured partially using some grounding wires as a trial-and-error-approach with the success that the data taken were at least somehow usable. The main suspect for the source of this noise then was the PXD for more than two years.

After this experience the Electromagnetic Compatibility (EMC) of the SVD system has been investigated systematically, mostly 2015 in a semi-anechoic hall in Zaragoza, Spain, using some of the best EMC measurement equipment available, but also in the HEPHY laboratory using relatively cheap and even self-made equipment. The conclusions were implemented into the SVD system afterwards. The system has been tested without noise issues at two test beams at CERN.

In April 2016 the next combined SVD/PXD beam test took place again at DESY. The noise was observed again, but the SVD system now proved to be immune against it. Despite that the SVD noise susceptibility has been measured systematically using a dedicated spectrum analyzer, but also some affordable equipment: self-made inductive probes and self-made current shunts on an USB oscilloscope. As a result, the noise source finally was located. It was not the PXD. And it probably would not have been found using only a spectrum analyzer...

This presentation shows on the Belle II SVD system how conducted noise can be identified systematically, how EMC test equipment can be used, how some of it even can be self-made, and how we immunized our system.

**POSTER - Board: N8 / 160**

**An Advanced Power Analysis Methodology Targeted to the Optimization of a Digital Pixel Readout Chip Design and its Critical Serial Powering System**

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A dedicated power analysis methodology, based on modern digital design tools and integrated with the VEPIX53 simulation framework developed within RD53 collaboration, is being used to guide vital choices for the design and optimization of the next generation ATLAS and CMS pixel chips and their critical serial powering circuit (Shunt-LDO). Power consumption is studied at different stages of the design flow under different operating conditions. Significant effort is put into extensively investigate dynamic power variations in relation with the decoupling seen by the powering network. Shunt-LDO simulations are also reported to prove the reliability at the system level.

**Summary:**

New hybrid pixel detectors supporting hit rates up to 3GHz/cm2 and unprecedented radiation levels will be developed by the RD53 collaboration between ATLAS and CMS experiments at HL-LHC. In this scenario the design of complex digital logic at the lowest possible power consumption requires special techniques to develop a reliable system. This is dictated by the need for a serial powering scheme, required to overcome the insurmountable limits of a standard parallel powered mode for system modules featuring high granularity.

In this context, the baseline scheme features modules placed in series and powered by a constant current. The Shunt-LDO circuit, composed of a LDO regulator generating the low supply voltage and a shunt consuming the current not drawn by the load, will be used. Therefore, the constant current flowing in the serial power chain will be determined by the maximum current required by the chip, which should be minimized. These requirements demand a different approach with respect to well-established
digital low power methodology. In this work a dedicated power analysis methodology, based on modern digital design tools and integrated with the VEPDX53 simulation framework developed within RD53 collaboration, is defined to guide vital choices for the design and optimization of both the chip and the Shunt-LDO.

The methodology presented is applied to a 65 nm pixel array, featuring similar characteristics to the foreseen RD53 pixel chip. Power behaviour is evaluated at different stages of the design flow, from early RTL/gate-level to detailed post P&R under different operating conditions. First, in order to drive architectural choices (e.g. critical use of clock gating) power estimations are performed at RTL/gate-level and power profiles are produced, thanks to the definition of an iterative algorithm. Simulations performed under RD53 operating conditions show a significant increase in power consumption when excluding any form of clock gating in the architecture, less tolerable than the power variations caused by it. Second, more detailed power analysis (post P&R) is necessary to provide accurate specifications to the powering system, whereas gate-level analysis shows around 50% underestimation. Average power estimations are obtained under different corners and activity conditions (e.g. extreme hit and trigger rate, consecutive triggers, high hit rate and trigger absence, just clocking the logic), in order to assess power impact of different factors, important to understand variations in different operation modes and guide design choices. Power variations, particularly critical for the target system, are also studied with extensive power profiling under the variety of operating conditions. Moreover, since low-pass filtering will be seen from the chip to the serial power network (due to on-chip decoupling, shunt-LDO decoupling, module decoupling), power peaks are evaluated at different time constants (1ns, 25ns, 100ns, 1 μs, 10 μs) and qualified on-chip decoupling estimation is performed to identify the critical time constant. Power profiles are also used as an input to Shunt-LDO simulations to verify its functionality and demonstrate the reliability of the powering scheme.

**POSTER** - Board: N6 / 140

**High Precision, Low Disturbance Calibration of the High Voltage System of the CMS Barrel Electromagnetic Calorimeter**

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The CMS Electromagnetic Calorimeter utilizes scintillating lead tungstate crystals, with avalanche photodiodes (APD) as photo-detectors in the barrel part. 1224 HV channels bias groups of 50 APD pairs, each at a voltage of about 380V. The APD gain dependence on the voltage is 3%/V. A stability of better than 60 mV is needed to have negligible impact on the calorimeter energy resolution. Until 2015 manual calibrations were performed yearly. A new calibration system was deployed recently, which satisfies the requirement of low disturbance and high precision. The system is discussed in detail and first operational experience is presented.

**Summary:**

The CMS Electromagnetic Calorimeter (ECAL) utilizes about 76000 lead tungstate (PbWO) scintillating crystals, the light from which is detected by Avalanche Photodiodes (APDs) in the central "barrel" region. The APDs were produced by Hamamatsu in collaboration with the CMS Experiment. Two APDs are glued on each crystal and are operated at gain 50 with a bias voltage of about 380 V. The High Voltage (HV) system consists of 1224 channels biasing each 50 APD pairs.

The requirement of the HV system to have an impact on the energy resolution of less than 0.2% translates into a needed voltage stability of better than 60 mV per month. All the HV boards were qualified prior installation and satisfy this requirement. Variations on a time scale longer than a month can be corrected for by the detector calibration with physics events.

The HV system utilizes CAEN A1520PE boards, located in the CMS.
service cavern and connected to the APDs via 120-m long cables. The HV channels use sense wires to correct for HV changes at the load.

In order to avoid inducing noise on the calorimeter signal measurement, the HV system was not equipped with a continuous monitoring system, but periodic monitoring and calibration campaigns are performed.

Until 2015 this operation was done manually, un-cabling the system in the service cavern and calibrating one by one all the HV boards with a precision multimeter. Due to the long time required to perform this operation, and to reduce mechanical stress on the hardware, the HV calibration was done once per year during the LHC winter shutdown.

A new calibration system was deployed at the end of 2015. It consists of mechanical switches, that can connect the high voltage cables to the CMS detector or to the calibration system, guaranteeing that no additional noise is introduced. Calibration cables draw the bias to a precision multimeter through a set of multiplexers. The calibration program cycles through all the channels allowing both to measure the voltage and to recalibrate the channels one by one if needed. The new HV calibration system is discussed in detail, along with first operational experiences.

**POSTER - Board: N5 / 36**

**System-Level Considerations of the Front-End Readout ASIC in the CBM Experiment from the Power Supply Perspective**

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Paper presents the Silicon Tracking System low-voltage power system design starting from the power budget and noise spectrum requirements resulting from the front-end chip design (STS/MUCHXYTER2). Power-supply rejection ratio simulation results, estimation on how the simulated and measured noise spectra of the voltage regulators would affect the front-end electronics, power budget and selection of feasible powering scheme in the experiment including aspects of area, power efficiency and radiation hardness will be presented.

**Summary:**

New fixed target experiments using high intensity beams up to 10 AGeV from SIS100 synchrotron presently being constructed at FAIR/GSI center are under preparation. Most of the readout electronics and power supplies are expected to suffer very high flux of nuclear reaction products and have to be radiation hard up to 3 MRad and sustain up to $10^{14}$ cm$^{-2}$ of 1 MeV neutron equivalent in their life time. Moreover, the minimum ionising particles under investigation leave very little signals in the sensors therefore very low noise level amplitude measurements are required by the front-end electronics for effective tracking. Sensor and interconnecting microcable capacitance and series resistance in conjunction with intrinsic noise of the charge sensitive amplifier are dominant noise sources in the system, however, single-ended architecture of the amplifiers used in the charge processing channels implicit potential problem with noise contribution from the power supply sources. Strict system-level constraints leave very little freedom in selecting power supply structure optimal with respect to: power
efficiency, power density on modules and cooling capabilities, but also noise injection to the front-end via the power supply lines. Noise level simulations of front end ASIC’s (STS/MUCH-XYTER2) and measurements’ results of power supply and conditioning electronics (selected DC/DC converter and LDO regulators) will be presented together with power supply structure in the Silicon Tracking System.

POSTER - Board: K5 / 89

Testing of Hybrid Circuits for the CMS Tracker Upgrade of Front-End Electronics

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The upgrade of the CMS tracker for the HL-LHC requires the design of new double-sensor, front-end modules, which implement L1 trigger functionality in the increased luminosity environment. These new modules will contain two different, high density front-end hybrid circuits, equipped with flip-chip ASICs, auxiliary electronic components and mechanical structures. The hybrids require qualification tests, before they are assembled into modules. Test methods are proposed together with their corresponding testing hardware and software. They feature functional tests and signal injection in cold environment aiming at finding the possible failures of the hybrids under real operating conditions.

Summary:

The future HL-LHC is imposing demanding requirements on its particle detectors. The luminosity increase results in higher radiation and data rate. A major upgrade of the CMS Tracker is foreseen to cope with these new constraints. It is designed to provide the most useful and accurate information about the trajectories of the collision products. To achieve these goals several features are implemented at the level of front end modules, such as lower mass, Level 1 track triggering functionality and a higher density of channels.

The future tracker structure is made of different versions of double-sensor modules that vary in the distance between their sensor planes and the type of sensors. Each module contains two high density front-end hybrid circuits. These hybrids host binary readout ASICs which are connected with strip sensors. Additionally, each hybrid is equipped with auxiliary electronic components and mechanical reinforcement structures, which also serve as a cooling interface. In total ten different hybrid geometries are foreseen in the design of the future tracker. It is planned to produce as many as thirty thousand pieces.

The hybrids need to be tested before they are used for module assembly. This step is crucial to ensure a high yield of fully functioning modules. The testing should allow tracking all possible failures affecting hybrid performance. The hybrid tests will be performed at room and low temperature by cooling hybrids directly via their thermal contacts. The low temperature testing is intended to be representative of the tracker operating conditions, requiring a specifically designed testing infrastructure with a humidity condensation protection feature.

The hybrid test parameters cover: the power consumption of the hybrid, the ASICs control registers accessibility, the functionality of input channels and fast data output interfaces. The input channels are connected with fine tracks to the bump bond pads on the front-end chips which cannot be visually inspected. The continuity must be specifically verified by other means. Developing a fast and reliable method for checking connectivity and functionality of all these channels has become a priority. The continuity checking techniques have been initially verified on prototype circuits based on CMS Binary
Chip 2 (CBC2). Several testing methods have been investigated for ease of implementation, repeatability and accuracy. One method which has been extensively investigated is a contactless charge injection system. Early implementations of this method have demonstrated its effectiveness, and have uncovered a weakness in the response of the CBC2 to simultaneous stimulation of many channels, which will be corrected in the next version of the chip.

The performance results of the proposed testing methods are presented from the point of view of accuracy, difficulties of physical implementation and duration of the test process. This study was conducted with a view to the development of a common protocol for hybrid circuits testing.

POSTER - Board: K4 / 173

Test Strategies for Industrial Testers for Converter Controls Equipment

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Power converters and their controls electronics are key elements for the operation of the CERN accelerator complex. To achieve a high MTBF of the system, a set of industrial testers for the converters controls electronics is used. The paper is a follow-up after a similar paper at TWEPP2015, including more test platforms (Boundary-Scan) and the outcome after test phase in production. We report on the test software and hardware design and test strategy applied for a number of devices, that resulted in maximizing the test coverage and minimizing the test design effort.

Summary:

Power converters and their controls electronics are key elements for the operation of the CERN accelerator complex, having a direct impact on its availability. To achieve a high MTBF (Mean-Time-Between-Failure) of the system and easy ways to verify equipment, a set of industrial testers for the converters controls electronics is used. In the manufacturing phase and to provide means to validate and repair failed modules, the roles of the testers are to validate mass production. The TE-EPC-CCE section, two main test system platforms were adopted: a PXI platform for mixed analogue-digital functional tests and a JTAG-BS (JTAG Boundary-Scan) platform for digital interconnection and functional tests. Depending on the functionality of the device under test, appropriate test platforms were chosen. The paper is a follow-up after a similar paper at TWEPP2015, including more test platforms (Boundary-Scan), and the outcome after test phase in production. We report on the test software and hardware design and test strategy applied for a number of devices, that resulted in maximizing the test coverage and minimizing the test design effort.

POSTER - Board: B7 / 30

Lessons Learned in High Frequency Data Transmissions Design

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HEP experiments requirements lead to highly integrated systems with many electrical, mechanical and thermal constraints. A complex performance optimisation is required. High speed data transmission lines are designed, while simultaneously minimising radiation length. Methods to improve the signal integrity of point to point links and multi-drop configurations are described. FEA calculations are essential to the optimisation which allow data rates of 640 Mbps for point to point links over a length of up to 1.4m, as well as 160 Mbps for multi-drop configuration. The designs were validated using laboratory measurements of S-parameters and direct BER tests.

Summary:

High speed transmission is required for data and trigger propagation in HEP experiments. The ATLAS ITk strips require point to point data transmission at 640 Mbps and multi-drop transmission at 160 Mbps over distances of up to 1.4m. Many constraints such as radiation length, thermal conductivity, grounding etc. require custom solutions. The optimal solution for the ATLAS ITk strips involves highly integrated systems based on carbon fibre structures. Complex optimisation of signal integrity, radiation length, electrical and thermal performance is required. As carbon fibre is electrically conductive it must be integrated into the grounding scheme. However it is a poor conductor, and should not be used in transmission lines. The dominant loss mechanism for our application is resistive loss. The theory is reviewed to explain the slow turn-on and how this leads to dispersion. Ways of combating this effect using data encoding and pre-emphasis are described. The advantages of microstrip and stripline configurations are reviewed from the perspective of minimising material. Multi-drop lines are attractive for distribution of clock and trigger with minimal material. These lines suffer from reflections from each load. FEA calculations are used to predict the magnitude of the losses. Several methods to minimise these losses are discussed. Laboratory measurements of S-parameters for 1.4 m long ITk strip bus tapes have been performed for point to point links and multi-drop lines. They are compared to FEA of the transmission lines. The measured S-parameters are then used to predict "eye diagrams". Good eye-opening was achieved for the longest lines and improvements with data encoding and pre-emphasis were studied. The multi-drop lines showed large reflections at high frequency, as expected from the FEA calculations. The reflections result in signal loss and ringing which generates Inter Symbol Interference. However the computed eye diagrams still showed reasonable eye opening at 160 Mbps, even with 28 capacitive loads along the line. Ideas on how to improve the signal integrity are discussed including series inductors, back termination and reducing rise times. Test tapes were produced with identical transmission lines to those on the proposed ITk strip bus tapes. More direct measurements of the maximum data rates that could be achieved with these test tapes have been performed using a BERT system. These tests confirmed that low Bit Error Ratio (BER) could be achieved for the long lines at data rates in excess of 640 Mbps. It was demonstrated that a large increase in data rates could be achieved with the use of 8b10b encoding as expected from transmission line theory. The system was also used with representative loads to measure BER for multi-drop configuration, demonstrating viability of multi-drop configuration working at 160 Mbps. This work is relevant to the topics of integrated systems, links and trigger. FEA calculations have helped achieve the required data rates by optimizing the trade off between minimal material and sufficient electrical performance. The performance was validated with laboratory measurements of S-parameters and BER.

POSTER - Board: 12 / 40

A PCI DAQ Board Prototype after the ATLAS Pixel Detector IBL-Layer 1 and 2 ROD Cards

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The ATLAS Pixel detector has inserted an additional inner layer called Insertable B-Layer (IBL) that is read out via two boards: the Readout-Driver card (ROD) and the Back-of-Crate card (BOC). In this presentation we summarize first the experience of building and commissioning the boards to read out the ATLAS Pixel detector, with particular emphasis to the ROD card. In addition, here it is presented the design and the preliminary tests of a prototype card, backward
compatible with ATLAS Pixel Detector, which also features PCI express and GBT and other I/O interfaces.

Summary:

This paper summarizes first the experience of designing, building, testing and commissioning the boards to read out the ATLAS Pixel detector, with particular emphasis to the ROD card. The current ATLAS Pixel Detector is composed in particular of four layers: IBL, B-Layer, Layer 1 and Layer 2. Except the B-Layer, the others have been equipped with a new generation of VME readout cards to improve the readout speed and to interface with the new IBL detector. However, for the upgrade of the LHC experiments, the pixel detectors will need electronics with additional features to interface with newer readout systems. The prototypes are intended to extend the capabilities of the current ATLAS Pixel Detector readout system and this is why we planned to design a new readout board backward compatible to the pixel detectors, compatible to the current readout firmware, plus extendable to future features such as being interfaceable with PCI express and GigaBit Transceiver (GBT) ports. In this way the board can connect to optical fibers like those implemented in the LHC experiments to read out front-end silicon detectors and, at the same time, is able to interface with commercial GPU boards, which use PCI ports at very high speed. The new design features modern FPGA generations (Kintex and Virtex-7) to maximize the potential of the internal soft-core blocks, like transceivers and parallel-to-serial converters. Also, a commercial processor (ARM family) will be used to run all the embedded software currently implemented into the IBL ROD firmware.

POSTER - Board: C3 / 169

Design of a Radiation Tolerant System for Total Ionizing Dose Monitoring Using Floating Gate and RadFET Dosimeters

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The necessity to improve the accuracy of the Total Ionizing Dose (TID) measurements at CERNs’ radiation zones, has driven the research of new TID-measuring candidates. For this purpose, a TID Monitoring System (TIDMon) is designed, that investigates the effects of the TID on a Floating Gate Dosimeter (FGDOS) compared to Radiation-sensing Field-Effect Transistors (RadFETs). The monitoring system is characterized inside the CERN test facilities where the LHC mixed radiation field is reproduced. The architecture of the TIDMon, the radiation tolerance techniques and the design choices adopted for the system are presented in this work.

Summary:

The need for upgrading the Total Ionizing Dose (TID) measurement accuracy of the actual version of the Radiation Monitoring system for the LHC complex, drove the development of a TID Monitoring (TIDMon) system based on the Floating Gate Dosimeter (FGDOS). The TIDMon offers a modular platform which allows to study different configurations of the FGDOS, to determine if it’s a good candidate compared to the RadFET that has already been used in the RadMon. The FGDOS is an ionizing radiation sensor based on a floating gate transistor structure. Prior irradiation, the floating gate is charged through an injector. Inside the sensor, an embedded MOS and a Voltage Controlled Oscillator (VCO) read and convert the gate potential into a square wave signal. During irradiation, the negative charge induced neutralizes the positive charge stored in the gate, reducing the gate potential. Two different floating gates can be selected in the sensor, with two different sensitivities – low and high, which allows the adaptation of the monitor sensitivity to the radiation field. The manual recharge, the automatic recharge, the sensitivity, the recharge and threshold frequencies of the FGDOS are configurable. In automatic mode, when the output frequency goes bellow the defined threshold (and thus the corresponding charge of the gate), the TIDMon automatically charges the floating gate to the desired recharge frequency. These frequencies are defined for each sensitivity level, such that to keep the sensor in its most linear operating range. The TIDMon provides also the possibility
to bypass the VCO, and thus obtain on the output the current induced by the floating gate, in order to characterize the floating gate directly.

The architecture of the TIDMon is built around a Flash-based FPGA (Actel ProAsic3) which embeds several custom controllers that manage the peripherals (ADC, sensors). The FPGA allows the remote control of the settings and offers a modular architecture, improving the FGDOS dosimetry data processing. An 8-channel 16 bit ADC is used to acquire the dosimetry from the RadFETs and the other analog signals (power supplies voltages, images of currents sources and temperature) that monitor the status of the board.

The architecture is based on the RadMon V6 whose radiation testing was performed using protons, 60Co, and 1 MeV neutrons at the components level. The TIDMon was tested at the system level with 60Co, and mixed field radiation. It was proven to be operational up to a TID of at least 25-30 krad (Si). The Triple Modular Redundancy (TMR) mitigation technique is applied on the registers automatically by means of a commercial synthesis tool, to increase the robustness of the FPGA embedded controller. The RAM blocks have been triplicated manually in the code because the tool was not able to do it automatically. The TIDMon system proved the robustness of its TID measurement during several irradiation campaigns and the FGDOS controller design showed good results. Further studies are required to continue to characterize the FGDOS to several environment factors (temperature, dose rate...) and irradiation campaigns have been planned.

POSTER - Board: B5 / 28

Adaption of Low Cost Safety COTS MCU For Low Level Radiation Applications in Accelerator Facilities

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Our work targets soft errors in embedded systems operating in particle accelerator physics experiments. We propose to use the safety mechanisms included in the low cost Cortex-R4F to mitigate Single Event Effects, as well as additional procedures to recover data from external memories. These procedures include making an interleaved backup of the program data by using the DMA controller. In case the CRC mechanism detects a mismatch either in the interleaved backup data or in the program/heap/stack, the faulty data can be rewritten from the copy or the original data.

Summary:

Our work is motivated by the growing concerns of soft errors in embedded systems operating in particle accelerator physics experiments. Until now, the problem is handled by using Application Specific Integrated Circuits (ASIC) with high radiation tolerance. Such ASICs are pricey and only available upon special fabrication ordering. Therefore, we propose to use and exploit the safety features of low cost, automotive, Commercial Off The Shelf (COTS) Micro Controller Units (MCU) with fault-tolerant Cortex-R4F processor, such as the TMS570 from Texas Instruments. This Cortex-R4F runs in lockstep mode to achieve dual processor redundancy, has ECC mechanisms for internal, tightly coupled memories as well as for flash program memories. It furthermore operates CPU-independent Cyclic Redundancy Check (CRC) and Direct Memory Access (DMA) controllers. The CRC is commonly used to detect mismatches of written data in several kinds of memories, among them the ones connected to the External Memory Interface (EMIF). Such mismatches can be caused for example by Single Event Effects (SEE). We furthermore propose additional procedures to recover data from memories managed by the EMIF which can be program memory, stack or heap data. These procedures include making an interleaved backup of the program data, to be stored in the external memory, by using the DMA controller. In case the CRC mechanism detects a mismatch either in the interleaved backup data or in the program/heap/stack, the faulty data can be rewritten from the copy or the original data, depending on where the error occurred. In ordinary MCUs, errors can propagate across operations, which leads to a situation where it is impossible to recover any damaged data. Thus, the inclusion of checkpoints is proposed, offering the following advantage: Any fault detected by the MCU safety features such as lockstep, ECC of internal memory, clock signal integrity and PLL status can be monitored in specific registers. For control applications in
accelerator facilities, such as CERN. EPICS libraries were adapted to the redundant COTS Cortex-R4F MCU by using the Real Time Executive Multiprocessing System (RTEMS) Board Support Package (BSP). Therefore, if an MCU error occurs without involving the EPICS libraries and Ethernet driver, the user can be informed immediately by porting the failure from the MCU fault register to an EPICS process variable which can be subsequently monitored in any computer connected to the EPICS Channel Access CA. For the future work, we intend to establish radiation limits where such a device can be operated by exposing the MCU to a wide variety of beam types. We will also look for mechanisms in which erroneous data can be recovered by other MCUs connected to the EPICS CA, or implement a different protocol in the same layer as CA to recover damaged data.

**POSTER - Board: C8 / 43**

**Radiation Hardened by Design, Low Jitter, 2.56 Gbps LVDS/SLVS Based Receiver in 65 nm CMOS**

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This paper proposes a 2.56 Gbps, radiation hardened by design, LVDS/SLVS like receiver designed in a commercial 65 nm CMOS technology. Simulation results predict 500 µW power consumption and 400 fs RMS output jitter. A replica receiver with a compensation loop is used to measure and compensate variations in the propagation delay of the output edges due to total ionizing dose (TID) radiation effects and/or process-temperature and voltage variations. This loop will ensure an equal propagation delay of the rising and falling output edges, to allow the use in accurate timing circuits.

**Summary:**

Many of today’s applications require high precision time-domain signal processing circuits like particle detectors in high energy physics experiments such as the CMS and ATLAS experiments at the Large Hadron Collider (LHC) in CERN or laser-ranging sensors. The key information in these applications is contained in the timing difference between multiple signals or events. This timing information is usually converted to binary data using time to digital converters (TDC). In large and/or complex systems however, the distance between the detector/event generator and the TDC can become rather large, calling for a highly time accurate, long distance, transmission of these signals.

Many applications now use Low Voltage Differential Signaling (LVDS) and Scalable Low Voltage Signaling (SLVS) for data transmission because of its robustness to interferences, low power consumption and high speed. The SLVS standard is comparable to the LVDS standard, with the difference of a 200 mV common mode voltage and 200 mV voltage swing instead of 1.2 V common mode and 400 mV swing. For data transmission applications, the regenerative nature of the receiver allows some tolerance to jitter provided the bit error rate remains low. However, in the envisaged sub-nanosecond timing applications, jitter is the major impairment to the performance of the system. When an LVDS/SLVS receiver is used in the signal path between the event generator circuit and the TDC, any time distortion introduced by the receiver, will cause a time measurement error and consequently will lower the system resolution. An accurate time measurement requires minimal variation in propagation delay for all edges at the output of the LVDS/SLVS receiver.

This paper focuses on the design of a radiation hardened by design LVDS/SLVS receiver which can be used in high resolution time measurement applications. This design uses an NMOS input pair, single ended output op amp structure where the output currents can be tuned in order to achieve an equal
propagation delay between the rising and falling edges at the output of the receiver. In radiation environments, the total ionizing dose (TID) will change the gain/propagation delay of the receiver, due to shifts in the threshold voltage and degradation of the charge carrier mobility. This will introduce a propagation delay mismatch between the rising and falling output edges. To compensate this mismatch, a replica receiver is added which is capable of measuring the difference in propagation delay between the two edges. When the propagation delays of the rising and falling edges are equal, an ideal clock at the input of this replica receiver must generate a clock signal at the output with a duty cycle of 50% and a common mode voltage of VDD/2. Any mismatch in this duty cycle, caused by the TID effects, will be measured by the integrating feedback loop and will be used to adjust the currents through the receiver in order to equalize the propagation delays of the output rising and falling edges.

**POSTER - Board: H8 / 128**

Integration and Testing of the DAQ System for the CMS Phase 1 Pixel Upgrade

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The CMS pixel detector phase 1 upgrade in 2017 requires an upgraded DAQ to accept higher data rates. A new DAQ system has been developed based on a combination of custom and standard microTCA parts. Custom mezzanines on FC7 AMCs provide a front-end driver for readout, and front-end controller for configuration, clock and trigger. The DAQ system is undergoing a series of integration tests including readout of the pilot pixel detector already installed in CMS, checkout of the phase 1 detector during its assembly, and testing with the CMS central DAQ.

**Summary:**

The CMS pixel detector will be upgraded in the 2016/17 LHC year end technical stop. A more efficient readout chip (ROC), along with an extra detector layer in both barrel and forward regions, and a substantial mass reduction inside the pixel detector tracking volume, will provide better tracking and vertexing performance. A higher bandwidth readout system is required to manage the greater rate of pixel data as the LHC luminosity increases and the hit occupancy of the modules increases. New backend DAQ system components, based on the microTCA platform, with front-end driver (FED) cards and front-end controller (FEC) cards, for readout and configuration/clock/trigger respectively, have been developed and prototyped with custom optical link mezzanines mounted on the FC7 AMC and custom firmware. The backend hardware is in production and pre-production parts are being used in several pixel detector test-stands, including readout and control of a pilot detector, a system of eight prototype upgraded pixel modules installed inside the present CMS forward pixel detector during LS1. The pilot detector is being read out with a prototype microTCA FED, and controlled with the prototype microTCA FECs. Assembly of the full, final upgraded pixel detector is proceeding in parallel with DAQ developments. Each of the assembled sub-structures of the final detector (four half-cylinders for forward pixels, and two half-barrels for barrel pixels) is being validated with the microTCA backend. In parallel, pixel DAQ integration tests with the CMS central DAQ system are taking place at Point 5, along with running of the pilot detector, in order to assure a smooth upgrade. This paper describes the DAQ system, integration tests and results, and an outline of the activities up to commissioning the final system at CMS in 2017.

**POSTER - Board: H1 / 136**

Precision Electronics for a System of Custom MCPs in the TORCH Time of Flight Detector

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The TORCH detector to provide low-momentum particle identification is an R&D project, combining Time-of-Flight and Cherenkov techniques to achieve charged particle π/K/p separation up to 10 GeV/c. The measurement requires a timing resolution of 70ps for single photons. Based on a scalable design, a Time of Flight (TOF) measurement system has been developed to instrument a novel customized 512-channel Micro Channel Plate (MCP) device. A Gigabit Ethernet-based readout scheme that operates the TORCH demonstration unit consisting of ten such MCPs will be presented. The trigger and clock distribution will also be discussed.

Summary:
TORCH has applications in experiments requiring low-momentum particle identification, for example to identify B-meson decay products in the upgrade of the LHCb experiment. The Time of Flight measurement requires a timing resolution of 70ps for single photons, which means that the electronics must provide better than 50ps time resolution.

The TORCH system uses 32-channel fast amplifiers/Time-Over-Threshold (TOT) ASICs (NINO-32s), followed by High Performance Time to Digital Converter ASICs (HPTDCs) coupled to a Micro-Channel Plate (MCP) detector for the fast timing measurement. In addition, the system must measure charge division using the TOT digitization to improve the spatial accuracy of the MCPs by a factor of two. This system has been designed to read out a single MCP with 256 channels; later this year, a Phase 3 custom MCP will be procured with 512 channels. In order to read out such an MCP, a new NINO board has been designed to provide twice the channel count and offering improved cooling arrangement. The new board contains 4 NINO-32 ASICs (2 previously), and 2 HPTDC boards (64 channels each) are connected to such a NINO board to provide 128-channel digitization. A Gigabit Ethernet-based readout board is connected to 8 HPTDC boards via a backplane to transfer data and provide clock, trigger and control signals. It connects to a PC with a signal Ethernet cable.

The final TORCH demonstrator will be instrumented with 10 MCPs. To read out such a system, a commercial Ethernet repeater is used to combine the 10 links into a single Ethernet cable to a PC. The readout system uses raw MAC protocol, to maximise efficiency. The PC can send control or configuration packets to a unique Ethernet address that is associated to a particular MCP. During operations, the PC will first configure the HPTDCs and NINOs, then instruct all HPTDCs to start measurement. The data are stored on HPTDC boards and readout board temporarily. The PC starts requesting data from the first MCP immediately, and once a fixed amount of data is received, then transferring on the first MCP is paused and a readout request is moved to the next MCP. During pause, the HPTDCs are still measuring but the data is not transferred over the Ethernet cable to avoid collation. A weighting factor is introduced in DAQ software to give priority to the MCP that has the higher occupancy. We have also implemented a time-out function, in case a faulty readout board blocks the readout the whole system.

A Trigger Logic Unit (TLU) is carried over from previous systems. A fan-out module is being prepared to distribute triggers and clocks to the 10 readout boards from a single TLU. The fan-out module also joins the busy signal via or-logic to indicate that a MCP modules cannot accept more triggers. The TLU will then stop issuing triggers to all readout boards. The TLU provides synchronisation to other systems, i.e. telescopes, Cherenkov counters, etc.
ATLAS Phase-II-Upgrade Pixel Data Transmission Development

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The ATLAS tracking system will be replaced by an all-silicon detector (ITk) in the course of the planned HL-LHC accelerator upgrade around 2025. The readout of the ITk pixel system will be most challenging in terms of data rate and readout speed. Simulation of the on-detector electronics based on the currently foreseen trigger rate of 1 MHz indicate that a readout speed of up to 5 Gbps per data link is necessary. Due to radiation levels, the first part of transmission has to be implemented electrically. System simulation and test results of cable candidates will be presented.

Summary:

ATLAS is preparing for an extensive modification of its detector in the course of the planned HL-LHC accelerator upgrade around 2025 which includes a replacement of the entire tracking system by an all-silicon detector (Inner Tracker, ITk) and a revised trigger and data taking system with triggers expected at lowest level at an average rate of 1 MHz. The five innermost layers of ITk will comprise of a pixel detector. The readout of the pixel layers will be most challenging in terms of data rate and readout speed. A new on-detector readout chip is designed in the context of the RD53 collaboration. The performance of the readout system was simulated based on hit rates from detector simulation combined with behaviour expected from the proposed chip design, assuming different buffer sizes to store data until trigger arrival with proposed trigger parameters. This simulation indicates that a readout speed of up to 5 Gb/s per data link is necessary in the innermost layers going down to 640 Mb/s for the outermost layers while adding a latency well below that imposed by the ATLAS trigger system. Up- and downlink communication to the on-detector electronics is foreseen to be largely optical. However, radiation levels close to the beam pipe prevent the placement of optical components close to the readout chips such that the first part of transmission has to be implemented electrically with signals to be converted for optical transmission at larger radii. Options to group data links of outer layers are considered in order to make use of the bandwidth to be made available for innermost layers and thus reduce needed material. Consequently, cables are being developed for electrical data transmission at rates of up to 5 Gb/s over several metres. Designs cover solutions such as twin-axial, twisted pair or flex cables and hybrids of these. Prototype cable performance was inspected with dedicated bit error rate testers based on FPGA boards or commercial types. Error rate measurements are complemented by attenuation behaviour derived from S-parameter analysis and eye-diagram inspection in addition to according simulations. Some of the cables under test demonstrated maximum payload rates above the desired data rate and thus provide good candidates for the ITk-Pixel readout.

A Versatile Small Form Factor Twisted-Pair TFC FMC for mTCA AMCs

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In continuous readout systems of particle physics experiments, providing a common clock, time reference and the distribution of critical low latency messages to the processing and fronted layers of the readout is a crucial task. In the context of CBM, a versatile small form factor TFC interfacing FMC was developed, offering bidirectional twisted-pair (TP) links for communicating between TFC nodes and a versatile clocking including voltage controlled oscillators and the connection to the telecommunication clock lines of mTCA crates. Being designed for both TFC Master and Slaves, the card allows rapid system developments without additional Slave hardware circuits.
Summary:

Timing and Fast Control (TFC) systems play an important role in the readout of particle detectors. They enable the deterministic recording of data at the frontend electronics (FE), which allows analyzing it in the latter processing layers as coherent data sets.

In the planned CBM readout, the FE in the irradiated area is connected through the radiation-hard GBTx ASICs to FPGA boards in the processing electronics room using optical fiber links. At the FPGA layer, data containers formed from the detector data are then transferred to the server farm through fiber-based 10 Gigabit links.

As a requirement of the self-triggered readout of the CBM system, the FE has to use a clock derived from the fiber link in order to guarantee a deterministic data recording. Thus, the TFC system is connected to the FPGA layer and provides a common reference clock for the fiber links’ transceivers towards the FE.

For studying the feasibility of different approaches, a preliminary TFC Master interfacing board was developed as part of our previous work. Though it was sufficient for showing the transmission of TFC data, it lacked features being required from a flexible TFC interface.

For that reason, in this article a new twisted-pair TFC FMC is proposed for the CBM readout, which offers a small form factor allowing it to be mounted onto FPGA-based AMCs for microTCA crates. Besides that, the card is evaluated with a prototype system, demonstrating both its versatility and its applicability for a TFC system inside the processing electronics room.

On this FMC, bidirectional Multi-point Low Voltage Differential Signaling (MLVDS) ICs are connected to galvanically isolated TP lines through multi-port RJ45 connectors.

The four bidirectionally operated pairs of the TP cable are used for different purposes. Fast control messages are exchanged between Master and Slave through two data lines. For the timing functionality, one pair is used for distributing a reference clock from a dedicated IC and another line for the timing control link.

The clocking IC is connected to the bidirectional clock lines of the FMC connector dedicated to receiving and transmitting clock signals respectively. In conjunction with a suitable AMC like the AMC FMC Carrier Kintex (AFCK), clocks may be distributed between the boards inside a crate using the telecommunication clock lines. This allows composing advanced TFC topologies like a frequency-locked Multi-Master TFC crate.

Besides that, different VCXOs are provided on the PCB which can be adjusted from the FPGA side. Together with the bidirectional timing link this allows a precise timestamping approach similar to the one applied in White Rabbit systems.

Last but not least, the card can also be used at the TFC Slaves since one of its ports also offers the complete functionality to lock a FPGA node to the TFC link.

In summary, the FMC card provides a versatile functionality which supports the rapid development and evaluation of a TP TFC system being integrated into an mTCA crate-based readout topology.

A Universal FMC-Based DAQ System

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Towards development of a 10MGy rad-hard ASIC, evaluation of innovative 3D integration technology and CMOS - active edge pixel sensor characterization, a versatile DAQ system is presented. Based on a Spartan 6 PCIe board, an FMC mezzanine card is developed providing a 68-channel digital input. Featuring automatic bi-directionality and variable output level (0.9V - 4.8V) with high impedance capability, each channel is independently adjustable. The 8.5ns transceiver rise times required 40MHz rate for HL-LHC conditions. An 8bit ADC combined with clock buffering and serialization, limit to four the number of control lines.

Summary:
Towards the development of a 10MGy radiation hard pixel ASIC, the evaluation of the innovative 3D integration technology and advances in CMOS and active edge planar pixel sensors, a versatile and universal data acquisition system is needed, compatible with different technologies. With availability, simplicity and low-cost as primary requirements, an FPGA-based DAQ system is developed based on a CERN developed FMC PCIe 2.0 carrier board. Base board provides a total of 34 differential or 68 direct line inputs hard-wired at 2.5V signal level.

A specially conceived FMC mezzanine card is developed, providing a programmable 58 digital channel input. Featuring automatic embedded bi-directionality and variable signal level from 0.9V to 4.8V with high impedance capability, each channel is independently adjustable. Use of an 8bit analog to digital converter allows for a quasi-continuous output signal level stepping. The 8.5ns transceiver rise time assures the required 40MHz input rate expected in HL-LHC conditions while, a fast on the fly channel independent switching is provided.

To minimize the number of needed control lines, clock distribution, buffering and serialized programming are exploited. In addition, six integrated trigger inputs are instrumented, compatible with both TTL and NIM standards via firmware control. A low noise amplifier and embedded switching power supply eliminate the need for external powering, restraining the system to standard FMC specifications in both footprint and powering requirements. Power dissipation studies at full load confirm a low thermal budget on the support structure with no need for external cooling components.

The FPGA firmware control module was conceived for fast integration with application-specific firmware, allowing direct communication and interaction with LabVIEW™ based or autonomous UNIX compiled data acquisition software. The system is provided as a full package with proven functionality as a silicon detector ASIC read-out while, its versatility allows for use in a variety of R&D projects.

POSTER - Board: J7 / 109

Digital Readout Board for CMS and TOTEM Precision Proton Spectrometer Timing Upgrade Project

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For the CMS and TOTEM Precision Proton Spectrometer Project, a digital readout board was designed to take front-end data of the Diamond Detectors and Quartz Timing Cherenkov Detectors, reformat the data timing packets, and transmit them to the CMS and TOTEM data acquisition systems through optical data links. This board is capable of having HPTDC or SAMPIC mezzanines for high-resolution timing measurement of the leading and trailing edges in the hit pulses with the resolution of 10 - 20 ps.

Summary:

The FPGA-based digital readout board is designed for the Precision Proton Spectrometer Timing Readout project along with the TOTEM Timing Upgrade project. The board is capable of data readout from two HPTDC mezzanine (each containing four HPTDC time to digital converter chips) or two SAMPIC time to digital converter mezzanine through different extensions. Data is then sent to the CMS data acquisition system using four 400 Mbit/s optical links implemented by the four-channel Pixel Optohybrid (POH), and to TOTEM data acquisition system via two optical links. One CCU25 chips has been mounted on the board to benefit from the maximum capability of this chip by having four parallel 8-bit, one master JTAG and at most sixteen I2C channels for controlling the board as well as programming the FPGA and communicating with the DAQ system. The selected Rad-Hard FPGA is a SmartFusion2 M2S150-FC1152 from Microsemi Co.

Data readout of the HPTDC mezzanine is done through dedicated 80 Mbit/s LV TTL serial lines without
trigger recovery, and dedicated 32-bit LVTTL parallel ports with trigger recovery. The four HPTDC chips on the mezzanine board form a token ring which is controlled by the main SmartFusion2 FPGA on the readout board.

For the beam test purposes, USB and FieldBus expansions are also implemented on the board using the QuickUSB and FieldBus components. Data readout from the mezzanines and board programming would be possible by these extensions through a special data protocol which is defined in the main firmware. For the transmitting readout data from the SAMPIC mezzanine to TOTEM data acquisition system, two GOH optical links has been added to this readout board due to TOTEM DAQ requirements. For the configuration purposes, the SAMPIC mezzanine FPGAs are programmed by the SmartFusion2 FPGA. The dedicated clock distribution systems will be used to synchronise the detectors installed on both sides in the tunnel at 220 m from CMS interaction point.

**POSTER - Board: H3 / 142**

**The Next Generation Front-End Controller for the Phase 1 Upgrade of the CMS Hadron Calorimeters.**

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In the Phase 1 Upgrade of the CMS Hadron Calorimeters, the ngFEC is the system responsible for distributing the LHC clock, the synchronization signals and the slow controls to the frontend electronics using a GBT bidirectional link. It is based on the FC7, a μTCA AMC developed at CERN and built around the Xilinx Kintex-7 FPGA. Its main features are: a fixed latency for fast signals across power cycles, a redundancy scheme in the communication with the frontend modules, and the ability to program all frontend modules. This contribution reviews the characteristics and the development status of the ngFEC.

**Summary:**

The ngFEC (next generation FrontEnd Controller) is the system responsible for fast and slow control within the Phase 1 Upgrade of the CMS Hadron Calorimeters. It is based on the FC7, a μTCA compatible Advanced Mezzanine Card developed at CERN and built around the Xilinx Kintex-7 FPGA. The ngFEC decodes the 40.07888 MHz LHC clock and the synchronization signals received from the backplane and distributes them to the frontend electronics using a GBT link. The latency of the fast control signals is fixed across power cycles and across identical ngFEC channels. Even if the direct link to a frontend module is broken, a redundancy scheme ensures a successful communication using the link to the neighboring frontend module. Thanks to the ngFEC all frontend modules can be remotely programmed through the JTAG standard. The CCM server software interfaces the ngFEC to the Detector Control System (DCS) which constantly monitors voltages and temperatures on the frontend electronics. This contribution reviews the characteristics and the development status of the ngFEC.

**POSTER - Board: H5 / 146**

**Design of an AdvancedTCA board Management Controller Solution**

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The AdvancedTCA (ATCA) standard has been selected as the hardware platform for the upgrade of the back-end electronic of the CMS and ATLAS experiments of the Large Hadron Collider (LHC). In this context, the electronics systems for experiments group for experiments at CERN is running a project to evaluate, specify, design and support xTCA equipment. As part of this project, an Intelligent Platform Management Controller (IPMC) for ATCA blades, based on a commercial solution, has been designed to be used on existing ATCA blades. This poster reports on the status of this project presenting the hardware and software developments.

Summary:

Originally developed for the telecommunication industry, the AdvancedTCA standard has been selected as a platform for the phase II upgrades of the ATLAS and CMS back-end electronics at CERN. In this framework, the CERN EP-ESE group launched in 2011 the xTCA evaluation project whose aim is to perform technical evaluation of equipment, provide support for the selected components across experiments as well as design and support standardized hardware controllers.

The AdvancedTCA standard, defined by the PCI Industrial Computer Manufacturer Group (PICMG), outlines a modular architecture by describing physical, electrical and functional specification. It offers a wide range of hardware management features to monitor (temperatures, voltages, current, etc.) and control (fan speed, power management, etc.) the system as well as ensure its proper operation (modules compatibility, current requirement, e-keying, etc.). These actions are performed by specific controller modules which are interconnected via an Intelligent Platform Management Interface (IPMI) bus: Module Management Controller (MMC) for AMCs, Intelligent Platform Management Controller (IPMC) for ATCA boards and Carrier IPMC for ATCA carrier as well as Shelf Manager for ATCA shelves and MicroTCA Carrier Hubs. In the frame of the CERN xTCA evaluation project, a commercial Intelligent Platform Management Controller (IPMC) solution from Pigeon Point was evaluated in 2015. Following this evaluation, a mezzanine card was designed to be used on existing AdvancedTCA blades compliant with a specific form factor (VLP DIMM-DDR3). The reduced dimensions of this form factor created challenges for the board layout and resulted in a very dense PCB. A first prototype of this IPMC has been recently received and is being tested. In parallel, the PCB layout is being improved and simplified in order to reduce cost and improve reliability. The testing phase is divided in three parts: the hardware with the validation of the power and the interfaces available on the connector, the firmware including the test of the modified FPGA design and the software for the embedded microcontroller. In the meanwhile, we are evaluating different ways to allow users to customize the IPMC to their specific ATCA blades with minimum effort (power sequences, sensors, e-keying, etc.). This poster introduces the progress made on this project with a focus on the difficulties faced during the prototype design and with a report on the test status and development roadmap.

POSTER • Board: I4 / 88

ALICE Inner Tracking System Readout Electronics Prototype Testing with the CERN “Giga Bit Transceiver”

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The ALICE Collaboration is preparing a major detector upgrade for the LHC Run 3, which includes the construction of a new silicon pixel based Inner Tracking System (ITS). The ITS readout system consists of 192 readout boards to control the sensors and their power system, receive triggers, and deliver sensor data to DAQ. To prototype various aspects of this readout system of the ITS, an FPGA based carrier board and an associated daughter card containing the CERN Gigabit Transceiver (GBT)
chipset has been developed. This contribution describes laboratory and radiation testing results with this prototype board set.

Summary:

The ALICE experiment is studying strongly interacting hadronic matter using nucleus-nucleus, proton-nucleus, and proton-proton collisions at the CERN LHC. To deal with the increased interaction rates expected for Run-3, the ALICE detector will be upgraded during the LHC shutdown 2019/20. The upgrades include a new, high-resolution, low-material Inner-Tracking System (ITS) based on Monolithic Active Pixel Sensors (MAPS) developed by the ITS collaboration. A total of 25k sensors are distributed in 7 concentric barrels (radii 22 - 400mm), sub-divided into staves (29 – 150cm length) and provide a detection area of 10m2 segmented into more than 12.5 G Pixels. On the inner 3 barrels, each stave consists of 9 sensors with individual data lines, while in the outer 4 barrels, sensors are combined into "modules" consisting of 2 rows of 7 sensors, where 1 "master" sensor collects the data from 6 "slave" sensors and sends them over 1 data line. These modules are arranged into 2 rows of 4 (7) modules for the middle (outer) 2 barrels.

The ITS upgrade requires a new readout system designed to be able to read the ITS data up to a rate of 100kHz (400kHz) for Pb-Pb (pp) collisions. The readout system connects to the sensor data, control, and clock lines on the detector side, receives trigger and control information from the control room, and delivers sensor data to the data acquisition system over (bi-directional) optical fibers to the control room. The readout system also needs to fulfill ancillary functions like controlling and monitoring the power system in order to quickly detect and interrupt latch-up states in the sensors.

The current readout unit design foresees a modular Readout Unit (RU), each connected to one stave, resulting in a total of 192 RU’s for ITS. The RU’s will be located 5m from the end of the staves in the experimental hall. This location is characterized by a radiation environment resulting in a total ionizing dose < 10krad and a high-energy hadron flux (capable of causing electronics single-event upsets) of ~1kHz/cm². The RU’s thus need to be designed radiation tolerant while being able to deal with the high-speed data links of the sensors. The design consists of an FPGA to handle the data collection and formatting, as well as the control of the sensors, and a radiation-hard fiber-optic transmission chipset, the "Gigabit Transceiver Optical Link" (GBT) developed at CERN for the LHC experiment upgrades. The GBT consists of the GBTx serializer/deserializer ASIC, the VTRx/VTTx optical transceiver/transmitter module, and the GBT-SCA slow controls ASIC.

In order to evaluate various aspects of this design including the radiation tolerance, a prototype RU has been designed based on a Kintex-7 FPGA carrier board and a mezzanine that accommodates the GBT chipset. This contribution will describe the GBT associated hardware and firmware design as well as bench and radiation tests performed with these prototypes.

POSTER - Board: J2 / 119

A Silicon Strip Telescope for Prototype Sensor Characterisation Using Particle Beam and Cosmic Rays

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We present the design and the performance of a silicon strip telescope that we have built and recently used as reference tracking system for prototype sensor characterisation. The telescope was operated on beam at the CERN SPS and also using cosmic rays in the laboratory. We will describe the data acquisition system, based on a custom electronic board that we have developed, and the online monitoring system to control the quality of the data in real time.

Summary:

We have designed and built a tracking system capable to operate on particle beam and also using cosmic rays in laboratory. The telescope consists of 8 layers of single-sided silicon strip detectors with 512 strips each and is used as reference tracking system for the characterisation of prototype silicon sensors.
The detectors are read out using Beetle chips, custom ASICs developed for the LHCb experiment, which provide the measurement of the hit position and pulse height of 128 channels. The detector size is about 10 cm x 10 cm and the strip pitch is 183 um. The maximum trigger rate accepted when operated on beam is 1.1 MHz while cosmic rays in laboratory are detected at a rate of about 1 Hz. The data acquisition system is based on a custom electronic board equipped with Xilinx-7 FPGA, providing the digitalisation of the analog signals, zero suppression and managing the data flow. For the signal digitalisation, multichannel 12-bit ADCs with high speed serial outputs are used. A TDC with sub-ns resolution is implemented in FPGA to measure the time interval between the triggers received by the Beetle chip and the sampling time. This feature is useful in order to determine the TDC value for optimal signal over noise ratio. A user friendly GUI was developed to configure and run the data acquisition system and monitor the quality of the data in real time.

Web-Based DAQ Systems: Connecting the User and Electronics Front-Ends

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Summary:

Web technologies are quickly evolving and are gaining in computational power and flexibility allowing for a paradigm shift in the field of DAQ systems design. Modern web browsers offer the possibility to create intricate user interfaces and are able to process and render complex data. Furthermore, new web standards such as WebSockets that bring the sockets technology to web browsers or WebWorkers that enable web applications to use multi-threading allow for fast real-time communication between the server and the user with minimal overhead. Those improvements make it possible to move the control and monitoring operations from the back-end servers directly to the user and to the front-end electronics, thus reducing the complexity of the data acquisition chain. Moreover, web-based DAQ systems offer greater flexibility, accessibility, and maintainability on the user side than traditional applications which often lack portability and ease of use.

As proof of concept, we implemented a simplified DAQ system on a mid-range Spartan6 FPGA development board (SP601) coupled to a digital front-end readout chip (VFAT2). The system is connected to the internet and can be accessed from any web browser. It is composed of custom VHDL code to control the front-end readout and of a dual soft-core Microblaze processor to communicate with the client.

The first Microblaze core is running an HTTP server that delivers static web content to the client upon connection. It makes use of a Memory File System to store files in the RAM and is able to handle a wide variety of HTTP request. It also sends and receives WebSocket requests to and from the users in order to broadcast data or receive commands. Using the later, clients are able to control the front-end readout chip and get feedback in real-time. Whenever an event is recorded, data can be transmitted to all connected clients and then displayed in their browser. This core acts as monitoring interface.

The second Microblaze core is coupled to the custom VHDL code and handles the communication with the front-end readout chip. It receives commands from the first core through an inter-processor communication system and parses the requests for the VHDL entities. This core acts as control interface.
Using the system described here-above users are able to connect directly to the front-end electronics, effectively by-passing the need for any intermediate server, to control the system and to get real-time monitoring information about it.

We will report on the latest web technologies and developments (WebSockets, WebWorkers, ...) that allow for advanced web-based DAQ system design and on the performance of such systems by presenting the results obtained with the system we implemented.

**POSTER** - Board: L2 / 143

**The CMS Electron and Photon Trigger for the LHC Run 2**

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The CMS experiment implements a sophisticated two-level triggering system composed of Level-1, instrumented by custom-design hardware boards, and a software High-Level-Trigger. A new Level-1 trigger architecture with improved performance is now being used to maintain the thresholds that were used in LHC Run1 for the more challenging luminosity conditions experienced during Run2. The upgrades to the calorimeter trigger will be described along with performance data. The algorithms for the selection of final states with electrons and photons, both for precision measurements and for searches of new physics beyond the Standard Model, will be described.

**Summary:**

The Compact Muon Solenoid (CMS) experiment implements a sophisticated two-level triggering system composed of the Level-1, instrumented by custom-design hardware boards, and a software High-Level-Trigger.

During Run 2, the LHC has increased its centre-of-mass energy to 13 TeV and will progressively reach an instantaneous luminosity of $2 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$.

In order to guarantee a successful and ambitious physics programme the CMS Trigger and Data acquisition (DAQ) system has been upgraded.

A new Level-1 trigger architecture with improved performance is now being used and a novel concept for the L1 calorimeter trigger is introduced: the Time Multiplexed Trigger (TMT). In this design, which is similar to the CMS DAQ or HLT architecture, nine main processors receive each all of the calorimeter data from an entire event provided by 18 preprocessors. The advantage of the TMT architecture is that a global view and full granularity of the calorimeters can be exploited by sophisticated algorithms. The goal is to maintain the current thresholds for calorimeter objects and improve the triggering efficiency. The introduction of new triggers based on the combination of calorimeter objects is also foreseen.

The performance of these algorithms will be presented, both in terms of efficiency and rate reduction using the proton collision data collected in 2016. The challenging aspect of the pile-up mitigation will be addressed along with the rejection of anomalous signals (spikes) in the APDs.

The impact of the improved selections on benchmark physics with electrons and photons in the final states will be discussed using as examples precision measurements of the Higgs boson properties and searches for new physics beyond the Standard Model.
Design and Performance of the Phase I Upgrade of the CMS Global Trigger

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The Global Trigger is the final decision stage of the Level-1 Trigger of the CMS Experiment at the LHC. Previously implemented in VME, it has been redesigned and completely rebuilt in microTCA technology, using the Virtex-7 FPGA chip family. This allows implementing trigger algorithms close to the final analysis selection, combining different physical objects. The flexible and compact new system is presented, together with performance tests at a proton-proton centre-of-mass energy of 13 TeV. Firmware and software developments for the operation and validation of the Global Trigger will also be discussed.

Summary:

The Global Trigger is the final decision stage of the Level-1 Trigger of the CMS Experiment at the LHC. Previously implemented in VME, it has been redesigned and completely rebuilt in microTCA technology, using the Virtex-7 FPGA chip family. This allows implementing trigger algorithms close to the final analysis selection, combining different physical objects received from the calorimeters and muon detectors. Electrons or photons, muons, jets, taus, as well as energy sums can be combined. Topological conditions and invariant mass triggers may be applied. The number and complexity of the algorithms making up the trigger menu are substantially increased compared to the legacy design. The new system, much more compact and flexible than the previous one, is presented. It is based on a single principal type of board, called MP7, which performs the logic calculations and which has initially been developed for the CMS calorimeter trigger at Imperial College, University of Bristol and Rutherford Appleton Laboratory. Auxiliary boards, developed at HEPHY Vienna, are used to receive external signals from other subdetectors and to manage the simultaneous operation of several MP7 boards in case of trigger menus with a large number of complex algorithms. Performance evaluations undertaken in parallel operation with the legacy system during the initial months of Run II of the LHC and during data taking in 2016 at a proton-proton centre-of-mass energy of 13 TeV will be presented. Details on the use of chip resources and link operation will be given. Firmware and software developments necessary for the setup, control, monitoring and validation of the Global Trigger will also be discussed.

POSTER - Board: M6 / 165

Readout and Trigger for the AFP Detector at ATLAS Experiment

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AFP, the ATLAS Forward Proton consists of silicon detectors at 205 m and 217 m on each side of ATLAS. In 2016 two detectors in one side were installed. The FEI4 chips are read at 160 Mbps over the optical fibers. The DAQ system uses a FPGA board with Artix chip and a mezzanine card with RCE data processing module based on a Zynq chip with ARM processor running Linux.

In this contribution we give an overview of the AFP detector with the commissioning steps taken to integrate with the ATLAS TDAQ. Furthermore first performance results are presented.

Summary:

The ATLAS Forward Proton detector aims to measure the transfer momentum and energy loss of very forward protons colliding in the ATLAS interaction point. For this purpose, the detector consists of two Roman Pots per ATLAS side at 205m and 217m from the IP, each of them containing a 3D silicon tracker and a time-of-flight detector in the far stations.

A first stage of installation took place during the LHC shutdown of 2015-2016. In that period, the two Roman Pot stations on one side
were installed, together with a silicon tracker in each station (AFP0+2) in February 2016. Functional TDAQ integration with the ALTAS experiment was achieved in May of the same year, during LHC’s luminosity ramp-up. During 40h of common run with ATLAS AFP TDAQ collected more than 20pb-1 when detectors were inserted at 20 sigma from the beams. At the same time, the detector commissioning took place. The installation of the full AFP detector is planned to be completed during the next shutdown (2016-2017).

The silicon detectors are bump-bonded to the FE-I4 readout chip, which is read-out with a FPGA board based on a Xilinx Artix chip, HSIO-2, and a mezzanine card that plugs into this board. The mezzanine card contains a RCE data processing module based on a Xilinx Zynq chip. The software for calibration and monitoring of the AFP detectors runs on the ARM processor of the Zynq under ArchLinux. The RCE communicates with the ATLAS Run Control software. Commands are transmitted from RCE to an optoboard over 200m of optical cable and then sent to each module via 8m of electrical twisted pair cable.

The trigger signal is obtained with the HitOr signal from each of the FE-I4 modules, which consist in a logical OR of the signals of all the columns in the detector. The length of the HitOr signal depends on the deposited charge in the silicon and the tuning parameters, and can span over several bunch crossings. Those signals are then sent to the Local Trigger Board (LTB) mounted at the station with the Hitbus chip. The Hitbus chip has 3 input channels for selectable trigger logic. The best three detectors of each station were chosen to contribute to the trigger. A majority vote logic was selected to reduce the time walk while minimising noise. The output of the Hitbus chip is a CMOS signal, which is then sent to a CMOS/NIM driver installed on the LTB and then sent over 260m of air-core coaxial cable to the Central Trigger Processor rack located underground. The signals from two stations enter a discriminator, where the length is shortened down to 23ns. The 23ns NIM trigger signal is then fed into the ATLAS LV1 standard trigger system at the longest acceptable latency for configuration used in the high luminosity runs. Copies of the discriminated signals are also sent to the AFP local trigger electronics and used in standalone calibration runs.

**POSTER - Board: L9 / 78**

**A Prototype for an Artificial Retina Processor Aimed at Reconstructing Tracks at the LHC Crossing Rate**

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We present the results for the prototype of a processor capable of reconstructing events in a silicon strip tracker at about 1 MHz rate with sub-microsecond latency. The processor is based on an advanced pattern-recognition algorithm, called “artificial retina”, inspired to the vision system of the mammals. We design and implement this processor on a DAQ board designed to run at 1 MHz event rate. This is the first step towards a real-time track reconstruction system working at the nominal collision rate of LHC.

Summary:

The goal of the “INFN-RETINA” R&D project is to develop and implement a parallel computational methodology that allows to reconstruct events with an extremely high number (>100) of charged-particle tracks in pixel and silicon strip detectors at 40 MHz, thus matching the requirements for processing LHC events in real time.

Our approach relies on a massively parallel pattern-recognition algorithm, dubbed “artificial retina”, inspired by studies of the processing of visual images by the brain as it happens in nature. The artificial retina algorithm is based on two main concepts. First, for each track pattern we compute a quantity R that measures how any combination of entered hits matches the pattern itself. Second, the hit sequence delivered to a pattern is an appropriate subset of all the events hits, reducing the data bandwidth involved in the process. Preliminary studies on simulation already showed that high-quality tracking in large detectors is possible with sub-microsecond latencies when this algorithm is implemented in modern, high-speed, high-bandwidth FPGA devices, opening a possibility of making track reconstruction happen transparently as part of the detector readout.

As first step, we design a sizable prototype of a tracking processor using a 6-layer silicon detector as model. The detailed geometry and charged-particle hits of this detector are used to assess the processor performances. The algorithm simulation shows that tracks can be reconstructed in this detector using with a track-parameter matrix with only 3,000 patterns.

In order to demonstrate that a track-processing system based on the retina algorithm is feasible, we build the designed prototype, fitting the whole system on 8 currently-used readout boards, each equipped with 4 Altera Stratix III FPGA's. Four boards, corresponding to 16 FPGA's, are used to implement the delivering of proper hit sequences to the next step, receiving as input data separately from each readout module of the detector. All the chips in each board are interconnected between them in a full-mesh configuration, in order to be able to deliver sequences containing hits from all the layers. The other 4 boards are used to implement the computation of R for 3,000 patterns. Each chip contains a pattern sub-matrix, where a search for local maxima is performed for each event.

All the processing steps were implemented successfully on the FPGA's at the nominal clock frequency of the board (160 MHz). We test the whole processing chain providing hit sequences as input, and correct parameters for reconstructed tracks were received on the output. Assuming hit sequences from real events that include background and noise, data can be processed at a 1.8-MHz event rate, using boards that had originally been designed for a 1-MHz readout-only functionality.

Finally, we report on the scalability prospects of this track processor to larger detector systems and to higher event rates.

POSTER - Board: L7 / 172

Pulsar IIb Design, System Integration and Next-Generation Full Mesh ATCA Backplane Test Results

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The Pulsar IIb is a custom ATCA full mesh enabled FPGA-based processor board which has been designed with the goal of creating a scalable architecture abundant in flexible, non-blocking, high
bandwidth interconnections. The design has been motivated by silicon-based tracking trigger needs. In this talk we describe the Pulsar II hardware and its performance, such as the performance test results with full mesh backplanes from different vendors, how the full-mesh is used for data transfer, how the inter-shelf and intra-shelf synchronization works and the experience gained throughout this process.

Summary:

On the Pulsar IIb board a large Virtex-7 (690T) FPGA is directly connected to the RTM, four FMC mezzanine card slots as well as the ATCA full-mesh backplane. The direct connection to the full-mesh enables the full diagnostic capabilities of the MGT transceivers to evaluate the quality of the links at speeds up to 10 Gbps. The abundance of high speed backplane links makes the Pulsar IIb an ideal test platform for characterizing ATCA backplane performance, and to date several vendors have submitted their latest high performance 14 slot full mesh ATCA backplanes to our group for testing. Our backplane test results indicate that channel performance consistency is one of the most significant challenges facing ATCA backplane manufacturers today. The COMTEL “Air/Plane” 100G full mesh backplane, which uses an advanced low loss substrate material, has to date yielded the best and most consistent link performance with all Pulsar IIb boards running all backplane links simultaneously at 10 Gbps without error.

Our Level-1 silicon tracking trigger demonstration system utilizes advanced time multiplexed data transfer schemes to deliver data for a given trigger tower into a single location for processing. The ATCA full mesh backplane offers a unique blend of high performance coupled with a high degree of flexibility. In our current demonstration system we utilize ten Pulsar IIb boards which all receive data from upstream and exchange data over the full mesh backplane. A rear transition module (RTM) which has been designed to support up to 400 Gbps bidirectional communication over fiber optic transceivers which are directly connected to the FPGA. The FMC mezzanine card slots are used for user-defined mezzanine cards, either for more system IO or additional data processing or both. There are a few mezzanine cards developed for the Pulsar II, by us and also by other groups. For example, we have developed one Pattern Recognition mezzanine card, which is a test platform for silicon tracking trigger R&D and supports both ASIC and FPGA (Xilinx UltraScale) based pattern recognition associative memory processors.

System integration testing involves not only sending data between Pulsar IIb boards, but also incorporating the Inter-shelf and Intra-shelf synchronization. In this talk we will present the Pulsar II hardware and its performance, our two full-crate integration tests including the Inter-shelf and Intra-shelf synchronization using CMS trigger framework control hardware, the results of our 40G and 100G ATCA full mesh backplane performance tests, and how the backplane is used for the development of low-latency time-multiplexed data transfer schemes. Today all of the Pulsar II serial links operate reliably at 10 Gbps. We must nevertheless continue to refine our layout techniques as FPGA transceivers and ATCA backplanes continue their evolution towards ever higher serial bit rates. We will discuss how the push towards higher serial bit rates has challenged us to focus on signal integrity at the PCB level, and the experiences gained throughout the process.

POSTER - Board: M8 / 127

**Processing of the Liquid Xenon Calorimeter’s Signals for Timing Measurements**

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For identification of neutron-antineutron pair production events in the CMD-3 experiment (BINP, Russia) near threshold is necessary to measure the particles flight time in the LXe-calorimeter with accuracy of about 3ns. The duration of charge collection to the anodes is about 5mks, while the required accuracy of measuring of the signal arrival time is less than 1/1000 of that. Besides, the signal
shapes differ substantially between events, so the signal arrival time is measured in two stages. To implement that, a developed special electronics performs waveform digitization and OnLine measurement of signals’ arrival times and amplitudes.

Summary:
One of the goals of the Cryogenic Magnetic Detector (CMD-3) experiment (BINP, Russia) is a study of the hadrons production in electron-positron annihilation. An important example of such process is a neutron-antineutron pair production near threshold. A signature of this process is a large energy deposition in the barrel. In the barrel calorimeter the antineutron annihilation typically occurs by 5ns or later after beams collision. For identification of such events it is necessary to determine the time of signal appearance with accuracy of few nanoseconds. The arrival time measurement and recognition of antineutron annihilation must be accomplished On-Line in 1.1mks after the beam crossing so that the trigger signal can be generated in time for registration of this event.

The liquid xenon based barrel calorimeter (LXe-calorimeter) consists of 14 cylindrical ionization chambers with anode and cathode readout, which are located co-axially at increasing radii. Each anode surface is divided in rectangular cells; the cells at all 14 anode surfaces are located so that the overlapping cells constitute stacks, or "towers", directed approximately to the interaction point. All anode cells of each tower are electrically connected, so the signals from those ionization chambers in which ionization was induced are added up. The sum signal of each tower is fed to a channel of electronics. The collection of electrons from the entire gap to the anode takes about 4.5mks. Thus, the typical signal of a tower is a current pulse with sharp rise and approximately linear fall; the total duration of the pulse is equal to the electrons collection time. However, the amplitude and shape of tower’s signal in a particular event depends on the energy deposition and ionization clusters pattern in the volume of the tower. For providing the best signal-to-noise ratio, a charge sensitive amplifier is used at the front end of the electronic channel; therefore the amplified signal available for further processing has the rising edge as long as tower’s signal, and the shape of this rising edge varies from event to event in correspondence with the shape of tower’s signal.

The duration of charge collection to the anodes is about 4.5mks, while the required accuracy of measuring of the signal arrival time is less than 1/1000 of that. Besides, the signal shapes differ substantially from event to event, so the signal arrival time is measured in two stages. At the first stage, the signal arrival time is determined with an accuracy of 1–2 discretization periods, and initial values of parameters for subsequent fitting procedure are calculated. At the second stage, the signal arrival time is determined with the required accuracy by means of fitting of the signal waveform with a template waveform. For the moment, the developed algorithm has been successfully implemented in hardware. The prototypes of signal processing modules for LXe-calorimeter towers was manufactured and successfully tested at the detector. A obtained timing resolution was close to the design value.

POSTER - Board: L4 / 125

A Neural Network on FPGAs for the z-Vertex Track Trigger in Belle II

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Background originating from events outside of the interaction point is going to play a major role in the upcoming Belle II experiment. In order to reduce this background a track trigger based on the reconstruction of an event’s z position is employed on FPGAs. This paper presents the architecture and implementation of neural networks and supporting preprocessing that is going to be used at the
upcoming cosmic ray test of Belle II. Using hit information from simulations figures of merit like latency, accuracy and resource demand are presented.

Summary:

The upgraded SuperKEKB collider is designed to achieve a luminosity of $L = 8 \times 10^{35} \text{cm}^{-2}\text{s}^{-1}$. This will lead to more machine background at the upcoming Belle II experiment, located at SuperKEKB, in comparison to its predecessor. Hereby background originating from events outside the interaction point is a major concern.

To reduce this background a track trigger based on neural networks is implemented on FPGAs. These networks are reconstructing the z (longitudinal) position of the event vertex, which is then used for background reduction. It uses the hit information from the Central Drift Chamber (CDC) of Belle II to estimate the z-vertex without explicit track reconstruction. Additional preprocessing is based on the track information provided by the standard CDC trigger.

An implementation of neural networks has to stay within the constraints of the Trigger. The reconstruction has to be completed within $1 \mu s$, meanwhile it has to be ensured that the limited resources available on the used FPGA are not exceeded. Additionally a sufficient resolution for the vertex reconstruction has to be achieved on the FPGA. The effects of using fixpoint calculation have to be carefully considered for this.

This paper presents the architecture and implementation of neural networks that are designed to be used in the upcoming cosmic ray test of Belle II. They’re supplemented by custom preprocessing algorithms, transforming input data from the central drift chamber of Belle II into a suitable representation.

The presented architecture encompasses two layers of neurons totaling 83 neurons that are executed in parallel. Since the input data arrival frequency is much slower than the achievable clock frequency for the network, processing of the inputs is pipelined and time multiplexed for each neuron. This allows staying within the available resources of the FPGA, especially multipliers, while still achieving the demanded latency. Bit widths used for the data within the network are selected to achieve the best trade-off between accuracy of the implementation’s calculation and resource consumption.

Evaluation of the presented architecture for neural networks is conducted by using hit information from the CDC derived from simulations. Figures of merit like latency, accuracy and resource demand are presented using this data.

Tile Rear Extension Module for the Phase-I Upgrade of the ATLAS L1Calo PreProcessor System

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After the Phase-I ATLAS upgrade the Tile calorimeter will have to provide its data via fast optical links to the new Feature Extractor (FEX) modules of the L1Calo trigger system. In order to provide the FEXes with digitised Tile data, new Tile Rear Extension (TREX) modules need to be developed and installed in the existing L1Calo PreProcessor system. The TREX modules are highly complex PCBs, with state-of-the-art FPGAs and high-speed optical transmitters working at rates up to 14 Gbps. The prototype design of TREX and first corresponding test results will be presented.

Summary:

The ATLAS Level-1 Calorimeter Trigger (L1Calo) is a hardware-based, pipelined system designed to identify high-pT objects based on coarse-granularity analogue input from the ATLAS Liquid Argon (LAr) and Tile Calorimeters. The L1Calo consists of three subsystems: the PreProcessor, to digitise the input signals and to extract a bunch-crossing-aligned transverse energy value from each pulse, and two object finding processors, the Cluster Processor and the Jet/Energy-sum Processor, which use as input the pre-processing results.
In the Phase-I upgrade, L1Calo will be extended with three subsystems to maintain the trigger performance at high LHC luminosity: the electromagnetic Feature Extractor (eFEX), the jet Feature Extractor (jFEX) and the global Feature Extractor (gFEX). The input to the FEXes is entirely digital. The LAr will directly provide the FEXes with digital trigger data via optical fibres. The Tile will continue to send analogue signals to the PreProcessor, which will then have to transmit the digital results to the FEXes.

The PreProcessor is a highly modular system consisting of 124 hardware-identical PreProcessor Modules (PPMs) organised into eight VME crates. The modules in two crates process analogue signals from the Tile, while the others process signals from the LAr. The PPMs receive the analogue signals through the front-panel and transmit the digital results via LVDS cables connected to the rear side.

In order to transfer the pre-processed Tile information to FEXes, Tile Rear Extension (TREX) modules will be developed and installed in the two crates processing Tile signals. Each TREX will act as a physical extension of the PPM in the corresponding crate slot, to transmit the real-time pre-processing results to the FEXes at a maximum rate of 11.2 Gbps via up to 48 high-speed optical links. Additionally, the TREX will have the tasks to provide a copy of the real-time data to the legacy L1Calo processors via 73 LVDS links, and to gather, format and transfer the PPM event data to the ATLAS DAQ system via additional optical links. For configuration, control, and monitoring purposes, the TREX will be connected to the computing infrastructure of the experiment via the PPM and the existing VME interface, while its operating conditions will be continuously monitored by the ATLAS Detector Control System.

The TREX will be based on the most recent PCB design technologies, FPGA devices and high-speed optical transmitters. The main challenge of the design will be to integrate a high density of components while maintaining the signal integrity required to achieve a bit error rate lower than $10^{-14}$. In this contribution, the functionality and development of the board as well as initial test results will be presented.

**POSTER** - Board: M4 / 122

**A High-Speed DAQ Framework for Future High-Level Trigger and Event Building Clusters**

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Modern data acquisition and trigger systems require a throughput of several GB/s and latencies down to the microsecond level. In order to satisfy such requirements, we developed a heterogeneous system with FPGA-based readout cards and GPU-based computing nodes coupled by fast links. Remote DMA engines are used for direct communication between Xilinx FPGAs and GPUs from AMD / “DirectGMA” and NVIDIA / “GPUDirect”. Scalability is ensured by InfiniBand interconnects using the same technologies. In this contribute we present the system architecture and we compare the performance of the different solutions in terms of data throughput and latency.

**Summary:**

Significant new challenges are continuously arising in High Energy Physics (HEP) experiments at the Large Hadron Collider (LHC) at CERN. The quest for rare new physics phenomena leads to the evaluation of Graphics Processing Units (GPU) as enhancement for the existing high-level trigger (HLT). The trigger upgrade requires faster and more efficient event selection. GPUs with its flexibility might also induce the possibility of new complex triggers that were not feasible previously. A HLT with efficient many-core parallelization of the event reconstruction offers the opportunity to significantly reduce the number computing nodes. To obtain the best results, HPC clusters with multiple GPUs require high-performance interconnect such as InfiniBand to handle the GPU-to-GPU communications and to
optimize the overall performance of the cluster. Because the GPUs put significant demands on the interconnects, high-performance links like InfiniBand are required to provide low latency, high message rates, and bandwidth in order to enable all resources in the cluster to run at peak performance. The Institute for Data Processing and Electronics (IPE) at the Karlsruhe Institute of Technology has developed an integrated data acquisition framework that provides on-line data processing in the range of GB/s. The integration of GPUs in trigger and data acquisition systems is for example used in HEP and synchrotron experiments. To optimize data throughput and latency, we have developed a custom readout architecture that enables fast communication between FPGA, GPUs and InfiniBand via Remote Direct Memory Access (RDMA). In this contribute we present the high throughput platform that is capable to transfer data from FPGA to GPUs and FPGA to InfiniBand by RDMA technologies. The proposed architecture is a candidate for future generations of event building clusters to collect all event fragments belonging to the same L1 trigger and to transmit the final events to the nodes of the HLT filter farms. Direct GPU connection could be used for high-performance HLTs where GPUs exchange data with GPU by InfiniBand or FPGA for a low latency processing.

Invited Talk / 178

Radiation hard High-Speed Optical Links for HEP

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Optical links are ubiquitous in particle physics data acquisition systems spanning experiment control, data-acquisition and trigger applications. With today’s computing power, future data acquisition systems could benefit from collecting data from large segments of the detectors and involve them in trigger systems. This places challenges on optical links for High Energy Physics requiring high data-rate and low-power consumption components. The HL – LHC upgrade radiation will be 10 times higher than in the LHC environment requiring careful choice and qualification of ASIC technologies. In this talk the LHC links will be reviewed and current developments for the HL – LHC upgrade discussed.

ASIC / 35

**A 1.2 Gb/s Data Transmission Unit in CMOS 0.18 μm technology for the ALICE Inner Tracking System front-end ASIC.**

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The upgrade of the ALICE Inner Tracking System is based on a Monolithic Active Pixel Sensor and ASIC designed in a CMOS 0.18 um process from TowerJazz. In order to provide the required output bandwidth (1.2 Gb/s for the inner layers and 400 Mb/s for the outer ones) on a single high speed serial link, a custom Data Transmission Unit (DTU) has been developed in the same process.

The DTU includes a clock multiplier PLL, a double data rate serializer and a pseudo-LVDS driver with pre-emphasis and is designed to be SEU tolerant.

**Summary:**

The upgrade of the ALICE Inner Tracking System (ITS) will see the replacement of its existing 6 layers with 7 layers of pixel detectors, based on Monolithic Active Pixel Sensor (MAPS). The new detector will feature a much higher granularity, owing to a pixel size reduction from 50 um x 425 um to 28 um x 28 um. Moreover, the innermost layer will be closer to the beam pipe, with a radius of just 22 mm. These two facts, combined with the increase in luminosity, will lead to a significant increase of the amount
of data and will thus require a higher data rate link. The foreseen required bandwidth are 1.2 Gb/s for the 3 innermost layers and 400 Mb/s for the 4 outer ones. For material budget and space considerations it is mandatory to implement such a link as a fast serial one integrated in the front-end ASIC (named Alpide).

The DTU (Data Transmission Unit) is the custom block designed to implement such a data link for Alpide. It is composed of 3 main parts: a PLL to multiply the 40 MHz master clock to 200 and 600 MHz, a Double Data Rate (DDR) serializer which provides the 400 Mb/s and 1.2 Gb/s serial data stream to a LVDS driver with pre-emphasis capabilities, which in turn provides the adequate driving strength to send the data to the readout unit located outside the detector volume.

The DTU includes a range of programmable features; the output and pre-emphasis currents are tunable up to 5 mA and 2.5 mA, respectively, via 4 bits DACs. Main PLL parameters such as the charge pump current and the VCO number of stages are also adjustable in order to compensate for PVT variations.

The DTU has been designed in the same CMOS 0.18 um of the Alpide ASIC and has been produced both as a standalone test chip and integrated in the Alpide-3 ASIC. Measurements on the test chip has shown that the DTU is fully functional at 1.2 Gb/s with a random jitter of about 10 ps and a deterministic jitter of about 50 ps. The DTU is still functional at 1.5 Gb/s albeit with a 20% jitter degradation. Measurements on the Alpide DTU have shown similar results when the Alpide is in idle mode. Unfortunately an increase of jitter correlated to the chip activity has also been observed. The issue has been addressed in the Alpide-4, currently in production, by a power domain separation and a general layout effort to reduce the capacitive coupling to the PLL sensitive nodes.

The DTU test chip has been tested for Single Event Upset tolerance with both ions at the INFN LNL Tandem facility and protons at the NPI cyclotron facility. A LET threshold of 3.7 MeV cm2/mg has been measured for the PLL. A second test with ions is scheduled for July at LNL for BER studies.

Systems, Planning, installation, commissioning and running experience / 25

The ATLAS Level-1 Topological Trigger Design and Operation in Run-2

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The ATLAS Level-1 Trigger system performs event selection using data from calorimeters and the muon spectrometer to reduce the LHC collision event rate down to about 100 kHz. Trigger decisions from the different systems are combined in the Central Trigger Processor for the final Level-1 decision. A new FPGAs-based AdvancedTCA sub-system was introduced to calculate in real time complex kinematic observables: the Topological Processor System. It was installed during the shutdown and commissioning started in 2015 and continued during 2016. The design and operation of the Level-1 Topological Trigger in Run-2 will be illustrated.

Summary:

Due to the increase of the LHC instantaneous luminosity and collision energy, the ATLAS trigger system in Run-2 needs to cope with five times higher event rates than in Run-1. Several upgrades were performed during the Long Shutdown 1 to improve the ATLAS trigger capability. In particular, a new Level-1 Topological (L1Topo) trigger system was designed and installed. It selects events based on topological event kinematics calculations like invariant masses between objects, minimum distance between objects, etc.

The L1Topo trigger system is a single processor shelf equipped with two processor modules and is part of the ATLAS Level-1 (L1) trigger system. The processor modules are identical copies with firmware adapted to run different topological algorithms. These modules are designed in AdvancedTCA form factor.

The L1Topo system receives optically and through the backplane real-time data from the L1 calorimeter and L1 muon systems. The optical signals are converted to electrical signals in 12-fibre receivers. Due to its big density Avago miniPOD receivers are used. The electrical high-speed signals are routed into two FPGAs, equipped with on-chip Multi-Gigabit Transceivers (MGT). The data is de-serialized in
the MGT receivers and parallel data enters the FPGA fabric. No data duplication is implemented at the PCB level. The two processors can communicate via their fabric interface to get access to data that cannot be received directly via the MGT links. Even though higher data rates are technically possible, a maximum bit rate for the inter-FPGA link of 1Gb/s per differential pair is anticipated. This limits parallel connectivity to 238 Gb/s of aggregate bandwidth.

The L1Topo input data consist of Trigger Objects (TOB) corresponding to jets, electromagnetic clusters, taus or muons. The TOBs information include the position of the object along with some qualifying information like its energy. Thanks to the large amount of logic resources in the FPGAs, more than 100 algorithms are executed using real-time data. The results of the algorithms are sent on both optical fibres and electrical cables to the Central Trigger processor (CTP), which is responsible of the final ATLAS L1 decision. The output to the CTP consists of individual bits indicating the decision of each of the topological algorithms. In addition, L1Topo provides through the data path the TOBs input received in addition to the decision per algorithm.

The commissioning of the L1Topo system started in 2015 and continues in 2016. Data triggered or rejected by the L1Topo system is analysed comparing the hardware decisions with the simulated ones using the appropriate L1 trigger objects that are saved in the data along with the trigger decisions and the rest of the event. An initial set of data triggered by the L1Topo system and used for the commissioning was taken during the heavy-ion run in 2015. The commissioning continues in 2016 during cosmic and proton-proton collisions data-taking. This talk gives an overview of the design, operation and commissioning status results.

Optoelectronics and Links / 45

Optical Link for Detector Instrumentation: In-Detector Multi-Wavelength Silicon Photonic Transmitter

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We report on our recent progress in developing an optical transmission system based on wavelength division multiplexing (WDM) to enhance the read-out data rate of future particle detectors. The design and experimental results of the prototype of a monolithically integrated multi-wavelength transmitter are presented as well as temperature studies of electro-optic modulators and optical (de-)multiplexers. Furthermore, we show the successful permanent coupling of optical fibers to photonic chips, which is an essential step towards packaging of the opto-electronic components.

Summary:

The ever-increasing number of electronic channels in detector instrumentation results in a keen demand on high data read-out capacity. An optical data transmission system based on wavelength division multiplexing (WDM) will provide a generous data rate up to the Tbit/s range.

In state-of-the-art solutions, individual optical fibers connect directly modulated laser diodes to a corresponding receiver in the periphery of the detector. Recently, we proposed a WDM-based optical transmission system [1], where a single optical fiber carries numerous optical channels. This increases the data read-out capacity significantly while reducing the number of individual fibers connecting read-out chips with the data acquisition units. Furthermore, the laser sources providing the optical carriers are located off-detector and thus do not contribute to the energy budget within the detector volume.

The essential building block is the monolithically integrated transmitter on a silicon-on-insulator (SOI) substrate. An optical demultiplexer separates incident optical channels in order to forward each of them to a Mach-Zehnder modulator, which encodes information on the respective carrier. A multiplexer
merges all data-carrying signals to be transported over a single optical fiber. The (de-)multiplexers are implemented as planar concave gratings (PCG), where the channel separation or merging is achieved by means of diffraction. The optical modulators are implemented by Mach-Zehnder interferometers consisting of two identical phase shifters.

We present the design and experimental results of a prototype of an integrated optical 4-channel transmitter with demultiplexer, modulators and multiplexer as well as a study on the influence of temperature on the individual components. As expected, the PCG filter characteristic is shifting with varying temperature over a range of 70 K. No other change in behavior is observed. Similar studies are performed on depletion-type pn-modulators. The variation of the temperature induces a constant offset of the operating point but does not affect the modulation efficiency.

To bring a photonic integrated circuit (PIC) to operation, packaging and a permanent coupling of optical fibers is required. Due to the tight positioning tolerances, a sub-micrometer precision alignment and bonding is necessary. We show recent progress of our activities in establishing a fiber coupling process, where the optical fibers are attached to the PIC by means of UV-curing adhesives. This coupling arrangement does not impose additional insertion loss compared to a continuously controlled fiber alignment in the laboratory. It appears to be permanently stable based on observing the coupling efficiency over more than a month.

Reference

P. Skwierawski et al. 2016 JINST 11 C01045

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The CMS Barrel Muon Trigger Upgrade

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The increase of luminosity expected by LHC during Phase1 will impose several constrains for rate reduction while maintaining high efficiency in the CMS Level1 trigger system. The TwinMux system is the early layer of the muon barrel region that concentrates the information from different subdetectors: DT, RPC and HO. It arranges and fan-out the slow optical trigger links from the detector chambers into faster links (10 Gbps) that are sent to the track finders. Results, from collision runs, that confirm the satisfactory operation of the trigger system up to the output of the barrel track finder, will be shown.

Summary:

In view of the increase of luminosity during Phase1 upgrade of LHC, the muon trigger chain of the Compact Muon Solenoid (CMS) experiment underwent considerable improvements. The muon detector was designed for preserving the complementarity and redundancy of three separate muon detection systems, Cathode Strip Chambers (CSC), Drift Tubes (DT) and Resistive Plate Chambers (RPC), until they were combined at the input to the Global Trigger. The upgrade of the muon trigger aimed at exploiting the redundancy of the three muon detection systems earlier in the trigger processing chain in order to obtain a high-performance trigger with higher efficiency and better rate reduction. Since
every additional hit along a muon trajectory further improves the fake rejection and muon momentum measurement, the upgrade seeks to combine muon hits at the input stage to the Muon Track-Finders layer rather than at its output. All the hits should then contribute to the track irrespectively of the sub-system that detects them. The upgrade introduced a regional segmentation that treats muon tracks separately depending on $\eta$. It distinguishes a barrel region (low $\eta$), an endcap region (high $\eta$) and a transition region between them ($|\eta|\approx1$) called overlap. In the new muon trigger chain, the adaptive layer for the track finder in the barrel region is called TwinMux. It allows for bringing forward the merging of the DT, RPC and HO (HCAL Outer barrel) trigger primitives, unburdening the trigger processors. TwinMux is charged of sending such combined primitive to the Barrel Muon Track Finder (BMTF) and, in addition, also the RPC and DT data uncombined are sent to the Overlap Muon Track Finder (OMTF) after applying a clusterization of the RPC hits. In both cases a scale up in the transmission rate, and hence a reduction in the number of links, is provided. TwinMux is also responsible for duplicating the trigger primitives in order to reduce connections between trigger processors increasing the reliability of the system. In the barrel region the combined primitives are sent to the BMTF that implements the legacy trigger algorithm of the DT track finder with the addition of several improvements in rate reduction at higher efficiency and quality. For instance BMTF implements an extension of the legacy algorithm for the Pt assignment that using the primitive bending angle obtains a factor 1.5 gain in rate for typical thresholds and the same efficiency at plateau for prompt muons. Moreover the BMTF reduced the legacy algorithm latency running at a speed three times faster than the legacy hardware. Both TwinMux and BMTF are single slot double-width and full-height µTCA board based around a Virex-7 FPGA and embedding the optics for high speed data transmission (up to 13Gbps). The BMTF board is an MP7 card (multipurpose hardware wide used in the trigger upgrade of CMS) while for the TwinMux a custom hardware development was necessary since the DT on-detector electronics transmit data at a low rate requiring a deserialization done by the standard I/O input of the FPGA.

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The Trigger Readout Electronics for the Phase-I Upgrade of the ATLAS Liquid Argon Calorimeters

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LHC is planned to run at high luminosity during Run 3 from 2021 through 2023. In order to improve the identification performance for electrons, photons, taus, jets, missing energy at high background rejection rates, a new trigger readout system is being designed to process the signals with higher spatial granularity. The LAr Trigger Digitizer Board (LTDB) that will process 320 Super Cells signals is being developed. In this paper, results of the 64-channel LTDB and LTDB pre-prototype will be presented. Progress of development of the LTDB prototype for the final trigger readout system will be discussed as well.

Summary:

The planned upgrade of the LHC will increase the instantaneous luminosity to $2 - 3 \times 10^{34} \text{cm}^{-2} \text{s}^{-1}$. The trigger readout electronics for the Phase-I upgrade of the ATLAS Liquid Argon (LAr) Calorimeters will be installed on the ATLAS detector during the second long shutdown of LHC in 2019/2020. The upgrade will improve the trigger energy resolution and efficiency for selecting electrons, photons, tau leptons, jets, and missing transverse momentum, while enhancing discrimination against pile-up. The readout of the trigger signals will process 34,000 so-called Super Cells at every LHC bunch-crossing at 12-bit precision and a frequency of 40 MHz.

The LTDB is the key electronics board for the upgrade. It will digitize the Super Cells signals and send processed data to the back-end electronics, where data are transmitted to the trigger processors. Each LTDB will process up to 320 Super Cells signals. The output data connection of an LTDB consists of up to 40 optical fibers running at 5.12 Gbps through the use of a custom serializer and optical link. With a total of 124 LTDBs in the system, the total rate to the back-end electronics is approximately 25 Tbps.

In order to evaluate performance of the upgraded electronics, understand the integration and manufacturing of large circuit board, an LTDB pre-prototype with the key components that are planned to be used for the LTDB has been developed. The LTDB pre-prototype processes the signals by the analog...
A circuit that will be used on LTDB. It uses 80 custom 12-bit ADCs to digitize the signals, 10 Xilinx Artix-7 FPGAs to process the ADC data, and 20 custom MTx dual channel optical transmitters to send the serialized data to back-end electronics.

An LTDB 64-channel test board has been developed to verify the final design. The board is also an integration test platform for the radiation-tolerant ASICs used on LTDB. There are 16 custom 12-bit ADCs to digitize the Super Cells signals, and 4 custom Link-on-Chip (LOCx2) devices to interface with the ADC, prepare the data and serialize them for the optical transmitter. There are also 4 custom MTx dual channel optical transmitters to transmit the data to the LDPB (Liquid Argon Digital Processing Board), 1 GBTx, 1 GBT-SCA and 1 MTRx to configure on-board devices, control the power supply and monitor the voltage, current and temperatures. The preliminary test results show the radiation-tolerant ASICs work properly.

The final version of the LTDB prototype is being designed. It will implement 80 custom 12-bit ADCs to digitize 320 Super Cells signals, 20 custom LOCx2 devices, 20 custom MTx dual channel optical transmitters, 5 each of the GBTx, GBT-SCA and MTRx modules to implement the timing, slow control and configuration of the on-board devices.

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Versatile Link PLUS Transceiver Development

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The Versatile Link PLUS project (VL+) targets the phase II upgrades of the ATLAS and CMS experiments. It will develop a radiation resistant optical link, operating at up to 10Gbps in the upstream and 5Gbps in the downstream directions with a smaller footprint and higher channel count than its predecessor. A low-profile package is being developed that allows volume production at reduced costs, but which nevertheless can be configured at assembly time to suit the individual needs of different detectors. This paper describes the development strategies and summarizes the status of the feasibility demonstration phase of the project.

Summary:

During the phase II upgrades of the ATLAS and CMS experiments at the Large Hadron Collider (LHC) several detectors will be replaced to improve their physics performance. To cope with the increasing data volume and the higher trigger rate, high-speed optical links will be deployed in large quantities as part of the upgrade programme. The tight space constraints and the high channel count of the detector electronics will require to develop a low-profile (20mm x 10mm x 2mm target), multi-channel front-end component. During their expected lifetime these components have to withstand the on-detector radiation levels (1 MGy total dose, 2e15 n/cm2 and 1e15 hadrons/cm2 total fluence) and they have to operate over a wide temperature range (-35 to +60 degC). The Versatile Link PLUS (VL+) project is developing custom front-end modules that fulfil these requirements. To suit the specific needs of different detectors, such as the number of transmit and receive channels, the modules will be configurable at assembly time.

To achieve the aforementioned goals with the lowest possible risk the VL+ project is pursuing two development paths with several industrial partners. In the first case, a full custom front-end module is being designed by CERN based on in-house developed radiation hard ASICs and qualified optical components, which will be assembled by an industrial partner. In the second case, CERN will work with commercial module manufacturers that are willing to customize their proprietary package to include the above mentioned components.
To demonstrate the feasibility of the full custom VL+ transceiver development, a prototype has been designed, manufactured and tested. Two additional prototypes that more closely resemble the desired front-end module are being designed. The paper will summarize the experience gained during this iterative process, and it will show measurement results obtained during functional and environmental tests. To launch the discussion about the second development path with various module vendors a procurement strategy has been defined. The paper will describe the proposed customization steps and it will show the results of the tests carried out on two candidate components provided by different manufacturers.

High speed electrical transmission line design and characterisation

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Many experiments require high data rates, implying custom link design using transmission line theory.

Transmission line theory is presented including FEA analysis of energy dissipation in exemplar designs. The choice of transmission line designs are reviewed.

Transmission line design principals and testing equipment are presented. The characterisation techniques of time-domain reflectometry and frequency-domain measurements are discussed and compared.

Bit-error-rate testing is presented and its limitations for design discussed. Finally, the gains in error free transmission rates due to signal equalization that corrects for signal degradation, including; pre-emphasis, CTLE or adaptive methods, is given.

Summary:

For data rates up to a few Mbps transmission hardware can be designed using DC electrical principals. PCB traces and cables are adequate if they pass a simple conductivity test. New design and testing rules are required for higher speed data links to function as required.

Vertex and tracking subdetectors of HEP experiments can delivery data rates up to 5Gbps, which would commercially be transmitted optically. However, due to the high radiation environment and low radiation length requirements electrical transmission is often required with custom designs.

The electrical engineering community has established basic design principals for high frequency transmission lines. Transmission line theory is presented, with different types of transmission lines analysed, including; two wire (twisted pair and twinaxial cables) and the stripline. Simulations of the electrical properties are performed using ANSYS Q3D Extractor. Q3D performs finite element analysis of defined structures based on the geometric layout and dielectric properties of materials. For expediency, 2D simulations based on data-link cross-sections were used as the link is assumed to be uniform over distance. Simulations calculated the expected electric performance over a range of frequencies. Complete electromagnetic characterization of different designs is obtained in the form of scattering parameters (S-parameters) from which reflection and transmission is assessed. Connection features such as differential signaling, impedance and length were adjusted to suit the simulation. Geometric representations of fields at a given frequency were used to illustrate flow of charge and hence data transmission through the design.

From the simulation of exemplar designs of transmission lines the choice of design for a given set of
boundary conditions is reviewed. When designing high-speed transmission lines, there are many key rules to follow. We discuss, based on our experience, several of these, including: using tightly coupled differential traces; using a continuous small signal return line following the data line; using guard traces between signal traces to reduce cross talk; matching the impedance of all cables and connectors to avoid reflections; using dedicated high-speed materials dielectric and copper layers. Moreover, great care has to be taken in connector and via layout.

The characterisation techniques of time-domain reflectometry and frequency-domain measurements (obtained via a network analyser) to measure signal distortion introduced by the transmission line are discussed and compared. The network analyser produces an $S$-parameter by measuring the magnitude and phase of the incident, reflected, and transmitted signals and is related to the familiar quantities of transmission coefficient, insertion loss and gain of the link. The time domain analysis further helps to identify transmission features in the physical item, for example layer stack-up and interconnects that cause crosstalk and reflections. Based on our experience we discuss the best methods to determine defects in transmission lines from $S$-parameters and TDR measurements.

Bit-error-rate testing is presented and its limitations for design discussed. Finally, gains in error free transmission rates due to signal equalization methods that corrects for signal degradation, including; pre-emphasis, CTLE or adaptive methods, are given.

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**An FPGA based track finder at Level 1 for CMS at the High Luminosity LHC**

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A new CMS Tracker is under development for the High Luminosity LHC from 2025. It includes an outer tracker based on “PT-modules” which will construct stubs, built by correlating clusters in two closely spaced sensors. Reconstruction of tracks from stubs is required if the tracker is to contribute to the Level1 trigger under increased luminosity. A concept for an FPGA-based track finder using a fully time-multiplexed architecture is presented. Results from a hardware demonstrator system, where a slice of the track finder has been constructed to help gauge the performance of a full system, will be included.

**Summary:**

The High Luminosity LHC (HL-LHC) will deliver luminosities of up to $5 \times 10^{34} \text{cm}^{-2}/\text{s}$, with an average of around 140 to 200 overlapping proton-proton collisions per bunch crossing. These extreme pileup conditions place stringent requirements on the trigger system to be able to cope with the resulting event rates. One of the goals of CMS for the high luminosity upgrade is to maintain the physics performance achieved during Run 1 in 2012. While the Level-1 (L1) trigger will be upgraded to provide a maximum trigger rate of around 750 kHz (compared to <100 kHz in Run1), even with this increase in rate the thresholds for basic objects (muons, electrons, jets etc) will have to be tightened if no new information can be provided towards the L1 trigger making decision. Therefore a L1 trigger that can make use of reconstructed data from the silicon strip tracker is desirable, thanks to its superior momentum and spatial resolution for charged particles.

The tracking trigger task is to deliver track objects to the L1 trigger within about $5 \mu s$, in order to allow this information to be merged with that from other sub-detectors. Given that a 40 MHz silicon-based tracking trigger on the scale of the CMS detector has never been built, it is essential to demonstrate the feasibility of such system.

A concept for an FPGA-based track finder using a fully time-multiplexed architecture is presented, where track candidates are identified using a projective binning algorithm known as the Hough Transform. The detector is segmented into eight trigger regions in $\phi$. By fully time multiplexing, each processing card receives all the data from an entire trigger region so that all regions can be treated, and demonstrated, independently. Results from a hardware demonstrator system, where a time slice of one track finding
region has been constructed to help gauge the performance and requirements for a full system, will be reviewed.

The demonstrator system itself is conceptually divided into logical processing elements each of which is implemented on separate identical boards. The board is the Imperial MP7, a processing card which is capable of handling 0.94Tbps on 72+72 optical input and output links, using the Xilinx Virtex 7 V690 FPGA. One advantage of this division into steps is that it allows algorithms to be tested in isolation or as part of the daisy chain, using common hardware and infrastructure. Provided the algorithms are scalable, it also allows for estimation of final performance without being limited to the boundaries of current FPGA technology. A description of the algorithms currently implemented will be presented and a discussion of future developments and prospects for this track finding proposal will be provided.

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**The 10G TTC-PON: Challenges, Solutions and Performance**

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The TTC-PON (Timing, Trigger and Control system based in passive optical networks) was first investigated in 2010 in order to replace the current TTC system, responsible for delivering the bunch clock, trigger and control commands to the LHC experiments. A new prototype of the TTC-PON system is now proposed, overcoming the limitations of the formerly presented solutions. A new upstream data transmission scheme relying on longer bursts is described, together with a high-resolution calibration procedure for aligning bursts in a time division multiplexing access. An error correction scheme for downstream data transmission is also depicted.

**Summary:**

The TTC-system (Timing, Trigger and Control) is responsible for distributing the bunch clock, carrying the level-1 trigger accept decision and some control commands to the detector sub-partitions. The current system employs a unidirectional optical link multiplexing two channels at 40Mb/s each, and an external electrical link is employed to allow busy/throttle status signals propagation from the front-end buffers to the trigger control system.

An alternative for this system, based on FPGAs and passive optical networks (PONs) was initially proposed in 2010 in order to overcome the limitations of the current TTC-system (low bandwidth, lack of bidirectionality). Passive Optical Networks are a consolidated solution widely adopted by the telecommunications industry in the FTTx (Fibre to the X) premises for delivering high bandwidth to the subscribers. It is based on a point-to-multipoint optical communication system, which allows bidirectional data transmission in two different wavelengths. A master node, called OLT (Optical Line Terminal), broadcasts information to several slave nodes (downstream data transmission) and the slaves, called ONUs (Optical Network Units), send information back to the OLT in a time division multiplexing (TDM) scheme.

The original TTC-PON prototype, based on 1G Ethernet PON technology, was built in 2010 and fully characterized in 2012, when a set of metrics was adopted to evaluate the quality of the downstream and upstream data transmission schemes. In 2015 a new prototype based on the XGPON technology was built. However, it presented some limitations in the upstream data transmission scheme (very low dynamic range, very sensitive to temperature variations, need for customization of the commercial components) and in the downstream data transmission scheme (low split ratio with a safe margin). In addition, all the previously developed prototypes were using a single FPGA to emulate the full system. Even though the FPGA firmware was carefully partitioned, this solution was not close enough to the final application.

A new prototype was therefore implemented using individual Kintex-7 FPGA development boards (KC705 boards) for each node of the system, which are independently controlled via Ethernet. In order to overcome the limitations of the formerly proposed solution, a new upstream data transmission scheme consisting of longer bursts (125 ns) has been defined and a fine calibration procedure allowing high-resolution (0.417 ns) burst positioning has been implemented. In the downstream data transmission
path, an error correction scheme is being developed in order to allow a higher split ratio. The challenges and proposed solutions of this new prototype will be presented together with a full characterization of the system.

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**ProtoPRM: An FPGA-Based High Performance Associative Memory Pattern Recognition Mezzanine**

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Pattern recognition associative memory (PRAM) devices are parallel processing engines which are used to tackle the complex combinatorics of track finding algorithms, particularly for silicon based tracking triggers. In the talk we present our latest PRAM-based pattern recognition mezzanine card design which supports both ASIC and FPGA based PRAMs, and describe how the PRAM interface and FPGA firmware modules work in conjunction to implement a high performance fully pipelined low latency track finding engine. This work is part of the overall program for Level-1 silicon-based tracking trigger generic R&D for high luminosity LHC.

**Summary:**

PRAM development has been limited mostly to the realm of ASICs, often a lengthy and expensive process. Field Programmable Gate Arrays, however, allow for quick iterations and low cost design cycles, making them an ideal hardware platform for designing and evaluating new PRAM features before committing them to silicon. At the functional level, our ASIC and FPGA based PRAM designs match closely. Input data is divided into six detector layers, and the coarse information of these layer hits are written to the PRAM device, which is programmed to look for matching patterns. The addresses of the matched patterns are then read out of the PRAM sequentially. Both the ASIC and FPGA PRAM designs are fully pipelined and allow for concurrent read-in (of current event) and read-out (of the previous event) operations. This two stage pipelined architecture offers important performance benefits.

It is in the implementation details, however, that the differences between the ASIC and FPGA PRAM designs become apparent. In our experience we have found that logic blocks which have been optimized for fine-grain ASIC architectures do not implement efficiently in coarse-grain FPGA logic cells without significant redesign. In particular, the pattern storage elements and backend sorting logic was completely redesigned to fit efficiently into Kintex UltraScale FPGAs while still retaining cycle-accurate emulation of our PRAM ASIC design.

Our prototype Pattern Recognition Mezzanine (protoPRM) board is a high performance track finding engine implemented using two Kintex UltraScale FPGAs. On this board the slave FPGA emulates the PRAM, as described above. The master FPGA is used to format and store input data, which is then used in conjunction with the PRAM output to find and fit tracks. First, incoming detector layer hits (called stubs) are remapped from a local to global coordinate system. From these global stubs coarse resolution super-strips (SSIDs) are generated and sent over a local bus (8 x up to 16.3Gbps MGT lanes) to the slave FPGA or PRAM, which outputs found patterns (called roads). While the PRAM is processing SSIDs, the full resolution stubs are stored in a database, called the data organizer. The data organizer is a new design which has been optimized for UltraScale BlockRAMs and completely eliminates intermediate address pointer structures. The result is a high performance, low latency, fully pipelined data structure which presents a FIFO-like write interface and reads out like RAM. Stubs recalled from the data organizer are now organized in terms of “hits of interests” or roads and are then sent to downstream stage for track fitting.

Firmware modules throughout the protoPRM have been significantly redesigned to reduce latency and support the pipelined PRAM interface. The protoPRM board will be used in our L1 tracking trigger
Neural hardware architectures for spatio-temporal data processing

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The brain is characterized by extreme power efficiency, fault tolerance, compactness and the ability to develop and to learn. It can make predictions from noisy and unexpected input data. Any artificial system implementing all or some of those features is likely to have a large impact on the way we process information. With the increasingly detailed data from neuroscience and the availability of advanced VLSI process nodes the dream of building physical models of neural circuits on a meaningful scale of complexity is coming closer to realization. Such models deviate strongly from classical processor-memory based numerical machines as the two functions merge into a massively parallel network of almost identical cells. The lecture will introduce current projects worldwide and discuss computational principles suited for the analysis of spatio-zemporal patterns in large data volumes.

**Trigger / 66**

Design and test performance of the ATLAS Feature Extractor trigger boards for the Phase-1 Upgrade

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In Run 3, the ATLAS Level-1 Calorimeter Trigger will be augmented by an Electron Feature Extractor (eFEX), to identify isolated e/g and t particles, and a Jet Feature Extractor (jFEX), to identify energetic jets and calculate various local energy sums. Each module accommodates more than 420 differential signals that can operate at up to 12.8 Gb/s, some routed over 20 cm between FPGAs. Presented here are the module designs, the processes that have been adopted to meet the challenges associated with multi-Gb/s PCB design, and the results of tests that characterise the performance of these modules.

**Summary:**

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Application of flash-based field-programmable gate arrays in high energy experiments

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Field-programmable gate arrays (FPGAs) based on flash memories provide a high radiation tolerance. We discuss potential application of the Microsemi IGLOO2 FPGAs in high energy experiments. We implement a 24 channel time-to-digital converter with a time binning of 0.78 ns and evaluate the performance. The time resolution is obtained to be 0.25 ns. The radiation tolerance against total ionizing dose is studied by irradiating gamma ray up to 10 kGy using Cobalt-60 source. The degradation of the performance on the ring oscillator, the phase-locked loop, and the high-speed transceiver is evaluated.

Summary:
Field-programmable gate arrays (FPGAs) are widely used in the experiments of high energy physics. FPGAs based on flash memories have relatively high radiation tolerance with respect to the FPGAs based on static random access memories. It extends the potential application of the FPGAs. In this study, the flash-based IGLOO2 FPGA produced by Microsemi is focused on. A time-to-digital converter (TDC) with time binning of 0.78 ns is implemented and tested. The radiation tolerance against total irradiation dose is evaluated using gamma ray up to 10 kGy.

An example of the application of the TDCs is the drift time measurement for the monitored drift tube chambers at the ATLAS experiment. The TDCs are implemented in application-specific integrated circuits, which have 24 channels per chip and time binning of 0.78 nsec. In this study, we implement a 24 channel TDC with a time binning of 0.78 nsec in the IGLOO2 FPGA. The time measurement is provided by the counters running with a frequency of 1.28 GHz. The counters are based on a multisampling scheme with quad phase clocks, each of which has a frequency of one fourth of the one for the counters. The quad phase clocks are produced from an external 40 MHz reference clock using highly reliable phase-locked loop circuit implemented in the FPGA.

As a performance evaluation of the implemented TDC, the differential nonlinearity is measured to be less than 0.5 of the time binning for all the least significant bits of the 24 channels. The integral nonlinearity is consistent with zero up to time window of 100 ns. The time resolution is obtained to be about 0.25 ns.

The radiation tolerance against total ionizing dose is studied with a dedicated test board which includes an IGLOO2 FPGA. Gamma ray is irradiated up to 10 kGy at the Cobalt 60 irradiation facility of Nagoya University in Japan. The degradation of the performance on the ring oscillator, the phase-locked loop, and the high-speed transceiver is measured. For the ring oscillator and the phase-locked loop, the frequency and the power consumption are measured. For the high-speed transceiver, the bit error rate and the eye diagram for several transfer speeds are extracted. The functionality of the firmware configuration is also tested.

In summary, we examine the performance of the flash-based Microsemi IGLOO2 FPGA. We implement a 24 channel time-to-digital converter with a time binning of 0.78 ns. The differential non-linearity is measured to be far below the time binning. The time resolution is obtained to be about 0.25 ns. The radiation tolerance against total ionizing dose is studied by irradiating 10 kGy of gamma ray using Cobalt-60 source. The degradation of the performance on ring oscillator, phase-locked loop, and high-speed transceiver is measured. Microsemi IGLOO2 FPGA extends the potential application of the FPGAs in high energy experiments.
This paper presents the results of an irradiation campaign up to 1 Grad on single transistors manufactured in a 28nm commercial CMOS technology. This technology is of interest for future upgrades for HL-LHC. NMOS transistors have been irradiated and electrical parameters have been measured. Moderate threshold voltage shift and sub-threshold slope degradation have been observed, while leakage current shows an increase of 3-4 orders of magnitude. These measurements are significant as this is the first technology evaluated for HEP applications using a High-K dielectric material for the transistor gate.

Summary:
During the next decade, the Large Hadron Collider at CERN will bring a factor ~10 increase in collision rate. Silicon Vertex Trackers will require to read out large area sensor matrices of highly pixelated detectors with low power consumption and high level of processing. In addition, exceptional levels of Total Ionizing Dose (TID), up to 1 Grad, and NIEL up to $10^{16}$ neq are foreseen. In order to comply with such challenging requirements, designers are considering to move to higher density CMOS technology nodes for the pixel readout channels.

In this paper we present the results of an irradiation campaign at the transistor level for a 28nm commercial bulk CMOS technology. A test chip containing standard and high threshold voltage (Vth) nMOSFETs and pMOSFETs and with several channel widths (W) and lengths (L) was fabricated for this purpose.

The irradiations were performed on standard Vth nMOSFETs, performed at the Physics and Astronomy Department of the University of Padova (Italy) with an X-ray source. The dose rate in SiO2 was about 8.3 Mrad/h. During irradiation, the NMOS devices were kept under standard ‘maximum-stress’ conditions (Vgs = Vds = 0.9V) and at room temperature. The chip was mounted on a semi-automatic probe station and contacted with a custom probe card with 32 probes. A Keithley 707 switching matrix connected the semiconductor device analyzer (HP4156) and the bias supply.

Standard Id vs Vgs and Id vs Vds characteristic curves were measured in steps up to a total dose of 1.05 Grad; electrical parameters like threshold voltage shift, sub-threshold slope, leakage current and saturation current were extracted.

The threshold voltage was extracted with the maximum transconductance method in linear region (Vds = 0.1V). The Vth shift trend depends on the transistor geometry and was found to be limited for wide transistors (monotonic decrease up to $\Delta$Vth = -40mV in the worst case) and more pronounced for narrow transistors. For the narrowest channel transistor (W=100nm, L=1µm), Vth shows a monotonic decrease up to $\Delta$Vth = -95mV at 250 Mrad, and then started to increase again up to 1 Grad. The calculated sub-threshold slope shows a similar trend: a limited increase, more pronounced for the narrow transistors ($\Delta$ss = +16mV/dec in linear region and $\Delta$ss = +22mV/dec in saturation).

No decrease in the saturation current is observed; instead a very pronounced increase of the leakage current has been measured for all transistors (up to 3-4 orders of magnitude). The observed leakage current is independent on W, as expected, since it comes from lateral parasitic transistors.

These results show that a state of the art High-K metal gate technology does not introduce unexpected bad behaviors when irradiated to HL-LHC levels and that therefore HEP designers may be able to use the use it and profit from the intrinsic low-power advantages which are accompanying this technology. An irradiation campaign on pMOSFETs is currently undergoing and results will be reported later.

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Real Time FPGA Design for the L0 Trigger of the RICH Detector of the NA62 Experiment at CERN SPS

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The NA62 experiment aims to measure rare kaon decays, in order to precisely test the standard model. The RICH detector of the experiment is instrumental in charged-particle identification and in measurement of their crossing time, with a resolution better than 100ps. Here we describe the design of the Level-0 trigger system for the RICH, which provides a precise time reference by counting the input hit multiplicity within programmable fine-time windows. Because the design doesn’t use spatial information and stands the maximum input rate of TDC-based NA2 systems, it can be employed also in other detectors.

Summary:

The NA62 experiment at CERN is focused on a precise measurement of the branching-ratio of the very rare kaon decay $K^+ \rightarrow \pi^+ \pi^0$. In order to achieve that, various detectors are placed along the fiducial decay region, where a high intensity $K^+$ beam is kept in vacuum. RICH detector aims to identify final-state particles (mostly $\pi$ and $\mu$) and measure their crossing time, with a resolution better than 100ps. In order to extract useful data from the intense flux, a three-level trigger system was developed. RICH L0-trigger (L0) provides precise time reference to the other levels of trigger, together with the multiplicity in a settable window. L0 is designed for TEL62 boards, which are the general-purpose boards for trigger and acquisition. The board is composed of 4 Pre-Processing FPGAs receiving data from 4 daughter cards (TDCs) and sending the output to a Sync-Link FPGA, which merges the data and sends them to the Level-0 processor and the PC farm. All TEL62 FPGAs are Stratix III devices, clocked with a frequency of 160 MHz. In the FPGAs both the acquisition and trigger modules coexist, so the design logic occupation must be the lowest possible.

The aim of the RICH L0 primitive-generating firmware is to produce clusters of hits belonging to the same Cherenkov circle. No spatial information is used and only time clusters are produced, making this firmware very general and suitable for other detectors. In order to obtain more generality, a common 32-bit data format called RICH format was developed. Each module of the firmware uses RICH format as input and output, in order to move the modules wherever they are needed and to easily validate the data flux inside the FPGA. This format makes the firmware ready to the employment of InterTEL boards, which will be used to interconnect TEL62 boards.

The core of the firmware consists of 64 cells, arranged in 16 rows. A distributor sends hits belonging only to a 25ns time frame to each row, avoiding to split clusters between two consecutive bunches. Each cell takes its first input as time reference and clusters hits in input within a time-window. A collector receives clusters from the rows, time-sorts them down to 100ps and formats them with the RICH format. Particular attention was paid to reduce combinatorial paths length, in order to save logic utilization and improve the maximum clock frequency reachable by the design.

All the algorithms produced are real-time algorithms, which can stand the maximum input rate of TEL62 and TDC based detectors. After successful simulations and tests on the actual environment, the system was implemented in RICH TEL62s. Thanks to a very general design and to a maximum reachable clock frequency greater than the used one, the system could also be used in L0 trigger of other TDC-based detectors of the NA62 experiment.

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First studies on AMS H35 CMOS devices for application in the ATLAS tracker upgrade

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H35Demo chips are HV-CMOS devices produced in the 350nm AMS technology with the purpose of inquiring the opportunity to introduce this technology in the next ATLAS tracker upgrade. Each chip includes four different pixel matrices and three test structures. The results of TCT (Transient Current Technique) and edge-TCT analysis on the test structures from with different substrate resistivity before and after irradiation will be shown. Also the first results from the stand alone readout of the monolithic matrices will be shown.

Summary:

The High-Voltage CMOS (HV-CMOS) technology has recently been introduced in the high energy physics community. The opportunity to include the pixel electronics within the sensor substrate brings major advantages to particle tracking detectors. Sensors produced in the HV-CMOS technology can be thinner, faster and cheaper with respect to the silicon detectors currently in use.

H35Demo chips have been produced in order to study the radiation hardness of such detectors and verify the possibility to introduce this technology in the next ATLAS tracker upgrade for the high luminosity LHC. These chips are HV-CMOS devices produced in the 350nm AMS technology (H35). They have been produced on wafers with different substrate resistivity ranging from the standard value of 20 Ω·cm to 1000 Ω·cm to increase the depletion region of the sensor.

Each chip includes four different pixel matrices, two of them are fully monolithic and can be read out stand-alone while the others two require to be bonded to a readout chip. All the four matrices are suitable to be read out via the FE-I4 readout chip through gluing or bump bonding. In addition the chip includes three test structures to characterize the sensor properties. The first includes the electronics for measuring the pixel intrinsic capacitance, the second is a matrix of nine pixels with a source follower output buffer, the third one is a single diode with eight neighbours that do not include additional electronics allowing to directly sample the signal waveform. This last structure has been used to characterize the samples with the Transient Current Technique (TCT).

The TCT allows to trigger the waveform readout on the injection of a laser pulse. The light crossing the sensor generates the electron-hole pairs inducing the signal. Illuminating the sensors from the side, a technique known as edge-TCT, it is possible to study the signal generation at different depths and measure the depletion depth of the substrate.

The results of TCT and edge-TCT studies performed on the test structures with different substrate resistivity before and after irradiation will be presented together with the first results of the stand alone readout of the monolithic matrices through the set-up developed at IFAE.

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Evaluation of GPUs for High-Level Triggers in High Energy Physics

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Modern High Energy Physics Trigger Systems require high data throughput on the Gigabyte scale and latencies in the range of a few microseconds.

Traditionally, those requirements could only be met by expensive, dedicated hardware like FPGAs and ASICs.

However, GPUs provide high-performance and pose an affordable and easily programmable alternative.

In this paper we evaluate modern GPGPUs as a flexible alternative to traditional approaches.

We discuss the performance, throughput and latency of commonly used algorithms and give an overview of possible benefits as well as downsides of this approach.

Finally, we give a brief outlook of possible future developments.

Summary:

The CMS experiment at the LHC at CERN will face a major luminosity increase in its upcoming phase 2 upgrade.

With a luminosity of $10^{34}$ cm$^{-2}$s$^{-1}$ corresponding to an increase in the number of collisions by a factor of 10 and pileups of around 140.

The detector produces roughly 50 Tb/s of tracker data that need to be processed by the trigger systems within a timing window of as low as 12 µs.

In order to meet such requirements, new trigger architectures need to be developed. Such systems are commonly developed based on FPGAs and ASICs, which, while being highly customizable for the application, are generally expensive, both in cost and maintenance time.

The Institute for Data Processing and Electronics at the Karlsruhe Institute of Technology has started to investigate alternative approaches for such trigger systems, based on modern high-performance computing (HPC) technologies.

One of the most promising trends in the area of HPC is the processing of data with the aid of general purpose graphics processing units (GPGPUs). GPGPUs have seen rapid advances in performance over the last decade.

Software development frameworks such as CUDA and OpenCL have further increased the accessibility of GPGPUs for scientific computing.

In this work we evaluate Track Seeding and Track Finding approaches, based on GPGPUs to be used as online Level-1 Track Trigger Systems at the example of the CMS experiment, specific to its phase 2 upgrade.

We compare the performance and latency on different generations of graphics cards, both on older and very recent hardware, as well as for both prominent Software Development Frameworks, OpenCL and CUDA, and discuss their respective benefits and limitations.

First results show processing times as low as 7 microseconds for the track seeding step, utilizing a Hough Transform approach, with a detector segmentation similar to what has been used by FPGA based trigger systems.

We present performance measurements for track seeding and track fitting and discuss their respective suitability for GPUs in general, as well as their flexibility with regard to possible changes in the not yet fully realized detector layout.

Furthermore, we also briefly discuss the quality of the used algorithms in terms of track finding efficiency, based on the official, preliminary Monte Carlo Simulation data for the detector. The results are validated by the CMS Software Framework (CMSSW).

An overview of recent graphics processors and memory developments is given, to provide an estimate of the performance that we may expect to see in the near future.

The results so far indicate that GPUs are a potential candidate for future trigger systems, while simultaneously offering more complex computational capabilities for the ever increasing requirements of HEP experiments.
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Summary:

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Introduction

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Design of an AdvancedTCA board Management Controller Solution

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FPGAs in radiation: Recent results from Kintex7

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Proposal of a specification for ATCA shelves used in experiments at CERN

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FPGAs in radiation: Recent results from Artix7

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Present and future xTCA developments in CMS DAQ group

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**FPGAs in radiation: Recent results from SmartFusion2**

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**Summary:**

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**A generic software component enabling communication between IP-Bus and OPC-UA**

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**GBT-FPGA tutorial**

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**Summary:**

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**The use of ATCA in CMS at the HL-LHC**

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**Discussion**

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**The CMS Level-1 Calorimeter Trigger for LHC Run II**

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Results from the completed Phase 1 Upgrade of the CMS Level-1 Calorimeter Trigger are presented. The upgrade was completed in two stages, with the first running in 2015 for pp and Heavy Ions and the final stage for 2016 data-taking. The hardware uses Xilinx Virtex-7 690 FPGAs and 10 Gbps optical links and operates in microTCA chassis. Stages of the upgrade were commissioned in parallel with the previous trigger. Innovations were evaluated, such as embedded linux on trigger processing boards and simultaneous eye-scans on data links. The final stage architecture is time-multiplexed.

Summary:

The LHC has resumed operations since the spring of 2015. During Run II, the instantaneous luminosity is expecting to exceed the design parameters of the machine. To maintain acceptance for proton and heavy ion collision events of interest without exceeding the 100 kHz limit, the CMS Level-1 (L1) trigger has been being upgraded. The L1 calorimeter trigger, which finds electrons, photons, tau leptons, jet candidates and computes energy sums, has been upgraded in two stages. In these intense conditions, both stages have implemented pile-up mitigation techniques in order to reach acceptable performance. Modern technologies offer an effective solution to achieve these goals. The upgraded system makes use of new Xilinx Virtex-7 based AMC cards form the microTCA technology.

The final stage of the upgraded architecture implements an innovative approach called the Time-Multiplexed-Trigger (TMT). Higher granularity inputs, algorithms operating on a wider field of view allow for improved position and energy resolution of regional and global quantities. Calorimeter trigger primitive data is transmitted on 1,152 optical links running at either 4.8 Gbps or 6.4 Gbps. This is pre-processed at Layer-1 before being time multiplexed to Layer-2 where each node processes data from the entire calorimeter. Optical interconnects are via 10 Gbps optical links, which allow easy reconfiguration or expansion as required. This has been made substantially easier with the early adoption of Molex Flexplane technology. Data is then de-multiplexed before sequential transmission to the Global Trigger.

Calorimeter Trigger Processor, Virtex-7 (CTP7) AMC cards serve as the Layer-1 pre-processors, and MP7s serve as the Layer-2 Master Processor nodes. This approach is designed to allow for a high processing clock speed of 240 MHz and thus efficient use of logic resources. The fully pipelined firmware approach of the TMT provides an efficient way to localize the processing, reduce the size and number of fan-outs, minimize routing delays and eliminates register duplication. All calorimeter object algorithms are placed and routed into a single board using a precise FPGA floorplanning. The High Level Trigger model inspired the design of the upgraded Level-1 system.

The talk will cover the technological aspects of the Run II calorimeter trigger system emphasizing the many challenges of its implementation and commissioning over the past year. Results of its performance during the first 2016 collisions of the LHC will be presented and used to illustrate the experience learnt in terms of commissioning this complex electronics systems which relies on the deployment of high-speed optical links and large FPGA processing. The AMC boards designed for this project are aiming towards a standardization of the data processing required for the future LHC electronics systems.

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Installation, Commissioning, and Running of the ATLAS Fast Tracker Hardware System

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The ATLAS detector at the LHC is in the process of integrating new components to handle the increased collision energies and luminosities being delivered since 2015. The Fast TracKer (FTK) is a hardware processor built to reconstruct tracks at a rate of up to 100 kHz and provide them to the high level trigger. FTK uses FPGA’s to match inner detector hits with pre-defined track patterns stored in associative memory on custom ASICs. This presentation describes the electronics facilitating FTK’s
massive parallelization alongside the planned installation and commissioning of the system during 2016.

Summary:

From 2010 to 2012 the Large Hadron Collider (LHC) operated at a centre-of-mass energy of 7 TeV and 8 TeV, colliding bunches of particles every 50 ns. During operation, the ATLAS trigger system performed efficiently contributing to important results, including the discovery of the Higgs boson in 2012. The LHC restarted in 2015 and will operate for four years at a centre-of-mass energy of 13 TeV and 14 TeV with bunch crossings every 25 ns. These running conditions result in the mean number of overlapping proton-proton interactions per bunch crossing increasing from 20 to 50. The Fast Tracker (FTK) will allow the trigger to utilize tracking information from the entire detector at an earlier event selection stage than ever before, enabling more efficient event rejection.

The FTK is designed to perform full scan track reconstruction of every event accepted by the ATLAS first level hardware trigger. To achieve this goal the system uses a parallel architecture, with algorithms designed to exploit the computing power of custom Associative Memory chips and modern field programmable gate arrays. The processor will provide computing power to reconstruct tracks with transverse momentum greater than 1 GeV in the whole tracking volume. The tracks will be available at the beginning of the trigger selection process, facilitating the development of more pileup resilient triggering strategies. The Fast Tracker system will be extremely large, with about 8000 Associative Memory chips and 2000 field programmable gate arrays, providing full tracking with a rate up to 100 KHz and an average latency below 100 microseconds. The system will begin commissioning in 2016, with full barrel coverage reached by the end of the year. We present the final version of the electronics, with details covering the hardware status and installation of the system. An overview of the commissioning status and first data-taking experience will also be presented.

Plenary / 21

TOFFEE: a fully custom amplifier-comparator chip for timing applications with silicon detectors.

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In this contribution we present the design of a 8-channel amplifier-comparator chip specifically optimized to match the signals produced by Ultra-Fast Silicon Detectors (UFSD). The time resolution of the TOFFEE – UFSD system is expected to be around 30 ps. The chip is designed in UMC 110nm CMOS technology, it has a 2x2 mm area and it requires 40 mW per channel. It features LVDS outputs and the signal dynamic range matches the requirements of the HPTDC system.

Summary:

The next generation of high-energy experiments will require the capability of taking data at unprecedented intensities, with hundreds of overlapping events. To face this challenge, we need the possibility to distinguish events separated by a few tens of picoseconds. For this reason, segmented silicon sensors with internal gain are being developed (the so called Ultra-Fast Silicon Detectors) so that they will provide the traditional silicon sensor benefits (segmentations, low leakage current, low noise, low capacitance) together with a much larger signal.

We have developed a fully custom ASIC to take advantage of this enhanced signal, optimizing the input stage of the chip to the signal shape of UFSD. The chip provides 8 independent amplifier-comparator channels, each with a comparator threshold controlled via an external voltage level. Each channel
comprises a trans-impedance amplifier followed by a discriminator, a stretcher and LVDS driver. The CSA amplifier is implemented with a cascode with split current sources for best noise performances. The discriminator gives an output step between 2 and 14 ns, however to be compatible with the HPTDC input logic (minimum signal length ~ 12 ns), the signal is lengthened by 10 ns. The chip uses two power values, 1.2 Volt for the analog part, and 2.5 Volt for the LVDS driver, with a total power consumption of 400 mW.

For a 6 pF input load, the gain value is around 7-10 mV/fC with a slope of 30-50 mV/ns and a r.m.s noise of 800 uV providing a SNR of ~ 75. For a much larger input capacitance of 60 pF the SNR drops to 14, with a slope of ~ 20 mV/ns and a r.m.s. noise of 1.4 mV. The rise time of the chip has been tailored to be equal to the collection time of a 50-micron thick UFSD sensor, around 1.8 ns, in order to optimize SNR.

The optimization of the chip design has been done using as inputs simulated signals from UFSD 50-micron thick sensors with a gain of 10, generated with the program Weightfield2. For a 6 pF input load, the combination of the TOFFEE chip coupled to 50-micron thick UFSD sensors with gain of 10 provides a r.m.s. time resolution between 25 – 35 ps.

The chip has been submitted in early May, and will be tested in the summer 2016.

The performance of the UFSD-TOFFEE system have been tailored to the need of the CT-PPS detector of the CMS collaboration. First beam test results should be available during the 3rd quarter of 2016, with installation during the winter shutdown 2016-2017.

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The VeloPix ASIC

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The LHCb upgrade, scheduled for LHC Run-3, will enable the experiment to be read out at 40 MHz in triggerless mode, with full event selection being performed offline. The Vertex Locator (VELO) will be upgraded to a pixel device with a new dedicated ASIC, the VeloPix, a 130 nm technology chip with data driven and zero suppressed readout. The sensors are positioned at just 5.1 mm from the LHC beams and the hottest ASICs will experience rates of more than 900 Mhits/s. The recently submitted ASIC will be presented along with the first test results.

Summary:

The LHCb upgrade, scheduled for LHC Run-3, will transform the experiment to a trigger-less system reading out the full detector at 40 MHz event rate. The Vertex Locator (VELO) will be a hybrid pixel system, featuring silicon pixel sensors with $55 \times 55 \mu m^2$ pitch, read out by the VeloPix ASIC. The sensors and ASICs will approach the interaction point to within 5.1 mm and be exposed to a radiation dose of up to 370 MRad or $8 \times 10^{15}$ 1 MeV n$_{eq}$ cm$^{-2}$. The hottest ASICs must sustain pixel hit rates of more than 900 Mhits/s and produce an output data rate of over 15 Gbit/s, adding up to 1.6 Tbit/s of data for the whole VELO.

This paper will present the VeloPix ASIC which has been developed for the readout of the upgraded VELO. This ASIC derives from the Medipix/Timepix family and has many features in common with the Timepix3, however the VeloPix is further optimised for speed and radiation hardness. Each ASIC reads out an array of 256 x 256 pixels with $55 \times 55 \mu m^2$ square pitch. TheASICs are flip chipped in groups of three to the silicon sensors, and a total of 624 ASICs are needed for the full VELO readout. In order to ensure the cooling of the ASICs within the LHC secondary vacuum the power consumption is limited to <3 W per ASIC; however the achieved performance is expected to significantly improve on this. The ASIC is designed in a 130 nm CMOS technology.

The ASIC readout is data driven and zero suppressed, and the implementation of the super pixel concept (4x2 pixel grouping) further optimises the bandwidth and available space. The timewalk is minimised
Because of the severe radiation environment the ASIC is equipped with SEU protection and is designed to cope with sensor leakage currents. In order to meet the huge data output rate requirement while keeping the power consumption within the budget a dedicated 5.12 Gbit/s output serialiser, the GWT (Gigabit Wireline Transmitter), has been developed. TheASIC has been submitted in April and we expect to show the very first performance results.

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**AM06: the Associative Memory chip for the Fast TracKer in the upgraded ATLAS detector**

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This paper describes the AM06 chip, a highly parallel processor for pattern recognition in high energy physics. AM06 contains memory banks that store up to $2^{17}$ patterns made up of 8x18 bit words and integrates SER/DES IP blocks for 2.4 Gb/s IO to avoid routing congestion. AM06 combines custom memory arrays, standard logic cells and IP blocks within a 168 mm$^2$ silicon area with 421 million transistors and can perform bitwise comparisons at 1.6 Pbit/s, consuming ~2 fJ/bit per comparison thanks to an optimized design based on XORAM cells.

**Summary:**

In this paper we describe the AM06 chip, which is a highly parallel ASIC processor for pattern recognition: its purpose is to find particle tracks in real-time as part of the Fast TracKer (FTK) processor, which is being installed in view of the next ATLAS upgrade. Version 6 of the Associative Memory chip is designed in 65 nm CMOS technology and is based on XORAM cell architecture. The AM stores segmented data and finds addresses that match a combination of segments with an input data sample. Being more than a memory device, it is an engine able to solve a class of combinatorial problems. The AM06 is tailored for real-time track finding in high-energy physics (HEP) experiments; however, it can be used also in many interdisciplinary applications (i.e., general purpose image filtering and analysis).

The chip has been designed with a mixed approach. AM core cells are fully customised to optimize area and power consumption. The remaining logic was been described in VHDL and synthesized in standard cells for rapid design and verification. Finally, serializer and deserializer IP blocks were used for data input and output, to avoid routing congestion at the PCB level. The AM serial data rate is between 2 GHz and 2.4 GHz, while the clock for parallel data rate inside the chip is 100 MHz.

The AM06 contains a large memory bank that stores all data of interest. The basic memory unit is a word of 18 bits; a set of 8 words from 8 different layers of the detector is called "pattern". The AM06 contains $2^{17}$ patterns. To reduce fake detection and to increase efficiency, the AM06 implements an elegant solution: "variable resolution patterns". De-serialized input data are fed to all memory blocks in parallel. A priority read-out tree has been used to serialize output results.

The AM06 is a complex VLSI chip with several parameters comparable with the Intel Core Duo processor. The chip contains 14 different clock domains, 7 different power domains, about 20 million standard cells, and about 421 million transistors. The AM06 performs synchronous bitwise comparison with a rate of about 1.6 Pbit/s. The latency from a
NEXT_EVENT signal to the first pattern readout out is in the range 25-30
clock cycles, referred to the IO clock. An alternative operation mode
reads pattern while hits are loading. In this case the latency is
similar and it is counted from the HIT that fires a pattern to the
first pattern out.

Power consumption has been a key point in the development of the chip. A
tough optimization was performed to reduce energy use to a value of ~2
fJ/bit per comparison. In the future, we plan to design a more powerful
and flexible chip in 28 nm CMOS, with the aim of achieving $2^{19}$ patterns
per chip with an even lower power consumption per comparison per bit.

Plenary / 4

Rad-hard DCDC converters for HL-LHC experiment’s tracker mod-
ules power distribution

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In the context of investigating a more efficient rad-hard power distribution scheme for HL-LHC track-
ers modules based on switching DC/DC converters, we developed two new prototypes, upFEAST2
and DCDC2S. The combination of upFEAST2 and two DCDC2S can provide the three required volt-
ages (2.5V for the opto-electronics, 1V for digital and 1.2V for analog circuitry).

DCDC2S and upFEAST2 are manufactured with commercial 0.13um and 0.35um high voltage CMOS
technology respectively. Design techniques, functional and radiation tests of the prototypes will be
discussed.

Summary:

The present design of pixel and strip modules for HL-LHC experiment trackers foresees a complex in-
tegration of different ASICs that requires several power domains: 2.5V for the optoelectronic drivers,
1.2V for the analog and 1V for the digital circuitry.

A very attractive power distribution scheme based on rad-hard DC-DC converters foresees different
conversion stages to obtain the required voltages. The first conversion stage is represented by a new
ASIC called upFEAST2 capable of converting 10-12V to 2.5V. The second stage is based on two ASICs
called DCDC2S, able to convert 2.5V to 1V and 1.2V respectively.

upFEAST2 is a modified version of the production ready FEAST2 ASIC, integrated in a similar 0.35um
high voltage technology in order to enhance its radiation tolerance (in particular the displacement dam-
age limit up to at least 5e15 n/cm²). upFEAST2 has been sent to production in March 2016 and it will
be available for test starting from June 2016.

DCDC2S is a completely new ASIC that has been designed in a commercial 0.13um technology. It
makes use of IO transistors rated 2.5V for the power part and 1.2V core transistors for the control cir-
cuity. DCDC2S is a fully integrated buck converter (except to input and output capacitor and inductor).
It includes overcurrent and input under-voltage protections.

The power transistors are two IO MOS with a width of 320mm and 240mm for the high and low side
respectively. The error amplifier has a bandwidth of 40Mhz and a Slew Rate of 10V/μs.

The internal oscillator is programmable from 1MHz to 10MHz with an external resistor. The voltage
reference is internal and it provides 0.3V with an error of 1% over 100oC and 400Mrad. The dead time
delay between the ON-states of high and low side power transistors is managed with the so-called "pre-
dictive logic". This logic reduces this delay as much as possible in order to increase the converter’s
efficiency.
A soft-start procedure is embedded to avoid too large inrush current at the start-up of the converter.
DCDC2S will be submitted in April 2016 and it will be available for test in July 2016.
Functional and radiation tests of upFEAST2 and DCDC2S will be presented at TWEPP.

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Reliability and failure mechanisms of Integrated Circuits and devices

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When scaling down CMOS towards smaller and smaller dimensions, the electrical fields inside the devices is increasing which leads to potential failures of the transistors. This can limit the lifetime of the circuits that are made in these technologies. As a result reliability is becoming more and more a fundamental limiting factor for the further downscaling of the technology. This lecture explains the main failure mechanisms that are acting at transistor level with focus on Time-dependent dielectric breakdown, Bias-temperature Instability and to a lesser extent also Hot carrier degradation. The basics as well as the test structures and characterization techniques needed to quantify the degradation, the voltage and temperature acceleration models and ways to cope with the problem and to improve the lifetime.

Summary:

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Test for timetable

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Summary: