MATRIX: a 15 ps resistive interpolation TDC ASIC based on a novel regular structure

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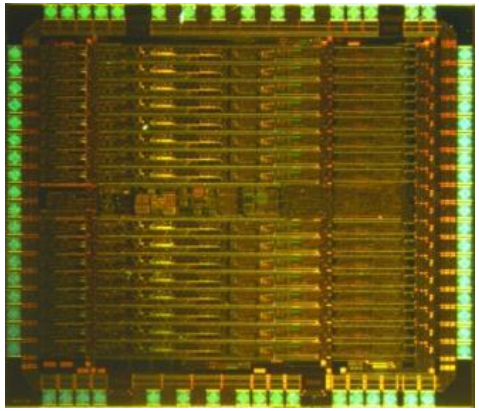
Outline

- **Motivation**
- MATRIX TDC Design Overview
- Measurement Results
- Conclusions & Future Work

Motivation

- SiUB PET ASIC ecosystem:
  - Broad experience in fast-timing ASIC designs.
    - FlexToTv1, FlexToTv2.
    - < 10-ps jitter floor.
    - 100-ps SPTR.
    - < 8% energy resolution.
    - Low power conspumption (~10 mW/ch).
    - **Continuous Time Binary Valued outputs.**



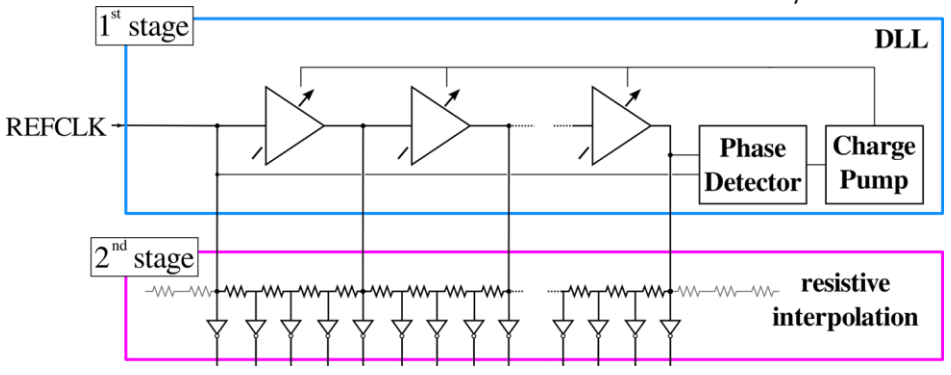
FlexToTv2 ASIC (0.35um BiCMOS)

- Challenge:
  - Time-of-Arrival (ToA) TDC for FlexToT timing signal output.
    - Resolution << FlexToT SPTR → 10 ps < LSB < 20 ps.
    - Very low power consmption (~10 mW/ch, full chip).
    - Jitter & timing resolution ~ 1 LSB.
    - **Technology: 180 nm.**

Motivation

- First TDC design temptative:
  - 4-ch TDC implementation based on state of the art.
    - An adaptation of L. Perktold and J. Christiansen TDC [1].
    - 2 levels of fine TDC (sub-clock):
      - 1st level: tunable buffers ~ 120 ps delay (180 nm technology).
      - 2nd level: resistive interpolation.
    - Number of resistive interpolation stages:
      - 8 stages per buffer: LSB ~ 15 ps.
    - Power consumption: ~18 mW (**schematic** level), ~4.5 mW/ch.
      - Almost half of the power budged spent on this block.
    - Resistive interpolation problems:
      - Require iterative adjust.
      - Mismatch issues.
      - Difficult to scale.

L. Perktold and J. Christiansen, 2013



Motivation

- Design potentially out of specifications:
  - Simulation results at **schematic** level:
    - Post-layout ~ 2X power consumption.
    - 1st level tunable buffers would increase with parasitics.

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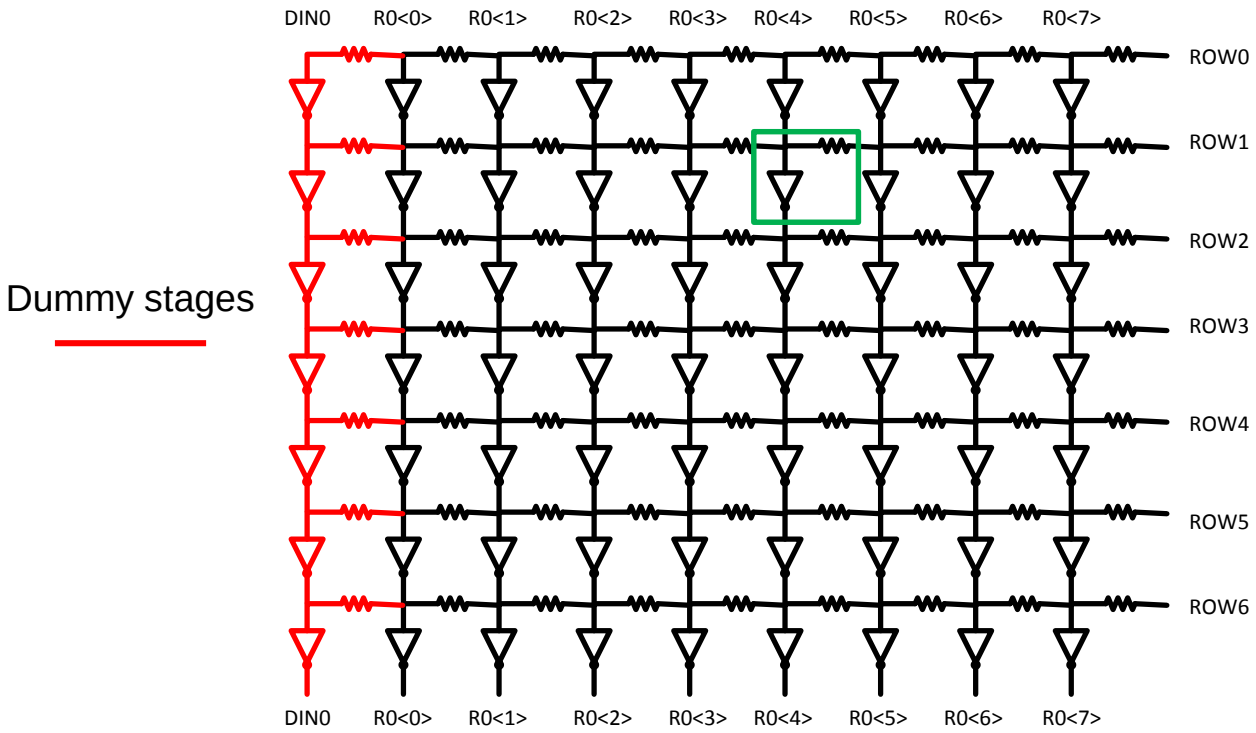
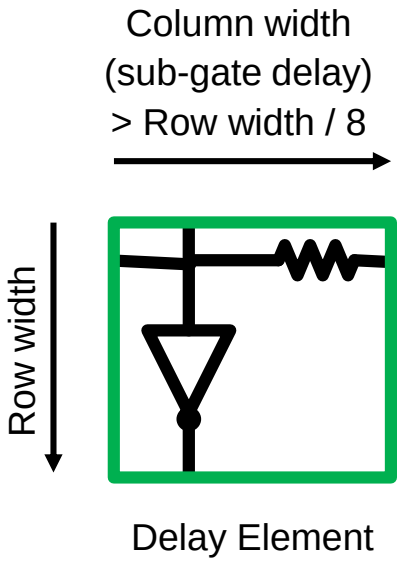
MATRIX TDC Design Overview

- A novel alternative was proposed:
  - Resistive Interpolation Mesh Circuit (RIMC).
    - Patent application EP16382039.2.



RIMC schematic.



MATRIX TDC Design Overview

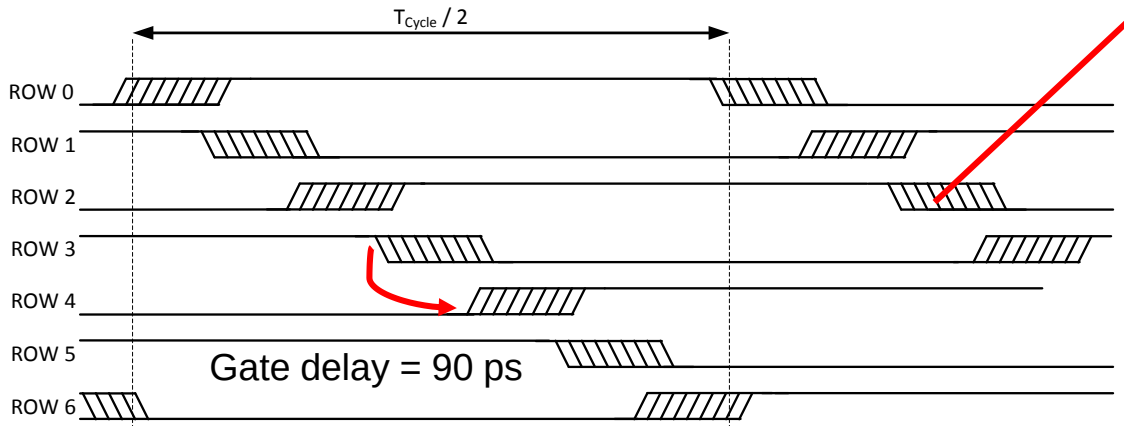
- A novel alternative was proposed:
  - Resistive Interpolation Mesh Circuit (RIMC).
    - Patent application EP16382039.2.

T_{Cycle}= 1250 ps

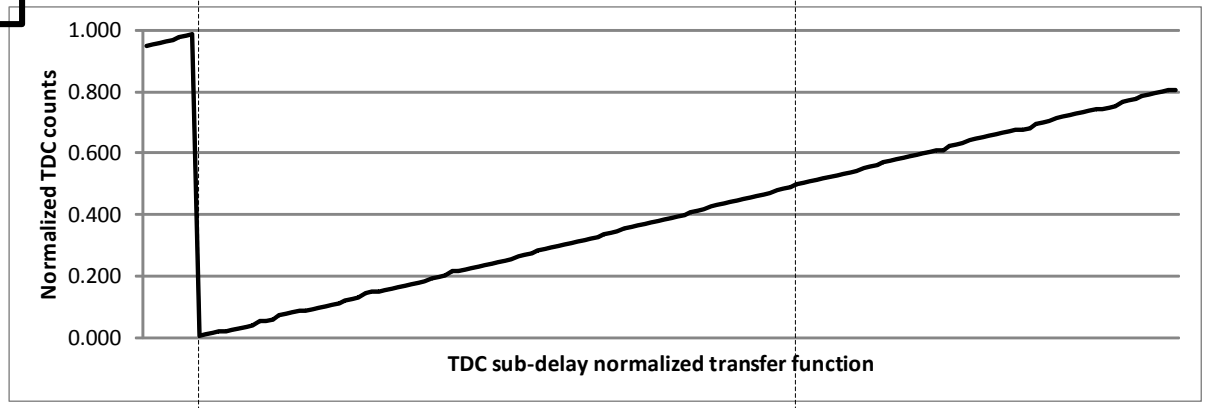
T_{Row} = 90 ps

T_{Col} = 15 ps

Overlap = 33%



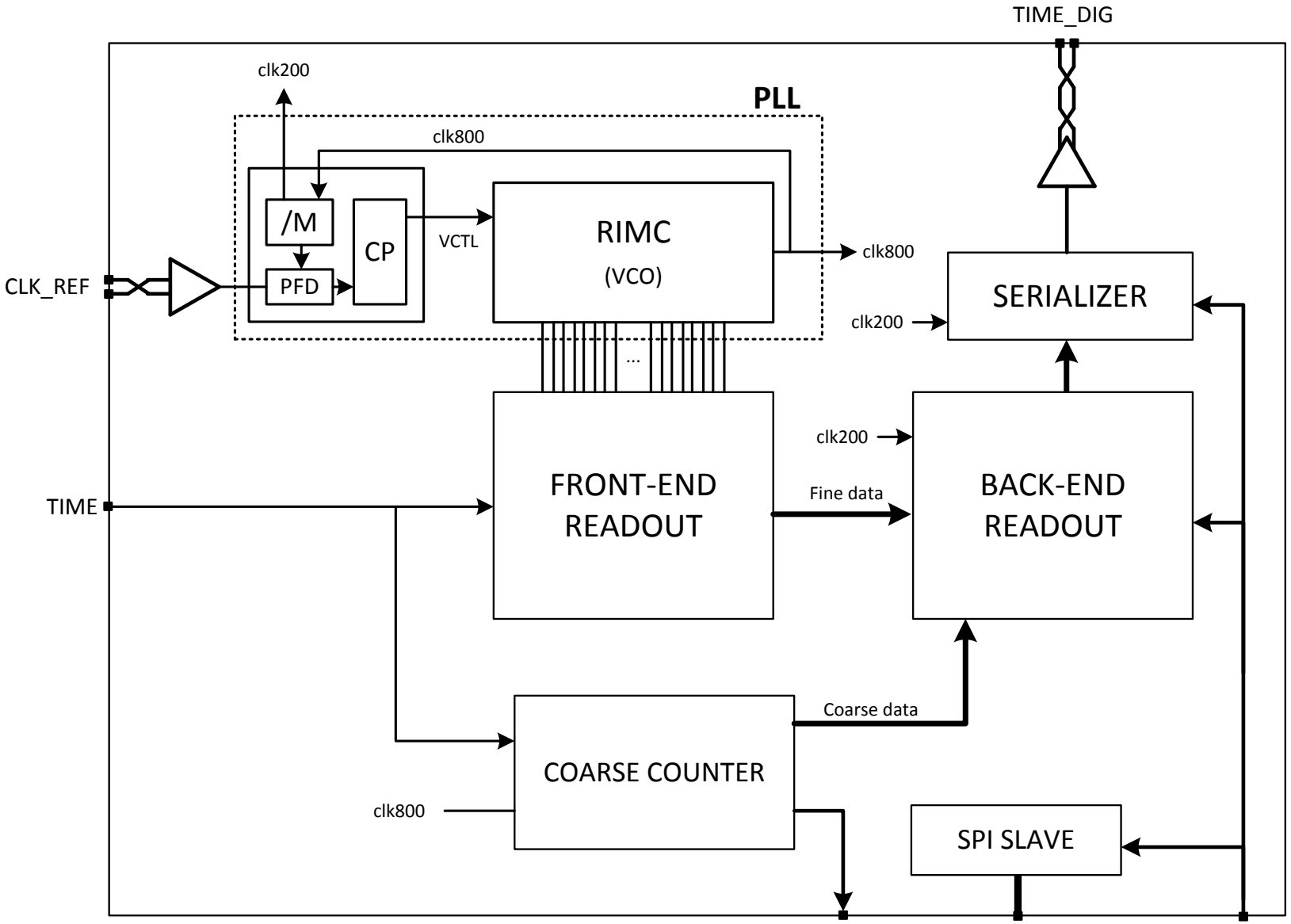
Chronogram of the RIMC clock nodes and normalized ideal transfer function.



MATRIX TDC Design Overview

- Benefits:
  - Reduced power consumption and area:
    - Few components (-50%): sub-delays covers half clock period.
  - Excellent process variability properties:
    - Very regular design (less neighboring effects).
    - Mesh structure averages variability.
  - Scalability and reusability:
    - Few changes on the Delay Element to modify TDC resolution/performance.
  - Very low design time:
    - Simple atomic structure: Delay Element (starved inverter + resistor).
    - The structure is repeated in 2D.
- Drawbacks:
  - Layout issues related to the 2D structure:
    - Track congestion.
    - Track lengths.

MATRIX TDC Design Overview



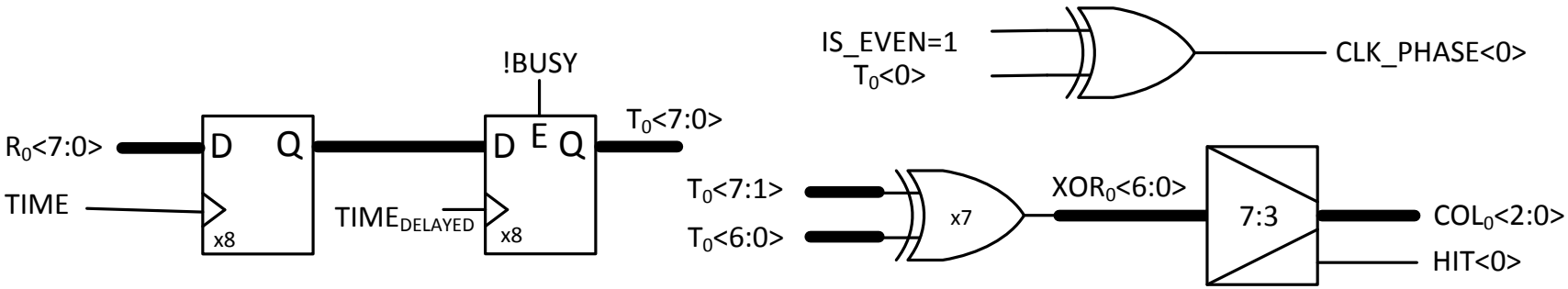
MATRIX TDC Design Overview

- PLL:
  - Supports M = 4 / 8 / 16.
  - PLL Clock Frequency = 800 MHz.
  - The RIMC is the VCO.

- Coarse Counter:
  - 10-Bit natural counter at 800 MHz.
  - Multilevel approach:
    - 2-bit counter at 800 MHz.
    - 8-bit counter at 200 MHz.
    - Clock domain synchronization to avoid metastability issues.
  - Full custom design.

MATRIX TDC Design Overview

- Front-End Readout (Fine Interpolator):
  - 4 channels.
  - Captures the polarity of the RIMC nodes.
  - Encodes the column(s) where transition(s) occurs.
    - It also gathers transition type (rising or falling).



Schematic of Row #0 of the Front-End Readout

- Serializer:
  - Two output types: Single Ended and LVDS.
  - Data rate:
    - 10 MHz sustained rate per channel (200 Mbps).

MATRIX TDC Design Overview

- Back-End Readout:
  - Syncronize Fine Interpolator and Coarse Counter data.
    - Coarse Counter provides a phase bit to align counters.
  - 4-Word per-channel FIFO:
    - TDC dead time = 20 ns.
  - Algorithm:
    - Row: 0~6 (3 bits).
    - Column: 0~7 (3 bits).

    Stage ID = Row * 8 + Column

    - Fine stage comptuation (8 bits, 0~219 LSBs):
      - Two hits (overlapping): Fine Stage ID = $ID_1 + ID_2$
      - One hit (no overlapping): Fine Stage ID = $2 * ID_1$
      - If phase bit is active, Fine Stage ID += 110

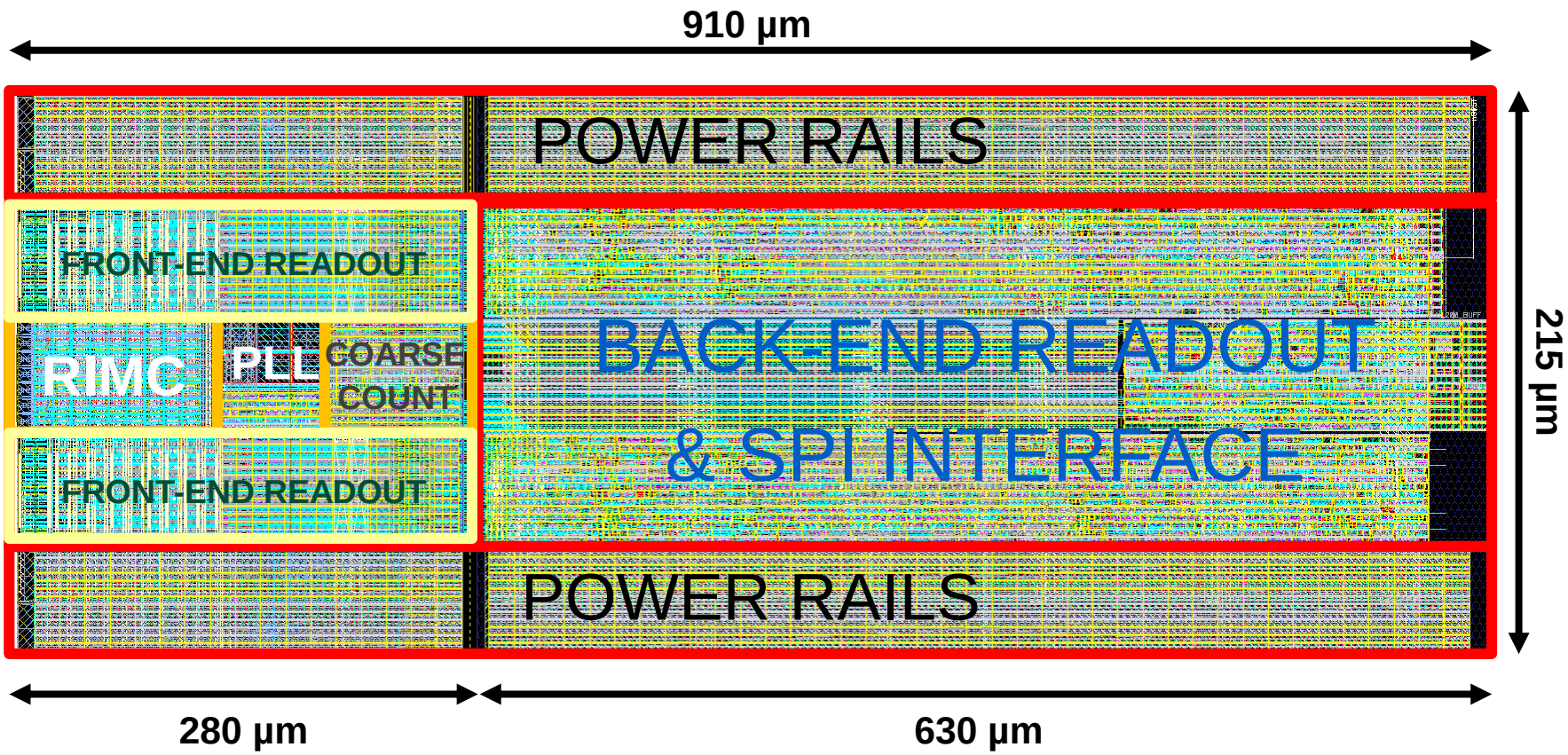
Full Scale = 1250 ps

1250 ps = 220 LSB

1 LSB = 5.68 ps (avg)

MATRIX TDC Design Overview:

- Front-End Readout size: 280x215 um^2.
- Back-End Readout size: 630x215 um^2.



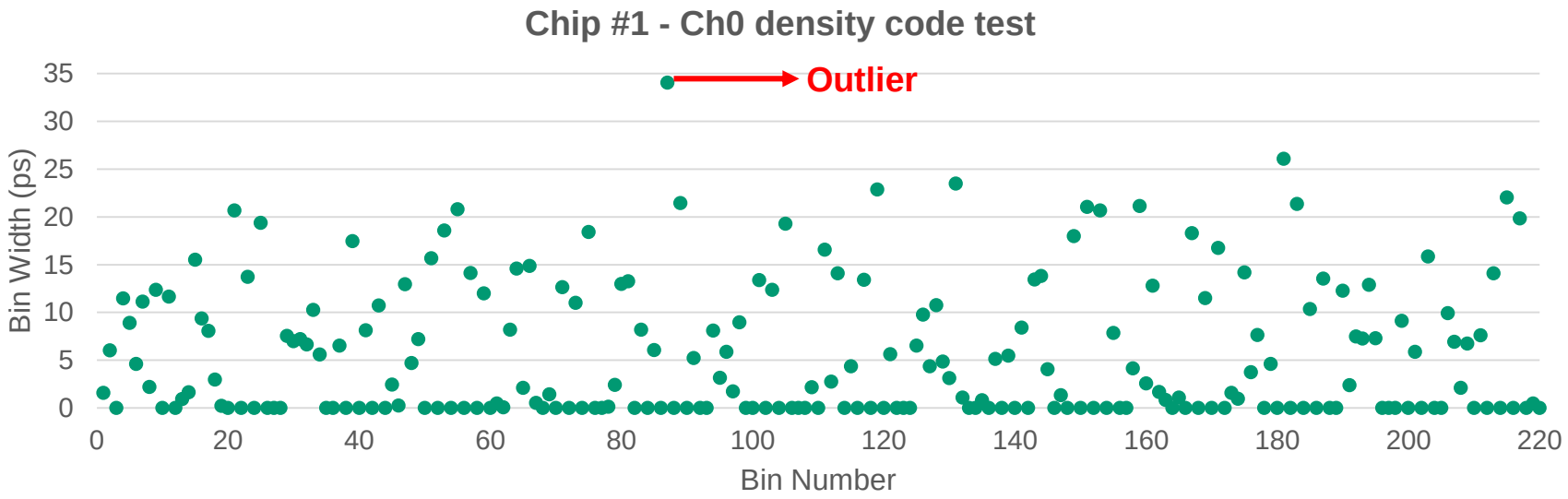
MATRIX TDC core layout.

Outline

- Motivation
- MATRIX TDC Design Overview
- **Measurement Results**
- Conclusions & Future Work

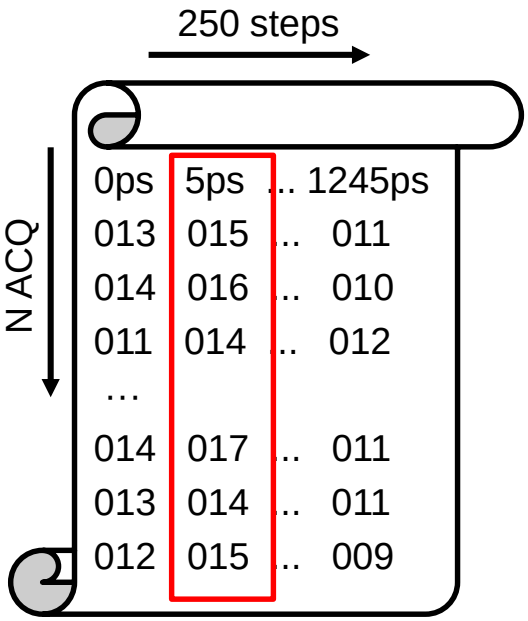
Measurement Results

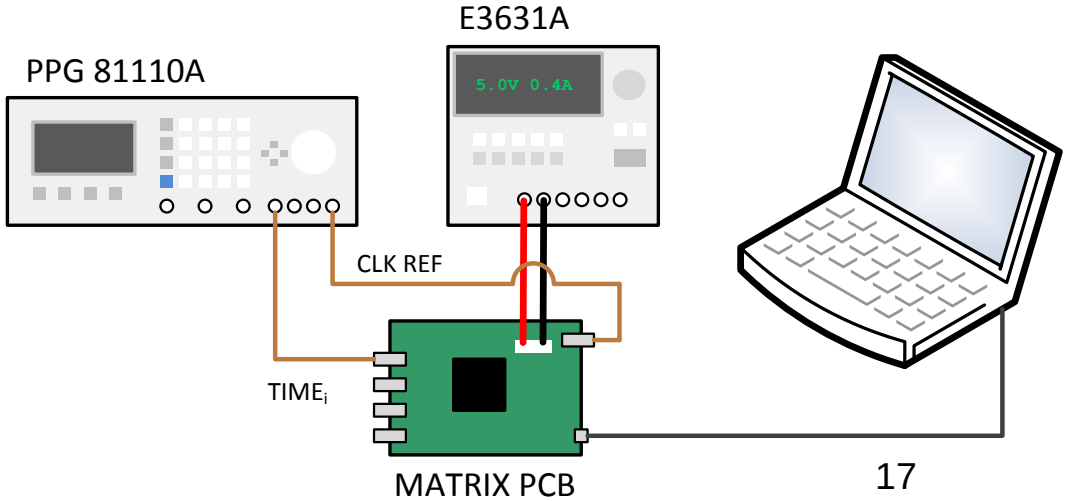
- Chip calibration:
  - Density code test:
    - 100K random pulse shots following an uniform distribution.
    - The number of hits per bin will indicate the bin size.
    - Used to calibrate MATRIX channels.
  - Test results:
    - Almost all the bins in the range between 0 and 25 ps.
    - Uncalibrated σ_{DNL} = 7 ps.



Measurement Results

- Linearity & Jitter test:
  - CLK REF → $TIME_i$ sweep:
    - Start: 0 ps, stop: 1245 ps.
    - Step: 5 ps. #steps = 250.
    - N acquisitions per step.
  - Jitter measurement (single shot precision):
    - **Stdev** of the N ACQ of each step.
  - Linearity measurement:
    - **Average** of the N ACQ of each step.

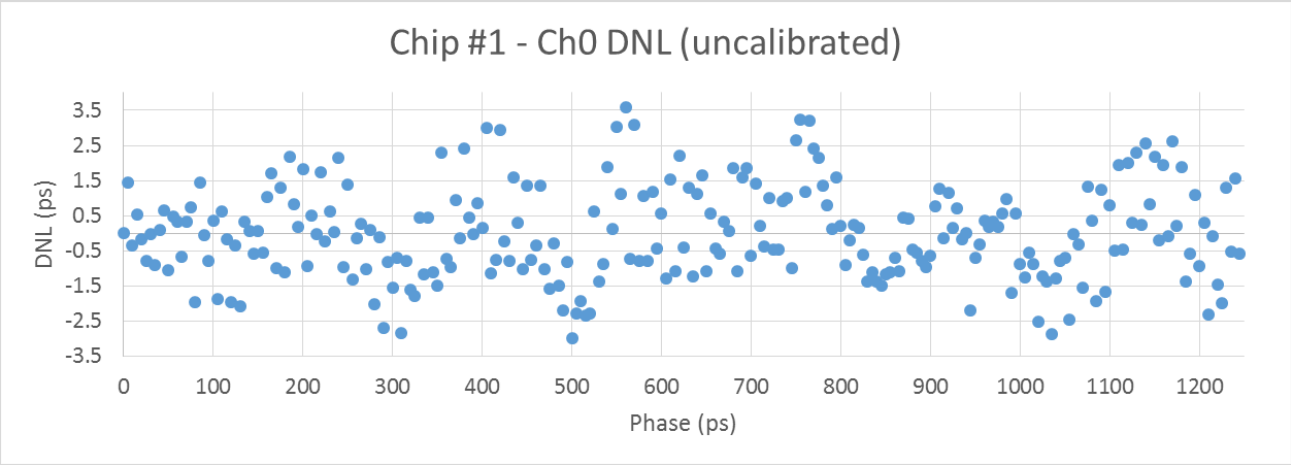




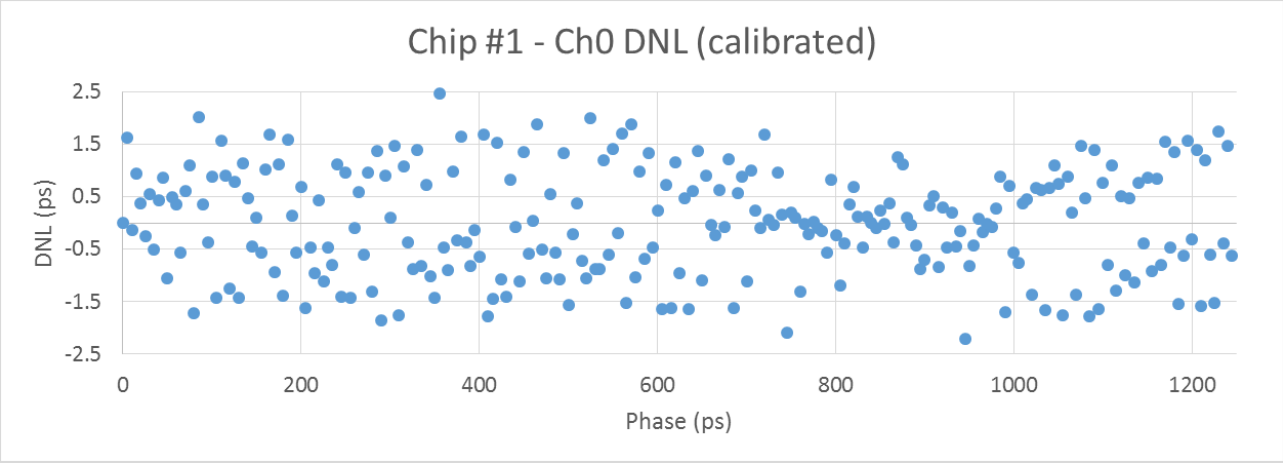
Linearity & Jitter test setup.

Measurement Results

- Linearity - DNL:



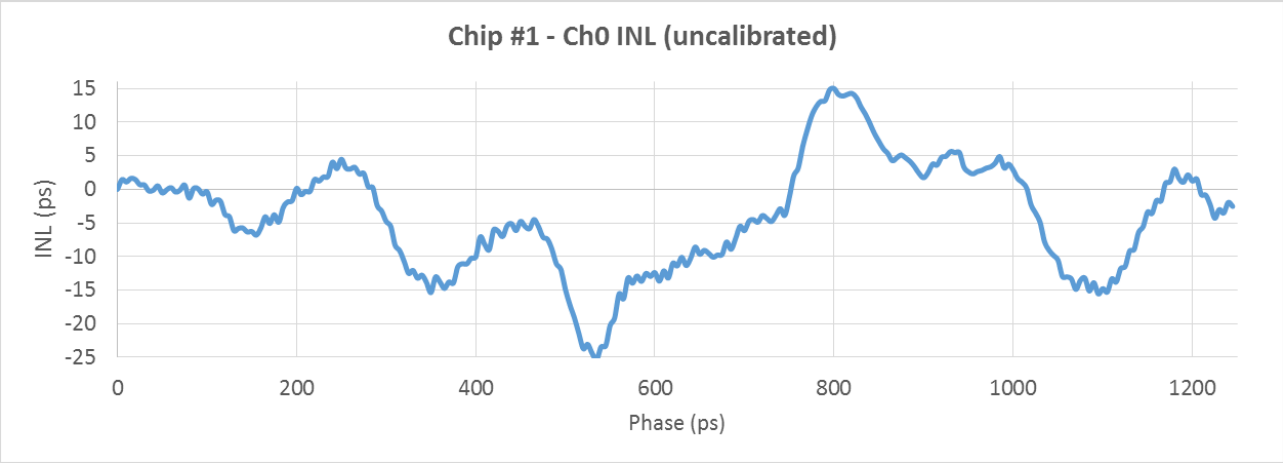
– Uncalibrated:
  - DNL = ± 5.1 ps
  - RMS DNL < 1.4 ps

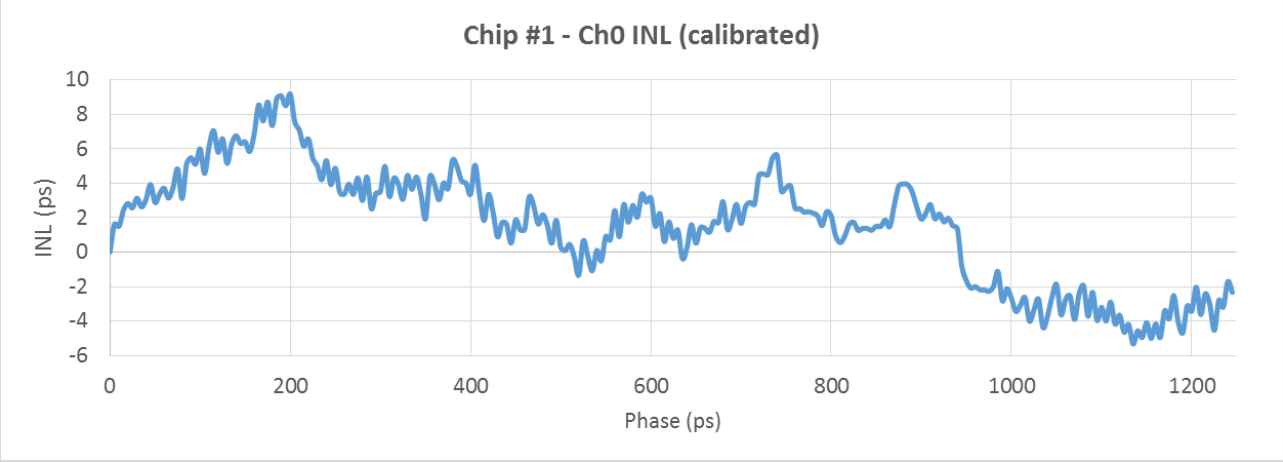


– Calibrated:
  - DNL = ± 4.7 ps
  - RMS DNL < 1.1 ps

Measurement Results

- Linearity - INL:



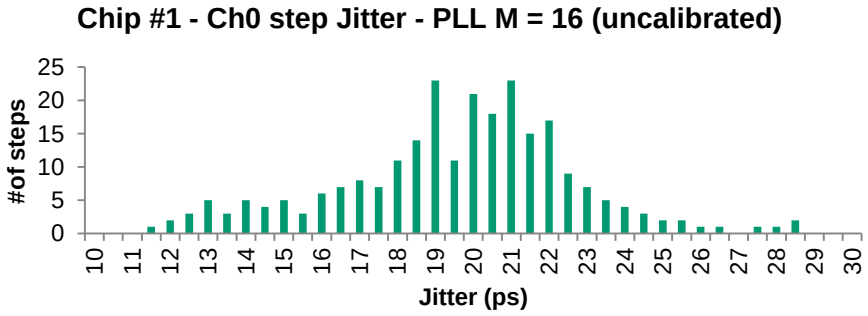


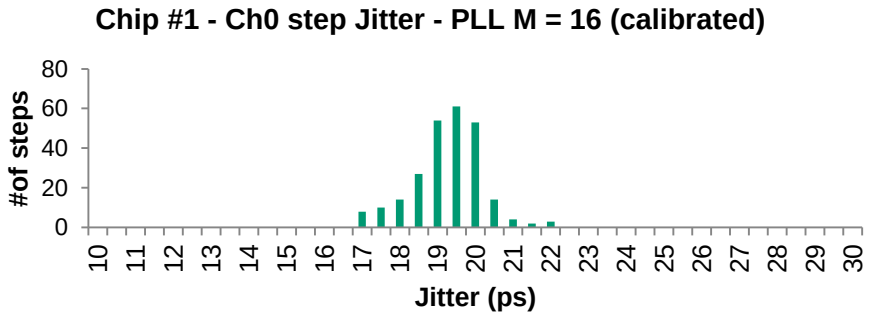
– Uncalibrated:
  - INL = ± 21.9 ps
  - RMS INL < 13.2 ps

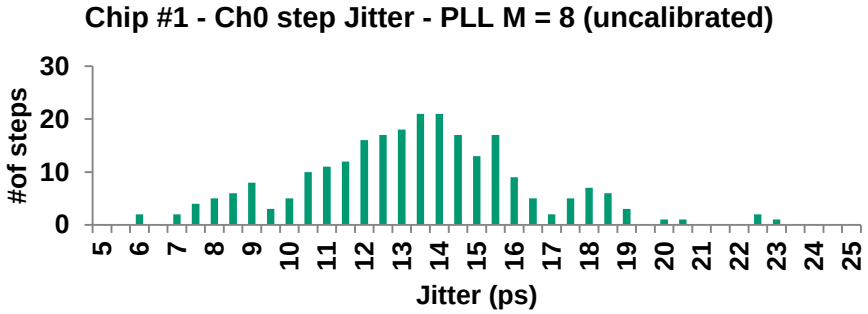
– Calibrated:
  - INL = ± 10.2 ps
  - RMS INL < 3.7 ps

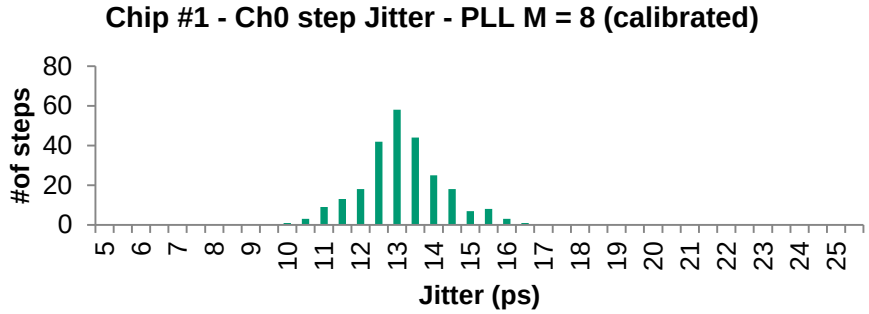
Measurement Results

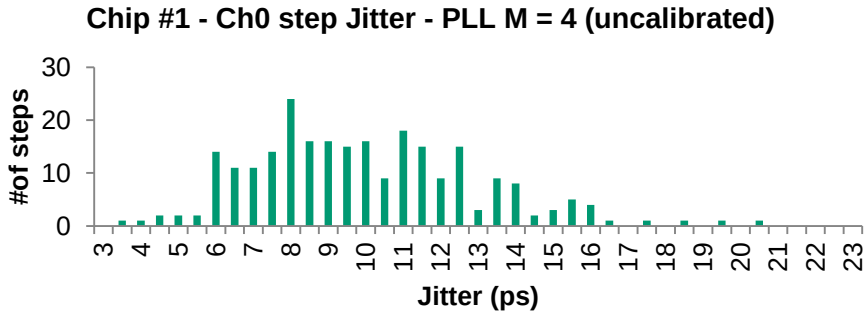
- Jitter (pulse generator + MATRIX TDC):

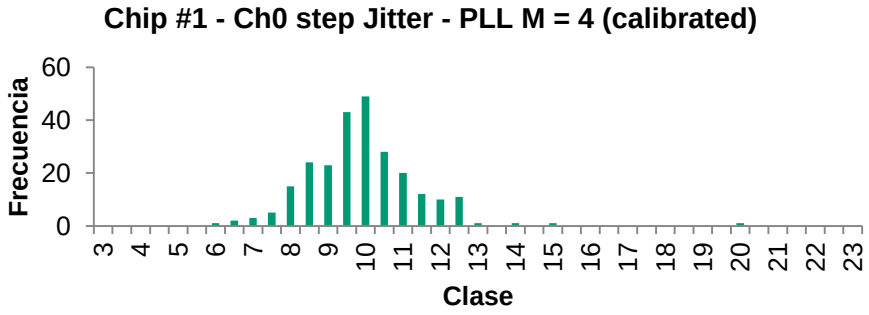












Measurement Results

- Jitter (pulse generator + MATRIX TDC):

PLL M	TDC Jitter (ps)	
	Uncalibrated	Calibrated
4	9.7	9.3
8	12.3	11.7
16	21.2	20.6

  - TDC jitter is dominated by PLL.
    - M = 4 has a natural frequency (ω_n) 2X M = 8 and thus jitter improves.
    - There is margin for the improvement in further MATRIX versions.

$$\omega_n = \sqrt{\frac{K_{VCO} \cdot I_{CP}}{M \cdot C_1}}$$

$K_{VCO} = VCO\ gain\ \left[\frac{Hz}{V}\right]$

$I_{CP} = CP\ current\ [A]$

$M = fb\ divisor$

$C_1 = large\ loop - filter\ \ cap\ [F]$

Measurement Results

- Power Consumption:
  - Measurements are slightly better than simulations.
  - Three operating modes:
    - **Standby**. Reference clock input disabled: **0.76 mW**.
    - **“Standby”**. On-chip PLL still working: **30.1 mW**.
    - **Low Power**. LVDS drivers with minimum differential swing: **45.2 mW**.
    - **Default: 56.3 mW**.

Proposal	Technology	Bin size	Time Res.	Pow/ch
S. Russo et al. (2011) [2]	180 nm	41 ps	14 ps	25 mW
L. Perktold et al. (2014)[1]	130 nm	5 ps	3 ps	43 mW
P. Keränen et al. (2015) [3]	350 nm	-	5 ps	80 mW
MATRIX (2016)	**180 nm**	**15 ps**	**4 ps**	**11.3 mW**

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Conclusions & Future Work

- Conclusions:
  - The new concept was successfully proved.
    - Design, prototype & test.
  - Performance:
    - Similar to other proposals. 4 ps RMS time resolution.
    - Outstanding low power consumption. 11.3 mW/channel.
    - Jitter should be improved. 10 ps for M=4, 20 ps for M=16.
    - We should consider the impact of wide bins (>30 ps) for some applications.
- Future Work:
  - MATRIX V2 with improved jitter.
    - Available in early 2017.
  - SoC PET ASIC (HR-FlexToT):
    - Analog signal processing.
    - MATRIX TDC.
    - Power consumption and cost effectiveness.

References

1. L. Perktold and J. Christiansen, “A multichannel time-to-digital converter ASIC with better than 3 ps RMS time resolution”; 2014 *JINST* **9** C01060

2. S. Russo et al., “A 41 ps ASIC time-to-digital converter for physics experiments” in *Nuclear Instruments and Methods in Physics Research*, Volume 659, Issue 1, p. 422-427.

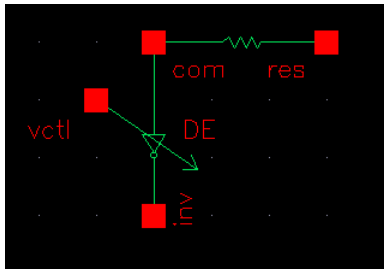
3. P. Keränen and J. Kostamovaara, "A Wide Range, 4.2 ps(rms) Precision CMOS TDC With Cyclic Interpolators Based on Switched-Frequency Ring Oscillators," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 12, pp. 2795-2805, Dec. 2015.

THANK YOU FOR YOUR ATTENTION!

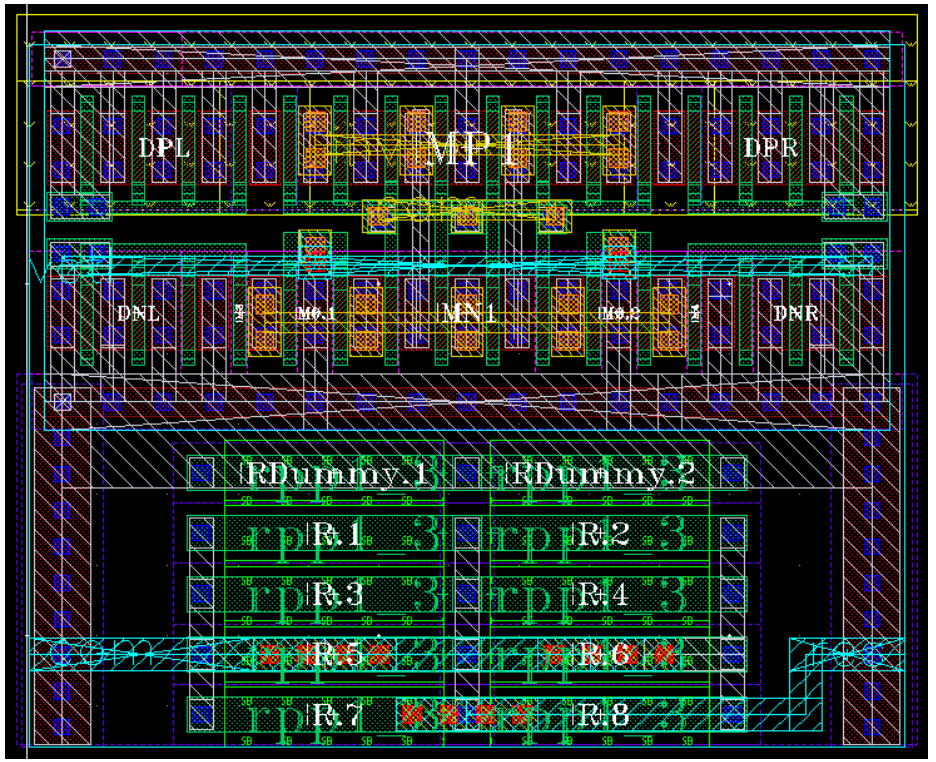
BACKUP SLIDES...

RIMC Layout

- Res. Interp. Mesh Delay Element:
  - Full custom design.
  - Design For Manufacturability (DFM) techniques to minimize systematic process variability:
    - Dummy structures.
    - Symmetric buffer design.
    - 1-D poly with constant pitch.
    - Continuous rectangular diffusions.
    - Dummy resistor.
  - Dummy transistors (DPR, DNR…):
    - More transistors allowed -if necessary-.



Delay Element symbol



Delay Element layout (~10 x 12.5 um^2).

RIMC Layout

- Res. Interp. Mesh Column design:
  - DEs are abutted to improve DFM.
  - DE stages are interleaved to equalize interconnection lengths.
  - The matrix building is as easy as concatenate the column N times.

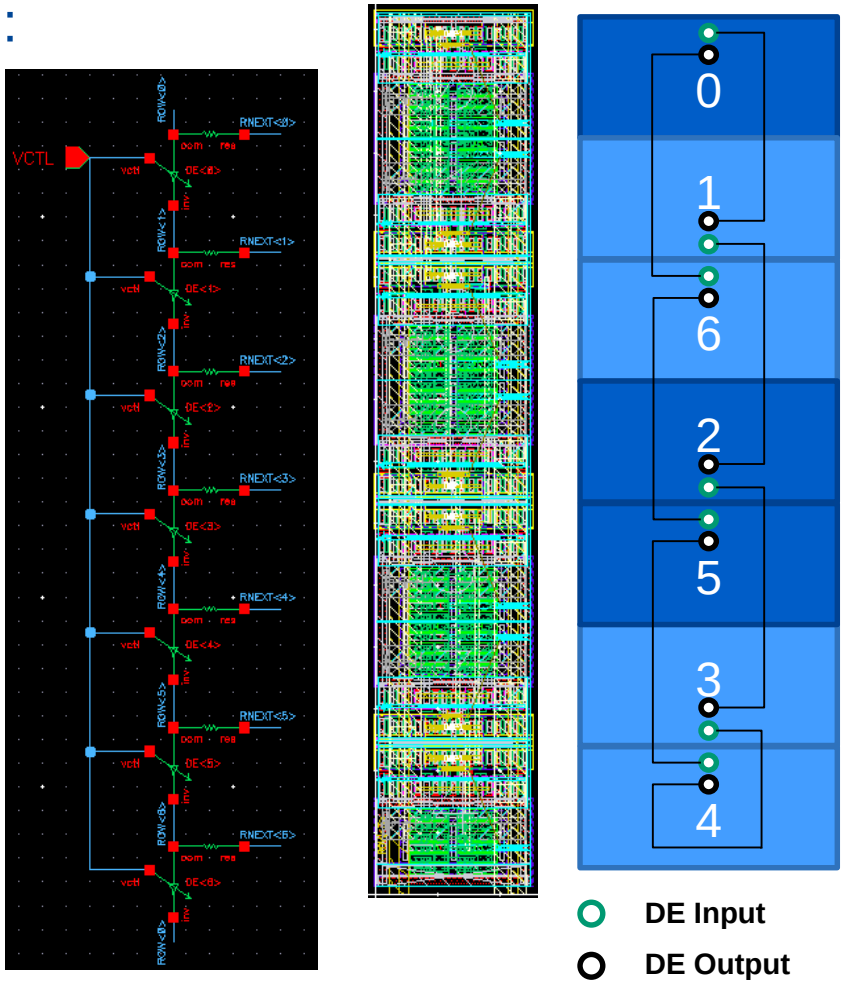
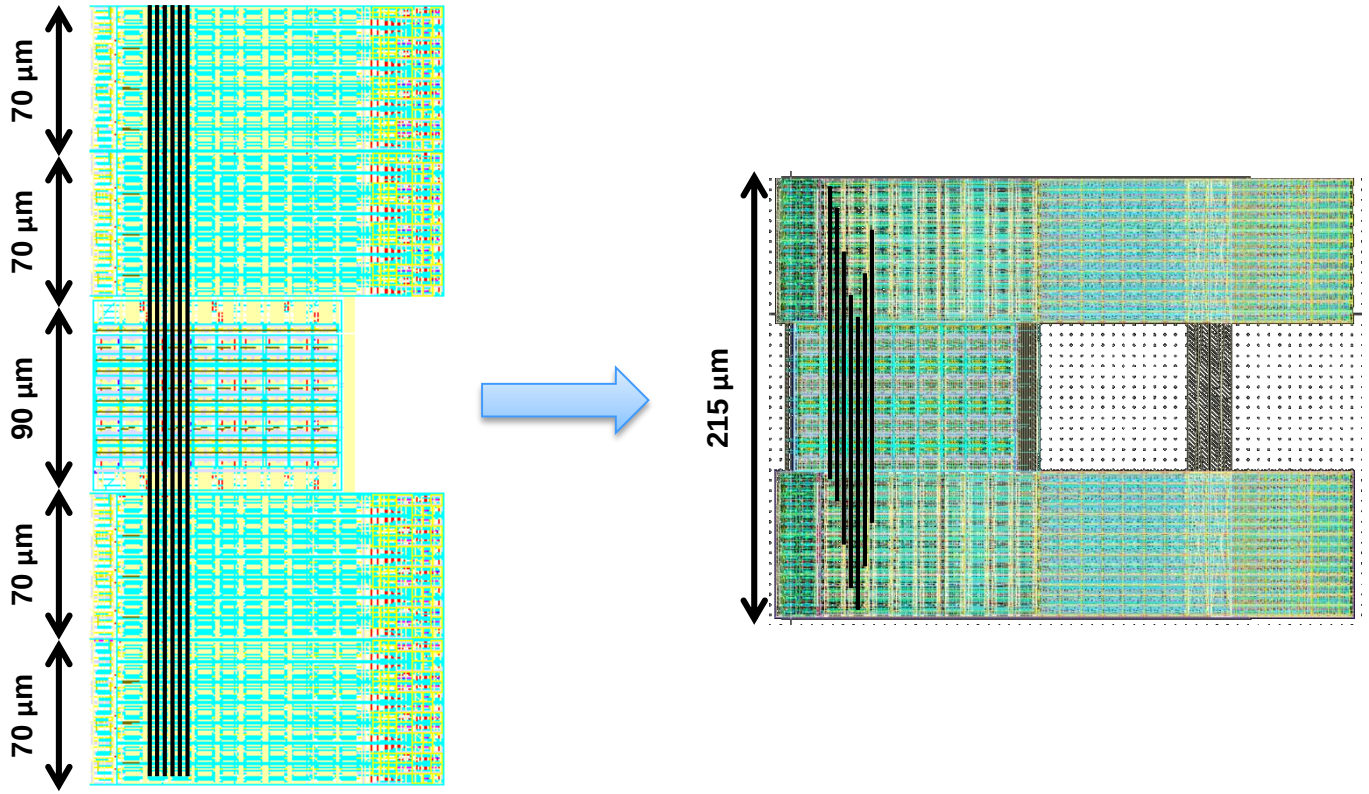


Fig 5: Schematic sample (left) , Layout sample (middle) and layout interconnection diagram (right).

RIMC + TCM Layouts

- Front-end Readout Improvements:
  - Track lengths were optimized.
  - TDC channels were stretched.
  - Dedicated horizontal power rails were removed.
  - Track capacitance decreased by factor 3 as a consequence (75 fF → 25 fF).

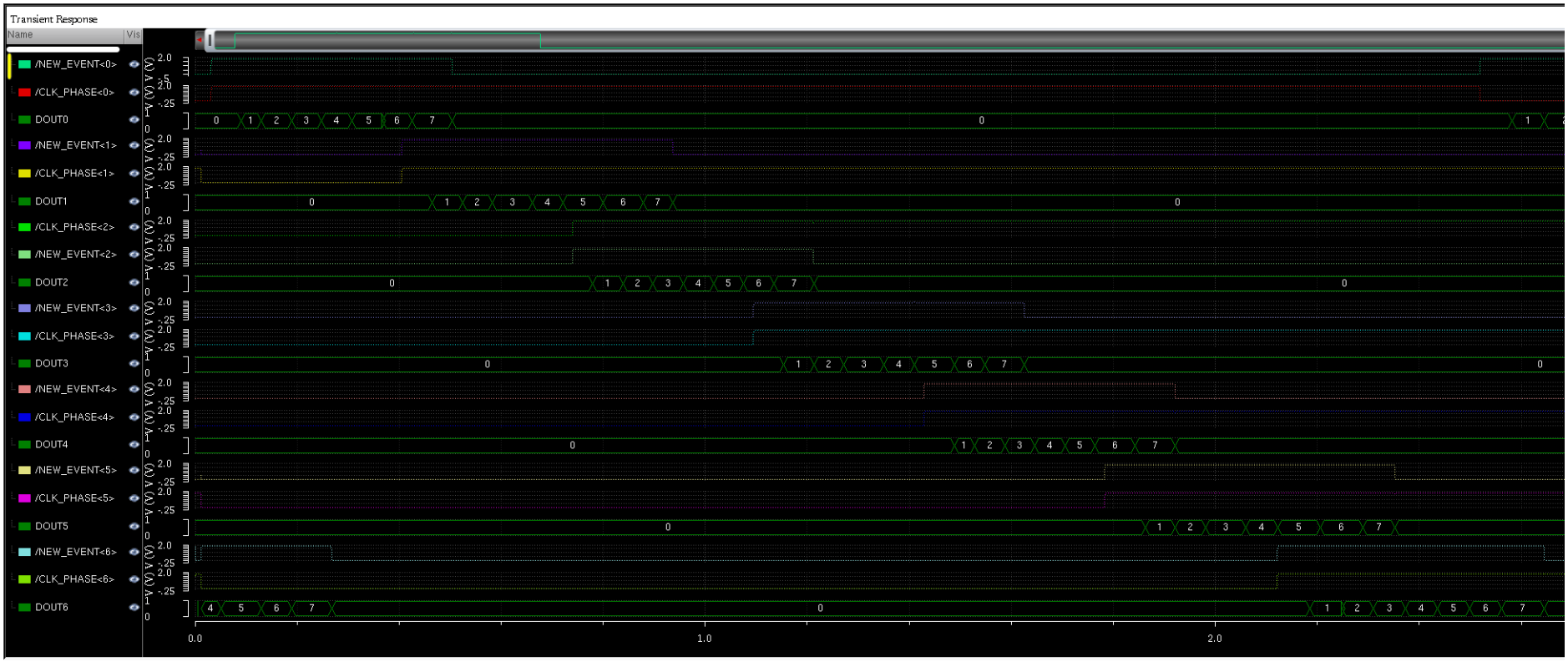


Simulation Results:

- Front-End Readout (fine interpolation) transfer function:
  - Phase between timing signal and clock is swept in steps of 1 ps along the 1.25 ns clock period.
  - For each event, we have:
    - The row(s) number(s) where the transition occurred (*NEW_EVENT<6:0>*).
    - The transition type: rising or falling (*CLK_PHASE<6:0>*).
    - Encoded row data (DOUT0<2:0>, DOUT1<1:0>, … DOUT6<1:0>).

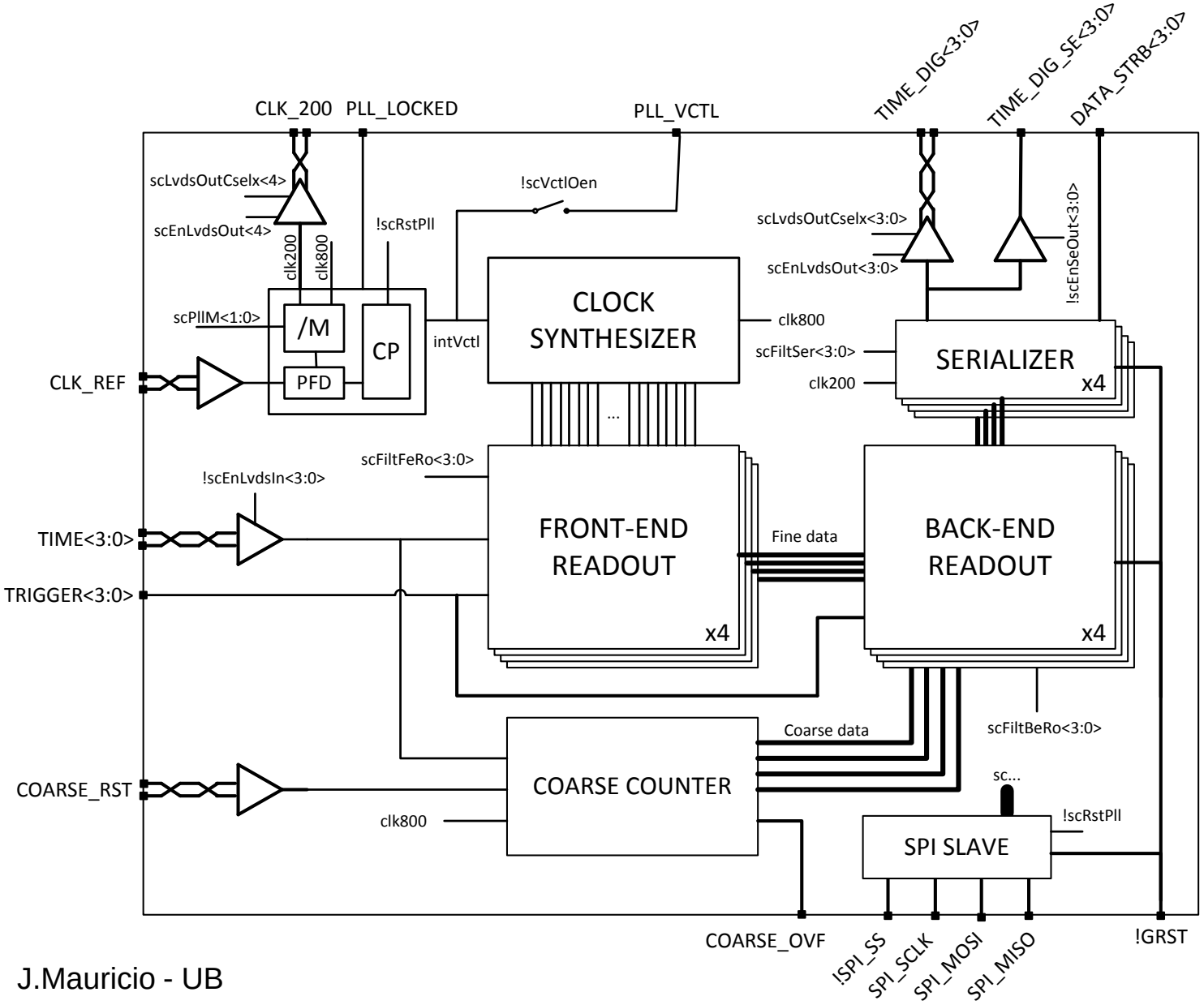
Simulation Results:

- Front-End Readout (fine interpolation) transfer function:



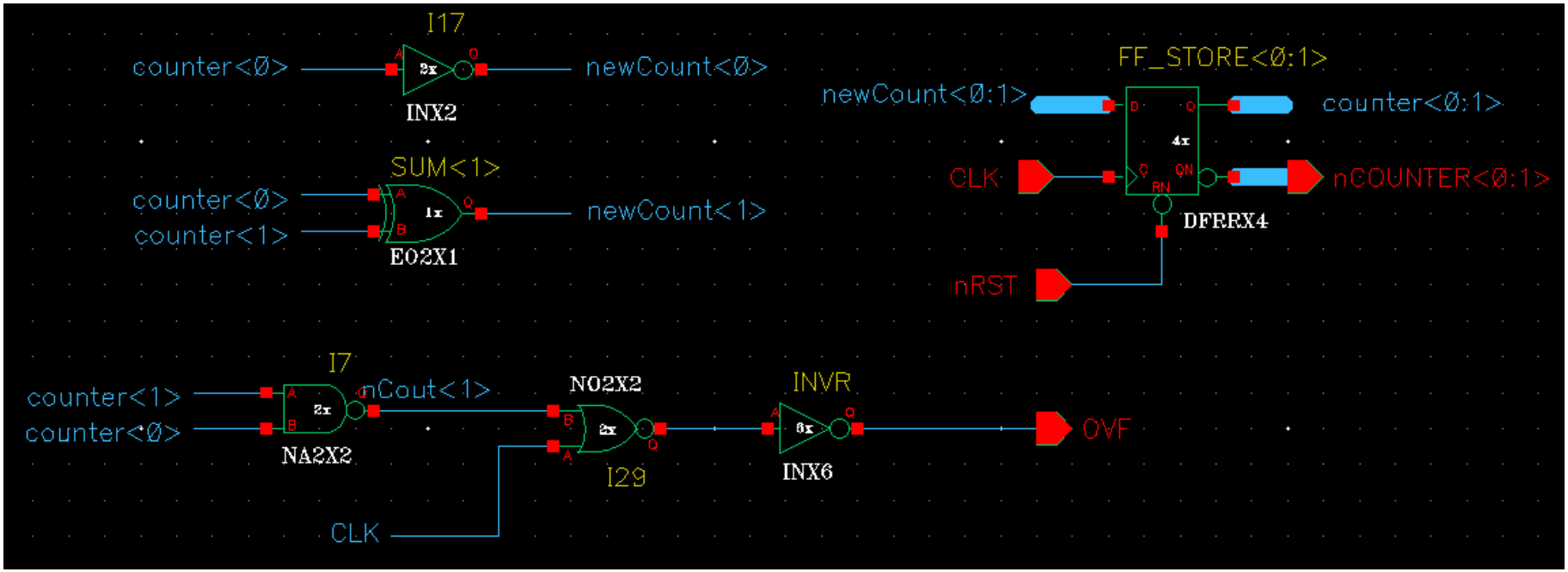
Front-End Readout (fine interpolation) transfer function output.

MATRIX TDC Detailed Block Diagram



Coarse Counter design

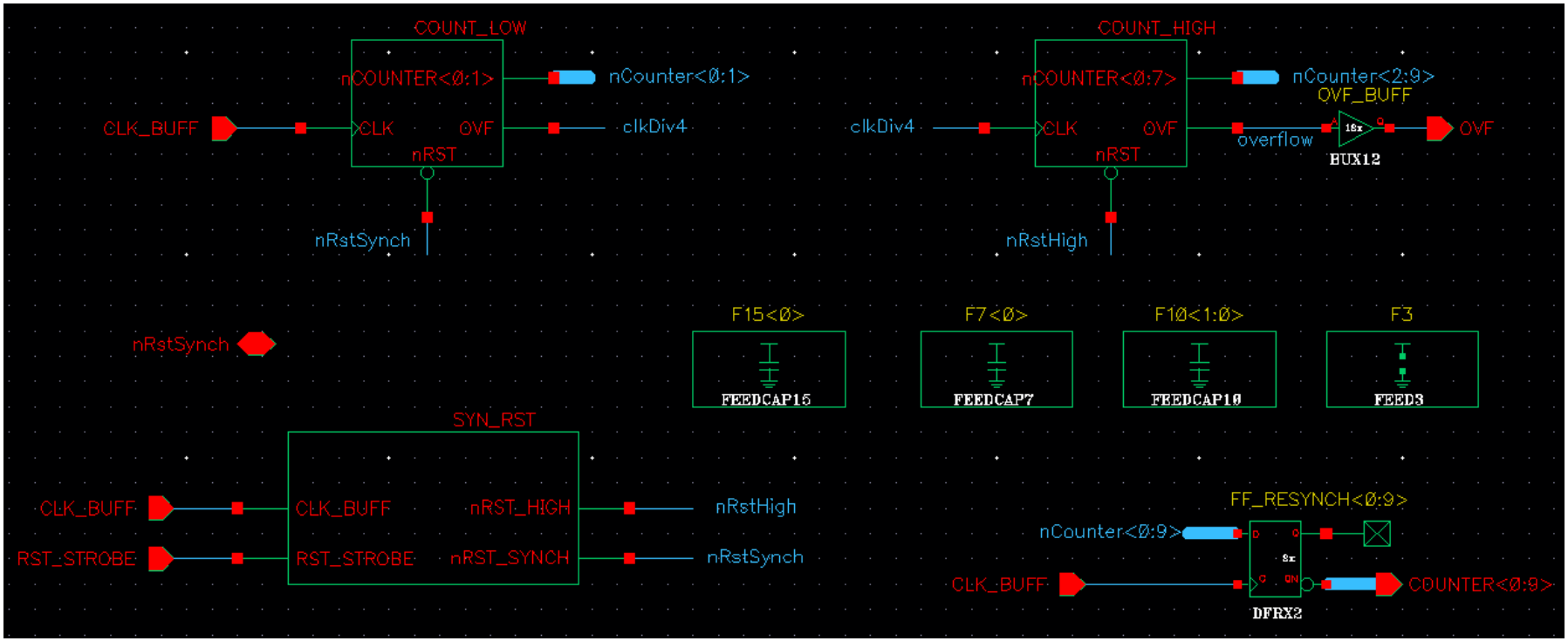
- 2-bit counter features:
  - Maximum parallelism.
  - The worst path is an XOR2.
  - Overflow signal is used to increase the 8-bit counter.



Schematic of the 800 MHz 2-bit counter

Coarse Counter design

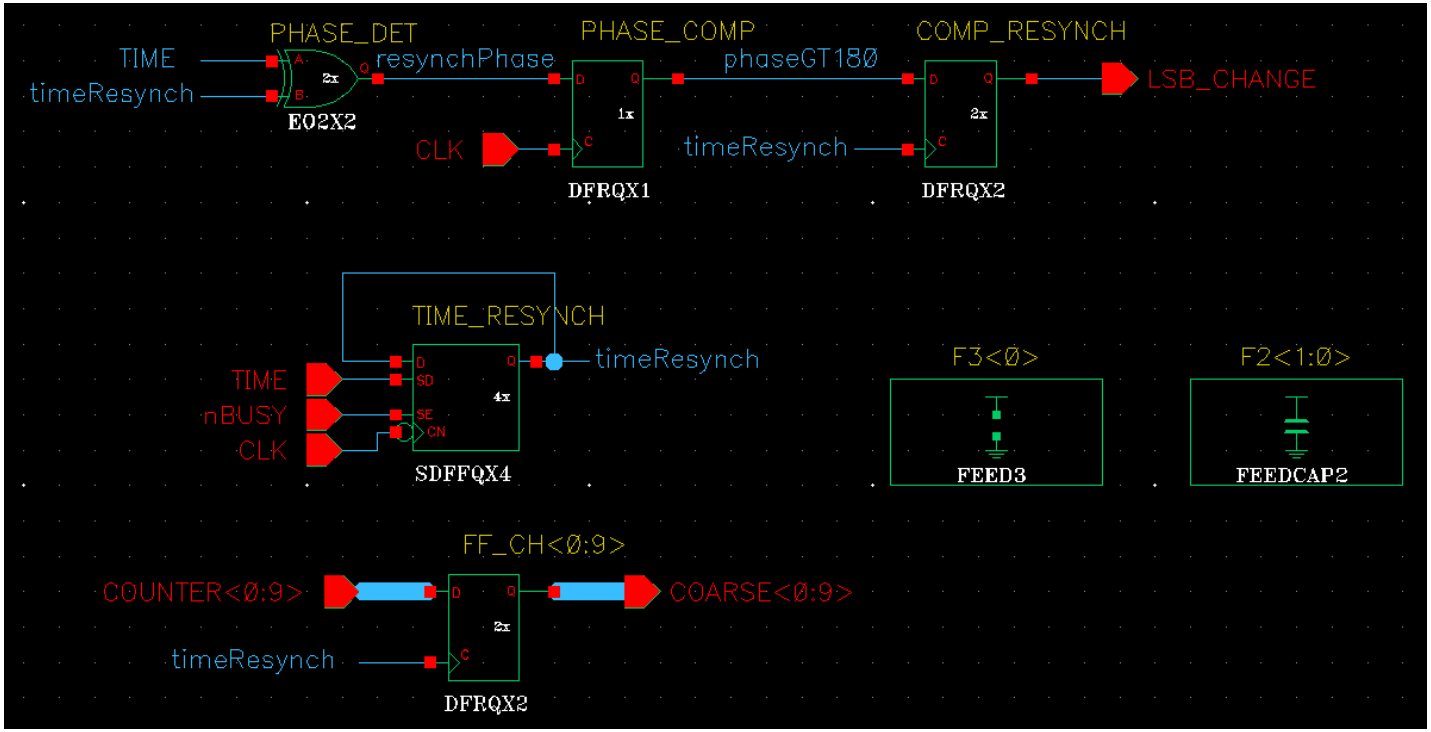
- Coarse counter features:
  - 2-level approach: 2-bit counter @ 800 MHz, 8-bit counter @ 200 MHz.
  - Counter values are resynchronized to avoid metastability issues.
  - Synchronous reset from an external signal.



Schematic of the 800 MHz 10-bit counter

Coarse Counter design

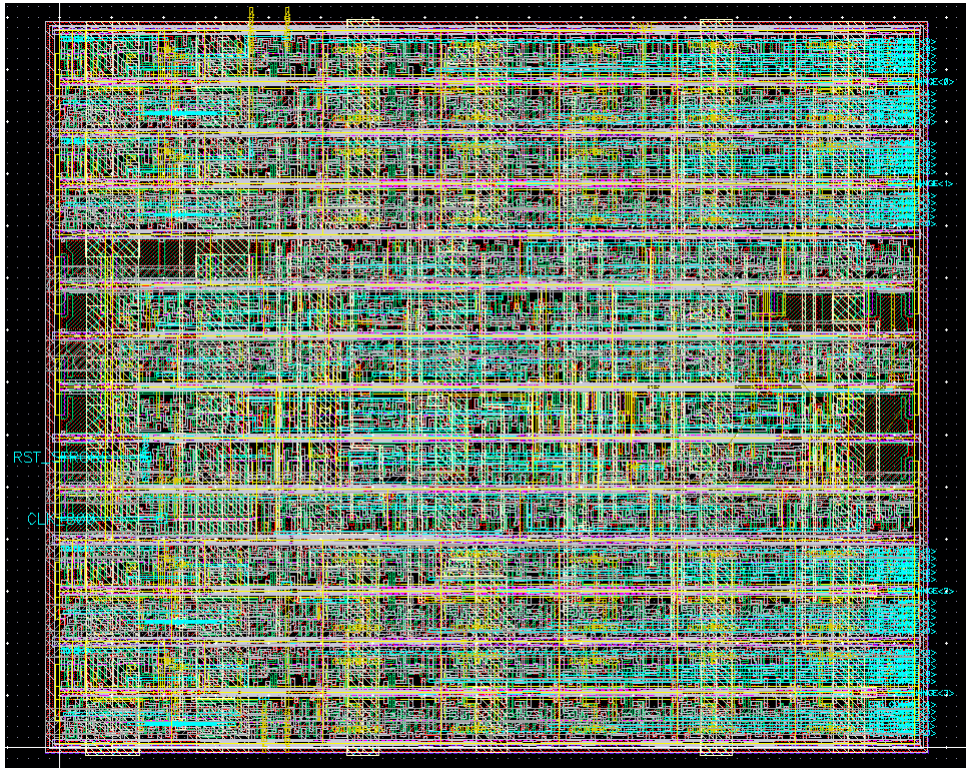
- Coarse counter channel capture features:
  - ToA signal (*TIME*) is discretized (*timeResynch*) at 800 MHz.
  - Discretized signal (synchronous) captures coarse counter safely.
  - *LSB_CHANGE* gives information about the phase (Coarse/Fine alignment).



Schematic of the per-channel Coarse Counter value capture

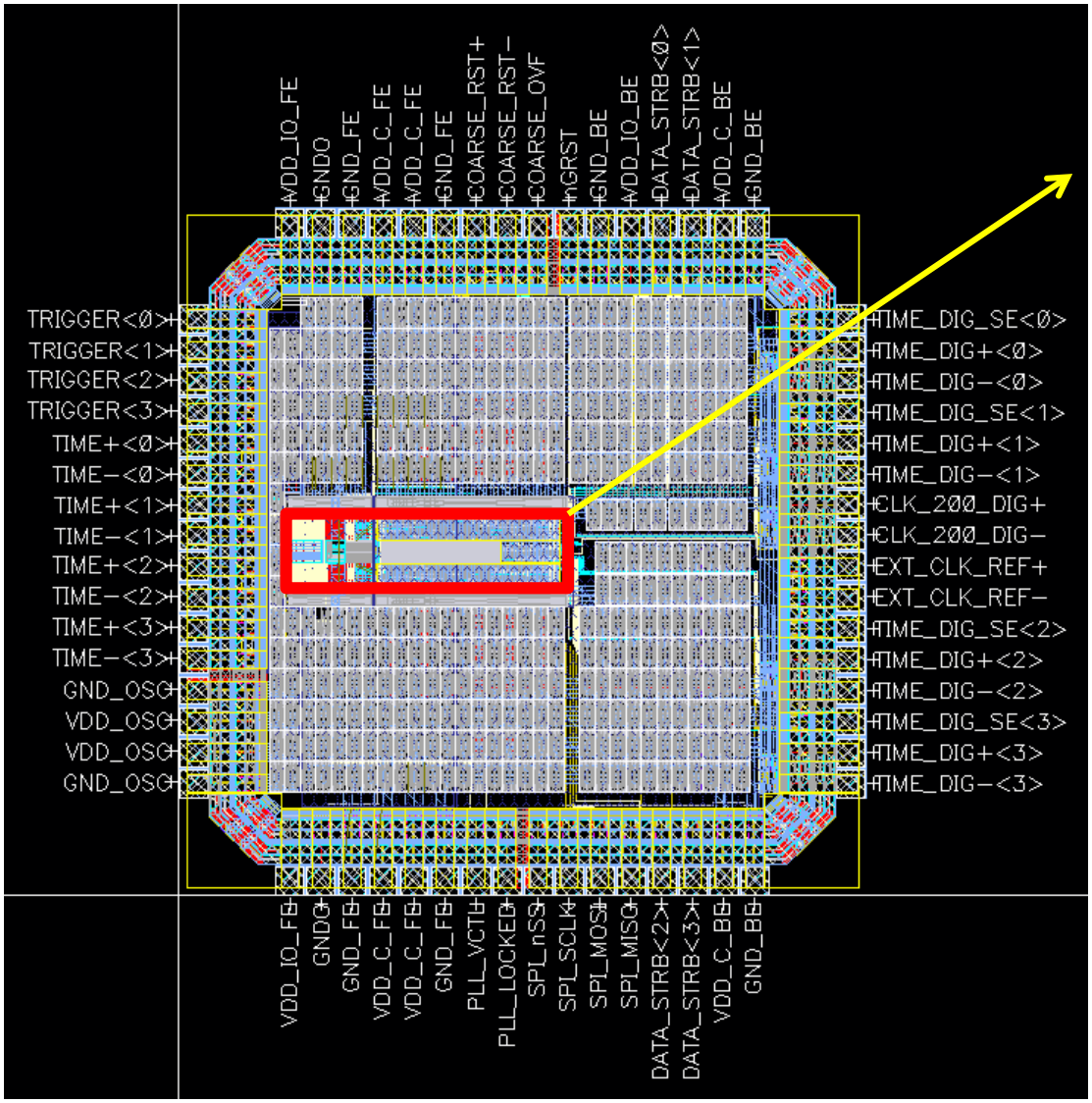
Coarse Counter design

- Coarse counter. Conclusions:
  - Power consumption: ~3 mW.
  - Reliability problems for supply voltages < 1.7 V at high temperatures.



Coarse counter layout (83 x 70 um^2).

MATRIX v1 Picture:



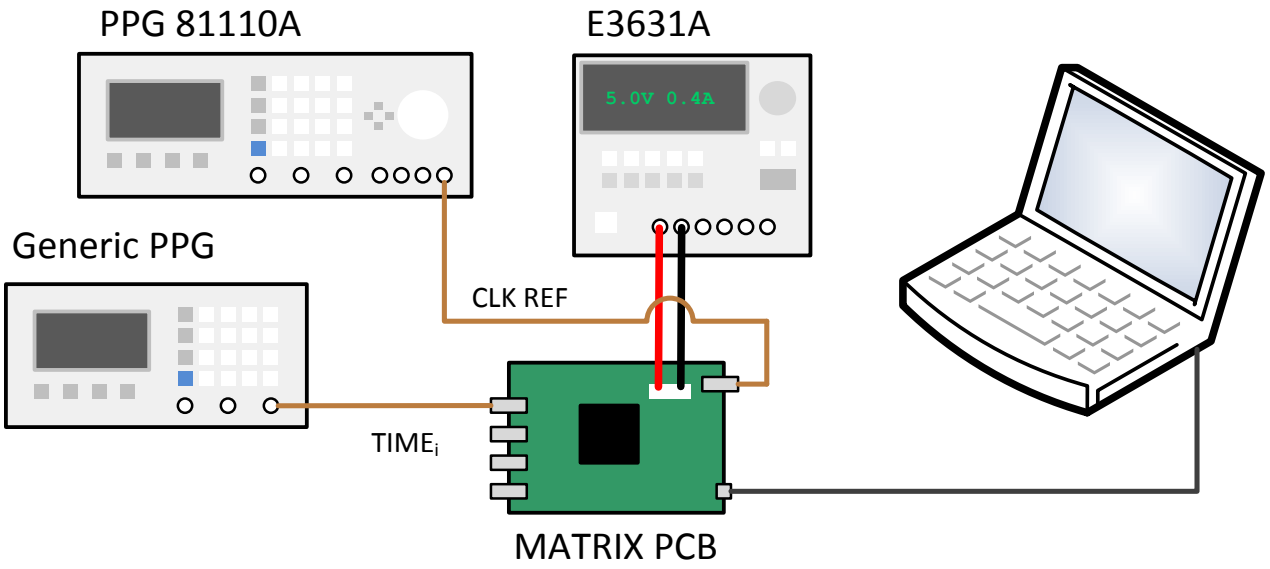
This is the core of the chip.

The rest are capacitors decoupling capacitors.

TDC V1 chip layout. Dimensions: X=2218 um, Y=2221 um.

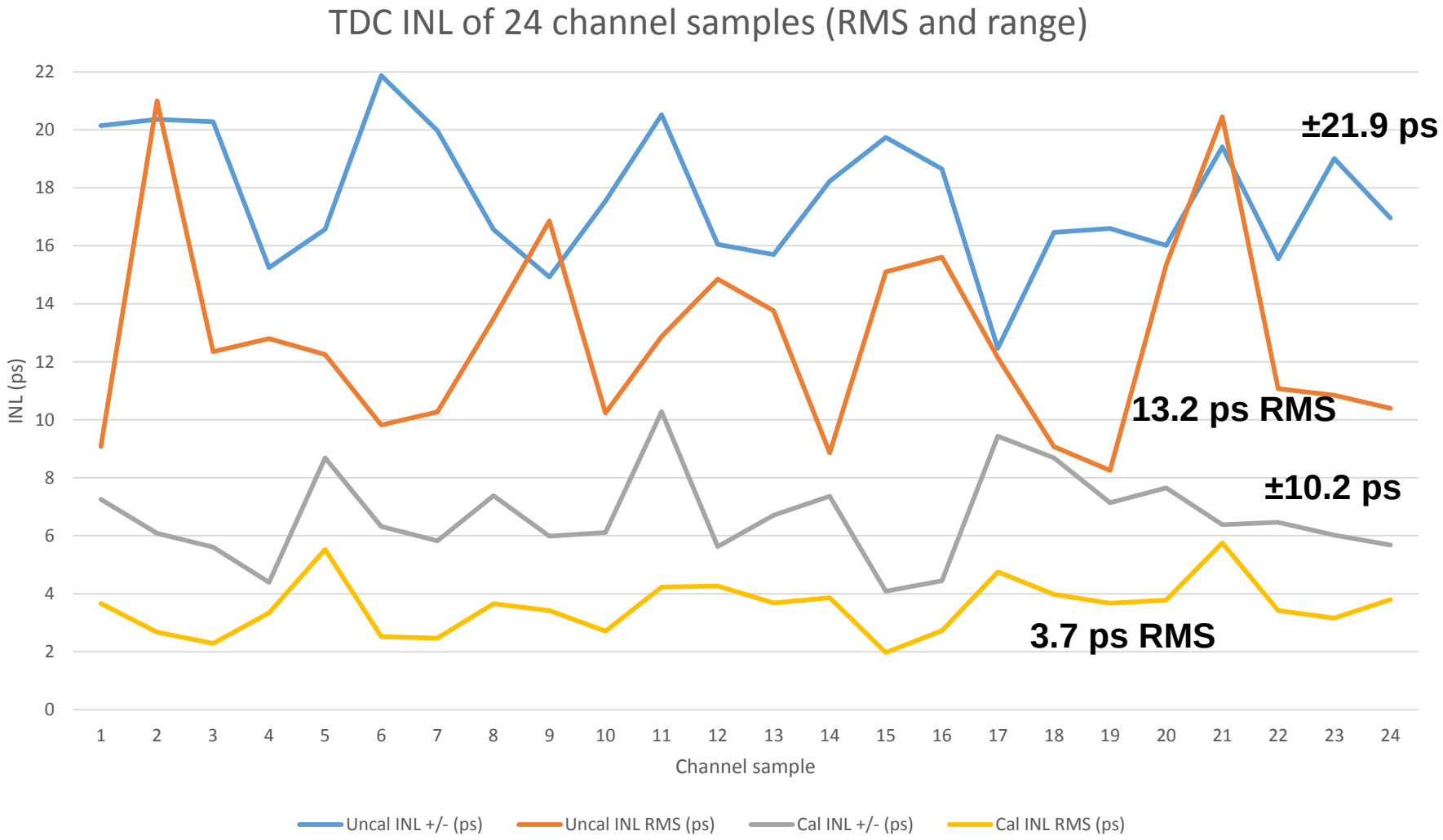
Code Density Test

- How it works?
  - Two uncorrelated pulse generators:
    - One for the CLK reference (50 MHz).
    - The second for uncorrelated timing pulses (12.45 KHz).
    - In theory, all the TDC bins have the same probability to appear.
      - Wider bins indicate linearity issues.



Code density test setup.

TDC INL Statistics



TDC DNL Statistics