MATRIX: a 15 ps resistive interpolation TDC ASIC based on a novel regular structure

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Outline

• Motivation

• MATRIX TDC Design Overview

• Measurement Results

• Conclusions & Future Work
Motivation

• **SiUB PET ASIC ecosystem:**
  – Broad experience in fast-timing ASIC designs.
    - FlexToTv1, FlexToTv2.
    - < 10-ps jitter floor.
    - 100-ps SPTR.
    - < 8% energy resolution.
    - Low power consumption (~10 mW/ch).
    - **Continuous Time Binary Valued outputs.**

• **Challenge:**
  – Time-of-Arrival (ToA) TDC for FlexToT timing signal output.
    - Resolution \(<\) FlexToT SPTR \(\rightarrow\) 10 ps < LSB < 20 ps.
    - Very low power consumption (~10 mW/ch, full chip).
    - Jitter & timing resolution \(~\) 1 LSB.
    - **Technology:** 180 nm.
Motivation

**First TDC design temptative:**
- 4-ch TDC implementation based on state of the art.
  - An adaptation of L. Perktold and J. Christiansen TDC [1].
  - 2 levels of fine TDC (sub-clock):
    - 1st level: tunable buffers ~ 120 ps delay (180 nm technology).
    - 2nd level: resistive interpolation.
  - Number of resistive interpolation stages:
    - 8 stages per buffer: LSB ~ 15 ps.
  - Power consumption: ~18 mW (schematic level), ~4.5 mW/ch.
    - Almost half of the power budgeted spent on this block.
  - Resistive interpolation problems:
    - Require iterative adjust.
    - Mismatch issues.
    - Difficult to scale.

L. Perktold and J. Christiansen, 2013
Motivation

- Design potentially out of specifications:
  - Simulation results at **schematic** level:
    - Post-layout ~ 2X power consumption.
    - 1\textsuperscript{st} level tunable buffers would increase with parasitics.
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MATRIX TDC Design Overview

- A novel alternative was proposed:
  - Resistive Interpolation Mesh Circuit (RIMC).
    - Patent application EP16382039.2.
**MATRIX TDC Design Overview**

- **A novel alternative was proposed:**
  - Resistive Interpolation Mesh Circuit (RIMC).
    - Patent application EP16382039.2.

![Chronogram of the RIMC clock nodes and normalized ideal transfer function.](image)

**Table:**

<table>
<thead>
<tr>
<th>ROW</th>
<th>TDC sub-delay normalized transfer function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td></td>
</tr>
</tbody>
</table>

**Key Parameters:**

- \( T_{Cycle} = 1250 \text{ ps} \)
- \( T_{Row} = 90 \text{ ps} \)
- \( T_{Col} = 15 \text{ ps} \)
- Overlap = 33%

**Diagram Notes:**

- Sub-gate delay = 15 ps
- Gate delay = 90 ps

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MATRIX TDC Design Overview

• **Benefits:**
  
  – Reduced power consumption and area:
    ▪ Few components (-50%): sub-delays covers half clock period.
  
  – Excellent process variability properties:
    ▪ Very regular design (less neighboring effects).
    ▪ Mesh structure averages variability.
  
  – Scalability and reusability:
    ▪ Few changes on the Delay Element to modify TDC resolution/performance.
  
  – Very low design time:
    ▪ Simple atomic structure: Delay Element (starved inverter + resistor).
    ▪ The structure is repeated in 2D.

• **Drawbacks:**
  
  – Layout issues related to the 2D structure:
    ▪ Track congestion.
    ▪ Track lengths.
MATRIX TDC Design Overview

• PLL:
  – Supports $M = 4 / 8 / 16$.
  – PLL Clock Frequency = 800 MHz.
  – The RIMC is the VCO.

• Coarse Counter:
  – 10-Bit natural counter at 800 MHz.
  – Multilevel approach:
    ▪ 2-bit counter at 800 MHz.
    ▪ 8-bit counter at 200 MHz.
    ▪ Clock domain synchronization to avoid metastability issues.
  – Full custom design.
MATRIX TDC Design Overview

- **Front-End Readout (Fine Interpolator):**
  - 4 channels.
  - Captures the polarity of the RIMC nodes.
  - Encodes the column(s) where transition(s) occurs.
    - It also gathers transition type (rising or falling).

- **Serializer:**
  - Two output types: Single Ended and LVDS.
  - Data rate:
    - 10 MHz sustained rate per channel (200 Mbps).

Schematic of Row #0 of the Front-End Readout
MATRIX TDC Design Overview

- **Back-End Readout:**
  - Syncronize Fine Interpolator and Coarse Counter data.
    - Coarse Counter provides a phase bit to align counters.
  - 4-Word per-channel FIFO:
    - TDC dead time = 20 ns.
  - Algorithm:
    - Row: 0~6 (3 bits).
    - Column: 0~7 (3 bits).
    - Stage ID = Row * 8 + Column
    - Fine stage computation (8 bits, 0~219 LSBs):
      - Two hits (overlapping): Fine Stage ID = ID₁ + ID₂
      - One hit (no overlapping): Fine Stage ID = 2 * ID₁
      - If phase bit is active, Fine Stage ID += 110

Full Scale = 1250 ps
1250 ps = 220 LSB
1 LSB = 5.68 ps (avg)
MATRIX TDC Design Overview:

- Front-End Readout size: 280x215 $\mu$m$^2$.
- Back-End Readout size: 630x215 $\mu$m$^2$. 
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Measurement Results

- **Chip calibration:**
  - Density code test:
    - 100K random pulse shots following an uniform distribution.
    - The number of hits per bin will indicate the bin size.
    - Used to calibrate MATRIX channels.
  - Test results:
    - Almost all the bins in the range between 0 and 25 ps.
    - Uncalibrated $\sigma_{DNL} = 7$ ps.

![Chip #1 - Ch0 density code test](chart.png)

Outlier
Measurement Results

- Linearity & Jitter test:
  - CLK REF $\rightarrow$ TIME$_i$ sweep:
    - Start: 0 ps, stop: 1245 ps.
    - Step: 5 ps. #steps = 250.
    - N acquisitions per step.
  - Jitter measurement (single shot precision):
    - Stdev of the N ACQ of each step.
  - Linearity measurement:
    - Average of the N ACQ of each step.

Linearity & Jitter test setup.
Measurement Results

- **Linearity - DNL:**

  - **Uncalibrated:**
    - DNL = ± 5.1 ps
    - RMS DNL < 1.4 ps

  - **Calibrated:**
    - DNL = ± 4.7 ps
    - RMS DNL < 1.1 ps
Measurement Results

- Linearity - INL:

  - Uncalibrated:
    - $\text{INL} = \pm 21.9 \text{ ps}$
    - RMS INL $< 13.2 \text{ ps}$

  - Calibrated:
    - $\text{INL} = \pm 10.2 \text{ ps}$
    - RMS INL $< 3.7 \text{ ps}$
# Measurement Results

- **Jitter (pulse generator + MATRIX TDC):**

<table>
<thead>
<tr>
<th>Chip #1 - Ch0 step Jitter - PLL M = 16 (uncalibrated)</th>
<th>Chip #1 - Ch0 step Jitter - PLL M = 16 (calibrated)</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image1.png" alt="Graph" /></td>
<td><img src="image2.png" alt="Graph" /></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Chip #1 - Ch0 step Jitter - PLL M = 8 (uncalibrated)</th>
<th>Chip #1 - Ch0 step Jitter - PLL M = 8 (calibrated)</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image3.png" alt="Graph" /></td>
<td><img src="image4.png" alt="Graph" /></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Chip #1 - Ch0 step Jitter - PLL M = 4 (uncalibrated)</th>
<th>Chip #1 - Ch0 step Jitter - PLL M = 4 (calibrated)</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image5.png" alt="Graph" /></td>
<td><img src="image6.png" alt="Graph" /></td>
</tr>
</tbody>
</table>

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Measurement Results

- Jitter (pulse generator + MATRIX TDC):

<table>
<thead>
<tr>
<th>PLL M</th>
<th>TDC Jitter (ps)</th>
<th>Uncalibrated</th>
<th>Calibrated</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td></td>
<td>9.7</td>
<td>9.3</td>
</tr>
<tr>
<td>8</td>
<td></td>
<td>12.3</td>
<td>11.7</td>
</tr>
<tr>
<td>16</td>
<td></td>
<td>21.2</td>
<td>20.6</td>
</tr>
</tbody>
</table>

- TDC jitter is dominated by PLL.
  - M = 4 has a natural frequency ($\omega_n$) 2X M = 8 and thus jitter improves.
  - There is margin for the improvement in further MATRIX versions.

\[
\omega_n = \sqrt{\frac{K_{VCO} \cdot I_{CP}}{M \cdot C_1}}
\]

\[K_{VCO} = VCO \text{ gain } \left[ \frac{Hz}{V} \right]\]

\[I_{CP} = CP \text{ current } [A]\]

\[M = fb \text{ divisor}\]

\[C_1 = large \text{ loop – filter } \text{ cap } [F]\]
Measurement Results

- **Power Consumption:**
  - Measurements are slightly better than simulations.
  - Three operating modes:
    - **Standby.** Reference clock input disabled: 0.76 mW.
    - “**Standby**”. On-chip PLL still working: 30.1 mW.
    - **Low Power.** LVDS drivers with minimum differential swing: 45.2 mW.
    - Default: 56.3 mW.

<table>
<thead>
<tr>
<th>Proposal</th>
<th>Technology</th>
<th>Bin size</th>
<th>Time Res.</th>
<th>Pow/ch</th>
</tr>
</thead>
<tbody>
<tr>
<td>S. Russo et al. (2011) [2]</td>
<td>180 nm</td>
<td>41 ps</td>
<td>14 ps</td>
<td>25 mW</td>
</tr>
<tr>
<td>L. Perktold et al. (2014)[1]</td>
<td>130 nm</td>
<td>5 ps</td>
<td>3 ps</td>
<td>43 mW</td>
</tr>
<tr>
<td><strong>MATRIX (2016)</strong></td>
<td>180 nm</td>
<td>15 ps</td>
<td>4 ps</td>
<td>11.3 mW</td>
</tr>
</tbody>
</table>
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Conclusions & Future Work

• **Conclusions:**
  – The new concept was successfully proved.
    ▪ Design, prototype & test.
  – Performance:
    ▪ Similar to other proposals. 4 ps RMS time resolution.
    ▪ Outstanding low power consumption. 11.3 mW/channel.
    ▪ Jitter should be improved. 10 ps for M=4, 20 ps for M=16.
    ▪ We should consider the impact of wide bins (>30 ps) for some applications.

• **Future Work:**
  – MATRIX V2 with improved jitter.
  – SoC PET ASIC (HR-FlexToT):
    ▪ Analog signal processing.
    ▪ MATRIX TDC.
    ▪ Power consumption and cost effectiveness.
References

1. L. Perktold and J. Christiansen, “A multichannel time-to-digital converter ASIC with better than 3 ps RMS time resolution”; 2014 JINST 9 C01060


THANK YOU FOR YOUR ATTENTION!
BACKUP SLIDES...
• **Res. Interp. Mesh Delay Element:**
  
  – Full custom design.
  
  – Design For Manufacturability (DFM) techniques to minimize systematic process variability:
    
    ▪ Dummy structures.
    ▪ Symmetric buffer design.
    ▪ 1-D poly with constant pitch.
    ▪ Continuous rectangular diffusions.
    ▪ Dummy resistor.
  
  – **Dummy transistors (DPR, DNR...):**
    
    ▪ More transistors allowed -if necessary-.
Res. Interp. Mesh Column design:

- DEs are abutted to improve DFM.
- DE stages are interleaved to equalize interconnection lengths.
- The matrix building is as easy as concatenate the column N times.

Fig 5: Schematic sample (left), Layout sample (middle) and layout interconnection diagram (right).
RIMC + TCM Layouts

- **Front-end Readout Improvements:**
  - Track lengths were optimized.
  - TDC channels were stretched.
  - Dedicated horizontal power rails were removed.
  - Track capacitance decreased by factor 3 as a consequence (75 fF $\rightarrow$ 25 fF).

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Simulation Results:

- **Front-End Readout (fine interpolation) transfer function:**
  - Phase between timing signal and clock is swept in steps of 1 ps along the 1.25 ns clock period.
  - For each event, we have:
    - The row(s) number(s) where the transition occurred ($NEW_EVENT<6:0>$).
    - The transition type: rising or falling ($CLK\_PHASE<6:0>$).
    - Encoded row data ($DOUT0<2:0>$, $DOUT1<1:0>$, … $DOUT6<1:0>$).
Simulation Results:

- Front-End Readout (fine interpolation) transfer function:

Front-End Readout (fine interpolation) transfer function output.

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MATRIX TDC Detailed Block Diagram

CLOCK SYNTHESIZER

FRONT-END READOUT

COARSE COUNTER

BACK-END READOUT

SERIALIZER x4

SERIALIZER x4

COARSE_OVF

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• **2-bit counter features:**
  
  – Maximum parallelism.
  
  – The worst path is an XOR2.
  
  – Overflow signal is used to increase the 8-bit counter.
Coarse Counter design

- Coarse counter features:
  - 2-level approach: 2-bit counter @ 800 MHz, 8-bit counter @ 200 MHz.
  - Counter values are resynchronized to avoid metastability issues.
  - Synchronous reset from an external signal.

Schematic of the 800 MHz 10-bit counter
Coarse Counter design

- Coarse counter channel capture features:
  - ToA signal (TIME) is discretized (timeResynch) at 800 MHz.
  - Discretized signal (synchronous) captures coarse counter safely.
  - *LSB_CHANGE* gives information about the phase (Coarse/Fine alignment).
Coarse Counter design

- Coarse counter. Conclusions:
  - Power consumption: ~3 mW.
  - Reliability problems for supply voltages < 1.7 V at high temperatures.
This is the core of the chip.

The rest are capacitors decoupling capacitors.

TDC V1 chip layout. Dimensions: X=2218 um, Y=2221 um.
Code Density Test

• How it works?
  – Two uncorrelated pulse generators:
    ▪ One for the CLK reference (50 MHz).
    ▪ The second for uncorrelated timing pulses (12.45 KHz).
    ▪ In theory, all the TDC bins have the same probability to appear.
      ◦ Wider bins indicate linearity issues.
TDC INL Statistics

TDC INL of 24 channel samples (RMS and range)

Uncal INL +/- (ps)
Uncal INL RMS (ps)
Cal INL +/- (ps)
Cal INL RMS (ps)

3.7 ps RMS
±10.2 ps
13.2 ps RMS
±21.9 ps
TDC DNL Statistics

TDC DNL of 24 channel samples (RMS and range)

DNL (ps)

±5.1 ps

±4.7 ps

1.4 ps RMS

1.1 ps RMS

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