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MATRIX: a 15 ps resistive interpolation TDC ASIC based on a novel regular structure

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This paper presents a 4-chanel TDC chip demonstrator with the following features: 15-ps resolution, 1280 ns dynamic range, dead time < 20 ns, up to 10 MHz of sustained input rate per channel, around 60 mW of power consumption and very low area in a 180 nm technology. The main contribution of this work is the novel design of the clock interpolation circuitry which is based on a resistive interpolation mesh circuit (patented) a two-dimensional regular structure with outstanding performance in terms of power consumption, area and low process variability.

Summary

This paper presents a 4-chanel TDC chip demonstrator with the following features: 15-ps resolution, 1280 ns dynamic range, dead time < 20 ns, up to 10 MHz of sustained input rate per channel, around 60 mW of power consumption and very low area (910x215 µm2) in a 180 nm technology.
The main contribution of this work is the novel design of the clock interpolation circuitry based on a resistive interpolation mesh circuit (RIMC). The RIMC (see picture attached) is a matrix where the timing difference between columns (sub-delay) is determined by the resistor value and the parasitic capacitance of the node, while the delay between rows is determined by the drive strength of the inverter. End-to-end delay between the first and the last node for a given row is higher than the inverter delay, and thus at least one clock transition occurs (either rising or falling) within 15 picosecond period.
This novel architecture has many advantages in terms of design time, scalability, reusability, power consumption, area and process variability issues. The atomic circuit of this repetitive structure is just a current starved inverter (3 transistors) and a resistor, which speeds up design time. The number of rows of the RIMC determines the dynamic range and thus the oscillation frequency of the mesh (800 MHz for this design), while resistor value together with the number of columns may determine TDC resolution (15 ps). This allows high reusability of previous designs and scalability. The use of starved inverters as delay elements makes this solution very efficient in terms of power consumption and area. Moreover, the RIMC is used as a voltage-controlled oscillator (VCO) for the PLL, leading to an extra chip area reduction. Lastly, this circuit presents excellent properties in terms of process variability since the mesh structure averages delay variations that may occur due to mismatch in transistors and resistors.
Apart from the RIMC the TDC comprises four time capture matrices (TCM) that store RIMC clock phases (fine timestamp) when a rising edge is produced at any of the inputs of the TDC. Captured data is encoded, buffered and transmitted via a serial interface when an event occurs. Since the acquisition dead time is less than 20 ns, the peak event rate that this chip can process is 50 MHz, while the sustained rate is 10 MHz per channel.
Dynamic range is extended by means of a 10-bit coarse counter which counts the number of complete clock periods at 800 MHz (coarse timestamp), and thus extending dynamic range up to 1280 ns. A fine synchronization circuitry is provided to allow coincidence measurements between different chips. The internal 800 MHz clock is synthesized by means of a PLL with configurable input clocks (50 / 100 / 200 MHz).
Chip prototype was submitted on February 2016 and encapsulated prototype samples of MATRIX are expected by June 2016.

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