Alpide DTU

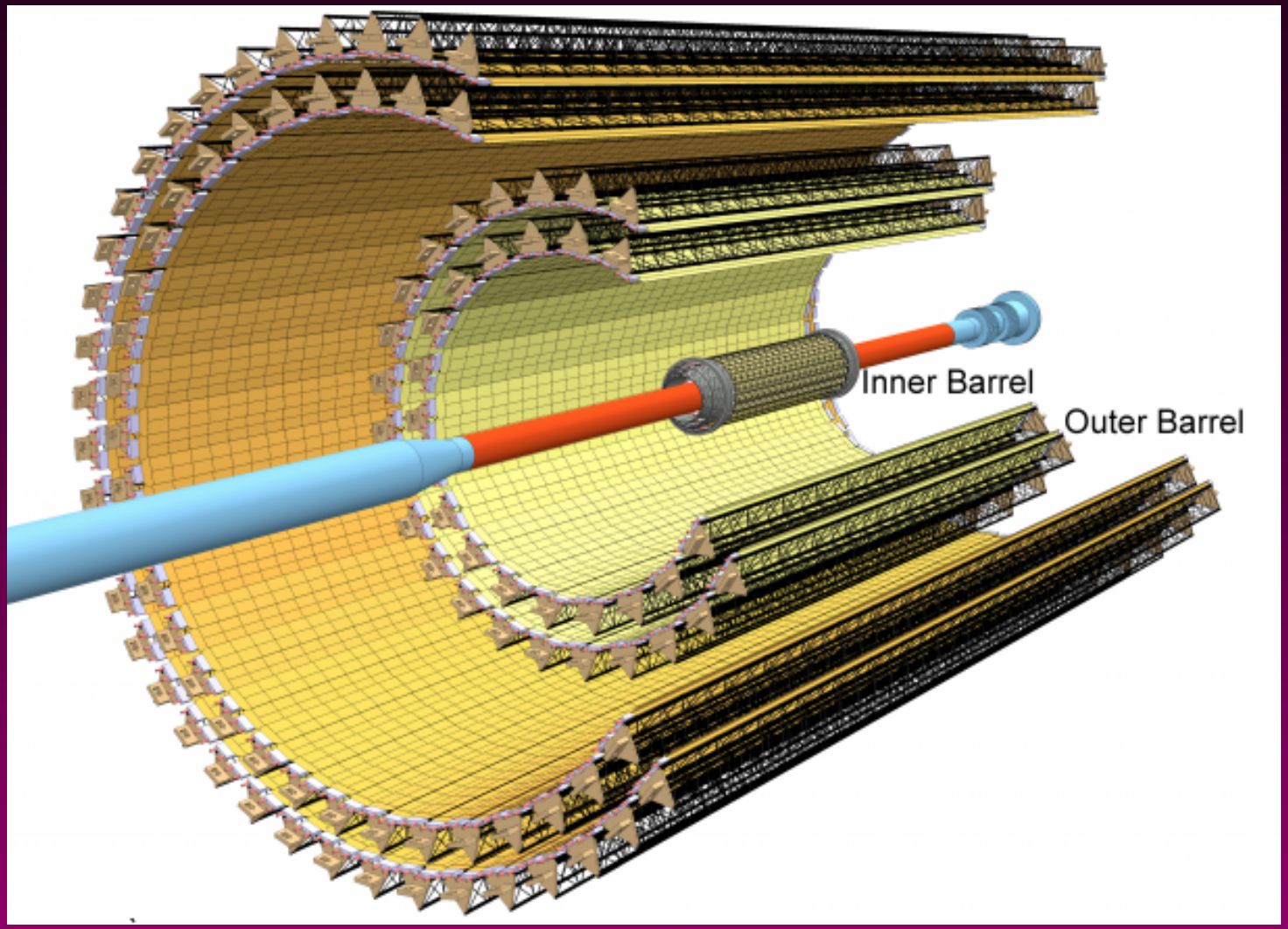
Sezione di Torino

A 1.2 Gb/s Data Transmission Unit in CMOS 0.18 μm for the ALICE Inner Tracking System front-end ASIC

G. Mazza for the ALICE collaboration

ALICE ITS Upgrade

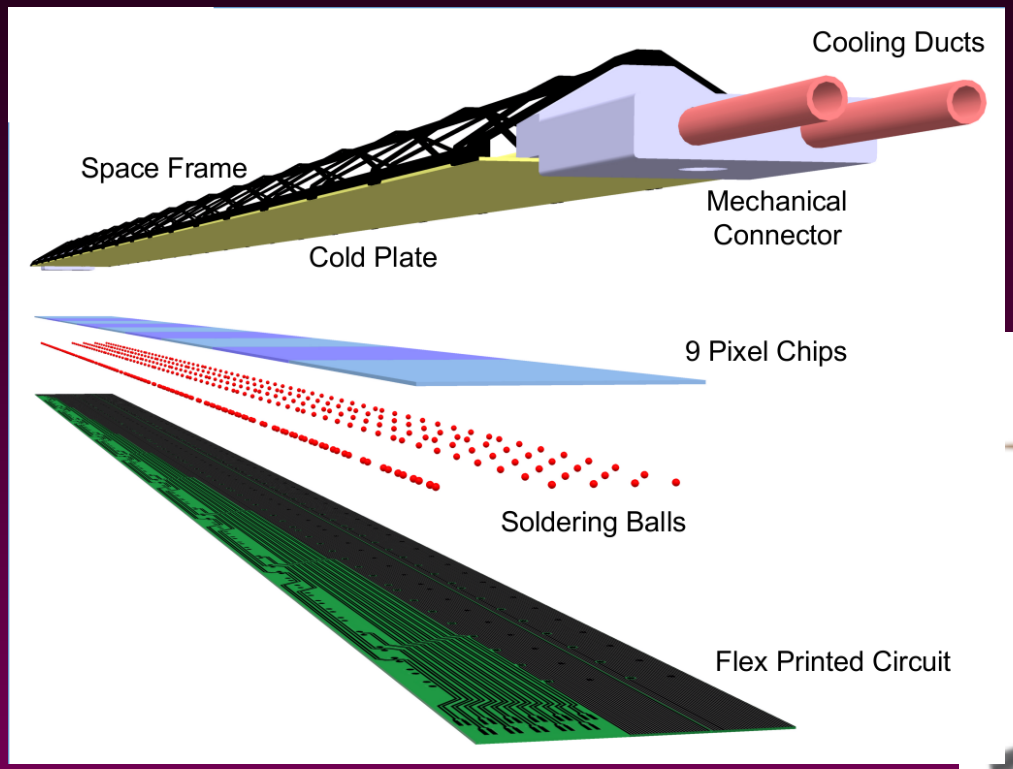
Sezione di Torino



- 7 layers based on CMOS sensors
- 48 inner barrel staves (290 mm) on 3 layers
- 54 middle barrel staves (900 mm) on 2 layers
- 90 outer barrel staves (1500 mm) on 2 layers
- Total active area ~10m^2
- Pixel size 28×28 μm^2
- ~24000 pixel chips (12.5×10^9 pixels)

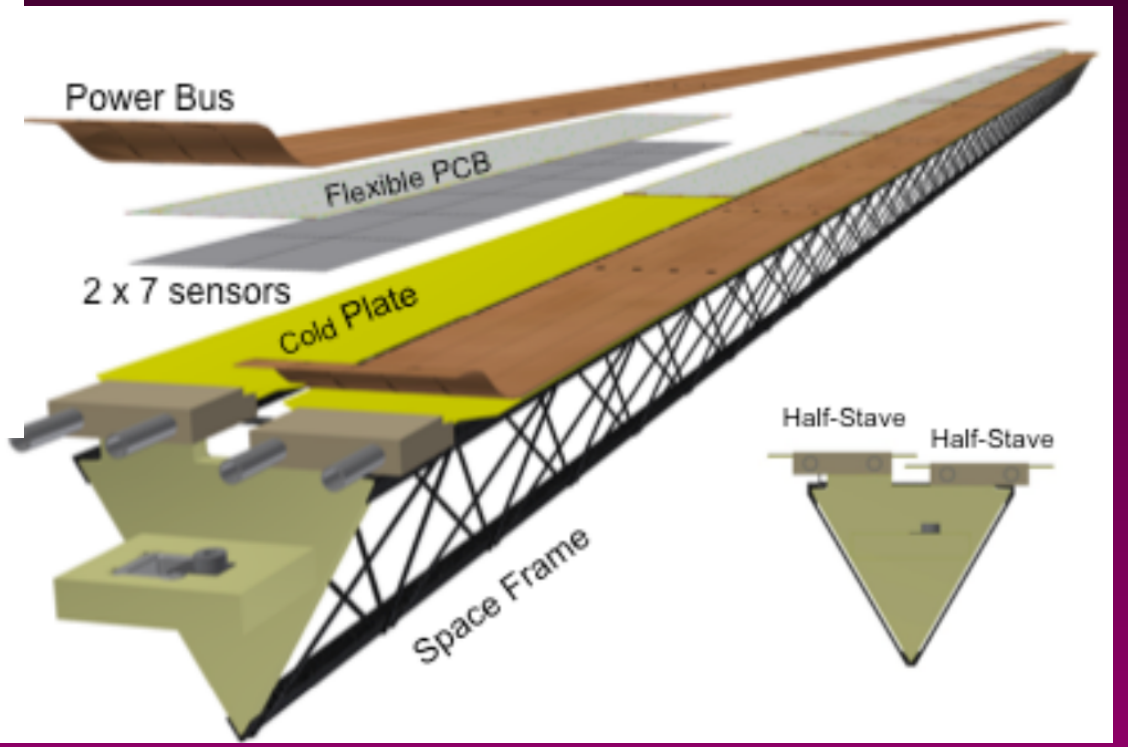
Staves

Sezione di Torino



module : 2×7 chips
MB Layers : 2×4 modules/stave
OB Layers : 2×7 modules/stave

IB Layers : 9 chips/stave



DTU specs

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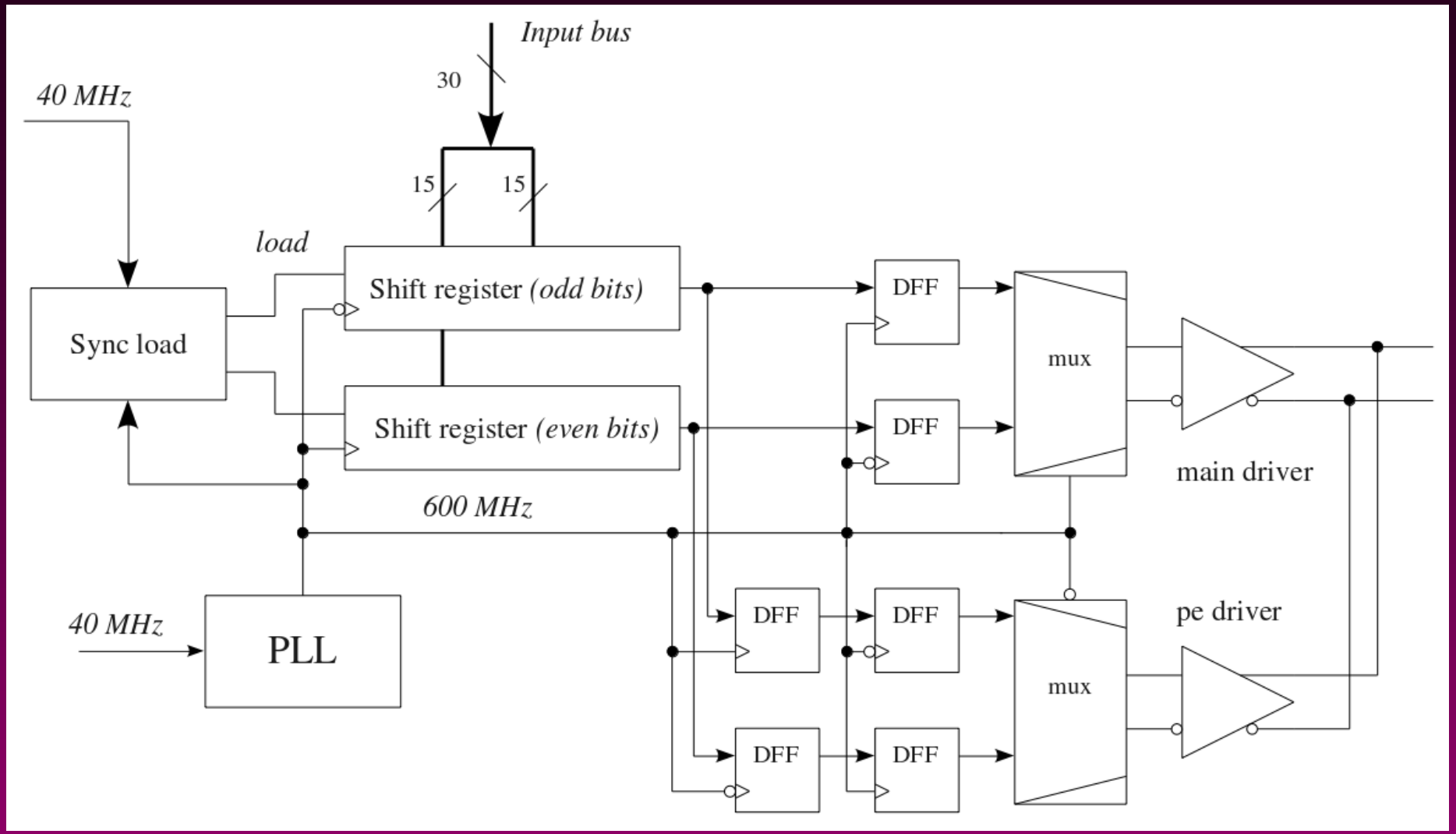
Input clock	*40 MHz*
Transmission clock	*600 MHz*
Transmission type	*Double Data Rate (DDR)*
Line/Data rate (inner layers)	*1.2/0.96 Gb/s (IB)*
Line/Data rate (outer layers)	*400/320 Mb/s (MB-OB)*
Data encoding	*8b10b*
Electrical protocol	*(pseudo)LVDS*
Technology	*CIS 0.18 µm*

DTU scheme

Sezione di Torino



DTU implementations

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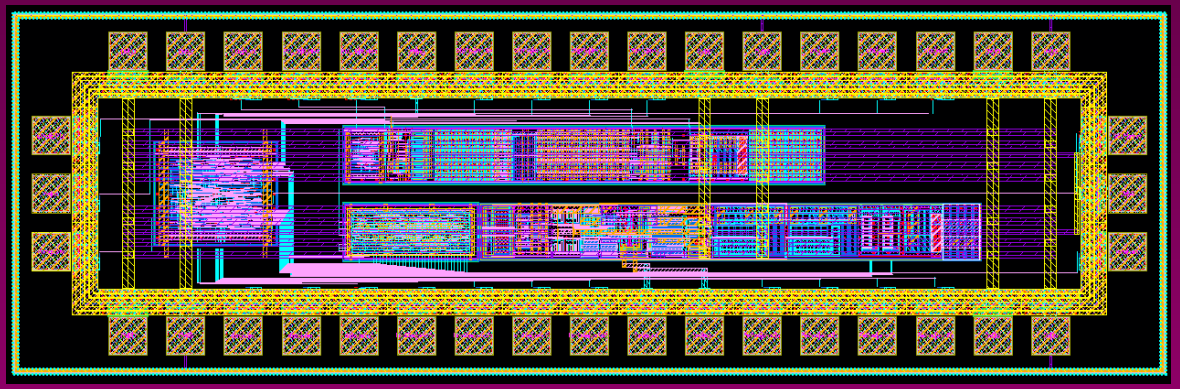
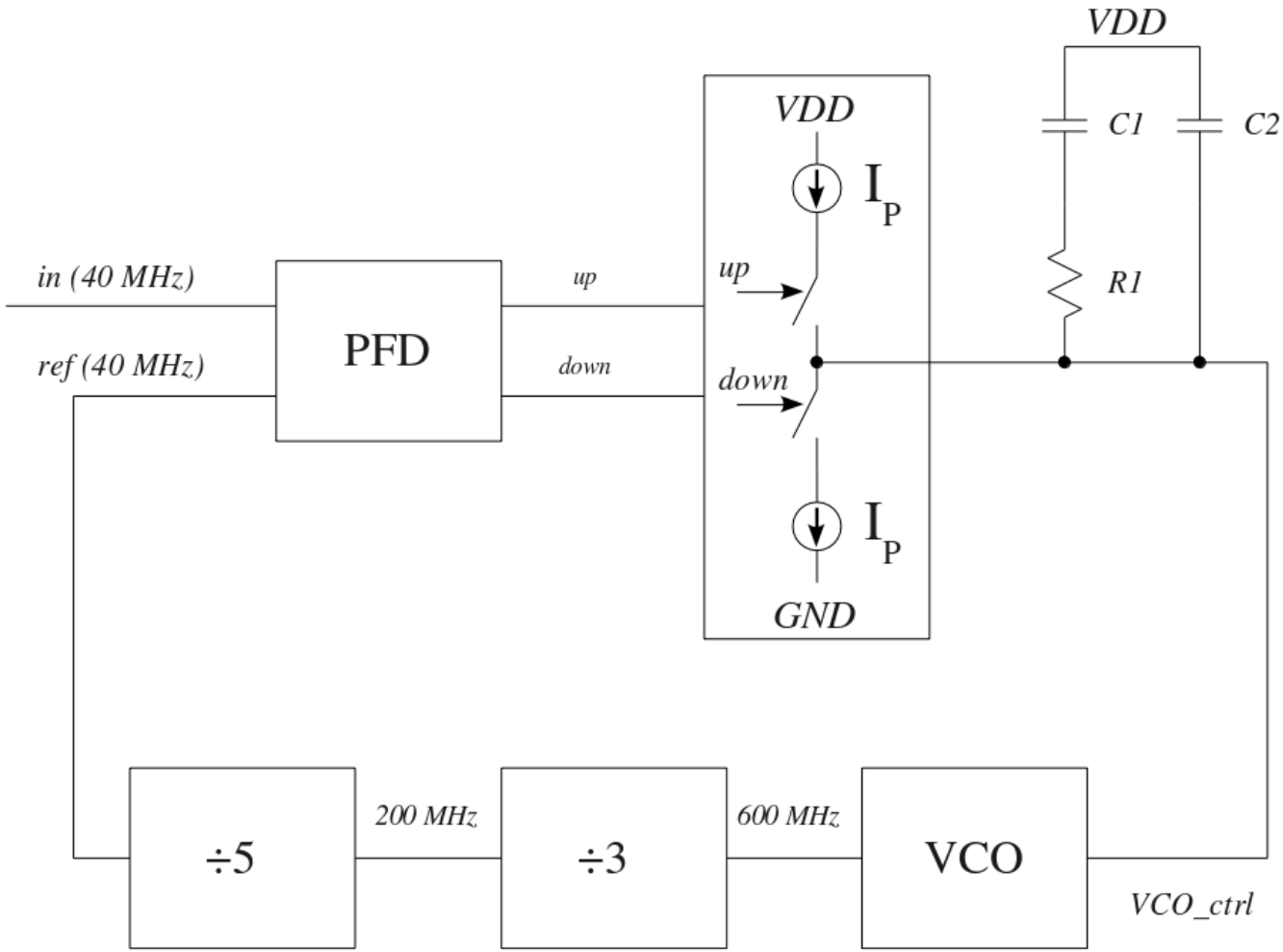
DTU has been implemented in two ASICs :

- Alpide v3 (and v4)
- DTU test chip
  - Layout size : 2.4 mm × 0.72 mm
  - 40 pads
  - includes PLL, serializer and driver + test features



PLL scheme

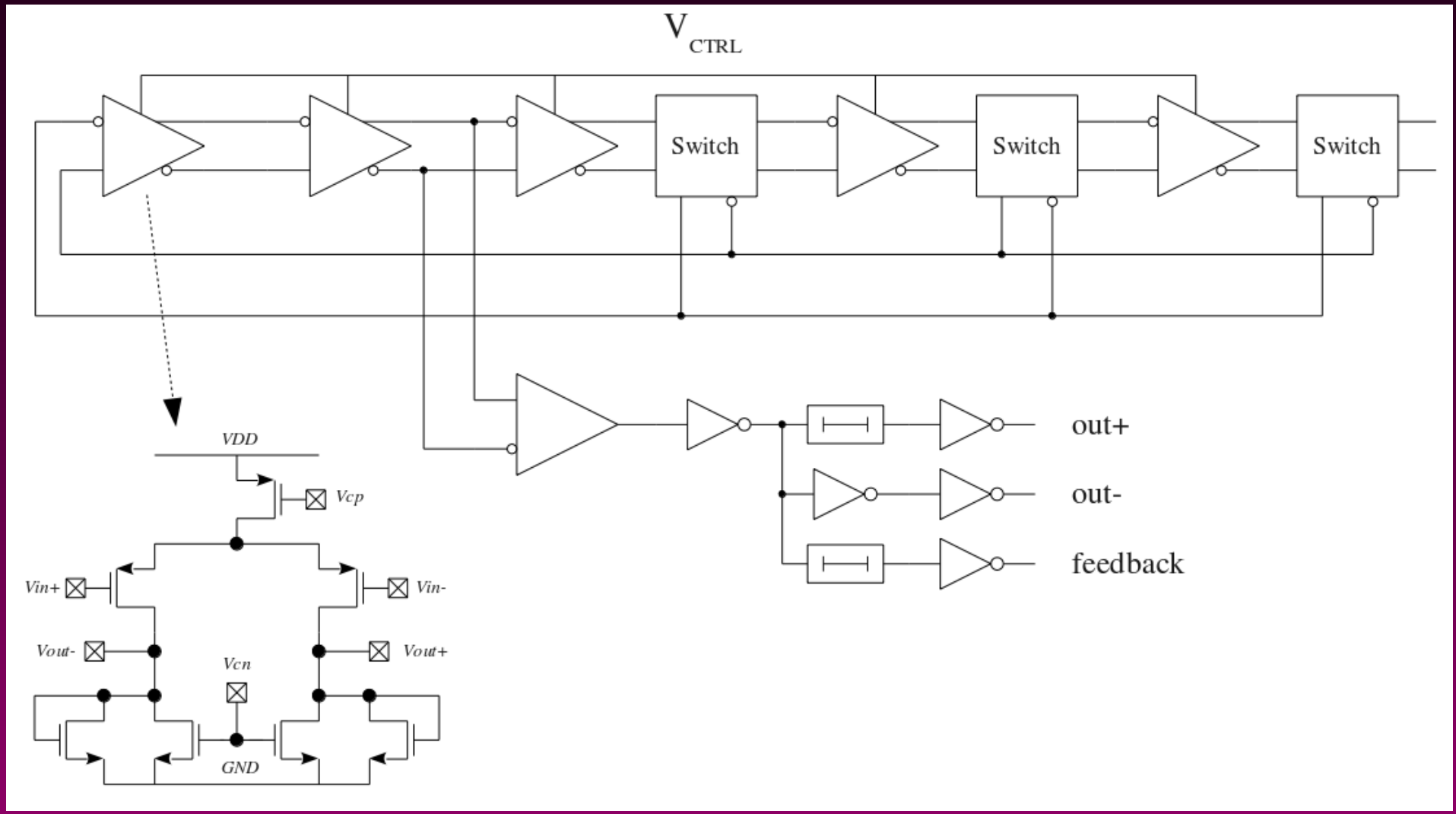
Sezione di Torino



- Input frequency 40 MHz
- Area : 1059×120 µm^2 *(form factor set by Alpide floorplan requirements)*
- Differential ring oscillator VCO *(range 500-700 MHz)*
- SEU tolerant frequency divider
- Lock time ~10 µs
- Power : 15.4 mW @1.2V

VCO scheme

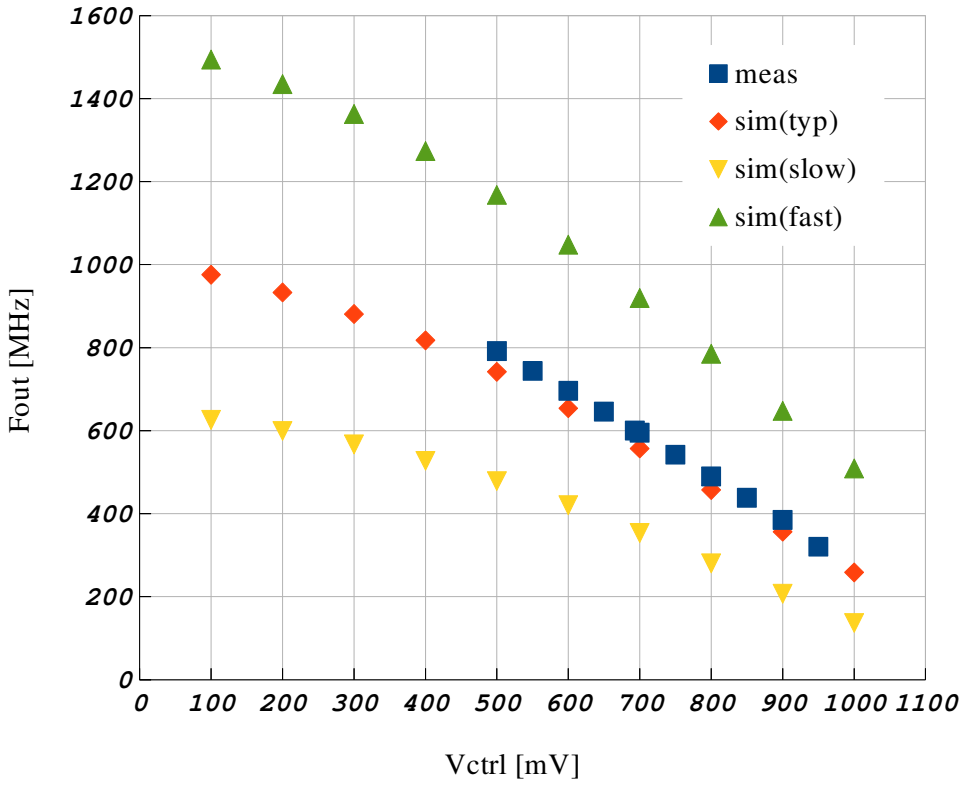
Sezione di Torino



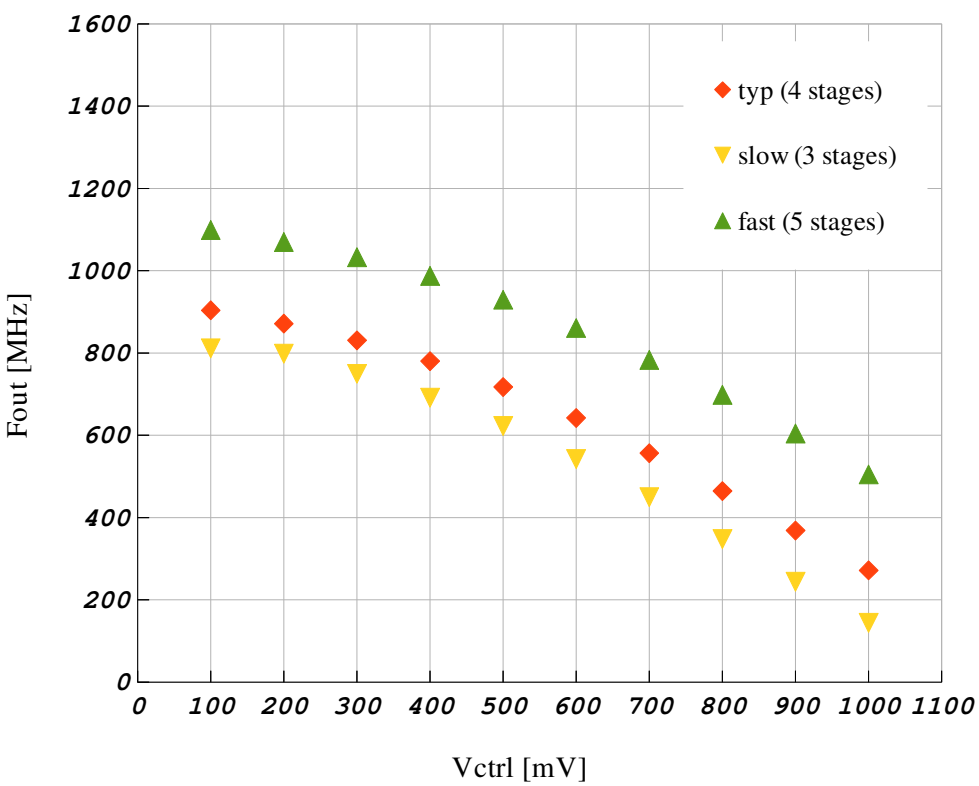
VCO frequency spread

Sezione di Torino

VCO with 4 stages (sim & measurements)

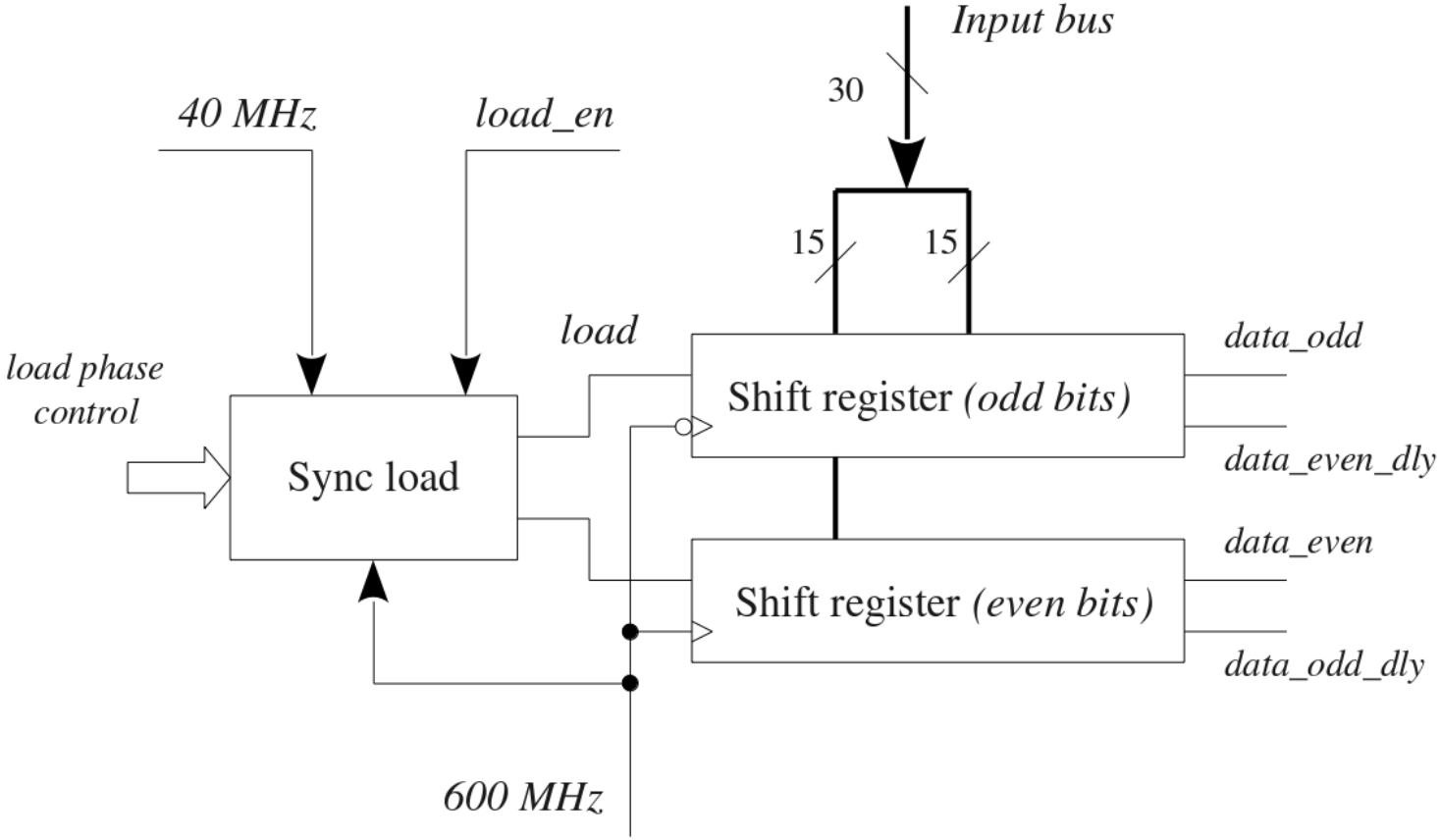


VCO with 3-4-5 stages (sim only)



Serializer scheme

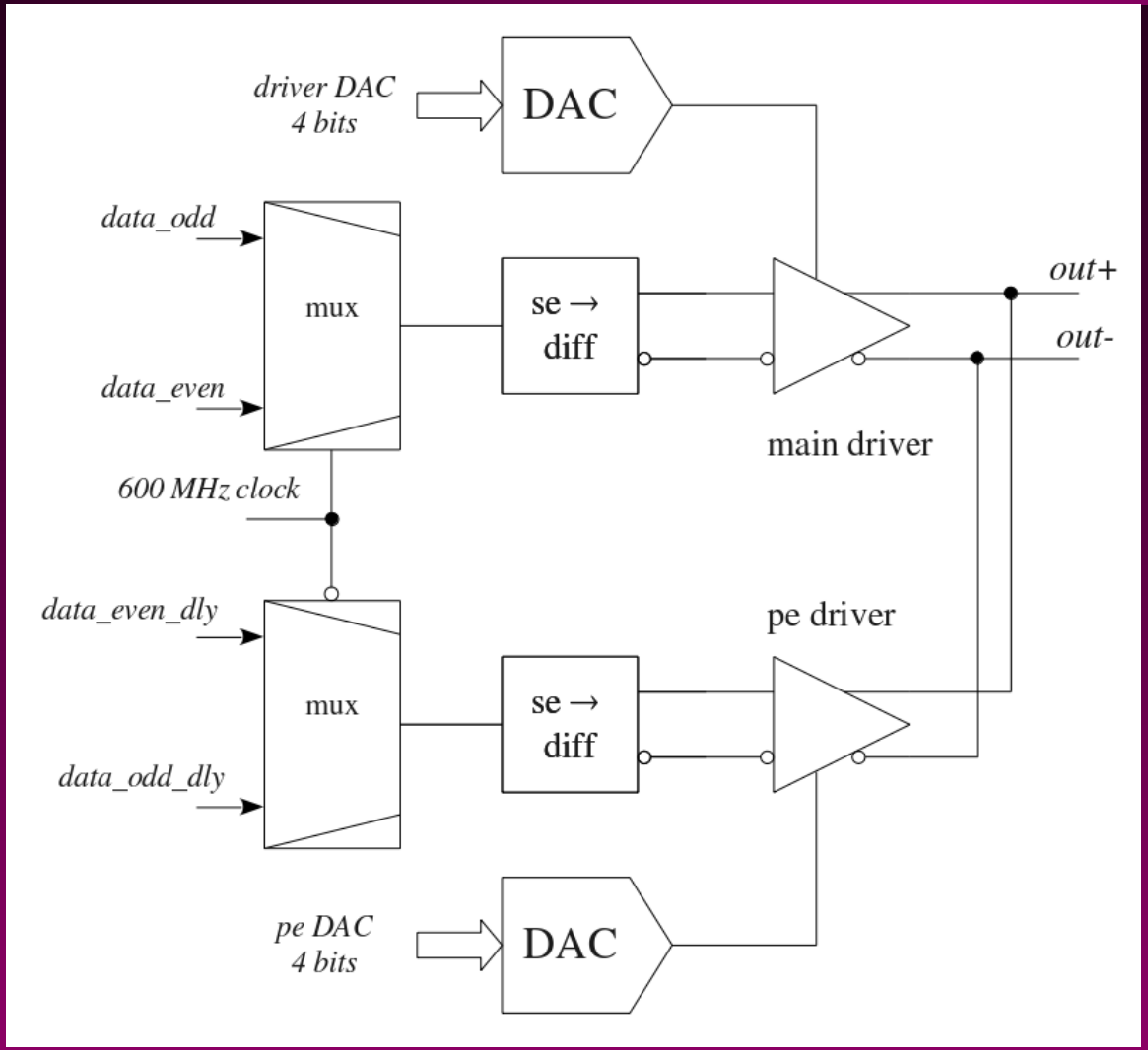
Sezione di Torino



- Double Data Rate
- TMR-based SEU protection
- Programmable phase control synchronization
- Power : 22.56 mW @1.2V

Driver scheme

Sezione di Torino



- Pseudo-LVDS driver
- CM voltage 900 mV
- Output current : 0÷5 mA in 312 µA steps (4 bits)
- Pre-emphasis current : 0÷2.5 mA in 156 µA steps (4 bits)
- Pre-emphasis time width : ½ clock cycle
- Power : 17.06 mW @1.2V *(at half driving and pe current settings)*

Main driver schematic

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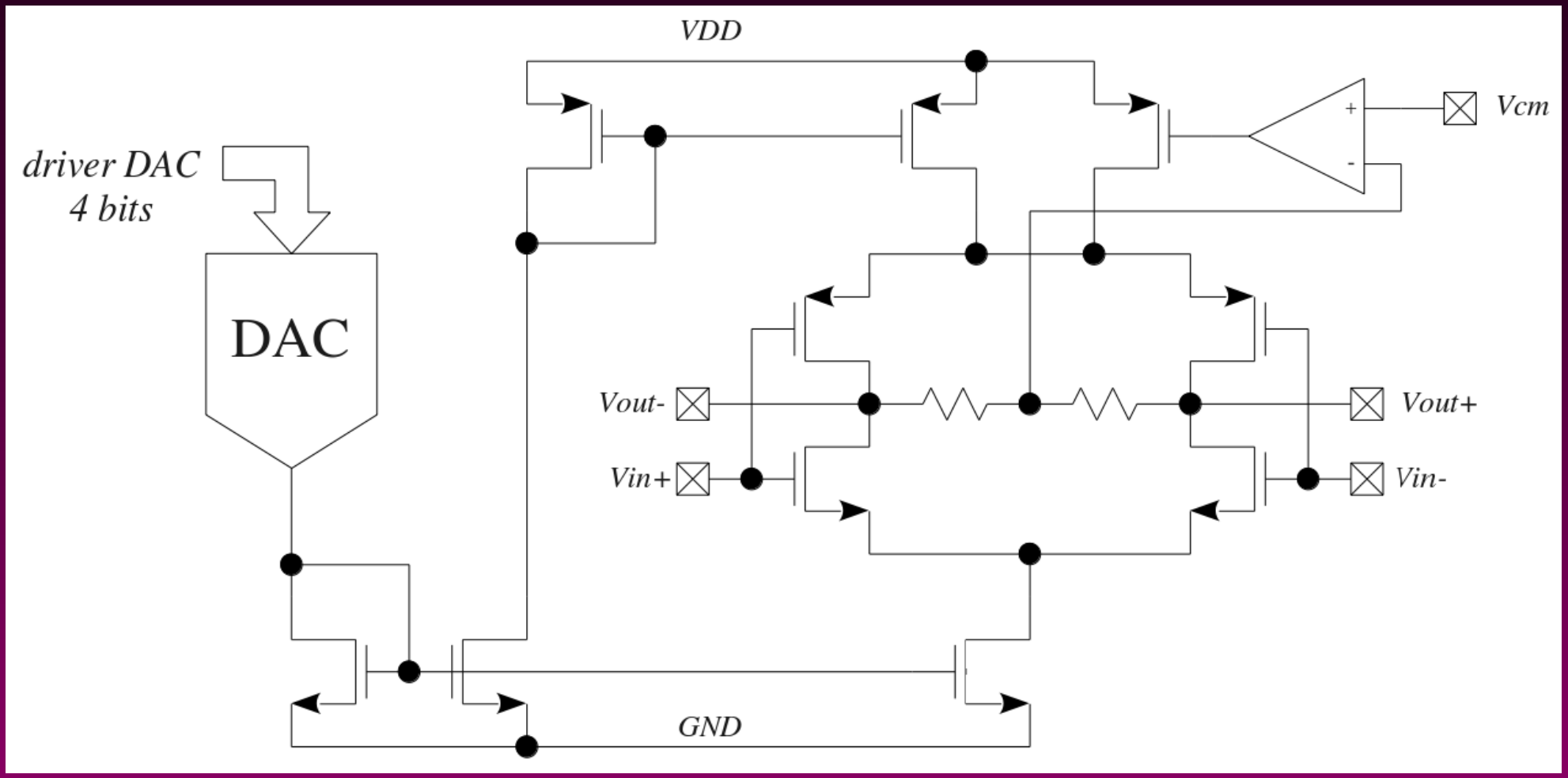
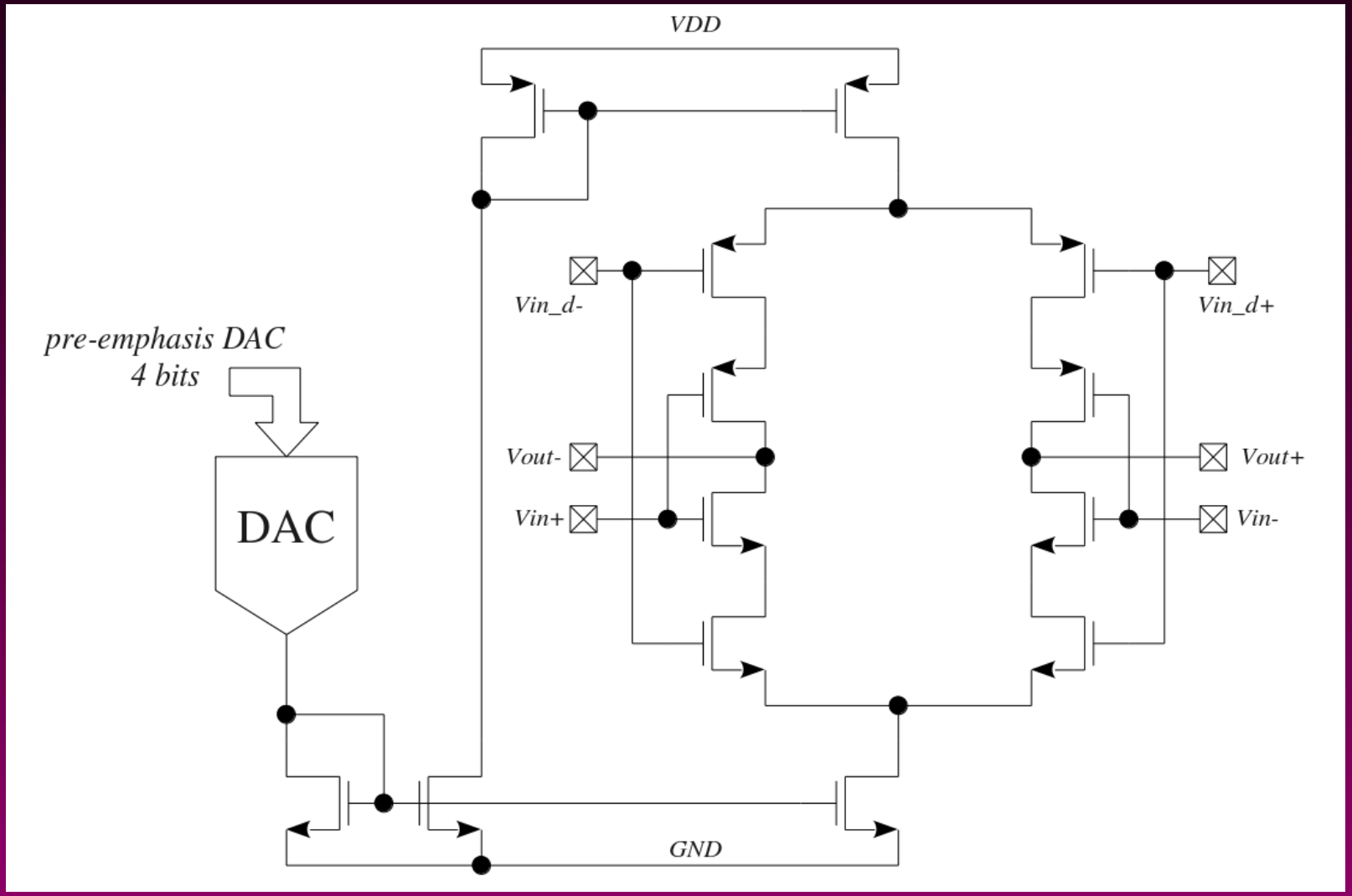


Pre-emphasis driver schematic

Sezione di Torino



PLL v1 test summary - 1

Sezione di Torino

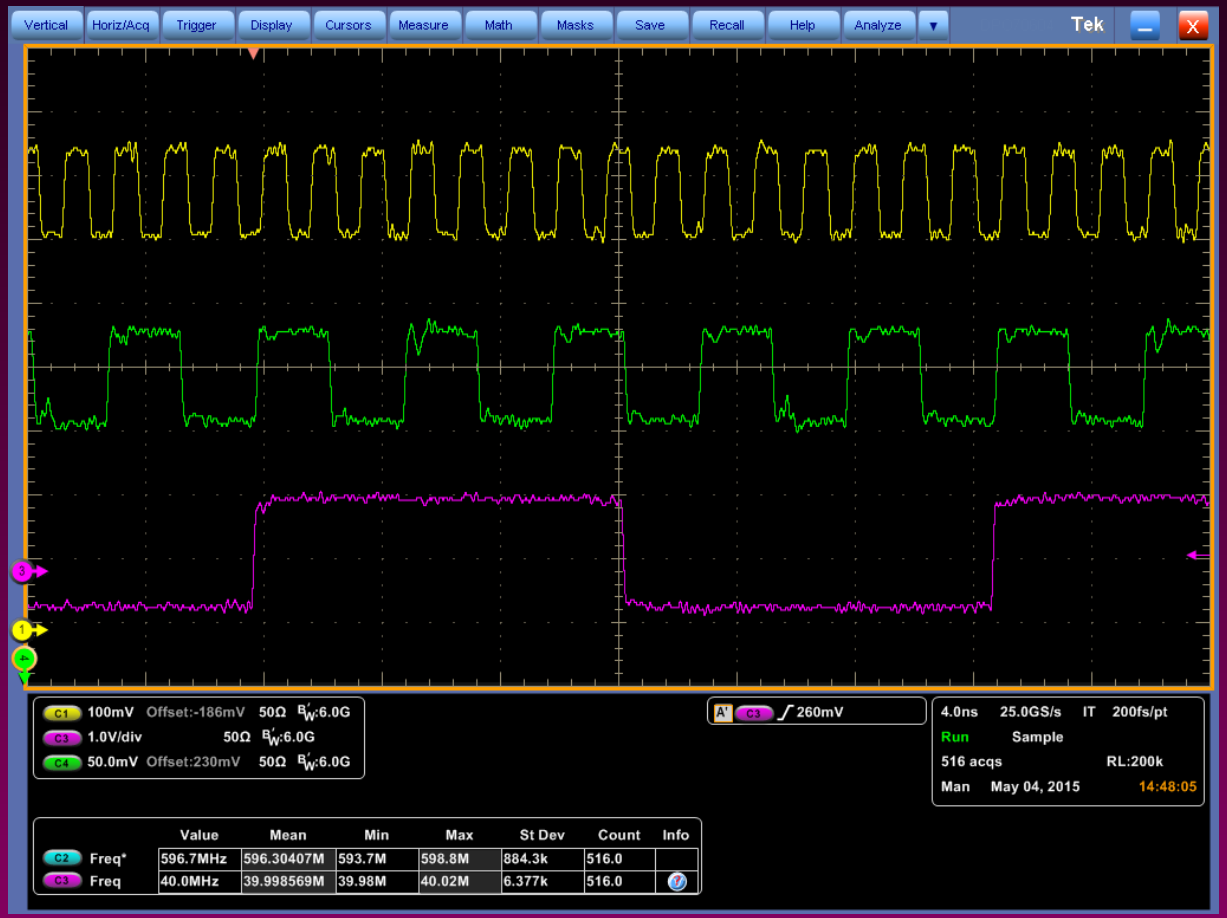
- Input frequency : 40 MHz
- Input frequency range : 30 MHz -50 MHz
- Main output frequency : 600 MHz ($f_{IN} \times 15$)
- Secondary output frequency : 200 MHz ($f_{IN} \times 5$)

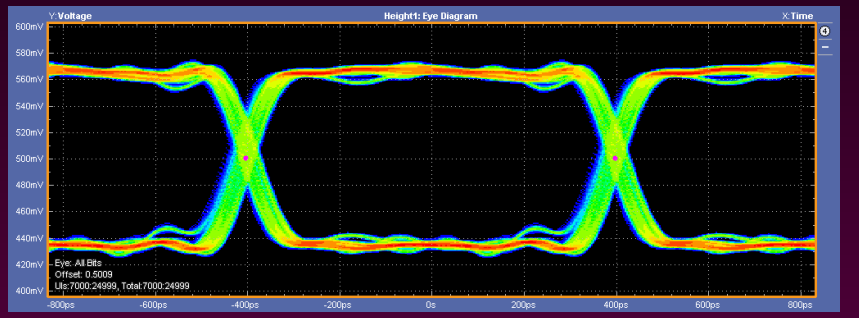
	Mean	*σ*
clock period	*1.667 ns*	*6.8642 ps*
clock frequency	*600.01 MHz*	*2.4708 MHz*
duty cycle	*50.79%*	*0.0896 %*

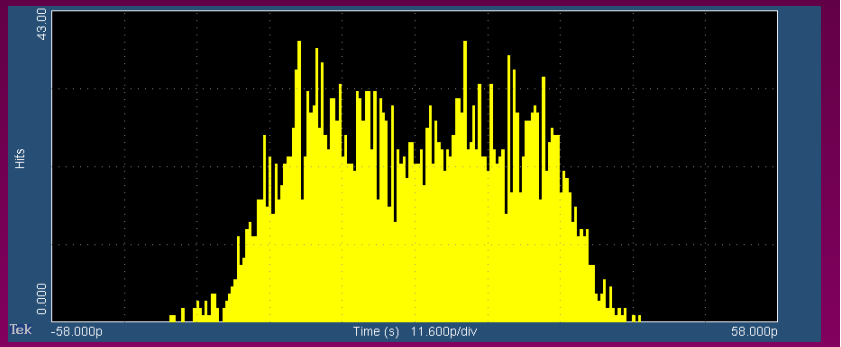
Random jitter	*4.736 ps (r.m.s.)*
Periodic jitter	*46.342 ps (pk-pk)*

PLL v1 test summary - 2

Sezione di Torino

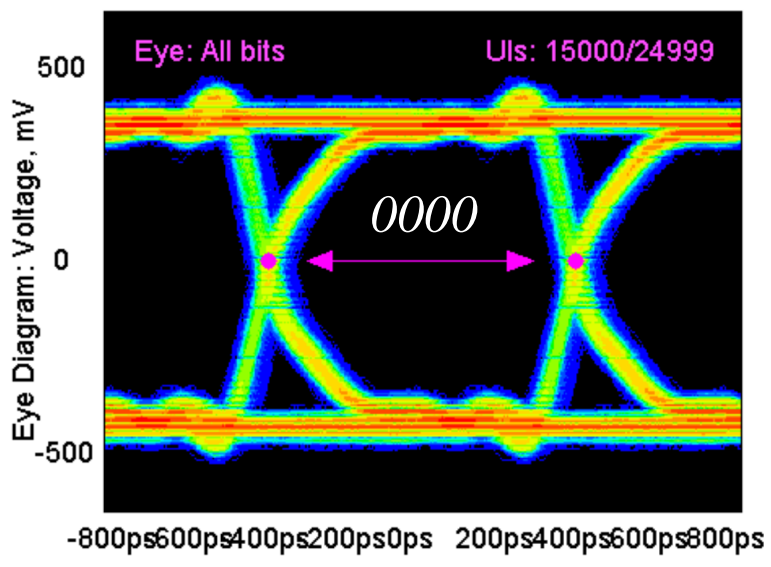






DTU test chip Electrical tests - 1

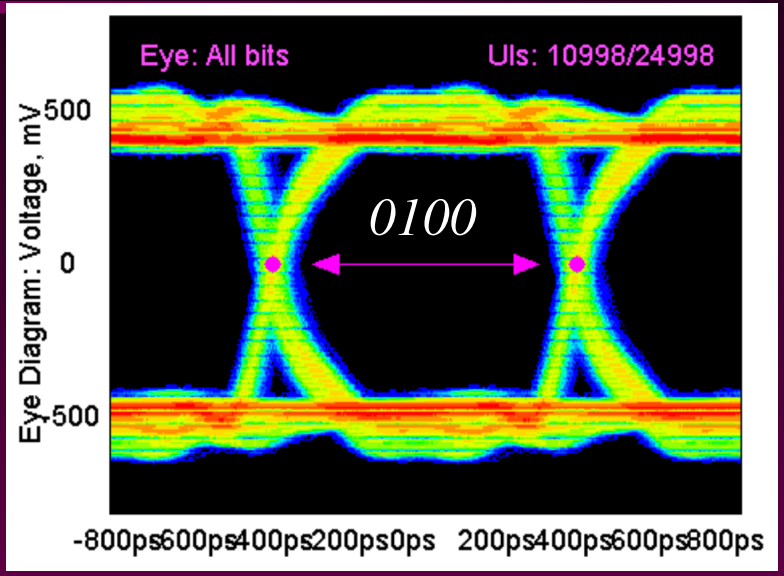
Sezione di Torino



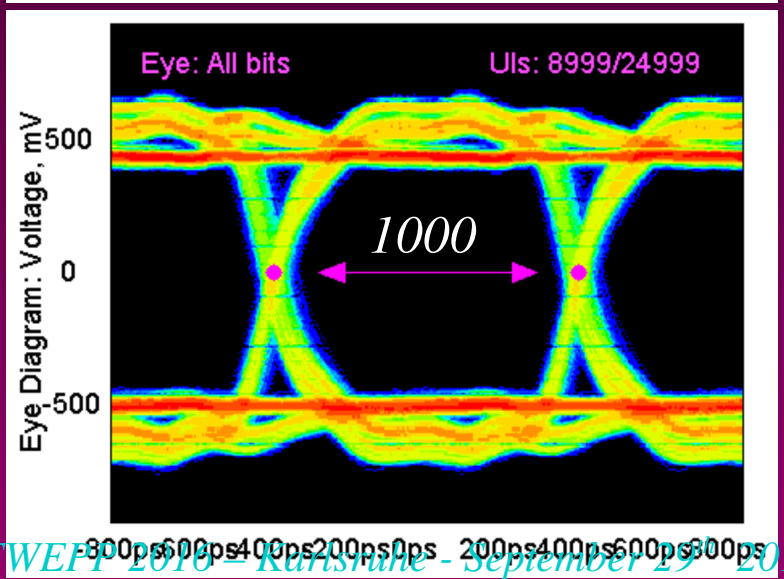
Drv DAC : 1000

Rate : 1.25 Gb/s

BER : 10^{-12}

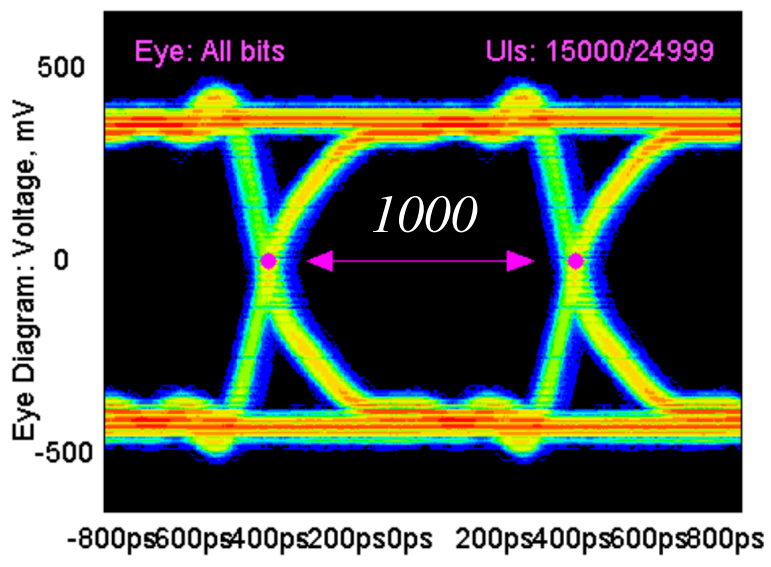


	PE 0000	PE 0100	PE 1000
Eye width	0.822 UI	0.826 UI	0.835 UI
Eye opening	0.738 UI	0.742 UI	0.716 UI
Rj	11.4 ps	10.9 ps	12.0 ps
Dj	48.8 ps	52.8 ps	57.4 ps



DTU test chip Electrical tests - 2

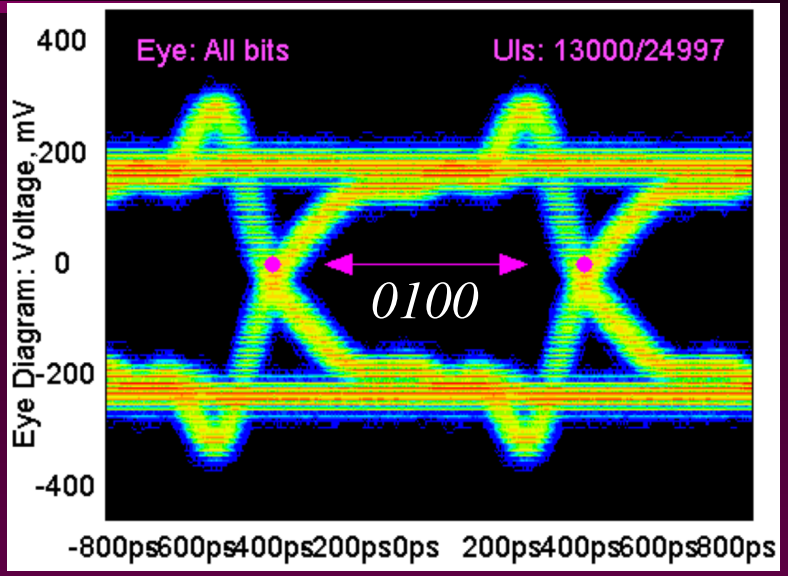
Sezione di Torino



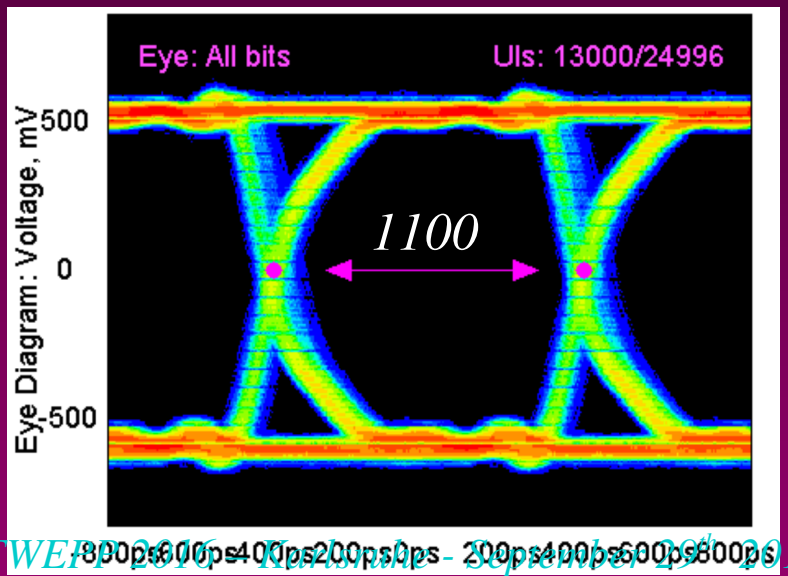
PE DAC : 0000

Rate : 1.25 Gb/s

BER : 10^{-12}

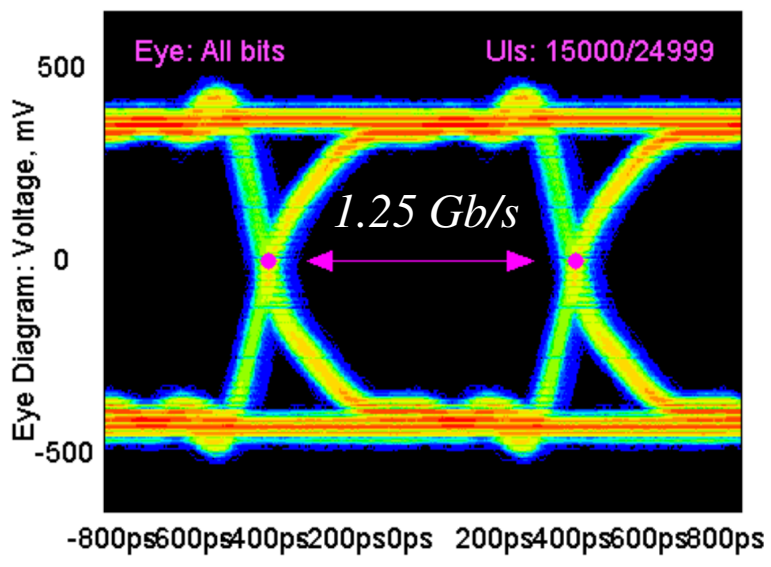


	DRV 1000	DRV 0100	DRV 1100
Eye width	0.822 UI	0.759 UI	0.819 UI
Eye opening	0.738 UI	0.645 UI	0.688 UI
Rj	11.4 ps	12.8 ps	11.4 ps
Dj	48.8 ps	102.7 ps	88.7 ps



DTU test chip Electrical tests - 3

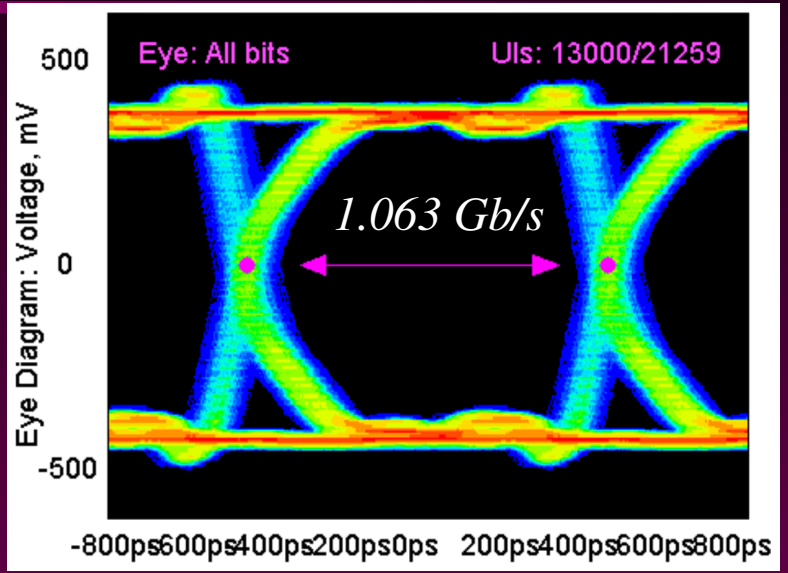
Sezione di Torino



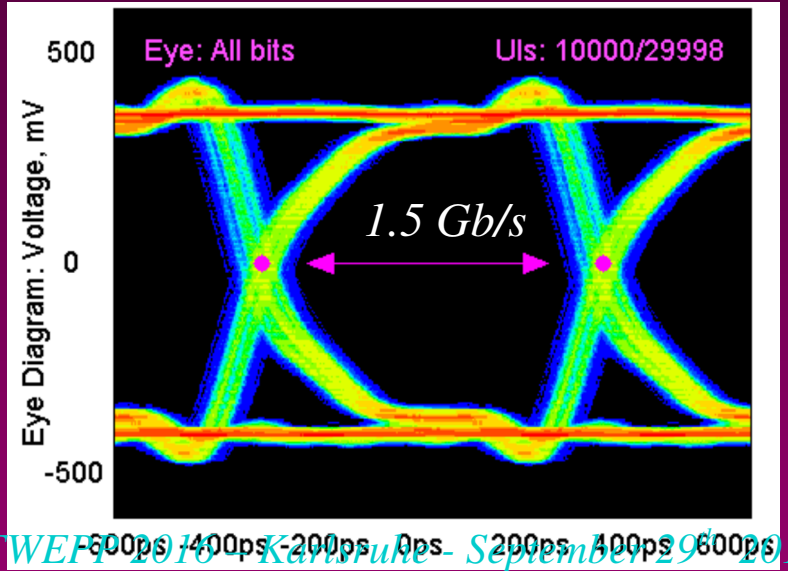
DRV DAC : 1000

PE DAC : 0000

BER : 10^{-12}



	1.25 Gb/s	1.063 Gb/s	1.5 Gb/s
Eye width	0.822 UI	0.814 UI	0.789 UI
Eye opening	0.738 UI	0.713 UI	0.708 UI
Rj	11.4 ps	14.2 ps	8.8 ps
Dj	48.8 ps	69.6 ps	71.5 ps



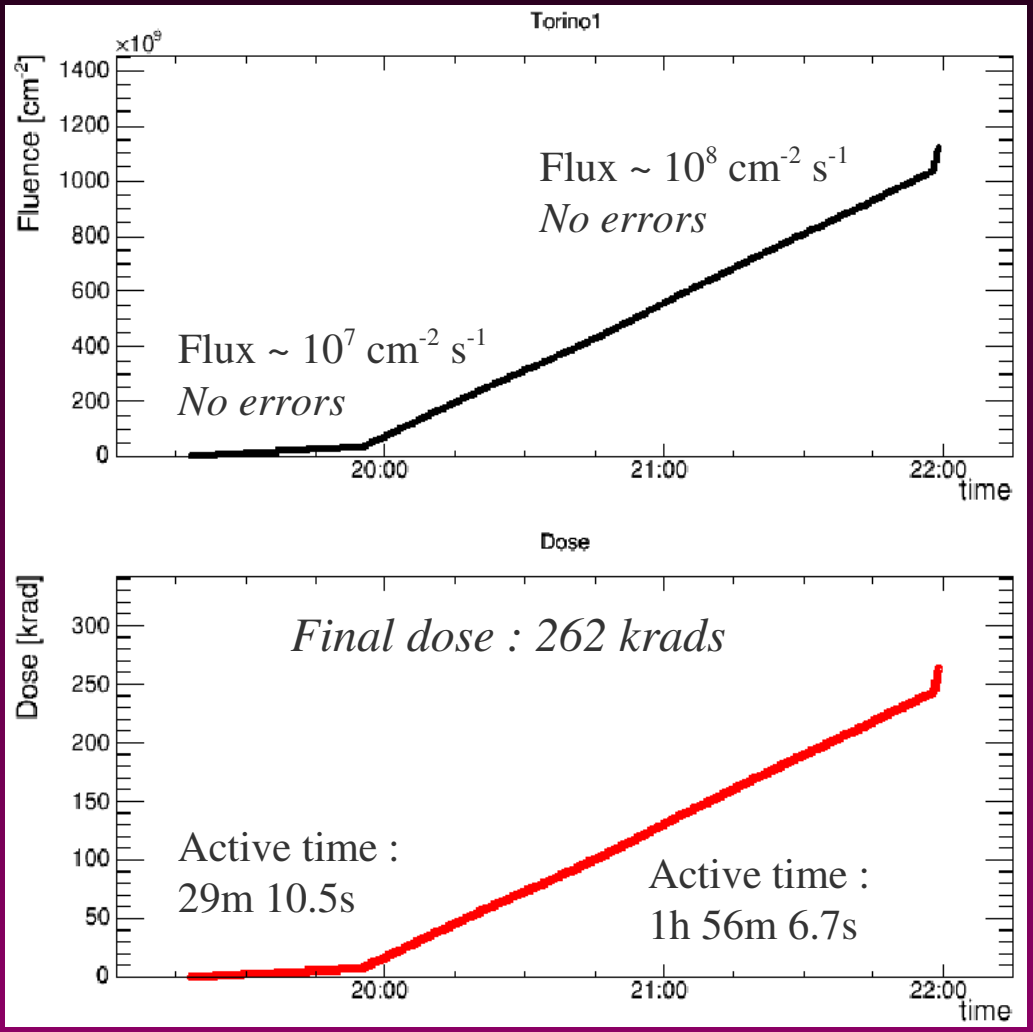
Irradiation tests

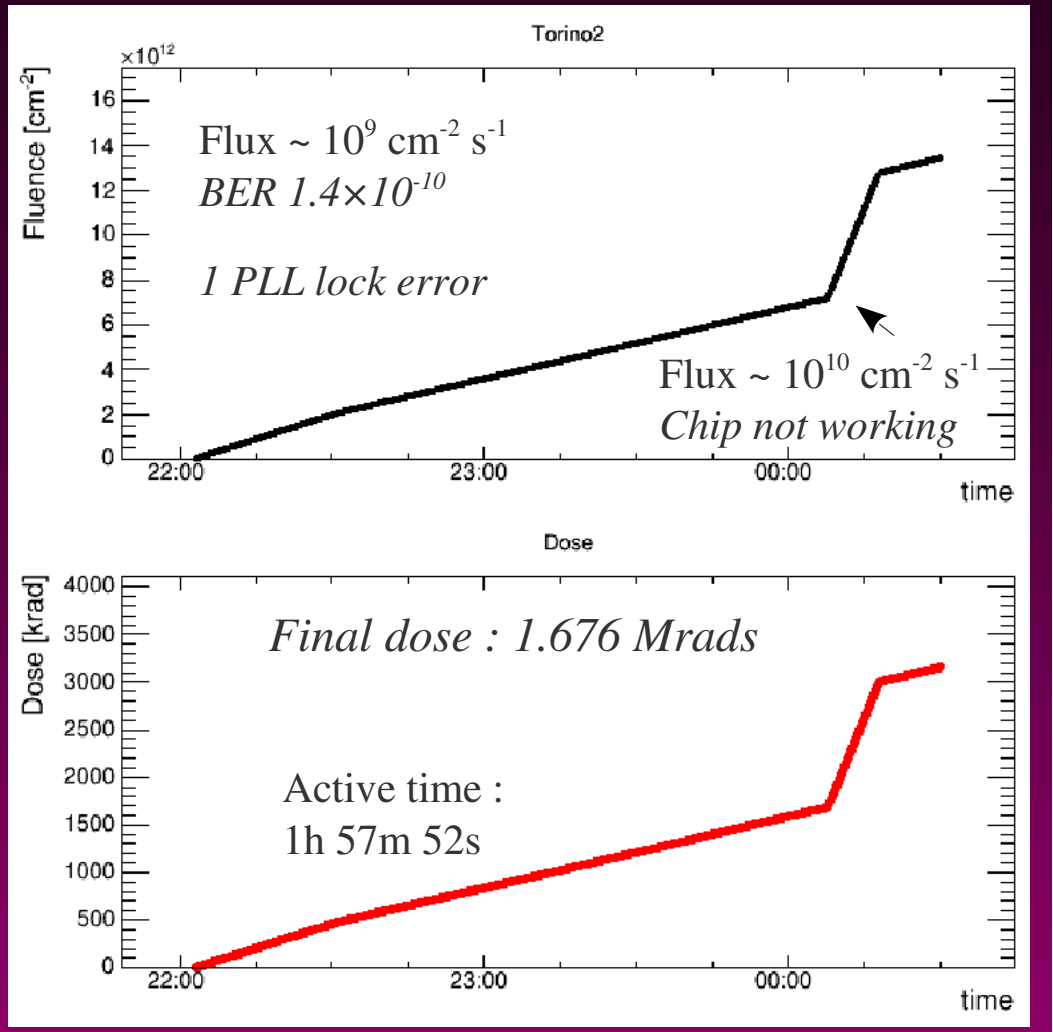
Sezione di Torino

- November 2015 : SEU test @ LNL Legnaro with ions
  - *chip partially damaged + set-up problems → results discarded*
- February 2016 : TID and SEU tests @ NPI Prague with 30 MeV protons
- July 2016 : SEU test @ LNL with ions

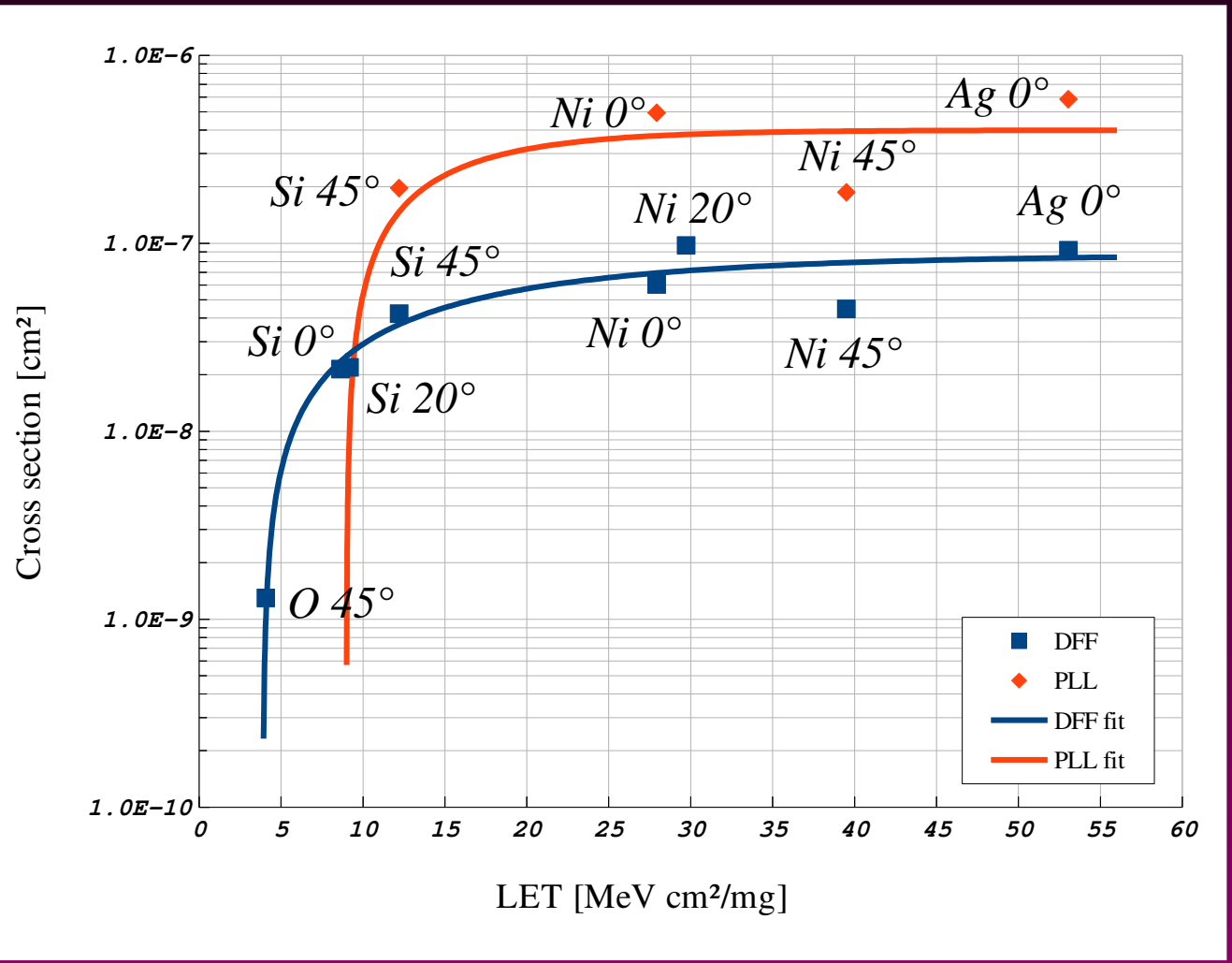
Test with 30 MeV protons

Sezione di Torino





PLL & DFF cross section



$LET_{TH} \simeq 3.9$ MeV cm^2/mg for the DFF

Note : DFF cross section is per bit

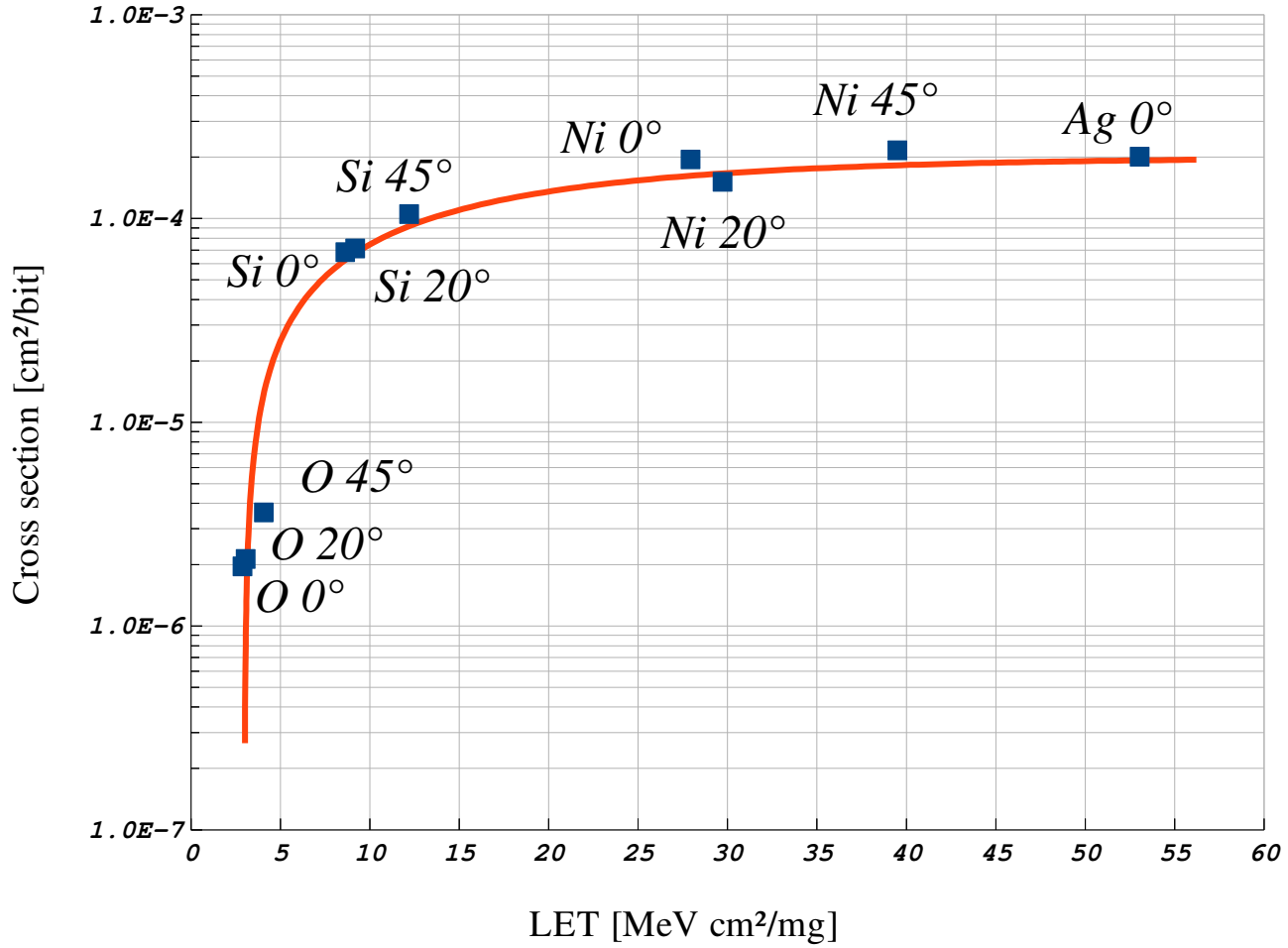
$LET_{TH} \simeq 9$ MeV cm^2/mg for the PLL lock

Estimated PLL loss of lock MTBF in layer 0 (108 DTUs) : 149h 33m

Only 1 (out of 37) GTX loss of lock

BER cross section *(preliminary)*

Sezione di Torino



$LET_{TH} \simeq 3$ MeV cm^2/mg for the serial data

Note : cross section is per bit

Estimated transmission MTBF in layer 0 (108 DTUs) : 42.8 s

Estimated BER per link : 3.53×10^{-14}

Receiver not optimized

Still to be fully understood (flux dependency ?)

Conclusions

Sezione di Torino

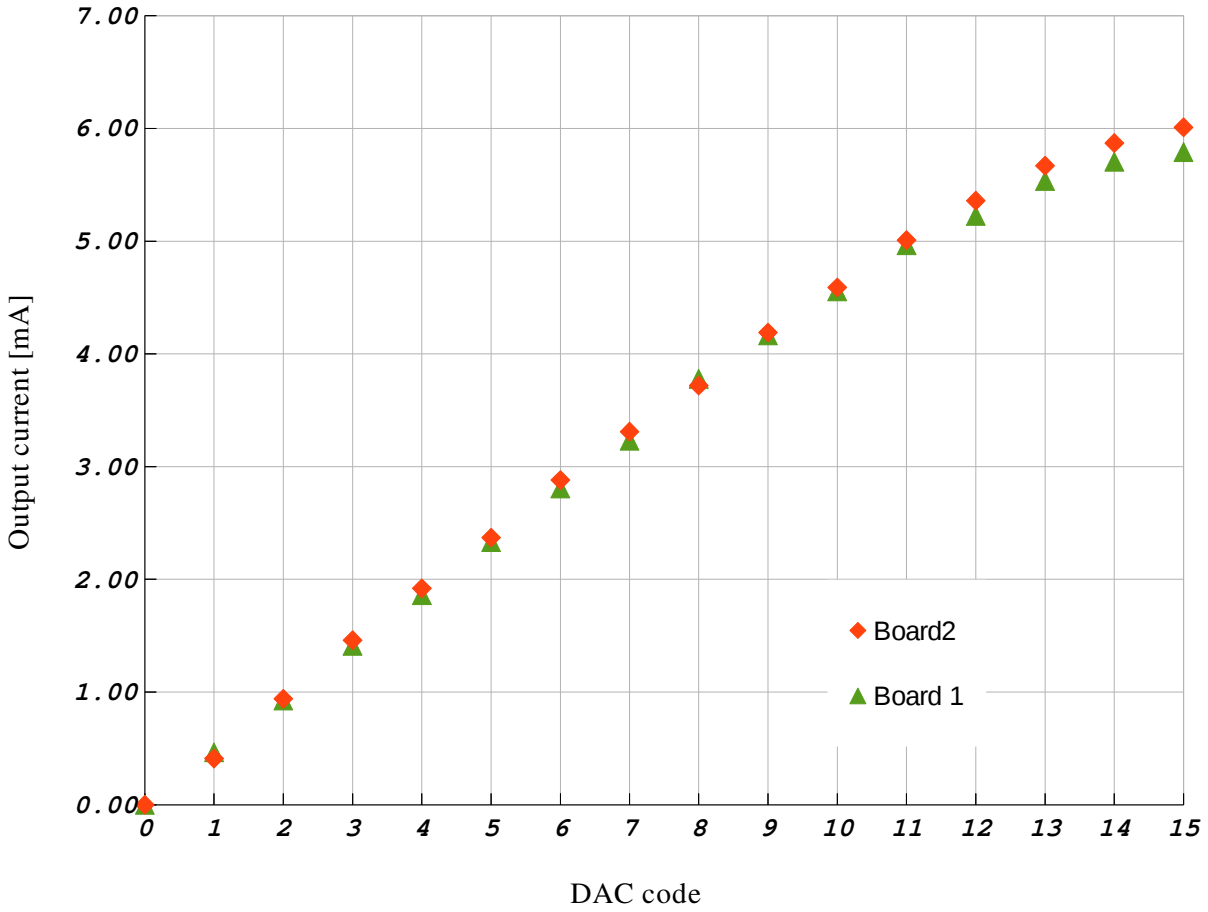
- A 1.2 Gb/s Data Transmission Unit (DTU) for the upgrade of the ALICE Inner Tracking System has been designed in 0.18 µm technology and tested
- The DTU consists of a PLL for clock multiplication, a DDR serializer and a pseudo-LVDS driver with pre-emphasis
- Electrical tests show that the DTU fullfills the specifications
- TID tests shows a radiation tolerance up to ~1 Mrad
- SEU tests shows a good behaviour in the expected ALICE environment. *Still something to be understood on BER aspect.*
- New DTU version (with supply better noise insulation) submitted in the Alpide chip. Test ongoing.

Spare slides

Sezione di Torino

Output amplitude

Sezione di Torino



Output current vs DAC code

Slope : 0.39 mA/DAC code

0.40 mA/DAC code

Intercept : 0.37 mA

0.39 mA

Note : current measurement absolute value not fully accurate *(too fast to have full voltage setting)*

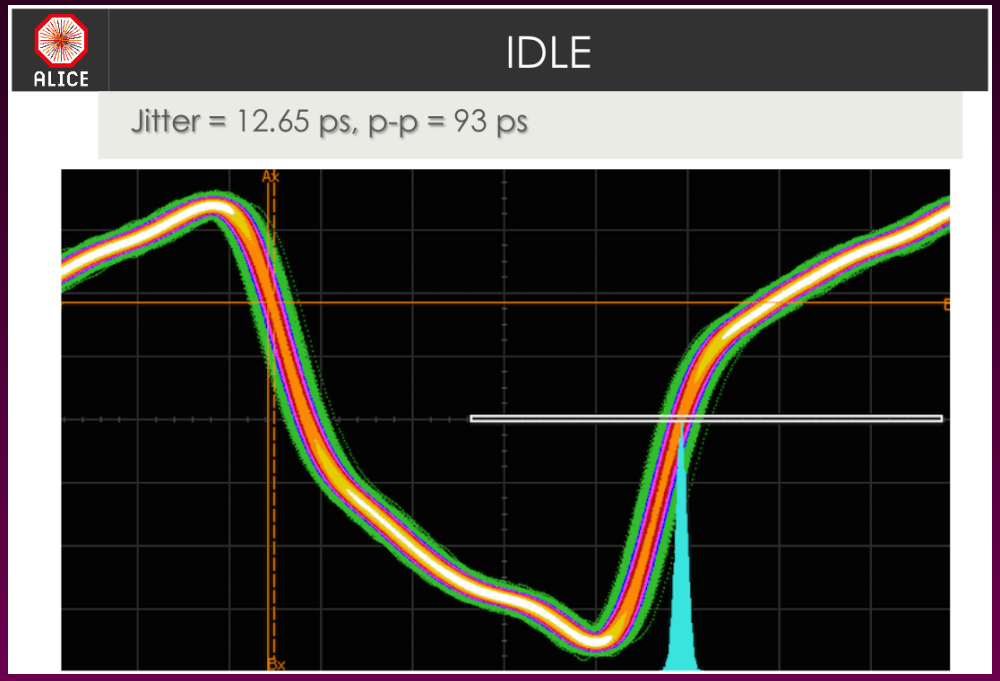
SEU test in Legnaro ion list

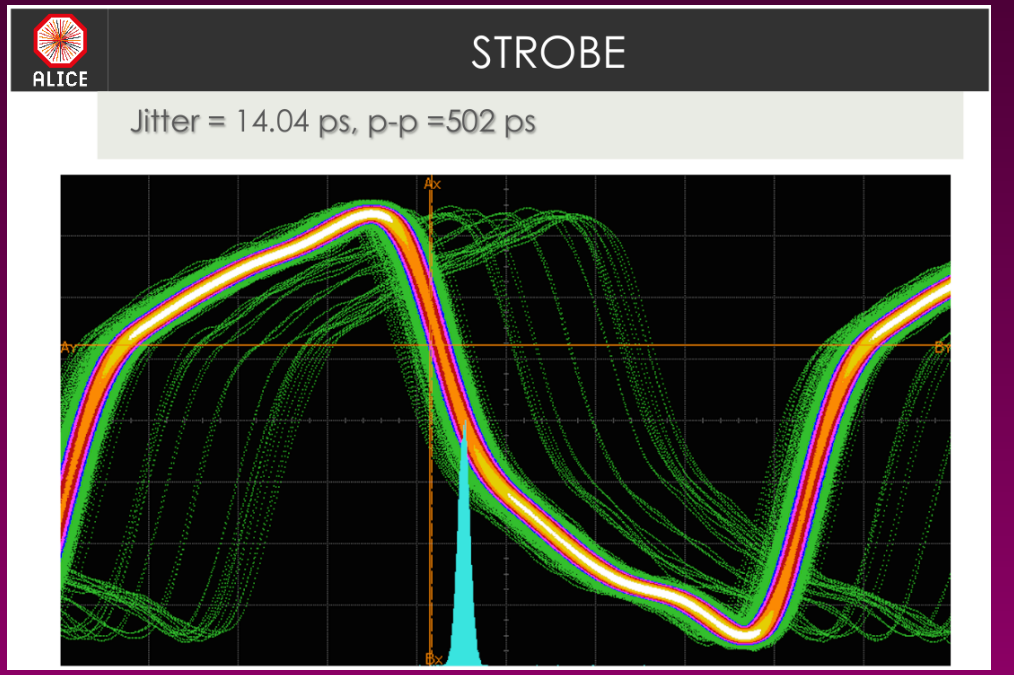
Sezione di Torino

Ion	*Angle*	*Energy [MeV]*	*LET [MeV cm²/mg]*
Ag	*0°*	*266*	*53.04*
Ni	*45°*	*220*	*39.50*
Ni	*20°*	*220*	*29.72*
Ni	*0°*	*220*	*27.93*
Si	*45°*	*157*	*12.20*
Si	*20°*	*157*	*9.18*
Si	*0°*	*157*	*8.63*
O	*45°*	*108*	*4.07*
O	*20°*	*108*	*3.06*
O	*0°*	*108*	*2.88*

Test results on Alpide

Sezione di Torino





Workarounds

Sezione di Torino

- The degradation is a function of the chip activity.
- Simulations show that the most critical component in terms of PSRR is the control line of the VCO
- Actions :
  - Filter on the VCO_ctrl line *(limited by stability issues)*
  - try to reduce the noise coupling of the *VCO_ctrl* line
  - improve decap cells distribution on the digital part
  - separate supply for the PLL at the chip level

Bit error table for protons

Sezione di Torino

Bit	# Errors	Bit	# Errors	Bit	# Errors
0	0	10	23	20	7.03×10^7
1	16	11	35	21	3.04×10^9
2	3.04×10^9	12	7.03×10^7	22	2.97×10^9
3	7.03×10^7	13	0	23	2.97×10^9
4	0	14	35	24	7.03×10^7
5	0	15	3.04×10^9	25	3.04×10^9
6	29	16	7.03×10^7	26	2.97×10^9
7	3.04×10^9	17	3.04×10^9	27	2.97×10^9
8	7.03×10^7	18	2.97×10^9	28	2.97×10^9
9	0	19	2.97×10^9	29	7.03×10^7