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# A 1.2 Gb/s Data Transmission Unit in CMOS 0.18 $\mu m$ technology for the ALICE Inner Tracking System front-end ASIC.

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The upgrade of the ALICE Inner Tracking System is based on a Monolithic Active Pixel Sensor and ASIC designed in a CMOS 0.18 um process from TowerJazz. In order to provide the required output bandwidth (1.2 Gb/s for the inner layers and 400 Mb/s for the outer ones) on a single high speed serial link, a custom Data Transmission Unit (DTU) has been developed in the same process.

The DTU includes a clock multiplier PLL, a double data rate serializer and a pseudo-LVDS driver with pre-emphasis and is designed to be SEU tolerant.

## Summary

The upgrade of the ALICE Inner Tracking System (ITS) will see the replacement of its existing 6 layers with 7 layers of pixel detectors, based on Monolithic Active Pixel Sensor (MAPS). The new detector will feature a much higher granularity, owing to a pixel size reduction from 50 um x 425 um to 28 um x 28 um. Moreover, the innermost layer will be closer to the beam pipe, with a radius of just 22 mm. These two facts, combined with the increase in luminosity, will lead to a significant increase of the amount of data and will thus require a higher data rate link. The foreseen required bandwidth are 1.2 Gb/s for the 3 innermost layers and 400 Mb/s for the 4 outer ones. For material budget and space considerations it is mandatory to implement such a link as a fast serial one integrated in the front-end ASIC (named Alpide).

The DTU (Data Transmission Unit) is the custom block designed to implement such a data link for Alpide. It is composed of 3 main parts: a PLL to multiply the 40 MHz master clock to 200 and 600 MHz, a Double Data Rate (DDR) serializer which provides the 400 Mb/s and 1.2 Gb/s serial data stream to a LVDS driver with pre-emphasis capabilities, which in turn provides the adequate driving strength to send the data to the readout unit located outside the detector volume.

The DTU includes a range of programmable features; the output and pre-emphasis currents are tunable up to 5 mA and 2.5 mA, respectively, via 4 bits DACs. Main PLL parameters such as the charge pump current and the VCO number of stages are also adjustable in order to compensate for PVT variations.

The DTU has been designed in the same CMOS 0.18 um of the Alpide ASIC and has been produced both as a standalone test chip and integrated in the Alpide-3 ASIC. Measurements on the test chip has shown that the DTU is fully functional at 1.2 Gb/s with a random jitter of about 10 ps and a deterministic jitter of about 50 ps. The DTU is still functional at 1.5 Gb/s albeit with a 20% jitter degradation. Measurements on the Alpide DTU have shown similar results when the Alpide is in idle mode. Unfortunately an increase of jitter correlated to the chip activity has also been observed. The issue has been addressed in the Alpide-4, currently in production, by a power domain separation and a general layout effort to reduce the capacitive coupling to the PLL sensitive nodes.

The DTU test chip has been tested for Single Event Upset tolerance with both ions at the INFN LNL Tandem facility and protons at the NPI cyclotron facility. A LET threshold of 3.7 MeV cm2/mg has been measured for the PLL. A second test with ions is scheduled for July at LNL for BER studies.

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